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Commissioning and LED System Tests of the Engineering Prototype of the Analog Hadronic Calorimeter of the CALICE Collaboration

Master-Thesis

by

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Contents

Introduction

In modern particle physics, collider experiments are used in the quest for answers to open questions. The highest energy particle accelerator to date is the Large Hadron Collider (LHC) at CERN, Switzerland. It aims to experimentally detect new particles or phenomena.

As a proton-proton collider, the LHC is a good instrument for the confirmation of the existence of previously undiscovered particles. However the precision achievable with proton accelerators is inherently worse than for a comparable e^+e^- experiment. To measure new particles and phenomena discovered at the LHC with highest precision, the construction of a complementary e^+e^- collider with up to 1.5 TeV center of mass energy is planned. To utilise the full potential of such an accelerator, excellent resolution detectors have to be developed. One goal of the detector development is a hadronic jet energy resolution of $30\%/\sqrt{E\,[\mathrm{GeV}]}$. This ambitious target in resolution can be achieved by incorporating new concepts of energy measurement as the particle flow approach, based on the exact tracking of particles in the whole detector, which demands very high granularity in all parts of the detector.

The CALICE collaboration develops different calorimeter concepts for a future accelerator experiment are developed and tested in prototypes. This also includes the integration of such detector concepts into a full detector concept. One investigated concept for a highly granular hadronic calorimeter consists of steel absorbers and scintillator tiles. Silicon photomultipliers (SiPM) are integrated into each tile for readout of the generated light signals. The planned calorimeter consists of up to 8 million scintillator tiles, making the integration of readout and digitisation electronics a necessity. As SiPM parameters have to be monitored constantly, a calibration system has to be included in the detector volume.

As a physics prototype of this calorimeter concept demonstrated its general feasibility, currently an engineering prototype is under development, which aims to fully realise the integration of readout and calibration electronics into the detector volume.

This thesis describes system tests for the LED based SiPM calibration system integrated on the current version of the engineering prototype. Results of gain calibration performance and output homogenisation are presented. Further, procedures and results from the commissioning of a 576 channel prototype layer for use in a hadronic test beam are presented. The commissioning part focuses on preamplifier configuration and MIP calibration.

1 Particle Accelerators and Detectors in High Energy Physics

Since Ernest Rutherford's discovery of the atomic substructure, a multitude of new particles have been discovered. Bigger and more powerful accelerators and detectors had to be constructed to create and study these previously unknown particles. The *Standard Model* (SM) [1–3] describes most of these then-new phenomena, but also predicted many effects which could be verified only long after its foundation in the 1960's. The overwhelming success of the SM, coupled with its few but definite shortcomings, lead to the construction of the highest-energy particle accelerator to date, the *Large Hadron Collider* (LHC) at CERN, Switzerland. Although the LHC has merely started its operational phase in 2010, the development of new colliders is ongoing. One common concept for a future high energy collider is a linear electron-positron collider.

This chapter gives an introduction to the SM itself, an example of a possible physics process studied in a lepton collider, the concepts of measuring the energy of particles created in high energy collisions and new accelerator and detector concepts under development.

1.1 The Standard Model of Particle Physics

The Standard Model of particle physics consists of 12 matter particles, called fermions, as shown in Figure 1.1 and their respective anti-partners, which have opposite quantum numbers but behave very similarly otherwise. All fermions have spin $\pm 1/2$. These particles interact via the electromagnetic, weak, and strong nuclear force mediated by four different gauge bosons. All gauge bosons have spin 1. Gravitation as the fourth known fundamental force is not included in the SM at all, as no mathematically consistent theory including both the SM and gravitation has been devised yet [5, 6].

1.1.1 Matter Particles

The matter particles are further divided into leptons and quarks. Leptons can exist as free particles on their own, while quarks, due to *confinement*, always appear in bound states called *hadrons*.

The family of leptons consists of the electron (e), the muon (μ) and the tau (τ) with their correspondent neutrinos ν_e, ν_μ, ν_τ. The first three particles have unity charge and rest masses between 511 keV and 1.77 GeV. Neutrinos are charge neutral and have very low but non-zero mass.

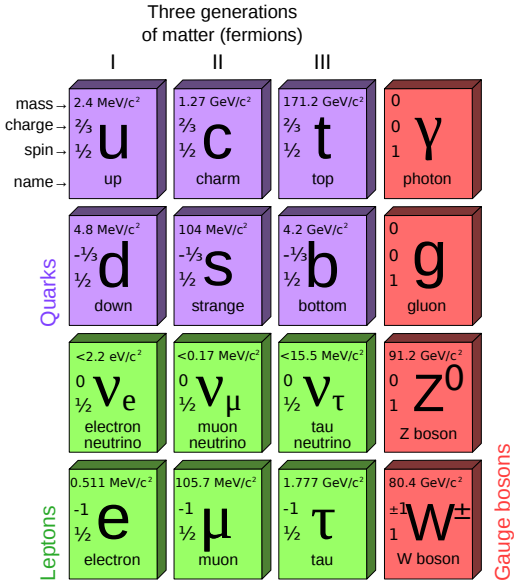


Figure 1.1: *Particles of the Standard Model [4, 5]*

The other 6 fermions of the SM are quarks. Quarks carry $\pm 1/3$ or $\pm 2/3$ electromagnetic charge. The quark masses range from 1.5 - 3.0 MeV (up-quark) to 174.2 GeV (top-quark) [5]. The *confinement* of quarks can be described by introducing an additional *color charge* and forcing every bound state of quarks to have neutral net color charge. This leads to bound quark states of either opposite color charge quark pairs called mesons, or three quarks of one color charge each, bound into so called baryons.

Both leptons and quarks can be classified into three generations. The first generation consists of the electron, its neutrino, and the up- and down-quark, which are stable particles. Higher generations are generally increasingly more massive and, except for neutrinos, decay into less massive particles down to the first generation. Because of this decay, all every-day matter consists of first generation particles only. Particles of higher generations can only be created and studied in high energy particle collisions.

1.1.2 Fundamental Forces

There are four known fundamental forces that govern the interaction of elementary particles. An interaction is called fundamental when it cannot be described in terms of other interactions. These forces are called the gravitational force, the electromagnetic force, the weak force and the strong force. Each force is mediated by force-carrying bosons. In Figure 1.1 these bosons are shown in the rightmost column.

Gravitation

Gravitation describes the interaction of particles caused by their mass-energy. On a subatomic scale the strength of gravitation is many orders of magnitude lower than the other forces, which makes its influence negligible. The theorised mediating particle of gravitation, the *graviton* has not been detected in experiments yet and, depending on the model, the hypothetical cross-section is far too low for detection in the foreseeable future. Neither has gravitation successfully been integrated into the SM.

Electromagnetic force

The electromagnetic force applies to all electrically charged particles and objects and was described already in classical physics from macroscopic experiments. On the subatomic level it is described by exchange of photons (γ) between charged particles. Examples for electromagnetic interactions are lepton pair-production and -annihilation as well as elastic scattering. As photons are massless, the reach of the electromagnetic force is infinite, although the effective distance is limited by the $1/r^2$ characteristic of the interaction.

Weak Force

The weak force is mediated by the exchange of $W^{\pm}$ and Z^0 bosons. All matter particles interact via weak interaction, which especially makes the weak interaction the only force applying to neutrinos. A unique property of the weak interaction is its ability to transform particles within the same group. For example in β-decays one of the neutron's d-quarks transforms into a u-quark by emitting a W^- which subsequently decays into an electron and an electron-antineutrino. Because of the relatively high masses of 80.4 GeV for $W^{\pm}$ and 91.2 GeV for Z^0, the Yukawa potential limits the range of the weak interaction to around 10^{-18} m.

Strong Force

Gluons are the massless mediators of the strong force, responsible for the creation of bound hadron states. The strong interaction applies to color-charged particles exclusively. As gluons are able to exchange color charge between interacting particles, they carry color charge themselves, which makes gluons interact with each other. This leads to an increase of the force between two color-charged particles with distance. Once the distance and thus potential energy between two quarks exceeds the threshold for quark pair production, a quark-antiquark pair is created from the vacuum. This reduces the potential energy of the gluons by the sum of the masses of the two created particles. Either the two new quarks form two mesons with the inital quarks, or more quark-antiquark pairs are produced. This process, called *hadronisation*, leads to a cascade of new mesons that share the momentum of the initial hadron. In very high energy experiments these narrow hadron beams can be detected as *jets*. Analysis of their total energy gives insight into the original process that created the initial meson.

1.1.3 Higgs Mechanism

It is apparent that the $W^{\pm}$ and Z^0 bosons have exceptionally high mass compared to the massless photon and gluon. The standard model at first does not offer any explanation, as the weak-mediating bosons are described as massless on their own. One possible mechanism of explaining their mass was developed by Peter Higgs [9]. Originating from electroweak symmetry breaking, the Higgs field is introduced which interacts with $W^{\pm}$ and Z^0 via the Higgs boson to give them their observed masses. Just recently first statistically significant signs of the Higgs boson have surfaced from the ATLAS and CMS experiments at the LHC [7, 8].

1.2 Higgs Production and Detection in e^+e^- Experiments

As this thesis covers work for application in a linear e^+e^- collider, one possible physics process studied in such an experiment is explained here. Exact measurements on the Higgs boson certainly are one of the primary benchmarks for a future experiment.

In e^+e^- collisions the dominant Higgs boson production processes are *Higgs-strahlung* and *vector-boson-fusion* (VBF). Schematic diagrams for both processes are shown in Figure 1.2. The cross sections of these and other less prominent production paths are shown

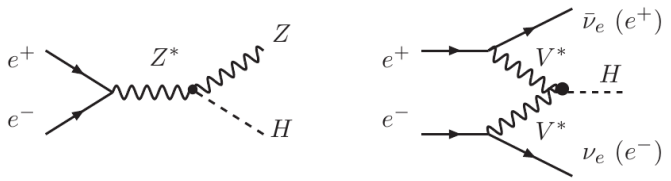
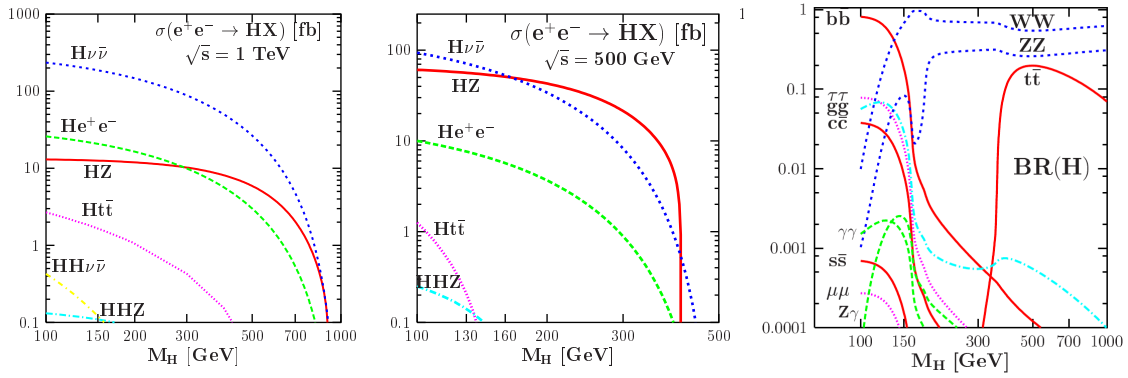


Figure 1.2: *Feynman graphs for Higgs production via Higgs-strahlung (left) and vector-boson-fusion (right).*

in Figure 1.3 for different collider energies. Assuming the new boson observed in LHC experiments to be confirmed as the Higgs boson at around 125 GeV, it will be predominantly produced by VBF of two $W^{\pm}$, with Higgs-strahlung producing around half that rate. VBF of two Z^0 bosons is around one order of magnitude less frequent than $W^{\pm}$-VBF. The cross section for Higgs-strahlung scales as $1/s$, while the WW-fusion cross section behaves like $\log(s/M_H^2)$, with s the squared center of mass energy $\sqrt{(s)}$. So at $\sqrt{s}$=1 TeV $W^{\pm}$-VBF is the most frequent process by far, with Higgs-strahlung more than one order of magnitude less frequent. Z^0-VBF Higgs production is slightly higher than Higgs-strahlung, a factor of ten less than the $W^{\pm}$-VBF process.

In Higgs-strahlung events a reconstruction of the Higgs itself is not needed to determine its mass, as the Z^0 carries the full beam energy reduced by the Higgs mass. Thus full reconstruction of the Z^0 is sufficient if the beam energy is well known. As the reconstruction of the Higgs decay is not needed, Higgs-strahlung is the optimal process for discovering a Higgs that decays differently than predicted by the SM.



(a) *Production rate at $\sqrt{s} = 500$ GeV.*

(b) *Production rate at $\sqrt{s} = 1000$ GeV.*

(c) *Higgs branching ratios.*

Figure 1.3: *Production rates and decay branching ratios for Higgs bosons depending on its mass. Recent experiments suggest a Higgs mass around 125 GeV [20, 21]*

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The two neutrinos created in $W^{\pm}$-fusion leave the detector without signal, thus making reproduction of the complete final state impossible. Reconstruction of the Higgs mass has to be done from its decay particles exclusively. As shown in Figure 1.3.(c), a Higgs boson around 125 GeV will decay into a $b\bar{b}$-pair most of the times.

1.3 Calorimetry

In particle physics, calorimeters are used to determine the energy of particles by absorbing them in matter. To measure the energy transferred from the particle to the material, a signal proportional to the energy loss has to be extracted somehow. The effective energy resolution of a real calorimeter is limited, for example because only a fraction of the total deposited energy is measured.

This section first describes different interactions of particles with matter, then discusses the design of *sampling calorimeters* and finally gives a short overview about the rather new approach of *particle flow calorimetry* to increase the resolution of calorimeters.

1.3.1 Interaction of Particles with Matter

A particle's interaction with matter depends mainly on its type and energy. Electrons and photons deposit energy only through electromagnetic interactions while charged hadrons can interact in both electromagnetic and hadronic processes.

High energy particles will generally trigger multiple interactions, thus creating many secondary particles. This *particle shower* also behaves differently for electromagnetic and hadronic processes. The behavior of single electromagnetic or hadronically interacting particles and their subsequent showers will be discussed separately in the following part.

Electromagnetic Interactions

High energy electrons and positrons ($e^{\pm}$) passing through matter will lose their energy mainly from *bremsstrahlung* and *ionisation*. Bremsstrahlung is synchrotron radiation created by the influence of the electric field of the atoms on incident charged particles. Energy loss from bremsstrahlung is proportional to the momentum of the particle itself:

$$-\frac{\mathrm{d}E}{\mathrm{d}X} = \frac{E}{X_0}, \tag{1.1}$$

with the parameter X_0 called *radiation length*. One radiation length equals the mean path of an $e^{\pm}$ after which its momentum is reduced to $1/e$. For materials with the atomic number $Z > 2$ and the mass number A

$$X_0 \approx \frac{716.4\,A}{Z(Z+1)\ln\left(\frac{287}{\sqrt{Z}}\right)}\left[\frac{\mathrm{g}}{\mathrm{cm}^2}\right] \tag{1.2}$$

is a suitable approximation for the radiation length. Muons and other heavy charged particles emit bremsstrahlung only at very high energies, as synchrotron radiation is suppressed for higher particle masses M with $1/M^4$.

At the critical energy E_c the $e^{\pm}$ energy loss contributions from bremsstrahlung and ionisation are equal, with ionisation dominating for energies below. Energy loss from ionisation can be parametrised by the *Bethe-Bloch* formula which can be stated as

$$-\frac{dE}{dX} = \mathrm{K}z^2\frac{Z}{A}\frac{1}{\beta^2}\left(\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right) \tag{1.3}$$

for muons and other heavy particles [5], where Z is the atomic number of the absorber material, A its atomic mass, T_{max} the maximum single collision energy transfer, I the mean excitation energy and K a constant term containing Avogadro's number, the electron mass m_e and the elementary charge e. The function $\delta(\beta\gamma)$ corrects for relativistic effects. Figure 1.4 shows the combined energy loss for muons in copper. Particles in the range $\beta\gamma \approx 4$ deposit minimum energy from ionisation and thus are called *minimum ionising particles* (MIP) [5]. The value of minimal energy loss can be parametrised as

$$-\left.\frac{\mathrm{d}E}{\mathrm{d}X}\right|_{mip} = 6\frac{Z}{A} - 1.25\left[\frac{\mathrm{MeV}}{\mathrm{g/cm}^2}\right]. \tag{1.4}$$

High energetic photons passing through matter will undergo $e^{\pm}$ pair production as long as their energy is above the threshold of twice the electron mass M_e=511 keV. The difference between photon momentum and electron mass is distributed into the electron momenta. The mean free path length until pair-production occurs can be expressed as $9/7X_0$ in terms of the radiation length.

Upon entering a dense material, the combination of bremsstrahlung and pair production from a photon or electron leads to a chain reaction in which new particles are created in a cascade, "the radiated photons convert, and the conversion pairs radiate"[22]. The cascade stops at the critical energy when bremsstrahlung ceases and ionisation becomes

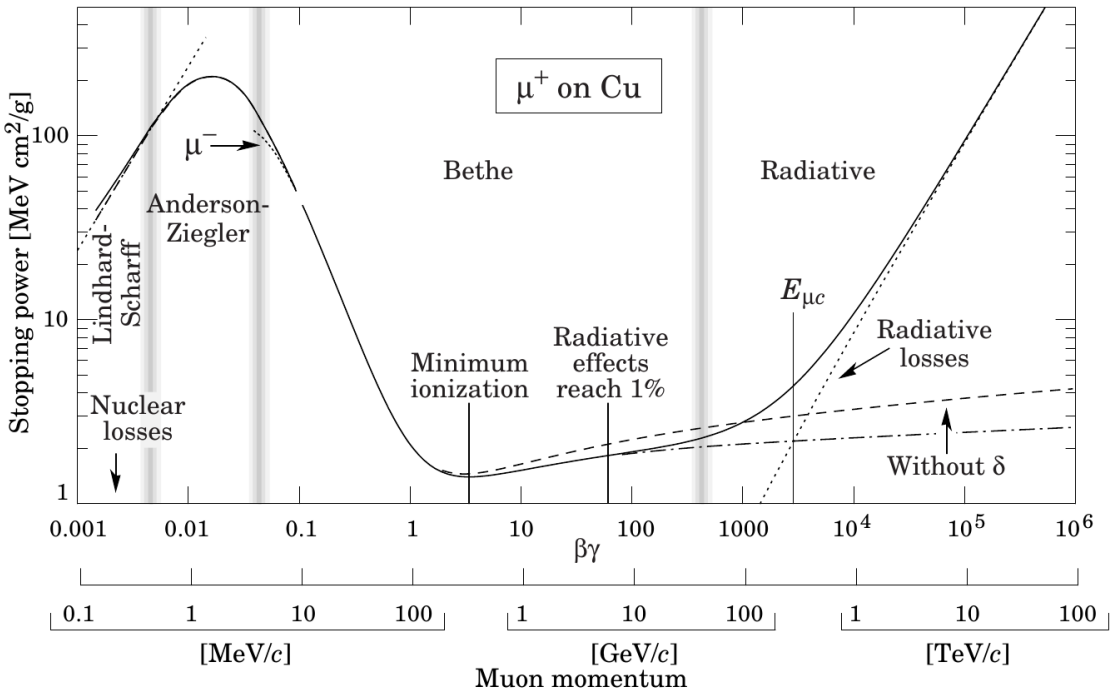


Figure 1.4: *Combined energy loss for muons in copper depending on its momentum. Transisitions between different models are indicated by vertical bands [5].*

the most dominant process. Ionisation generally does not induce further cascades, so $N \sim {}^{E_0}/_{E_c}$ particles are produced in total.

For measuring the total energy of a particle shower it is important to contain the full shower in the calorimeter, as not to lose energy to *leakage*. For example, expressed in radiation lengths, $16\,X_0$ of material are needed for 99% shower containment at 1 GeV total energy. The shower depth scales logarithmically with energy, so for 1 TeV energy, $27\,X_0$ of material are needed.

In transverse direction, the *Moliere radius* ρ_M is the characteristic radius of a cylinder that on average contains 90% of the shower energy. It can be parametrised as

$$\rho_M = \frac{X_0}{E_c} \cdot 21.2\,\text{MeV}. \tag{1.5}$$

Generally the shower shape is different for each event because of statistic fluctuations in the first few steps of the cascade. This raises the need to sample the energy deposition at different representative positions inside the shower, for example in a sandwich calorimeter (see subsection 1.3.2). An example electromagnetic shower is shown in Figure 1.5.(a).

Hadronic Interactions

Besides ionisation, charged hadrons lose energy from inelastic scattering on other nuclei. In collisions of the incoming hadron with a single nucleon inside a nucleus, the momentum transferred to the nucleon causes an *intra-nuclear cascade* by subsequent collisions from the hit nucleon with other nucleons inside the nucleus. This *spallation* produces multiple neutral and charged pions (π^0, $\pi^\pm$) and other hadrons, including nucleons emitted from the nucleus.

The mean free path before an inelastic interaction occurs is called *nuclear interaction length* λ_I and for A > 7 can be parametrised by [24]

$$\lambda_I = \left(20A^{0.4} + 32\right)\left[\frac{\text{g}}{\text{cm}^2}\right]. \tag{1.6}$$

According to the ratio of cross sections for inelastic scattering on protons the interaction length for pions is around ${}^3/_2$ of nuclear interaction length [23]. In materials with low atomic mass A, λ_I and X_0 are very similar, but for high-A material the difference increases rapidly. For the example of tungsten $X_0 = 3.5\,\text{mm}$ but $\lambda_I = 9.9\,\text{cm}$ [5]. As every real calorimeter is limited in its size, dense, high-A materials like Pb, Fe or W are used as absorber material. In comparison to elecromagnetic showers, hadronic interactions happen on a larger scale in these materials, making a greater material depth a necessity.

The π^0 from spallation processes will decay into two photons almost instantly, seeding an electromagnetic subcomponent of the total energy. $\pi^\pm$ have much longer mean lifetimes and thus induce further hadron interactions before decaying into a muon and a corresponding neutrino most of the time.

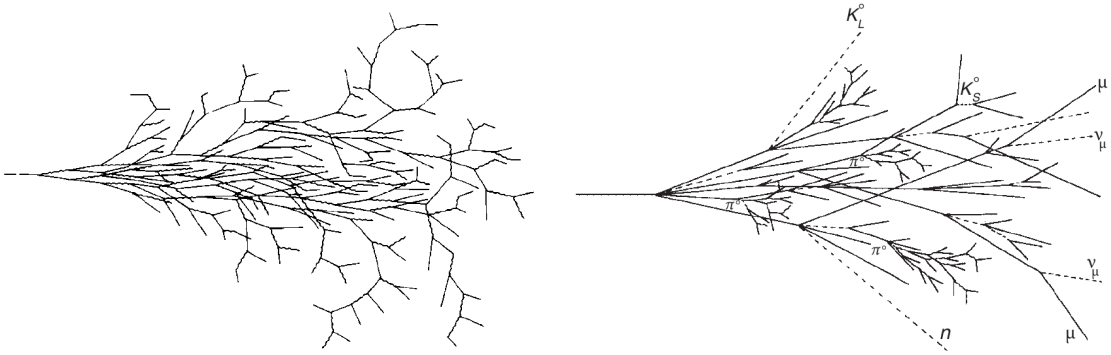
Neutrons have to be treated separately, as they can travel long distances through the calorimeter, losing only undetectable amounts of energy per elastic interaction with nucleus. Once slowed down enough, the probability of *neutron capture* increases for some

materials, creating a localised energy deposition. The distance of this deposition to the original incident hadron both in space and time can be large on the scale of such showers, making the assignment of neutrons to their correspondent showers a non-trivial task.

Up to 20% of the energy of the hadronic part is called *invisible*, as it goes into nuclear binding energy and target recoil, gives no measurable signal and thus impedes energy reconstruction. The invisible energy fraction is an important parameter in the overall resolution of a hadronic calorimeter (see subsection 1.3.2).

Many more processes take part in hadronic interactions but cannot be discussed in-depth here. Generally hadron showers are characterised by the high particle multiplicity per interaction with less overall interactions compared to electromagnetic showers. This causes stronger overall fluctuations in shower shape and development. Figure 1.5.(b) shows a schematic shower example. Neutral and charged hadrons are created at each nuclear interaction, some of which immediately decay into diphoton pairs which creates local electromagnetic subshowers. Higher energy hadronic fragments may travel further away from the inital interaction point until performing the next nuclear interaction. The overall size of the shower is thus described in terms of λ_I while the substructure develops on the scale of X_0. To contain most 95% of a hadronic shower, on average $8\,\lambda_I$ of Fe are needed in longitudinal direction for an incident pion of 100 GeV. In transverse direction a cylinder with radius λ_I contains around 90% of the shower energy [23]. Fluctuations in both directions are significant.

In opposition to electromagnetic showers which develop near-instantly, hadronic showers have limited propagation speeds, mostly because of slow and delayed neutral components. To reduce confusion between different showers (as needed in the particle flow approach, see subsection 1.3.3), evaluating the time information might prove to be a valuable tool. An example of this is shown in Figure 1.6.



(a) *Electromagnetic shower*

(b) *Hadronic shower with electromagnetic subshowers, dashed lines depict neutral hadrons.*

Figure 1.5: *Schematic visualisation of an electromagnetic and hadronic shower.*

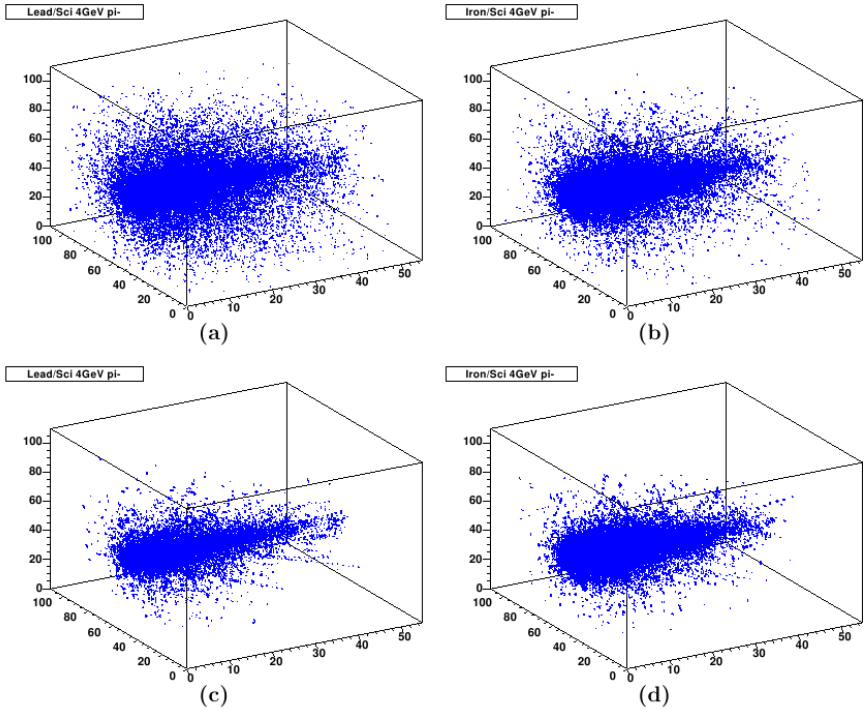


Figure 1.6: *Simulated shower from a 4 GeV pion for lead (a) and iron absorbers (b), (c) and (d) show the same shower with a timecut on $t < 5$ ns [31].*

1.3.2 Sampling Calorimeters

As no signal can be extracted from most materials with good absorbing capabilities, *active material* has to be included inside the calorimeter to extract a signal proportional to the deposited energy. This active region only measures the direct energy loss of charged particles inside this region while neutral particles only give an indirect signal. In ionisation chambers and semiconductors as active material, the signal consists of accumulated charge. In scintillators and Cerenkov detectors incident particles create a light pulse which can be read out by photodetectors.

A common calorimeter concept consists of alternating layers of dense absorber material and active layers perpendicular to incident particles, called *sandwich calorimeter*.

For a simple shower model with total generated charged particles N, of which only a constant fraction N_{vis} is passing through the active layers, N is proportional to the total energy E_0. N_{vis} varies statistically and thus gives the Poisson standard resolution of $\sigma\sqrt{N_{vis}}$. Since N, N_{vis} and E_0 are proportional to each other, the energy resolution can be parametrised by

$$\sigma = \frac{A}{E_0} \tag{1.7}$$

with the *stochastic constant* A. Every real readout system adds signal-independent noise of the form $\sigma_N = B$ to the signal. B is governed by the amount of noise per channel times the total amount of channels. Detector miscalibration and other inherent imperfections in the calorimeter setup further decrease the achievable resolution by $\sigma_l = C \cdot E$ proportional to the deposited energy. These contributions are statistically uncorrelated and thus can be added in quadrature to yield the the standard parametrisation of the energy resolution of a calorimeter

$$\frac{\sigma}{E} = \frac{A}{\sqrt{E}} \oplus \frac{B}{E} \oplus C. \tag{1.8}$$

In practice current electromagnetic sampling calorimeters reach resolutions of $\approx \frac{10\%}{\sqrt{E}}$ [25]. Even better results can be obtained from homogenous calorimeters like the CMS ECAL and the NA48 experiment with $\frac{2.8\%}{\sqrt{E}}$ and $\frac{3.5\%}{\sqrt{E}}$ respectively [26,27].

For hadronic calorimeters the achievable energy resolution is much worse because of the huge fluctuations in the hadronic shower development that gives rise to many uncertainties. As parts of the hadronic energy are invisible the energy/MIP conversion factor is different in pure hadronic showers than in a pure electromagnetic cascade. The ratio between hadronic and electromagnetic energy differs from event to event, making an averaged energy/MIP conversion factor imprecise. The fluctuation of the invisible energy fraction of up to 40% adds even more uncertainty to the energy scale of the whole shower. Different hardware and software techniques can be applied to improve the hadronic energy resolution, but still the best hadronic calorimeter to date, built by the ZEUS collaboration, only offers a resolution of $\sigma/E = \frac{34\%}{\sqrt{E}}$.

Different approaches for improving the hadronic energy resolution during software reconstruction are used [28]. With a highly granular calorimeter it is possible to iden-

tify local energy depositions from electromagnetic subshowers for selective energy-dependent reweighting. The *dual readout* approach includes a second kind of active material into the calorimeter, which enables the distinction between hadronic and electromagnetic showers from their emission of Cerenkov radiation [29].

1.3.3 Particle Flow Calorimetry

In a hadronic calorimeter, usually hadron jets are measured rather than single particles. The energy resolution for such jets is typically worse than for single particles. In order to improve the total jet energy resolution of a calorimeter, the *particle flow* approach combines the response of the tracker, electromagnetic and hadronic calorimeter with advanced algorithms for pattern recognition.

Comparing the energy resolutions, the central tracker of a detector usually performs much better than the calorimeters for a wide energy range. For the *International Large Detector* the energy threshold for which the calorimeters outperform the tracker in terms of resolution is ∼200 GeV in the ECAL and ∼510 GeV in the hadronic calorimeter [33]. If each track leaving the tracker can be assigned to a collection of hits in the calorimeters, these calorimeter hits can be discarded and their energy replaced with the tracker momentum information. This only works for charged particles, neutral particles neither give signals in the tracker nor are their trajectories bent by the magnetic field. Energy depositions in the calorimeters without a track leading to them are measured in the calorimeter. A schematic sketch of this is shown in Figure 1.7.

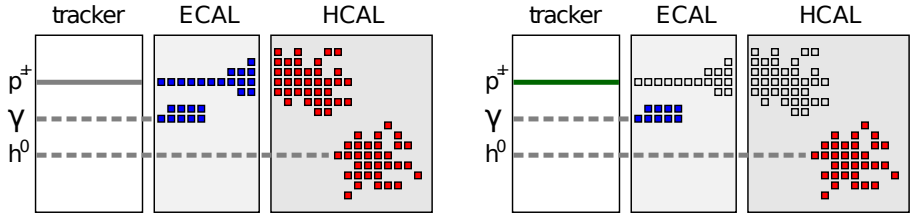


Figure 1.7: *Schematic view of classic calorimetry (left) in opposition to particle flow calorimetry (right). In the classic approach, particle energy is measured from the deposition in the calorimeter. With particle flow, the charged particles are measured from their tracker path curvature.*

On average the total jet energy is carried by 62% charged hadrons ($h^{\pm}$), 27% photons (γ) and 10% neutral hadrons (h^0). The missing 1% are neutrinos which are undetectable. In a classic calorimeter 72% of the total energy would be impaired by the hadronic energy resolution of the combined ECAL and HCAL, while only the 10% h^0 give no other signal than energy deposition in the calorimeter. In the optimal case of each particles energy measured with the highest possible resolution the total jet energy resolution is

$$\frac{\sigma}{E} = 0.62 \cdot \sigma_{h^{\pm}} \oplus 0.27 \cdot \sigma_{\gamma} \oplus 0.10 \cdot \sigma_{h^0} \approx \frac{19\%}{\sqrt{E\,[\mathrm{GeV}]}}. \tag{1.9}$$

In practice this resolution is not reached, as often single tracks and calorimeter hits are overlapping, so that the assignment is not perfect, called *confusion*. If neutral particles

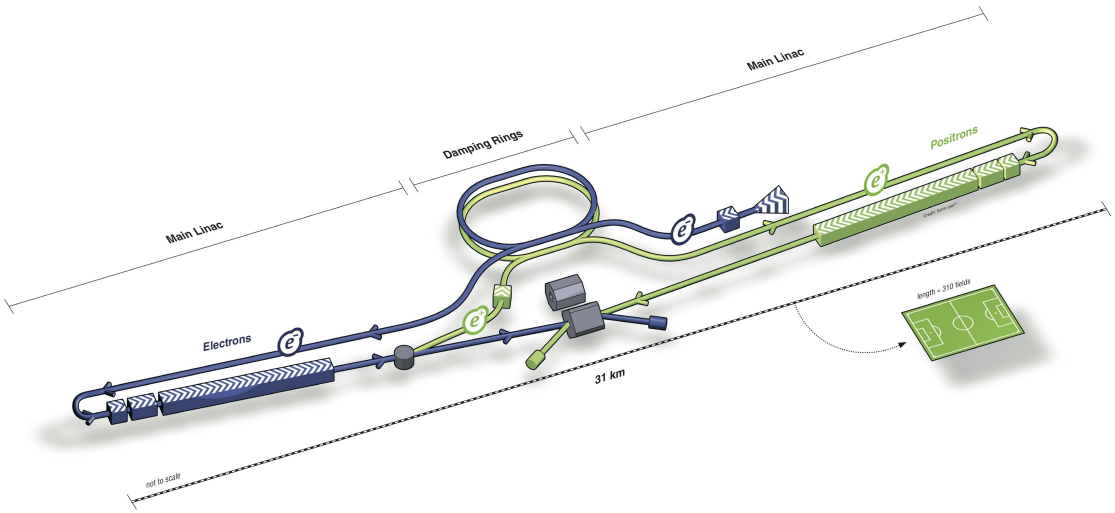


Figure 1.8: *Schematic view of the International Linear Collider [17].*

deposit energy in the same calorimeter cells as charged ones, their energy is wrongly assigned to a track and lost in the total energy sum. Also fragments belonging to a hadronic cascade can be wrongly identified as additional neutral particles and thus be counted twice into the jet energy. Including these effects a jet energy resolution of $\frac{\sigma}{E} \leq \frac{30\%}{\sqrt{E[\mathrm{GeV}]}}$ is reachable.

To make this procedure worthwhile, a very finely granulated calorimeter and a very efficient tracking system is needed to minimise confusion. Further advances in the algorithms for shower and particle separation will also improve the overall performance. The particle flow concept has been tested with data from the CALICE AHCAL physics prototype [30].

1.4 The International Linear Collider

The *International Linear Collider* (ILC) is a concept for a future high energy e^+e^- linear collider. Two opposing linear accelerator tracks on a total length of 31 km accelerate electrons up to 500 GeV or even 1 TeV in a later upgrade. A conceptual sketch is shown in Figure 1.8.

Electrons are created either directly from photo-emission or via photo-induced field emission. These electrons are then accelerated to 5 GeV before injection into the electron damping ring. To create positrons, a part of the electrons are sent through the main linear accelerator into an undulator, generating photons. Interaction of these $\sim$ 10 MeV photons with a tungsten absorber leads to e^+e^- pairs exiting the target. Such positrons can be filtered out, pre-accelerated to 5 GeV and injected into the positron damping ring.

The damping rings maintain the energy of their respective particles while forming packets of particles called *bunches* of around 20×10^9 particles each. They also *cool* down

the individual particles per bunch by equalising their longitudinal momenta and reducing their transverse momenta, effectively improving the beams emittance. After both beams are conditioned to acceptable levels, they are injected into their respective LINACs where they are accelerated to their final energy of up to 250 GeV per beam. In total 2625 bunches spaced 370 ns apart are injected, leading to a bunch train of $\sim$ 1 ms length. Shaping and conditioning takes 198 ms, so the train collision rate at ILC is around 5 Hz.

In order to achieve competitive luminosity with such low collision rates (compared to the LHC design rate of 40 MHz) the physical dimensions of the bunches have to be minimal, resulting in a planned lateral bunch size of $640 \times 5.7\,\mathrm{nm}^2$. To further increase the physics capabilities of the ILC, both particle beams are polarised and their polarisation can be set up. This allows for interesting possibilities, e.g. selective enabling and disabling of certain production processes which are suppressed for some polarisation combinations.

It is planned to have two separated multi-purpose detectors at the ILC. As a linear collider naturally only has one interaction point, the two detectors have to be designed in such a way, that a fast switch between them is possible within a day. As each detector has to be put into place with sub-millimeter precision, this is an enormous challenge on the engineering side. The final focus magnets are part of the detector and require even higher precision in the nanometer region. At the moment there are two verified detector concepts, the Silicon Detector (SiD) and the International Large Detector (ILD), which is elaborated further in the next section.

Generally the ILC is based on technologies that are already approved to be feasible or even in use at the moment, for example the XFEL and FLASH at DESY use the same accelerator technology. As such construction could start with minimal delay.

1.5 The International Large Detector

One possible concept for a multi-purpose detector at the ILC is the *International Large Detector* (ILD) [19]. The different parts of the detector are concentrically arranged around the beampipe. All trackers and calorimeters are placed inside the superconducting magnet. The exact design and implementation is not finally fixed, as for each module several technology alternatives are still under consideration.

Magnet

The ILD magnet is planned as a superconducting solenoid, creating a magnetic field of 3.5-4 T parallel to the beam axis. To improve the total energy resolution no additional material should be between trackers and calorimeters, leading to the magnet also encasing the calorimeters. As an increase in magnet size leads to a sharp rise in associated costs, the maximum magnet dimensions are fixed. This also defines the requirements on the maximum dimensions of trackers and calorimeters. The magnet is surrounded by a

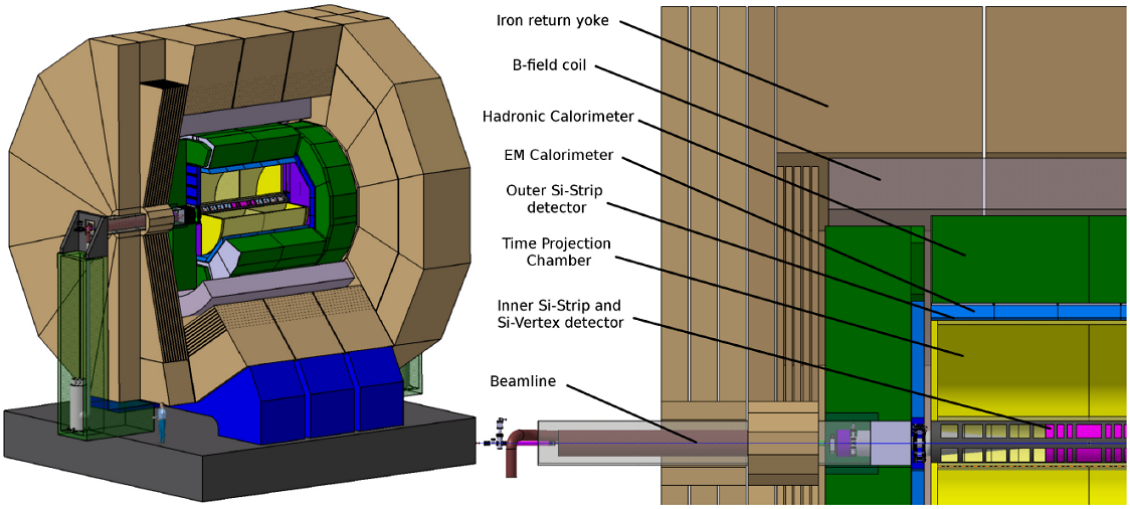


Figure 1.9: *Schematic view of the International Large Detector [19].*

massive iron return yoke to improve the magnetic field homogeneity inside the coil and to minimise stray magnetic fields outside of the detector.

Vertex Detector

Directly around the interaction point a semiconductor pixel tracker is foreseen. With its very high spatial resolution it is used to measure the exact origin (*vertex*) of single jets. Hadrons containing a bottom quark are sufficiently long lived to travel a certain distance before decaying, but not enough to reach the calorimeters. So usually the jet resulting from a decaying b-hadron has its starting point some millimeters outside the main interaction vertex. Thus vertex detectors are an important tool to correctly identify b-jets.

Two different designs are under consideration for the vertex detector, one consists of five evenly spaced silicon layers around the center of the beampipe, the other one is constructed in three double layers for six silicon layers total. As the main pixel detector does not extend to the lowest angles between beampipe and particle trajectory, a lower resolution silicon strip detector is installed to cover nearly the full solid angle reaching well into the endcaps.

Time Projection Chamber

For the measurement of charged particle momenta in the ILD, a the large *Time Projection Chamber* (TPC) with a diameter of 1.5 m is foreseen. The TPC is filled with gas at precisely controlled conditions. An electric drift field inside the TPC is created from a central cathode with both endcaps posing as anodes. A traversing particle leaves a trail of free electrons and ionised gas on its trajectory of which the electrons drift towards the anode.

At the end plates the electrons undergo gas amplification, either from *Micromegas* or *Gas electron multipliers*. After the amplification stage the electrons are sampled spatially on a fine grid of pads, while the impact times allow reconstruction of the particles position along the beam axis.

This allows for full 3D reconstruction of particle paths with up to 224 points per track, enabling an excellent momentum measurement from the radius of the bent trajectories. From the signal, information about ionisation power and thus particle type can be obtained. Because of the low mass of the whole system, minimum energy is lost in traversing the TPC.

Electromagnetic Calorimeter

The electromagnetic calorimeter (ECAL) is realised as a sandwich calorimeter with tungsten absorbers. For the active layers either $5 \times 5\,\mathrm{mm}^2$ silicon pads or $10 \times 4.5 \times 0.2\,\mathrm{mm}^3$ scintillator strips are under consideration. To increase energy resolution for lower energy electrons and photons, the absorber plates gradually increase in width outwards of the center. The total width of the ECAL is around 20 cm, corresponding to ~ 24 radiation lengths X_0 with tungsten absorbers.

Hadronic Calorimeter

The hadronic calorimeter is also planned as a sandwich calorimeter, with 48 layers of 16 mm steel absorber, summing up to 5.5 nuclear interaction lengths λ_I of material. The steel is a non-ferrous alloy to not interfere with the magnetic field of the outer solenoid.

As space inside the solenoid is limited, the gap between absorbers is only 5.4 mm. To reduce dead material inside the detector not only the active material but also all of the readout electronics have to fit inside this gap.

Several readout options are in development. The digital version features *glass resistive plate chamber* (GRPC) readout in $1 \times 1\,\mathrm{cm}^2$ cells, while the analogue concept consists of $3 \times 3\,\mathrm{cm}^3$ scintillator tiles. The current engineering prototype of the analogue hadronic calorimeter is the topic of this thesis and thus described in further detail in chapter 2.

Muon System

Because of the cleaner events at a lepton collider the muon system can be much simpler than in the current experiments at the LHC. For example no triggering on muon tracks is needed. It is planned to integrate the muon system into the iron yoke to achieve limited calorimetric performance, acting as a tail catcher for showers that are not fully contained in the hadronic calorimeter. The readout technology has not been decided yet. A prototype using scintillator strips has been used at test beams at CERN and Fermilab in 2006-2008, but also a gas based readout is feasible.

2 The CALICE AHCAL Engineering Prototype

The analogue hadronic calorimeter (AHCAL) of the CALICE collaboration [11] is a sandwich calorimeter based on scintillator tiles in development for possible use in the ILD at the ILC accelerator. The *engineering prototype* (EPT) of the analogue hadronic calorimeter of the CALICE collaboration reaches out to fully integrate the readout and calibration electronics into the active layers of the calorimeter.

In this chapter first the motivation for building such a detector and its sampling technology is explained. After that the current status of the EPT hardware, which is used for all the measurements of this thesis, is elaborated.

2.1 Motivation

The main benchmark of the calorimeter system developed by the CALICE collaboration is the calorimetric distinction between Z^0 and $W^{\pm}$ in their hadronic decay modes with 3σ significance, as depicted in Figure 2.1. For this a total jet energy resolution of $^{30\%}/\sqrt{E}$ is needed. As conventional calorimetry does not manage to reach that goal, the particle flow approach is utilised. To meet the requirements of the particle flow algorithm a highly granular hadronic calorimeter based on scintillator tiles with individual readout, the AHCAL, was proposed and the physics prototype realised.

The AHCAL *physics prototype* is a sandwich calorimeter consisting of 39 layers of steel absorbers (1×1 m wide, 17 mm thick) resulting in 5.3 nuclear interaction lengths λ_I of material. 38 scintillator layers are interleaved with the absorber plates. The active layers are segmented into scintillator tiles between $3 \times 3\,\mathrm{cm}^2$ and $12 \times 12\,\mathrm{cm}^2$. As this prototype is made for pure test beam use, the beam usually hits near the center, perpendicular to the absorbers. Therefore only the central region is equipped with the smallest tiles with decreasing granularity towards the outer parts, to reduce the total number of channels. One active layer of scintillators with its differently sized tiles is shown in Figure 2.2. Each tile is read out by an individual silicon photomultiplier per tile (see section 2.2). However, digitisation, data acquisition, power supplies and the calibration system are handled externally from the detector volume, taking up more space than the detector itself. This also leads to a large number of cables running between detector and acquisition crate. This makes it impossible to scale this prototype up to the projected 8 million channels needed for a full ILD hadronic calorimeter.

The development of a scalable prototype suitable for use in the ILD has since culminated in the current version of the engineering prototype. The EPT aims to integrate

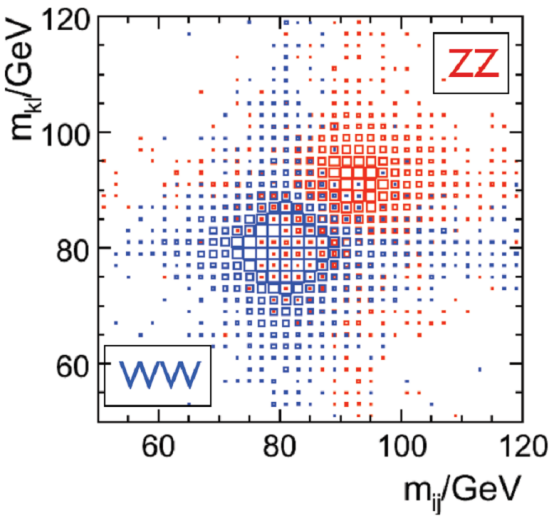


Figure 2.1: *Reconstructed masses from simulated hadronic $W^{\pm}$ and Z^0 decays for a hadronic calorimeter with $30\%/\sqrt{E}$ resolution [19].*

readout, calibration and power supplies into the detector while maintaining a strict power consumption, as no active cooling is foreseen inside the HCAL.

As tests in the DESY electron beam have already shown promising results, a full EPT layer of $72 \times 72\,\mathrm{cm}^2$ with nearly 600 readout channels is currently commissioned for use at the SPS hadron test beam in November 2012 as an extra readout layer of the CALICE digital hadronic calorimeter (DHCAL) prototype. This test aims to measure time resolved hadron showers as well as showcasing the stable test beam operation of the EPT.

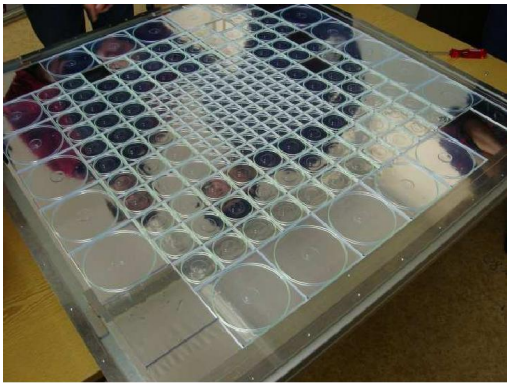
2.2 Sampling technology

The organic scintillators generate scintillation light from incident particles and guide it through the embedded wavelength shifting fiber onto the light detector in each cell. The following section elaborates on the used scintillating tiles and explains the working principle of pin photodiodes in general. Finally the resulting properties of silicon photomultipliers are discussed.

2.2.1 Scintillator Tiles

The scintillator tiles used in the EPT are made of polystyrene mixed with small amounts of scintillating additives. Around 1% of p-terphylene is added as main scintillating ingredient, emitting light in the range of 340 nm. As most photo detectors are not sensible for such wavelengths, the tile is doped with 0.03% POPOP. The absorbtion spectrum of

(a) *CALICE detector setup consisting of ECAL (front) AHCAL (center) and TCMT (rear) in the test beam at Fermilab.*



(b) *A single scintillator layer of the CALICE AHCAL physics prototype.*

Figure 2.2: *Pictures of the CALICE AHCAL physics prototype.*

POPOP closely matches the emission spectrum of p-terphylene, reemitting at around 410 nm wavelength.

As the silicon photomultipliers used in the EPT are most sensitive in the green visible spectrum, a wavelength shifting fiber (Kuraray Y-11) is embedded into the tile, which emits photons of approximately 500 nm wavelength. One end of the fiber is equipped with a small mirror, the other end is facing the SiPM. The fiber thus captures photons created inside the tile and guides them towards the SiPM.

To minimise light crosstalk between neighboring tiles the edges are chemically matted and thus diffusely reflect light back into the tile. A picture of a scintillating tile used in the EPT is shown in Figure 2.3.

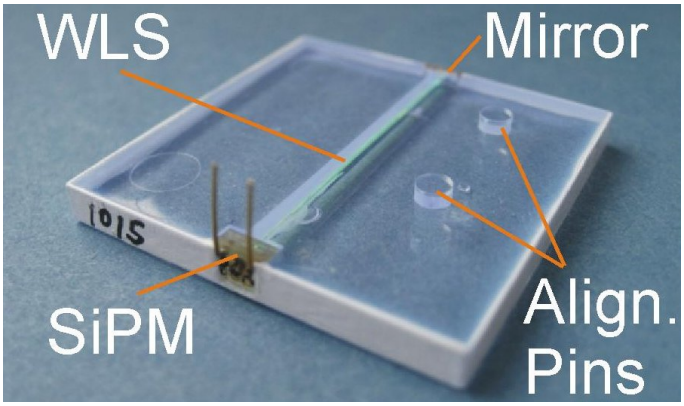


Figure 2.3: *Scintillator tile with integrated SiPM as used in the AHCAL EPT.*

2.2.2 PiN-Photodiodes and Operation Modes

Standard semiconductor diodes consist of a single small semiconductor substrate with two differently doped regions. At the transition between those regions, the *pn-junction*, negative charges drift into the p-doped area, generating an electric field opposite to their drift direction until an equilibrium is reached. The depleted region around the pn-junction then is void of any free charge carriers and behaves like an insulator. Applying a bias voltage U_B across the pn-junction increases the dimensions of the depletion zone and increases the electric field strength. Electron-hole-pairs generated inside this area drift apart before recombination, thus generating a small current that can be detected.

By introducing an *intrinsically* depleted (non doped) layer between the p- and n-doped areas, the depletion zone widens by the width of the intrinsic layer. The electric field is maximal over the complete width of the intrinsic layer. This dramatically increases the area in which ionising particles can be detected. Doping and resulting electric field strength are illustrated in Figure 2.4.

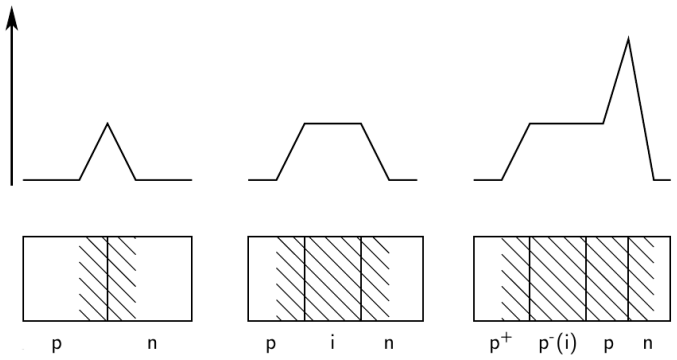


Figure 2.4: *Schematic doping and electric field strengths for a pn-diode, in-diode and APD [33].*

PiN-Operation

The energy threshold for generation of a single electron-hole-pair in silicon is 3.4 eV, in the range of visible photons. As no inherent signal amplification takes place in this mode, single visible photons only generate one electron charge as a signal, which is too small to be detected by the read out electronics. MIPs penetrating a pin detector generate around 15 electron-hole-pairs per nanometer of traversed material, which leads to a total signal of $15 - 20$
$cdot10^3$ electron charges in a typical detector of 250 µm thickness. The generated signal is practically independent of the temperature and exhibits relatively small noise.

Operation in Avalanche-Mode

To increase the signal generated by single incoming photons, the electric field strength inside the diode has to be increased to the point, where single electrons are accelerated

enough to generate further electron-hole-pairs on their own. This is accomplished by surrounding the intrinsic layer with a normal positively doped (p) and a strong positively doped (p^+) area in addition to a substantial increase in reverse voltage U_B . Electrons generated in the depletion zone drift into an area of very high electric field where they are accelerated enough to generate an electron avalanche. Holes created by the electron avalanche have a much higher effective mass and thus do not gain enough energy to generate new electron-hole-pairs, which also causes the avalanche to cease once all electrons have reached the p-doped area.

Around 100 – 1000 electron-hole-pairs are created per initial ionisation process, a substantial increase compared to the pin-diode before. Still at such small amounts of charge it is difficult to discriminate single photons .

The amplification of APDs strongly depends on the applied bias voltage and ambient temperature, making the operation of APDs a delicate task.

Operation in Geiger-Mode

Higher amplification can be achieved by further increase of the bias voltage U_B. This increases the electric field enough to enable the generation of new electron-hole-pairs from accelerated holes, too. This leads to permanent creation of new electron-hole-pairs across the pn-junction resulting in a constant current through the diode. This *breakdown* is kept up until U_B falls below the breakdown voltage U_{BD}, which is the minimum voltage needed to continue the avalanche. If U_B is applied via a sufficient resistor in the order of 1 MΩ, the surge of current during breakdown causes enough voltage drop (*quench*) on U_B that the avalanche is canceled. After the current ceases the diode again is subjected to the full U_B. This gives the formula for total ejected charge per generated avalanche

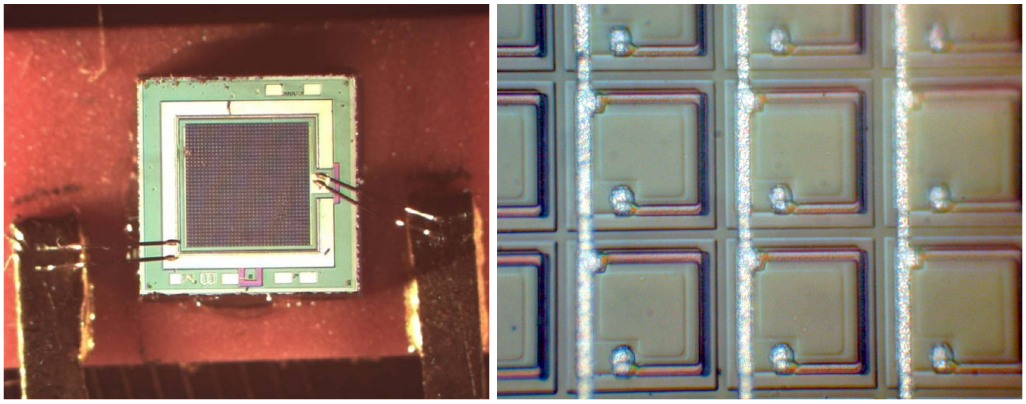
$$Q = C \cdot (U_B - U_{BD}), \tag{2.1}$$

with the APD capacity C (which in itself may slightly depend on U_B). The generated signal is independent of the energy and multiplicity of the incoming particles, as the charge ejected from the diode is not influenced by the initial amount of electron-hole-pairs. The effective gain on a Geiger-mode diode ranges from $3 - 50 \cdot 10^5$.

2.2.3 Silicon Photomultipliers

To regain the possibility to measure light pulse amplitudes with Geiger-mode APDs in the form of counting photon multiplicities, several hundred to a few thousand such diodes are connected in parallel on single devices, called silicon photomultipliers. Such devices are capable of detecting single photons while maintaining a dynamic range from the number of pixels that can be hit simultaneously. The diodes and their quenching resistors are arranged on a single chip in a rectangular pattern of a few mm^2 surface area in total. A microscopic picture of a SiPM chip and single SiPM pixels is shown in Figure 2.5.

As all pixels are connected in parallel, the output signal is the sum of the signals of each individual pixel. Each single pixel releases the identical amount of charge upon



(a) *Full SiPM* **(b)** *Single SiPM pixels*

Figure 2.5: *Microscopic pictures of a SiPM and single pixels.*

firing. Thus the number of hit pixels per incoming light pulse can be calculated by the total measured charge divided by the charge of one single pixel firing. As all diodes are read in parallel no spatial resolution can be extracted from the signal of a single SiPM.

Dark Rate

Thermal excitation and quantum mechanical tunneling continuously generate electron-hole-pairs inside the depleted part of the diode. The avalanches and signals caused by these spontaneous processes are not distinguishable from real signals from incoming photons.

The tunnel probability increases with the strength of the electric field which is raised with higher bias voltage U_B. Thus higher bias voltage leads to a direct increase in dark rate.

However, the probability of several pixels randomly firing at the same time decreases rapidly with the number of concurrent pixels firing. This makes the dark rate, which can be up to 500 kHz for single pixel events, manageable at trigger thresholds above several pixels.

Quantum Efficiency

The quantum efficiency describes the probability of a single incident particle to create a charge avalanche. The quantum efficiency of a semiconductor detector generally depends on the energy and type of the incident particle as well as the diode's material composition. A higher electric field strength in the depleted area can prevent electron-hole-pairs from recombinating immediately, effectively increasing the quantum efficiency with the applied bias voltage U_B.

Gain Dependence on Temperature

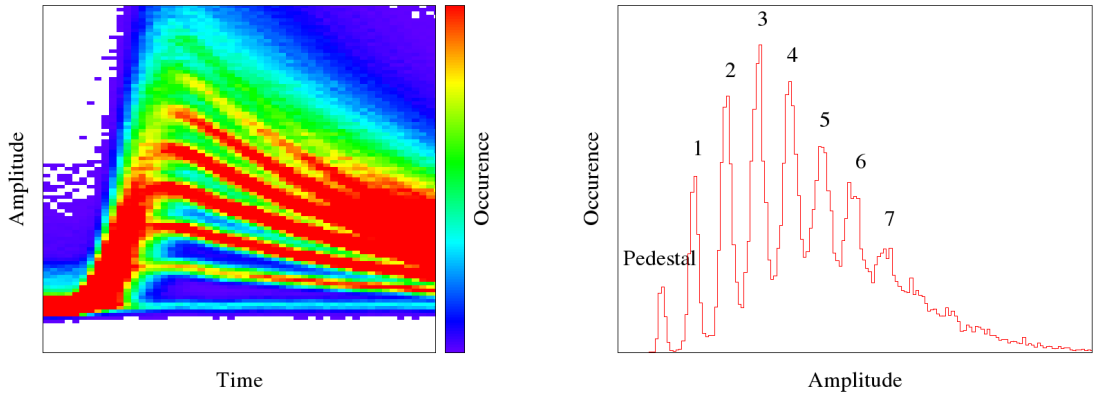
Although less dominant than avalanche-mode APDs, the gain of Geiger-mode APDs has a strong negative dependence on the ambient temperature in the order of $-1.7\%/\mathrm{K}$. This can be explained by thermic excitation of vibrational modes in the silicon lattice, increasing the probability of elastic interactions that transfer energy, but do not cause ionisation. This effectively increases U_{BD}, thus decreasing the total charge emitted per pixel. If the temperature effect on U_{BD} is well understood, U_B can be adjusted accordingly to keep the APDs gain constant.

Gain Calibration

Because of large individual variations in gain, optimal bias voltage and response to environmental factors, the gain factor of each SiPM in the AHCAL has to be monitored constantly to ultimately determine the amount of energy deposited per tile. As each pixel should emit the same charge upon being hit, the charge spectrum of a SiPM illuminated by short (∼ns), low-amplitude (2-4 average photon hits) flashes of light exhibits a quantisation of detected charges. This results in a spectrum composed of single peaks.

The first of these peaks represents the *pedestal*, the readout value for no signal, while the others are *pixel peaks*. Such *single photon spectra* (SPS) can be fitted, for example with a sum of single Gaussian distributions. From the distance between these peaks the SiPM gain can be extracted in arbitrary digitisation units. Together with the pedestal position, these can be utilised to convert measurements to the *pixel scale*. The pixel scale is a normalised measure of the detected light amplitude.

An example SPS is shown in Figure 2.6.



(a) *Time resolved distribution of signal shapes.*

(b) *Time slice of the spectrum shown in (a) with clearly visible single photon peak structure.*

Figure 2.6: *Single photon spectrum from small light amplitudes pulsed into a SiPM [33].*

MIP calibration

For physical interpretation of the recorded data, the pixel scale is not sufficient, as the mean number of pixels fired per incident particle may vary between tiles because of differences in tile-SiPM coupling quality and SiPM quantum efficiency. To calibrate this so called *lightyield* or *MIP response*, a spectrum of measured light amplitudes from incident MIP like particles has to be taken. To generate such signals, in principal true MIPs such as multi GeV muons would be needed, which are only available at hadron accelerator test beams. As a first simplification and good imitation of muons, multi GeV electrons can be used, as available from the DESY-II test beam facilities.

An easier way of generating such signals is by using a radioactive β-source in the MeV energy range and a trigger-scintillator downstream of the tile under test. Only electrons that lose relatively few energy in the tile are able to reach the second scintillator, thus triggering only on coincident signals from both scintillators gives signals similar to MIPs. This is realised in the *TileTester* [12] for single tiles, it is is however complicated to do for bigger setups like full calorimeter layers.

Application in Calorimetry

Compared to photomultiplier tubes (PMTs), SiPMs have crucial advantages regarding application in the AHCAL project. Most importantly SiPMs are substantially smaller than PMTs, enabling the integration of the light detection into the active layer of the calorimeter. Transferring the scintillation light out of the detector via fiber optic cables for external light detection is not feasible with the amount of channels foreseen for the AHCAL. SiPMs are also completely insensitive to magnetic fields, which is important as the AHCAL will be housed inside the detector magnet. Tests in magnetic fields up to 4 T did not show functional impairment [43]. The voltages needed to operate SiPMs are substantially lower than for PMTs. At this time, the cost for single SiPMs is in the range of tens of Euros per unit, already cheaper than PMTs. The price per unit is expected to go down until construction of the ILD. The achievable gains are similar between SiPMs and PMTs. Irradiation of SiPMs leads to increased dark rates, but the expected radiation dose received in a hadronic calorimeter is low enough to tolerate the resulting dark rate increase over its projected lifetime [32].

The use of SiPMs is also connected with certain disadvantages compared to PMTs. Bias voltages have to be set up and adjusted according to temperature for each SiPM within ± 10 mV. Gains differ between SiPMs and have to be constantly recalibrated. Noise rates at single photon threshold are large because of the high number of pixels on a single SiPM but are very well manageable for multi-pixel signals. Because of the finite number of pixels, SiPMs show non-linear behaviour for higher amplitude signals. This effectively increases the dynamic range of a SiPM beyond its number of pixels, but the energy resolution suffers from the systematic uncertainties of modeling the saturation curve and decreased effective ADC resolution.

2.3 SPIROC2b chip

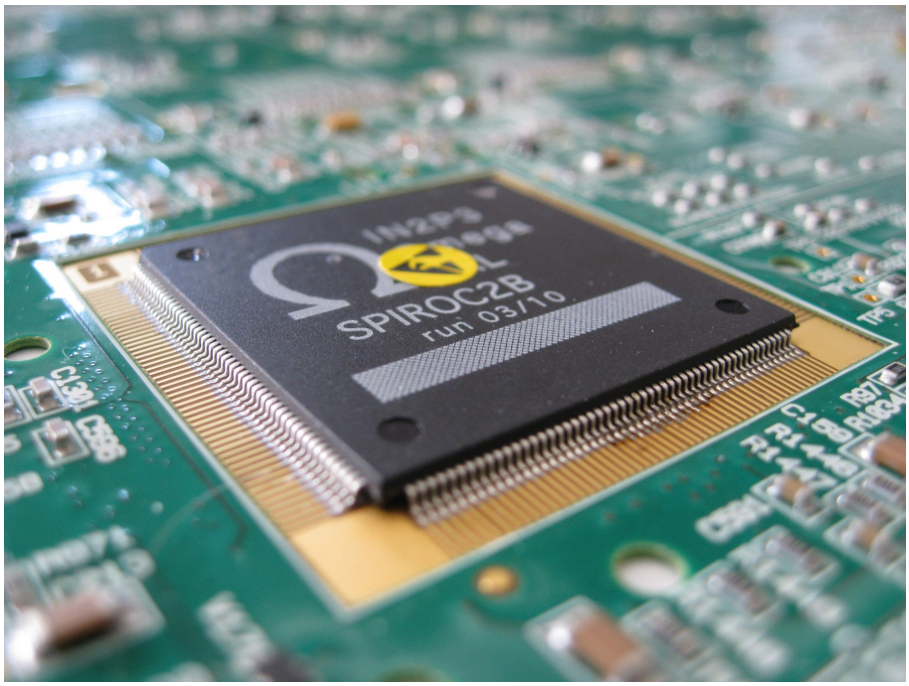


Figure 2.7: *A SPIROC2b ASIC mounted on a HBU PCB.*

The SPIROC (Silicon Photomultiplier Integrated ReadOut Chip) is an application specific integrated circuit (ASIC) in development by Omega at LAL, Orsay [13]. The chip is specified to provide individual bias voltages and readout for 36 SiPMs, including self-triggering, timing measurements and 12 bit digitisation resolution, while maintaining a very low net power consumption of 25 µW per channel. Setup of each chip is done via slowcontrol shift registers that are sequentially written from an external source. 16 events per channel can be stored inside analogue memory cells on the chip before digitisation and readout takes place.

In addition to the operation voltages (5 V for the input DAC, 4.5 V for the bandgap ADC voltage reference, 3.5 V for the rest of the chip), the timing of each acquisition, digitisation and readout step has to be supplied from external clocks, which have to be synchronised to an external main clock (which is called *DIF_CLK* on the HBU, see section 2.5).

All setups used in this thesis are equipped with the SPIROC2b version of the chip. First samples of the newest version SPIROC2c have arrived at DESY, but are not used for the hadron test beam setup. Figure 2.7 shows a picture of the chip integrated into the HBU.

2.3.1 SiPM Bias

For optimum performance each SiPM needs to be operated at its individual bias voltage, as listed by the SiPM manufacturer. Each channel comprises an 8 bit digital-analog-converter (DAC) at its input pin that generates a voltage U_{IDAC} between 0-5 V, as depicted in Figure 2.8. With the other SiPM pin connected to the global bias voltage U_B, the potential across the SiPM is $U_{Beff} = U_B - U_{IDAC}$.

The theoretical voltage resolution of this input DAC is $^{5\,\mathrm{V}}/_{256} \approx 20\,\mathrm{mV}$. As the DAC is constructed with minimal power consumption as the main goal, the non-linearity of the DAC curve is on the order of 1 LSB. The achievable voltage range is also usually less than 5 V (see section 4.2). The power consumption of the input DAC is very low, in the order of 1 µW.

While unprogrammed and during slowcontrol programming, the DACs are disconnected, floating the input pins without fixed potential. This is done not to damage the SiPMs from over voltage during programming.

2.3.2 Signal Path

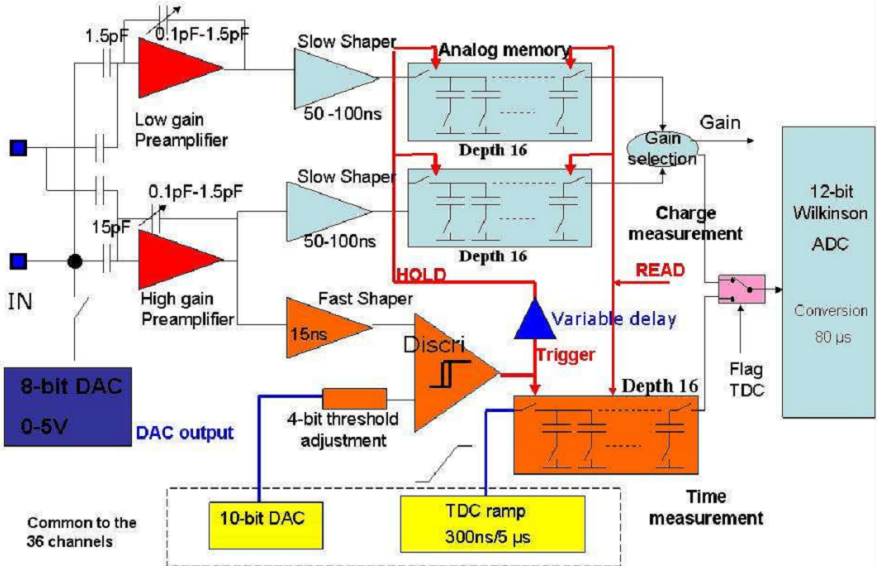


Figure 2.8: *Signal path of the SPIROC2 family. Some values written into the diagram are not up to date anymore.*

A schematic signal path diagram of SPIROC2b is shown in Figure 2.8. The signal is split into a high-gain and low-gain path, botch of which are sampled after a slow shaper (low-pass integrator) with a configurable time constant of 25-175 ns. The autotrigger signal is generated from the high-gain path, but using a faster shaper with a time constant of 15 ns. If the signal after the fast shaper exceeds a given trigger threshold voltage, the slow shaped signals are sampled (*hold*) after a configurable time delay (*hold time*).

This also triggers a TDC reading. After all 16 memory cells per channel are filled with sampled signals, or when externally initiated, the digitisation and readout processes are started.

Gain Modes

The SPIROC2b chip features two parallel gain paths. The high-gain mode is used for small signals and calibration up to 100 fired pixels, corresponding to around 6 MIPs. low-gain mode has a fixed 1:10 ratio compared to high-gain mode, extending the dynamic range up into SiPM saturation. The signals for both modes are generated in parallel from two separate charge preamplifiers with switchable feedback capacities for gain adjustment. Feedback capacities can be configured in a 6 bit register from 25 fF to 1575 fF in 25 fF steps. Individual channel preamplifiers can also be switched off in slowcontrol.

As only two memory cells can be digitised and read out per event, an auto gain feature is implemented on the chip to retain full ADC dynamic range while still being able to read out the TDC value. This is realised by switching to low-gain if the high-gain path is near or over the upper end of its dynamic range. An additional bit flags each event with the gain path used.

Digitisation

Digitisation of the data stored in the analog memory cells is performed by a 12 bit *Wilkinson ADC*. The memory cells are discharged by a constant current source while measuring the time until the voltage from the memory capacity drops below a threshold, which is proportional to the initial charge in the memory cell.

2.3.3 Trigger Modes

SPIROC2b can run in fully auto triggered mode and also excepts external triggers. Additionally an external validate can be used in combination with the auto trigger, so that only events that are coincident with an external trigger are saved.

Auto Trigger

The global trigger threshold can be configured for the whole chip via a 10 bit register with 4 bits of fine tuning per channel. The first triggered channel in a given DIF_CLK cycle triggers sampling of all 36 channels. Channels triggering after the first in the same DIF_CLK cycle only overwrite their own memory cell. For each event every channel that exceeded the trigger threshold carries the HIT_BIT flag.

External Trigger

An external trigger signal can also be fed directly into SPIROC2b. For an externally triggered event all HIT_BIT flags are set.

However, even in external trigger mode, the auto trigger can not be disabled completely. Even for the highest possible global threshold some channels will fire the auto trigger. As the hold times will usually differ between external trigger and auto trigger (because of different propagation delays), an auto triggered event gives wrong but otherwise indistinguishable readings. This makes external trigger not usable in test beam conditions. For the current use this poses no problem, as no meaningful TDC information can be obtained in external trigger mode.

External Validate

To combine the advantages of external and auto trigger modes, external validate allows to only save events that are coincident with an external signal (e.g. from a scintillator). In normal auto trigger mode the memory cell pointer is increased to the next memory cell for all channels after each DIF_CLK cycle, if at least one channel was triggered. In externally validated mode this memory cell pointer is decreased again if no external trigger signal was registered at the same time. The timing for this validation signal has to be very precise to work properly. Lab tests have shown the external validate mode to work, but ongoing tests at the DESY electron test beam will have to show the feasibility of running the timed hadron test in external validate mode.

For the external validate mode to work at all, the DIF_CLK frequency has to be reduced from the 5 MHz used in ILC mode, to around 250 kHz as used in test beam mode. The feature was implemented specifically to reduce the amount of noise acquired during test beams, which usually feature lower acquisition rates than projected for the ILC.

2.3.4 TDC

The SPIROC2b TDC chip is implemented as a time to amplitude converter. A linear voltage ramp is generated which is sampled and stored in a memory cell similar to the ADC. At the beginning of each DIF_CLK cycle the voltage ramp has to be reset, which creates deadtime in the TDC. To circumvent that reset deadtime, two separate voltage ramps are used (*dual ramp TDC*) which are activated at alternating clock cycles. That gives each ramp time to reset while the other one is ramping up. The switching between ramps is done by a multiplexer. A schematic for this is given in fig. 2.9.

The TDC voltage slope can be switched between a steep and shallow slope. The steep slope is designed for use in ILC-like conditions, with the ramp length matching the ILC collision frequency of 5 MHz. For operation in test beams the slower ramp is used to minimise relative deadtime from multiplexing.

2.3.5 Power Pulsing

Even with the low power dissipation design of SPIROC2b, the power budget cannot be met in continuous operation of the chip. To improve on this, only the parts of the chip needed for each individual readout phase are powered. For example the ADC only needs to be switched on during digitisation, while the full analog part can be switched

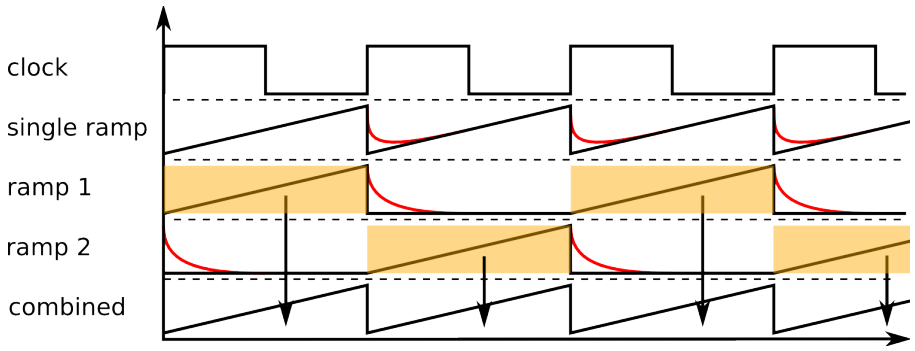


Figure 2.9: *Schematic working principle of a dual slope TDC, reset effects are shown in red.*

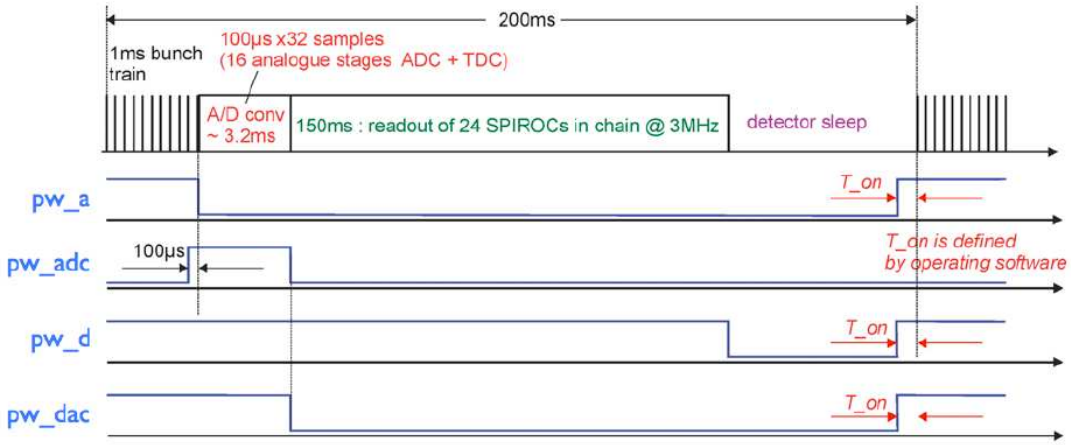


Figure 2.10: *Power pulsing scheme relative to the ILC bunch timing structure. [39]*

off during digitisation and data transfer between bunch trains. A proposed scheme for activation of different parts of the chip relative to the ILC bunch train structure is given in Figure 2.10. The signals labeled *pw_* control the power supplies of the corresponding part of the chip. *pw_a* powers the analog part, consisting of preamplifiers, shapers and memory cells. It can be switched off outside of data acquisition and thus has a very low duty cycle. The digitisation part is supplied by *pw_adc* after acquisition. The digital part of the chip can only be switched off via *pw_d* when the chip is idle between bunch trains. All internal DACs needed for acquisition and A/D conversion are controlled by *pw_dac* and switched off during data transfer. The input DAC controlling SiPM bias voltages is always switched on to minimise the chance of damage to the SiPMs from overvoltage.

2.3.6 Known Problems

As SPIROC2b is a prototype chip, some functionality issues are to be expected. Most of the observed issues pose problems for standard operation, but can be circumvented by extra effort.

First Event

The event in the first memory cell is always lost between acquisition, digitisation and data transfer and thus has to be ignored by the data acquisition (DAQ) software. This renders only 15 of the 16 total memory cells usable. Also around 5-10% of the remaining events transfer with an ADC value of exactly 0 instead of the signal amplitude (*zero-reads*). This can easily be recognised in any analysis of the data, posing no problems except for missed statistics.

TDC Multiplexer

The TDC multiplexer responsible for switching between TDC ramps induces a TDC deadtime of up to 50 ns, 25% of the total ramp length in ILC mode. This makes the ILC mode completely unfeasible for use in timed test beams at the moment. Also the TDC does not reach its specified resolution goals because of non-linearities in the voltage ramp. The relative deadtime is much less for the TDC test beam mode, which is preferred for a timed test beam anyway.

Pedestal Shift

A bigger issue on SPIROC2b is the *pedestal shift*, which shifts the global pedestal level depending on the total charge injected into the inputs of the chip. If several channels saturate at once, the pedestal level can even go into the negative ADC region, reading as zero. This poses a problem mainly for calibration measurements, as usually the pedestal shift expected for signals from typical test beam measurements is only in the range of a few MIPs at once, which is low enough not to be a problem. For calibration measurements several workarounds have to be used. It is possible to calibrate channels in several runs with only parts of the channel active at a time. Lowering trigger rates and possibly signal amplitudes also helps in reducing the effect. A quantitative analysis of the effect is presented in section 4.6.

Input DAC

The input DACs greatly differ in slope and mostly do not reach the full specified dynamic range of 0-5 V. This makes individual measurements of each input DAC response curve necessary, for which a fast procedure has already been devised (see section 4.2).

SPIROC2c

A new release of the chip (SPIROC2c) has been issued to fix most of these problems. First tests at DESY indicate that first event problems and zero-reads are no longer present. According to the developers the critical pedestal shift has been rectified, but confirming tests are still underway.

2.4 Detector Integration

Integration of the AHCAL barrel into the ILD detector is planned with the calorimeter being divided into two sections along the beam axis, which each have a length of 220 cm. Each section is subdivided into 16 half-octants, as shown in Figure 2.11. One half-octant

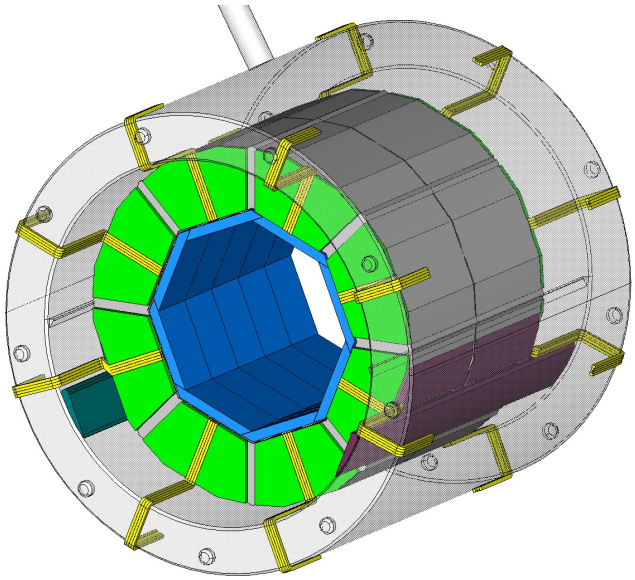


Figure 2.11: *Integration schematic of the AHCAL barrel into the ILD detector volume.*

covers the full height of the AHCAL of 110 cm with 48 layers of steel absorbers and the corresponding number of active layers. The active layers are divided into three parallel *slabs* of six sequentially connected PCBs (HBU) each. At the front face of a sector, one DAQ interface board per layer provides connection to the data acquisition system and power supplies.

2.5 The HCAL Base Unit

The active layer of the AHCAL engineering prototype consists of HCAL Base Unit (HBU) boards [14]. Each HBU of the dimensions $36 \times 36\,\mathrm{cm}^2$ carries 4 SPIROC chips, summing up to 144 scintillating tiles total. As the total height of the active layer is constrained by

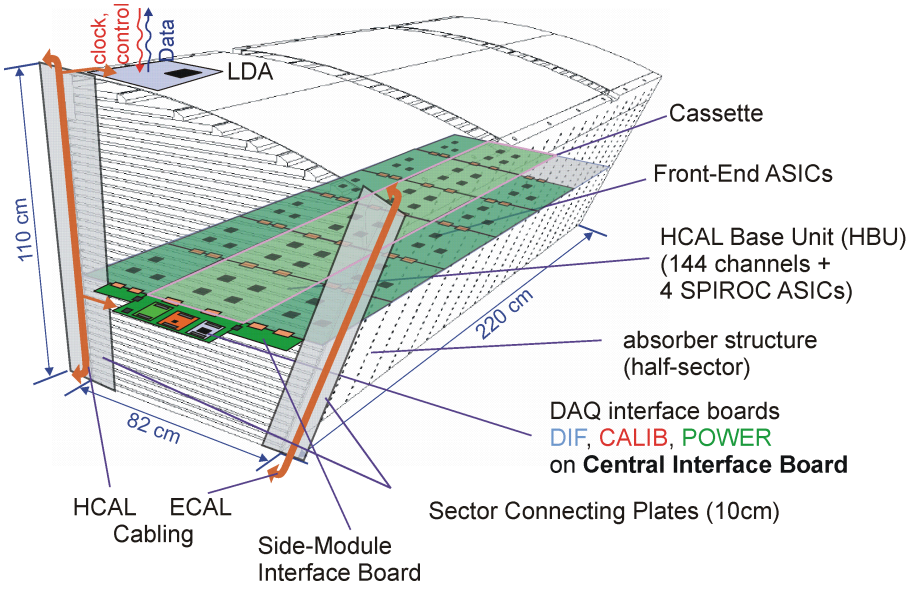


Figure 2.12: *ILD AHCAL half-octant, depicted with a single active readout layer.*

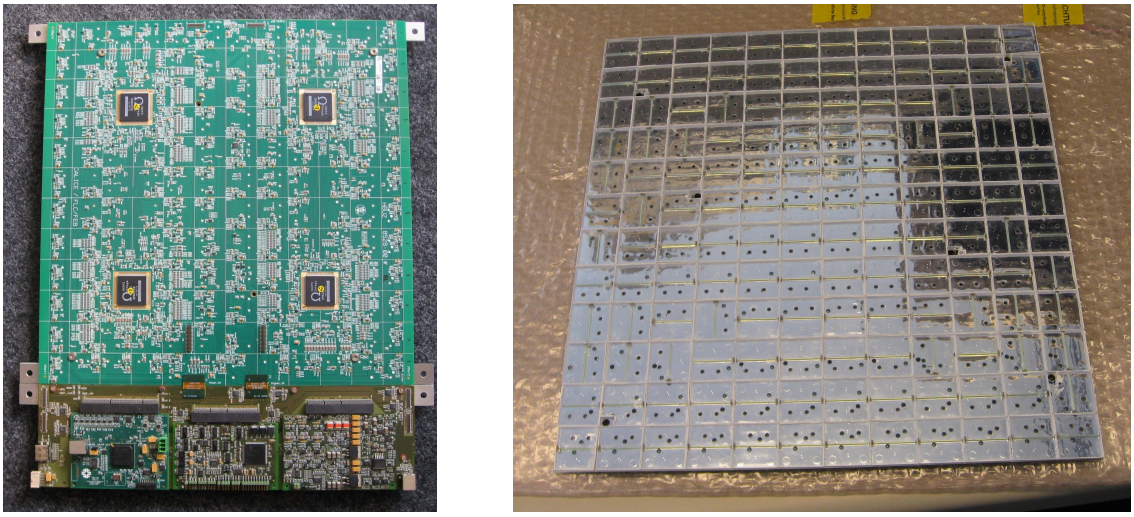
the gap between absorber plates, the total height of the PCB and electronic component cannot exceed 2 mm, which is shown in Figure 2.14. The HBU PCB is thus manufactured at only 0.8 mm thickness, around half of a standard process. Still the plastic packaging of the SPIROC2b chip, with its height of 1.4 mm, would not fit inside the absorber gap. To still be able to use the standard ASIC packaging the ASIC is lowered 0.5 mm into milled pockets on the PCB (see Figure 2.7). Specifically manufactured flat flex cables with extra-thin connectors are used for data and power links between HBUs of one slab, as height limitations also apply there (see Figure 2.15).

The scintillating tiles are mounted beneath the HBU, held into place by alignment pins on the tiles, as shown in Figure 2.3, snapping into holes on the HBU. To minimise problems with slightly varying tile dimensions, a 0.1 mm gap is planned between tiles. Laser cut reflective foil is applied to the tile-side of the HBU, to reflect back light exiting a tile, as shown in Figure 2.13.

Three different HBU versions were produced until now. The first version HBU1 and two revisions of HBU2. The current version is thus the second revision of HBU2.

2.5.1 Central Interface Board

One Central Interface Board (CIB) per AHCAL layer is responsible for control of the SPIROC ASICs, voltage supply and management of the calibration systems while providing power and signal connections to the three slabs of one layer. The central slab directly connects to the CIB, the outer slabs are connected via *side interface boards*. The functionality of the CIB is implemented on three mezzanine PCBs, fulfilling specific tasks each, as shown in Figure 2.16.



(a) *HBU top view connected to CIB.* ***(b)*** *HBU bottom view with mounted scintillator tiles.*

Figure 2.13: *Pictures of HBU2.*

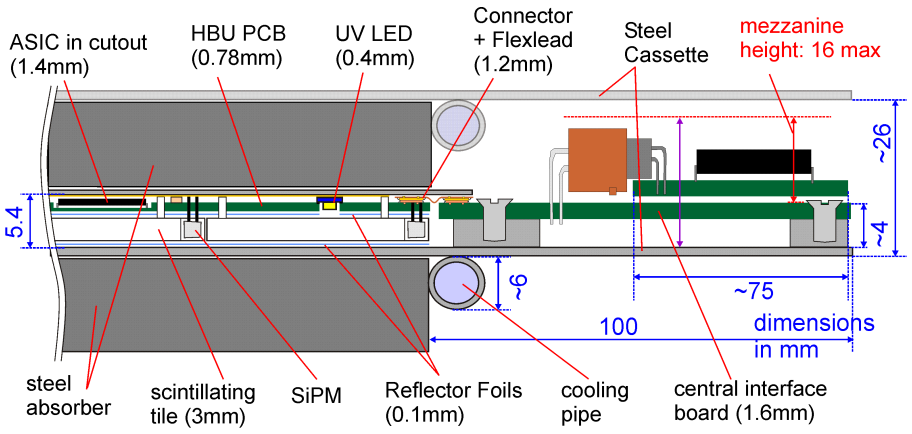


Figure 2.14: *Schematic cross section of an active calorimeter layer, including CIB.*

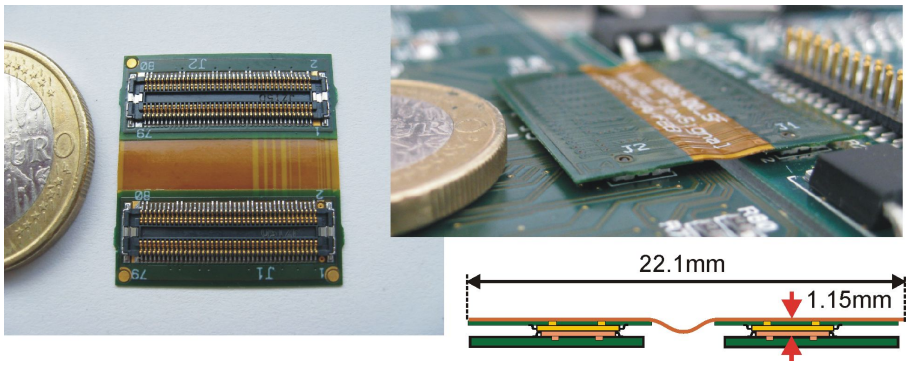


Figure 2.15: *Custom flex leads for connection between HBUs, HBU to CIB and CIB to SIB.*

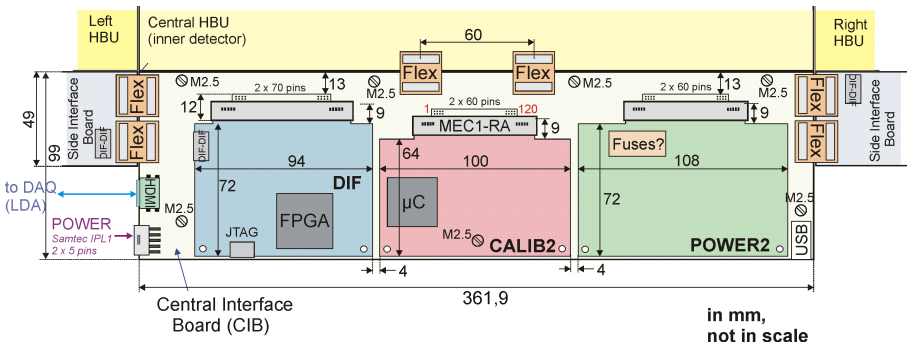


Figure 2.16: *Central Interface Board schematic.*

POWER2 Board

The POWER2 board generates most voltages needed for operation of the HBU from supply voltages of 6 V, 12 V and a variable high voltage. The high voltage supply is around 50 V, depending on maximum needed SiPM bias voltage. Output voltages generated from the 6 V input are 3.3 V, 4.5 V and 5 V for the SPIROC chips, an additional 5V̇ line for USB operation and 3.3 V for the LED and charge injection systems. The 12 V input is only used for the CALIB2 calibration DAC. In addition to voltage generation, the POWER2 board also enables power pulsing the HBU electronics as explained in subsection 2.3.5.

Up to three different high voltages HV1-HV3 can be generated on the POWER2 board by setting up the HV regulators via soldered voltage dividers. Each HBU is supplied with all three of these high voltages and it has to be set via soldering jumpers on each HBU, which one is used as U_B. This enables one layer to cover a wider range of SiPM bias voltages than the range of the SPIROC input DACs only, if SiPMs are equipped onto individual HBUs sorted by bias voltage. To compensate for ambient temperature influence on SiPM gains, the bias voltage supplies can be tuned down from the DAQ software.

CALIB2 Board

The LED gain calibration system (as further explained in the next section) on the HBU is controlled by the CALIB2 board. A NXP LPC2214 microprocessor provides short trigger pulses of 1..255 ns and a calibration voltage DAC in the range of $V_{Calib} = 0..10$ V to the LED system integrated on HBU2. The trigger pulses are synchronised with the triggers sent to the SPIROC chip by the DIF and can thus be used for SiPM gain calibration.

DIF Board

The DIF (Detector InterFace) manages communication between SPIROCs, POWER2, CALIB2 and the off-detector side. The Xilinx Spartan3-2000 FPGA on the DIF generates DIF_CLK and all SPIROC steering signals, including power pulsing if enabled. The FPGA also handles data transfer to the DAQ system, which currently is only implemented via USB to a LabView software (see section 2.7). Implementation of other data transfer paths is foreseen and can be implemented into the FPGA firmware, making the DIF a core component independent of the connected DAQ system.

The DIF also features inputs for external trigger, spill, and validate signals.

2.6 LED calibration system

For continuous calibration of the SiPM gain and monitoring of the SiPM saturation behaviour inside the calorimeter, short light pulses have to be generated and distributed into the scintillator tiles. A system based on individual LEDs per channel has been developed at Wuppertal University during the last years and is implemented on the current

revision of the HBU. Another concept developed by Prague University aims to distribute light pulses into multiple tiles via a single notched fiber [15].

2.6.1 Requirements

The SiPM calibration system hast to cover a large range of LED amplitudes. To measure single photon spectra for SiPM gain calibration, small light amplitudes in the range of 1 – 5 fired pixels per pulse are needed. The light pulses have to be shorter than the integration time of the preamplifier of the SPIROC input stage of 25 – 175ns and not longer than the time constants of scintillator tile and WLS fiber, thus 10 ns duration or less are required. For cross-calibration between different gain settings as well as calibration of SiPM saturation, much higher amplitudes up to several thousands of single-pixel amplitudes are needed. Specifications regarding pulse width can be less strict than for the generation of SPS, but still should not exceed 50 ns.

The light amplitude between different tiles should be as homogeneous as possible to minimise the number of calibration configurations needed to calibrate the full detector. If homogeneity can not be ensured directly from the system design, a mechanism to equalise the light amplitudes across different channels should be included.

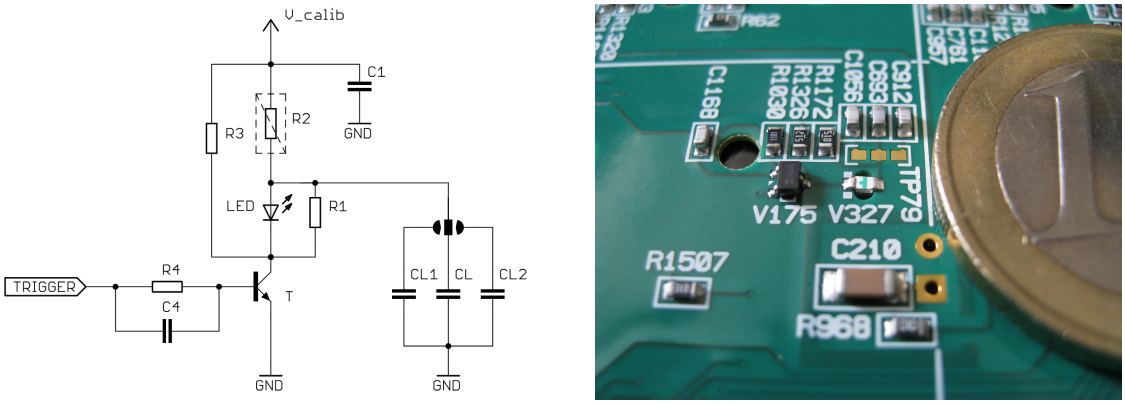
Depending on how the calibration scheme is implemented into the ILD operation, the possible repetition rate should go up to 1 MHz, to fill up empty memory cells with LED events without substantially increasing the SPIROC power-on duty cycle to keep the power budget.

As the system needs to be scalable to a full ILD calorimeter, cost per channel must be low enough to make a full calorimeter calibration system feasible. A small PCB footprint helps the integration onto the HBU. A system with centralised light sources (e.g. one per layer) also needs to be integratable into the calorimeter concept, as most space usable for electronics inside the calorimeter is already accounted for.

2.6.2 Implementation

The circuit diagram and a photo of a single channel of the Wuppertal LED calibration system is given in Figure 2.17. The primary components consist of the capacitor CL, transistor T and a single LED per channel. CL is charged by V_{Calib} , and discharges through the LED if the transistor is closed by a trigger pulse. The emitted light amplitude directly depends on the charge flowing through the LED and thus on V_{Calib} and the capacity of CL. The exact values for each component are tabulated in Table 2.1. The influence of each extra component and the optimisation of their values in thoroughly explained in [33] and thus not discussed in detail here.

It is notable that the chosen LED emits in the UV spectrum, as that type was one of the few available LEDs emitting light out of a single pn-junction (*single quantum well*) in contrast to the more common *multi quantum well*, which have a higher overall light output. Single quantum well LEDs produce shorter pulses, as multiple pn junctions may start emitting at different potential differences and different timings. The production of the LED type used has been discontinued shortly after being picked for the EPT.



(a) *Circuit schematic [33].* ***(b)*** *Photo of implementation on HBU2.*

Figure 2.17: *Single channel LED pulser circuit.*

As the chosen LEDs may vary in light output, the extra capacities CL1 and CL2 are included to equalise the LED response by manually closing the soldering jumpers, connecting one or both in parallel to CL. The global output amplitude can be controlled via V_{Calib} which is generated by the CALIB2 board.

The LED trigger generated by the CALIB2 board is transferred to the HBU via a Low Voltage Differential Signal (LVDS) line. As the typical output current of the used LVDS receiver is not enough to drive 144 LED circuits simultaneously, its output is connected to 8 operational amplifiers (OPAMPs), which trigger 18 LED circuits each. The schematic of this HBU implementation is depicted in Figure 2.18.

2.7 Software

The data acquisition system used for all tests in this thesis is based on a USB connection with a LabView software running on standard PCs. This system was first devised as lab testing environment for the earliest HBU revisions and SPIROC chips, but has since grown into the only DAQ software available for the EPT. Despite the limited data rate of the USB connection, even beam tests are possible with reduced acquisition rate.

DAQ Software

The main software interface is shown in Figure 2.19. From the software all DIF and CALIB2 parameters such as triggers mode, trigger delays and LED calibration voltage DACs are set up. Slow control files generated by the slow control software described below can be loaded into the SPIROC chips.

For each measurement the number of memory cells to fill before readout, as well as the number of readout cycles can be configured. The output data format is a human-readable text format with one line per single event. As no zero-suppression is imple-

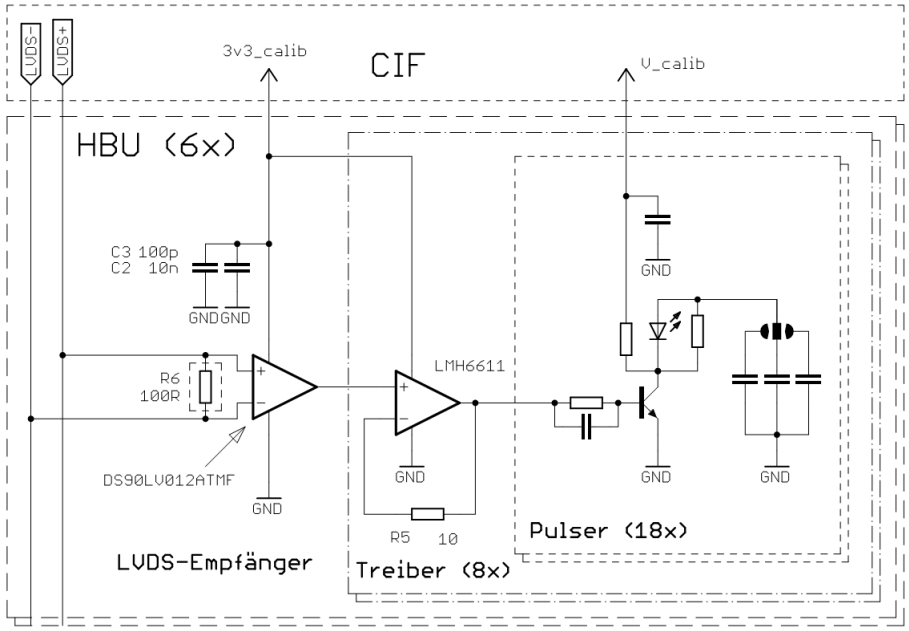
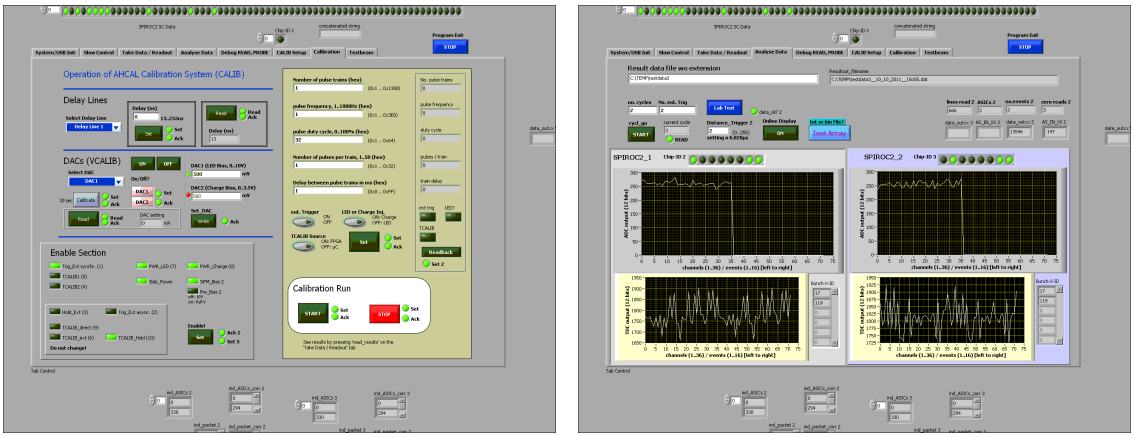


Figure 2.18: *Implementation schematic of the LED calibration system on the HBU2 [33].*



(a) *Calibration and trigger setup.* ***(b)*** *Online monitor.*

Figure 2.19: *LabView front panel of the EPT USB DAQ software.*

Table 2.1: *Components of the LED system assembled on HBU2.*

Component	Value
CL	150 pF
CL1	87 pF
CL2	22 pF
C1	10 nF
C4	50 pF
R1	87 Ω
R2	not assembled
R3	5 kΩ
R4	1 kΩ
LED	LEDtronics SML0603-395-TR
T	BFR183W

mented into the DAQ, one external trigger produces 36 lines of data per SPIROC. In parallel to the SPIROC read out, external slow control data can be written into the output files. In the current implementation, the temperatures measured by sensors on each HBU and POWER2 board are included, usable for SiPM gain compensation and temperature monitoring.

The readout speed of the DAQ system is around 0.1-0.2 s per ASIC, so for the hadron test beam layer consisting of 16 SPIROC2b chips and 576 tiles a total calorimeter readout rate of $\approx \frac{1}{16 \cdot 0.15\,\mathrm{s}} \cdot 16 \approx 6\,\mathrm{Hz}$ is achieved. For operation in the ILC beam structure, the readout rate is specified as 80 Hz.

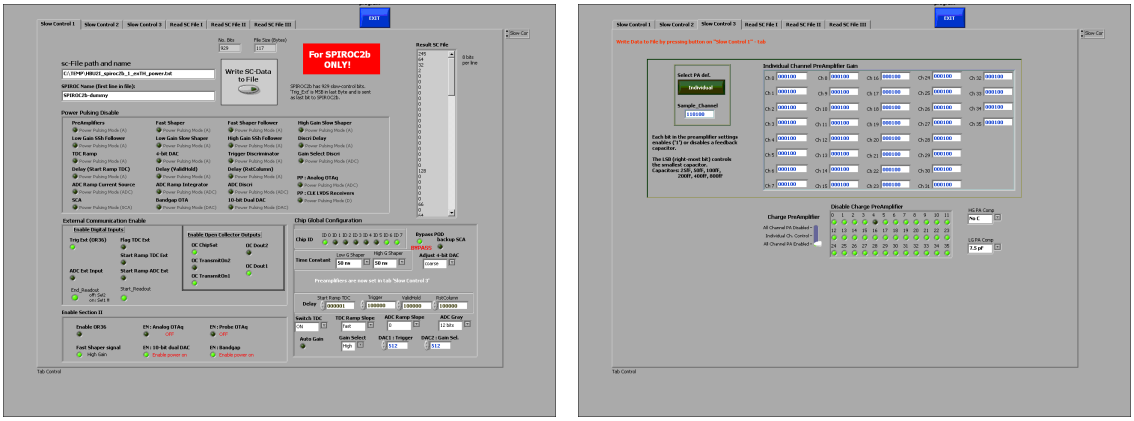
Slowcontrol

In the slowcontrol software, shown in Figure 2.20, all properties of the SPIROC chip as internal delay lines, trigger thresholds and preamplifiers can be set up and written into text files. The text files generated can be transferred into the SPIROC chips from the main DAQ software. Configuration files can also be read back to verify configurations.

Every slowcontrol bit of the SPIROC chip can be set up in the software. For example the preamplifier capacitor bitmask can be set up for each channel individually, including disabling single or all preamplifiers (see Figure 2.20.(b)).

Scanning Utility

As neither main DAQ nor slowcontrol are designed to perform several consecutive measurements while scanning through a parameter, an external tool was developed for that task. The direct implementation of that functionality into the main DAQ would further bloat the software and raise issues with scanning over values set in slowcontrol. Via



(a) *SPIROC slowcontrol main setup.* ***(b)*** *Preamplifier setup page.*

Figure 2.20: *LabView front panel of the EPT slow control software.*

the LabView internal *VI-Server* feature, a direct interface into both main DAQ and slow-control software is established, which enables the direct modification of variables inside these programs. This is *not* an elegant or sustainable way of LabView programming, but has proven to work. In the current version, the values of V_{Calib} , the hold time, input DACs, preamplifier feedback capacitors and the global trigger threshold can be automatically scanned with a configurable number of taken events per setting. For example this software enables the automated measurement of LED calibration runs with different LED voltages with high statistics over night without manual intervention. A screenshot of the application front panel is shown in Figure 2.21.

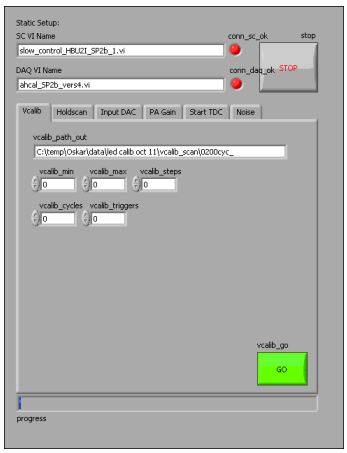


Figure 2.21: *LabView front panel of the EPT slowcontrol scan utility.*

3 LED Calibration System Tests

During development at the Wuppertal, the LED calibration system has only been tested in single channel pulser circuits without integration into the HBU. Such PCBs contain one pulser circuit each, supplied from commercial external voltage supplies and triggered by a commercial grade pulse generator. Under these conditions, the optimal choice of LED type and other components could be derived [33]. This optimised circuit is implemented into the HBU2 as explained in section 2.5.

Using the LED system, tests of the full HBU signal chain from the scintillator tile through signal sampling and digitisation can be performed. This is primarily used to judge the performance of SiPM gain calibration in the EPT, but also for different calibration tasks, some of which were not even thought of during development of the system.

In addition to the full readout chain approach, the Wuppertal LED system test stand is used to determine LED pulse quality of each individual channel. For this purpose it has been fitted with a PMT which can be automatically positioned over each LED to capture single pulse shapes.

All SPS measurements are performed on the same HBU2 (Revision 1) in high gain mode. It was equipped with 72 previously unused tiles from ITEP for full readout chain tests at DESY. After that the PCB was used in Wuppertal while the tiles remain at DESY and are a equipped in the timed hadron test beam layer.

This chapter describes tests and results obtained from measurements with the full EPT readout path. Also first results from the modified test stand are presented.

3.1 Gain Calibration

Gain calibration is done by flashing small amplitude light pulses into each scintillator tile mounted on the HBU. During operation the light amplitude can be controlled by setting the V_{Calib} DAC in the DAQ software.

The time between pulses can also be configured and, for purposes of this tests, has been set to the maximum value of 1.741 ms. Values near the maximum pulse frequency do not give enough time for the C_L capacitors to fully recharge after each pulse.

3.1.1 Single Channel Calibration

For an optimal SPS from a single channel, V_{Calib} should be set up to activate between 1-5 pixels per pulse on the given channel, resulting in a SPS as shown in Figure 3.1. A higher light amplitude with more pixels fired is harder to fit, as the individual pixel peaks start smearing into each other, and thus takes a disproportional amount of statistics to get

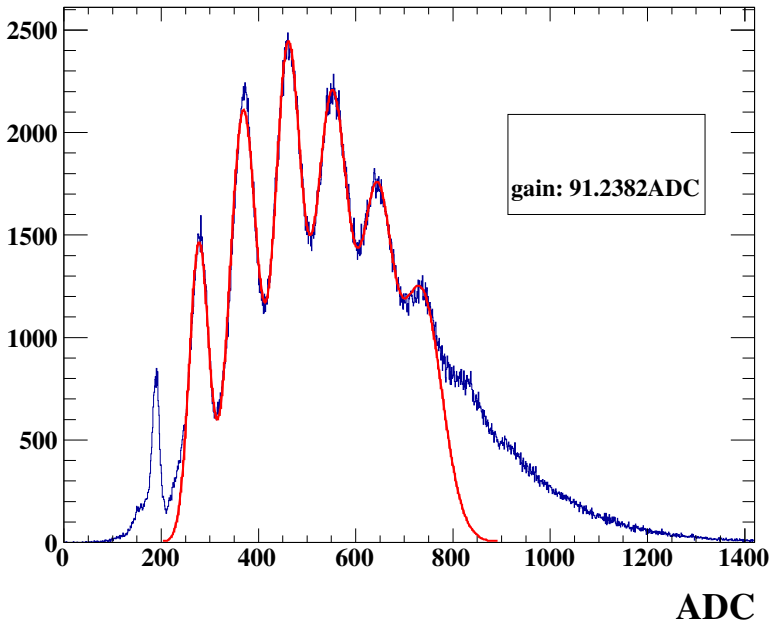


Figure 3.1: *High statistics single photon spectrum fitted with multiple gaussian functions.*

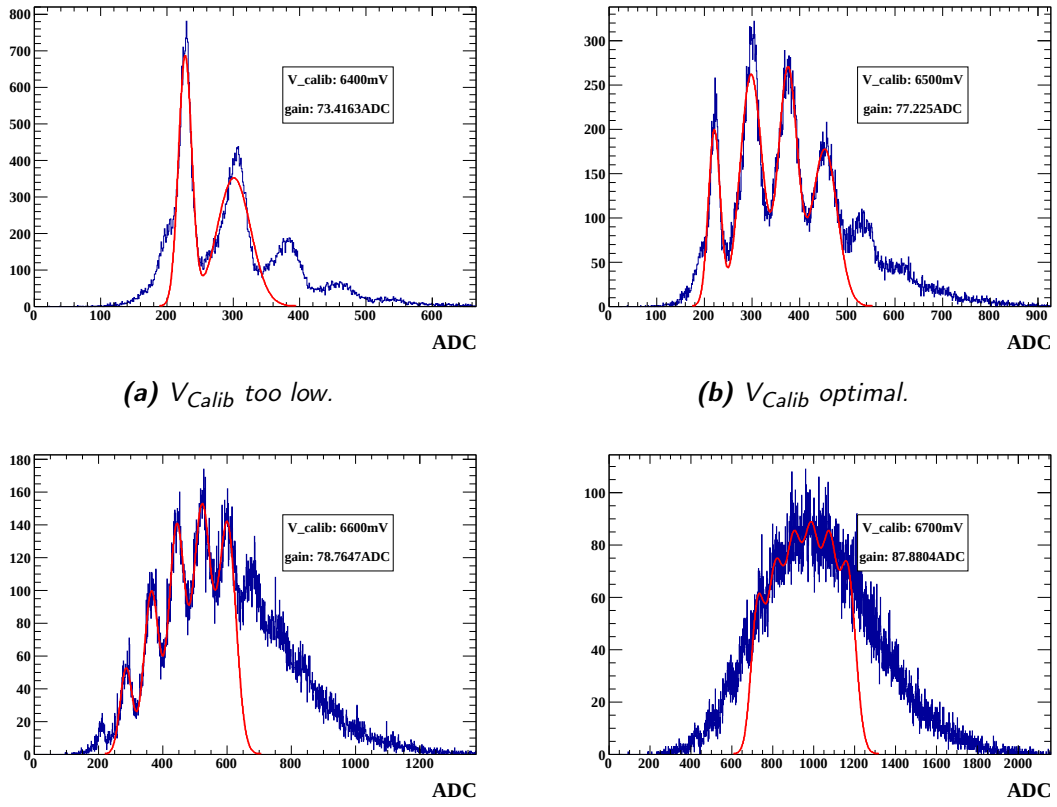
fitable results. If the light amplitude is too low, not enough pixel peaks are generated at all, resulting in only the distance between pedestal and first pixel to be fitable. Because of the asymmetric pedestal shape, this biases the fitted gain towards lower values. Depending on the readout technology, the distance between pedestal and first peak might not reflect the true gain, as charge preamplifier response is not necessarily linear for very small charges. Figure 3.2 shows the SPS from the same channel for different values of V_{Calib} .

3.1.2 Multi Channel Calibration

For the operation of the detector, all channels have to be calibrated at the same time to keep up with changing environmental conditions.

The *threshold voltage* at which a channel starts to emit enough light to create a signal discernible from the pedestal differs between channels. Reasons for that and possible counteractions are discussed in section 3.2.

To decrease the total time needed for calibration, the number of events per voltage setup can be decreased by adding up spectra of different V_{Calib} setups of the same channel. In this case only the sum of all spectra is fitted once. The total number of events (and



(a) V_{Calib} *too low.*

(b) V_{Calib} *optimal.*

(c) V_{Calib} *high.*

(d) V_{Calib} *too high.*

Figure 3.2: *Single photon spectra of the same channel at different V_{Calib} values containing 64000 events. The spectrum shown in (a) is not well described by the applied fit, the fit in (d) gives a wrong result.*

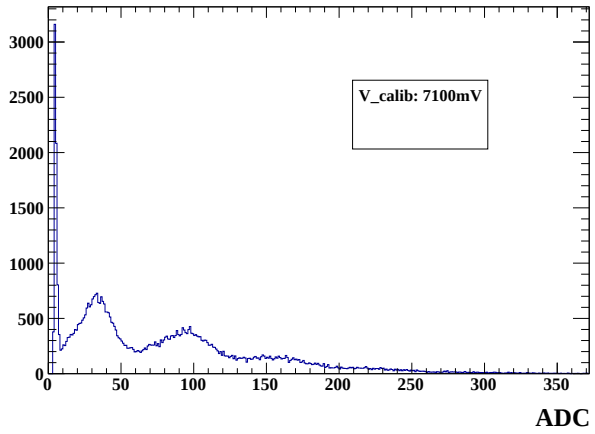


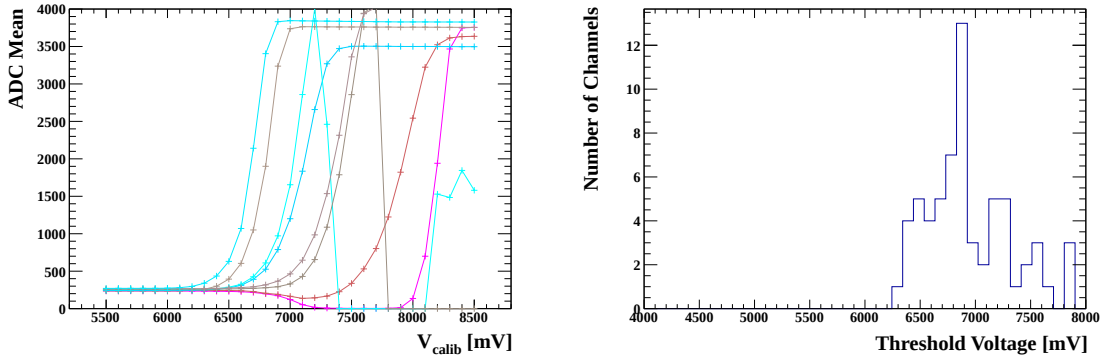
Figure 3.3: *Single photon spectrum showing a pedestal effectively shifted into the negative ADC region, CL = 150 pF.*

hence time for calibration) needed is less than with the simple approach described before, as the number of events for the summed spectrum can be considerably less than the total events needed for several independent fits while achieving similar gain determination accuracy. This calibration scheme has been successfully used in the LED system of the CALICE AHCAL physics prototype [36] (also see section 2.1).

However the pedestal shift effect of the SPIROC2b makes this scheme of calibration impossible, as the peak positions shift downwards for higher values of V_{Calib} as the average preamplifier load rises (see section 4.6 for further information). To keep the calibration time minimal, the step width used to scan V_{Calib} and the statistics per run have to be chosen carefully. Lab measurements have shown, that for CL = 150 pF, fitable spectra can usually be obtained for a single channel within a V_{Calib} window of 200-300 mV, limiting the maximum V_{Calib} step width to 100 mV. Depending on the mean number of pixels fired, about $10 - 50 \cdot 10^3$ events are needed for a good fit. Figure 3.2 shows that at 64000 events the spectrum for a lower V_{Calib} is very smooth, while for the highest shown voltage the spectrum has visibly more fluctuations per bin.

Even when taking full statistics for each calibration voltage, pedestal shifting heavily interferes with gain calibration. Apparently the pedestal value can effectively be shifted to *negative* ADC values, resulting in cut-off SPS as shown in 3.3. As the exact preamplifier problem leading to pedestal shifting is not known, its influence on the preamplifier gain is not predictable. It is possible that not only all ADC values are shifted, but also the ADC scale is warped, effectively rendering SPS taken in that region useless.

Plotting the mean ADC value versus V_{Calib} gives a general understanding of the range in V_{Calib} needed to cover all channels, as shown in Figure 3.4. Extracting the V_{Calib} *threshold voltages* where the mean ADC value exceeds 400 tics, which is roughly the range where good SPS are located, shows that the range of 6000-8000 mV has to be scanned



(a) *LED response.*

(b) *Threshold voltage distribution. Mean = 6967, RMS = 394.1,* $\frac{RMS}{mean} = 0.057$

Figure 3.4: *LED response in ADC counts versus* V_{Calib} *voltage and extracted voltage threshold distribution at CL* $= 150\,pF$*. The drop in LED response from around 7000 mV on is caused by pedestal shift.*

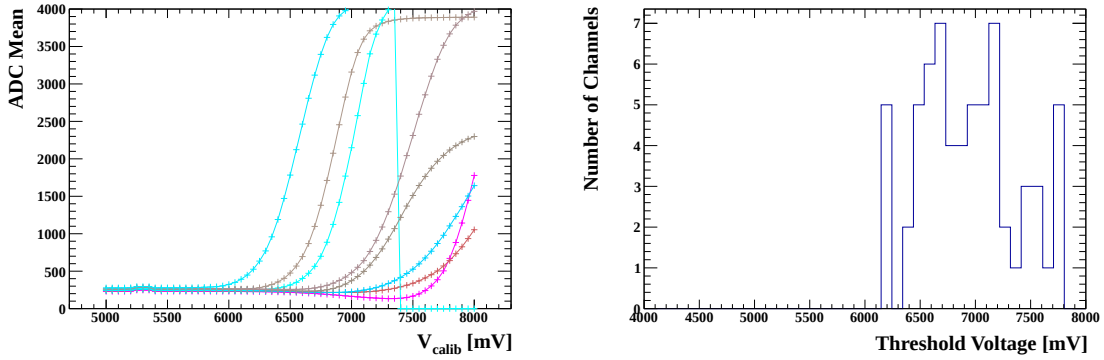
in order to calibrate each chip. The LED response plot also shows the pedestal shift effect.

Some channels dropping from ADC values near saturation down to near zero is caused by the autotrigger on SPIROC2b. As it is not possible to completely disable all auto triggering, the AT threshold is set to maximum. In the range of preamplifier saturation, sometimes the auto trigger fires randomly. This only happens for very large signal amplitudes higher than the saturation level and thus does not influence measurements.

Scanning the V_{Calib} range of 6000 mV – 8000 mV in steps of 100 mV leads to $21 \cdot 64000$ total events to be taken for a full calibration run of the two chips used in this setup, taking around 8 hours to complete. By improving DAQ timings in LabView and the DIF board, a slight increase in the readout rate might be possible. The biggest potential for decrease in calibration time lies in reducing the amount of voltages needed. As the V_{Calib} distance between measurements should not be increased as to obtain at least two fitable SPS per V_{Calib} scan for crosscheck, the spread of LED threshold voltages has to be decreased.

3.2 LED Response Equalisation

To equalise the LED response between channels for a given V_{Calib} voltage, the extra calibration capacities CL1 and CL2 can be switched in parallel to the main capacity CL via soldering jumper, increasing the total calibration capacity. This increases the LED current during a pulse, as all charge accumulated in the capacitors is forced through the LED. The light amplitude emitted from the LED is positively correlated, though not necessarily linearly, to the current going through. Thus a decrease in LED threshold voltage is expected when adding a capacitor parallel to the main calibration capacity.



(a) *LED response.*

(b) *Threshold voltage distribution. Mean= 6937, RMS= 448.1,* $\frac{RMS}{mean} = 0.065$

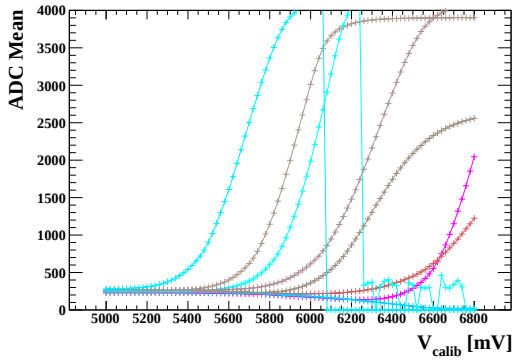
Figure 3.5: *LED response in ADC counts versus* V_{Calib} *voltage and extracted voltage threshold distribution at* $CL = 172\,pF$.

With the main calibration capacity CL = 150 pF and the equipped extra capacities of CL1 = 22 pF and CL2 = 87 pF, total calibration capacities of 150 pF, 172 pF, 237 pF and 259 pF can be configured. Performing a V_{Calib} scan, as described in the previous section, for each possible setup yields the LED response curves and voltage threshold distributions given in Figure 3.5, 3.6, 3.7. As expected, the threshold voltages shift down to lower values for higher calibration capacities, as does the width of each distribution, as described by its RMS. As the the LED response slopes get steeper, this width is not a suitable variable for judging the number of needed V_{Calib} values on its on, because of the finer voltage steps needed to achieve the same granularity in emitted light amplitudes. The *relative width* $^{RMS}/_{mean}$ is a more suitable observable for such comparisons.

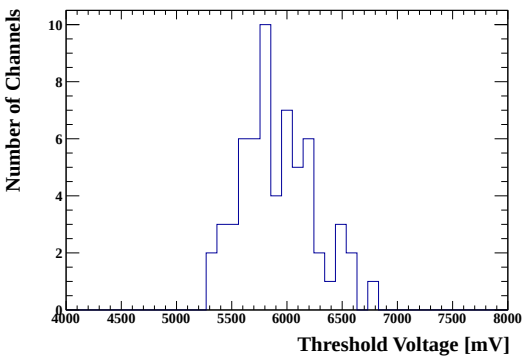
The SPS quality is not affected by adding parallel calibration capacities, as shown in Figure 3.8. This is expected, as the pulse quality in terms of jitter and pulse length is nearly independent of the calibration capacity in the value range used here [33]. The fitted gain varies between different measurements as the environmental conditions were not controlled and the measurements were done over several days.

The functional relation between threshold voltage and calibration capacity is shown in Figure 3.9 for some example channels. From the curve shapes no apparent parametrisation can be obtained. This could be attributed to parasitic capacities generated from the soldering process or from capacitive effects generated in the PCB traces. The measurement process is biased from pedestal shift effects for channels with relatively high threshold voltage, as is apparent on all of the LED response plots, and thus can only give a rough idea of the actual LED output amplitude.

To equalise the LED response for each channel, a target threshold voltage, that all channels should match as closely as possible, has to be defined. From Figure 3.9 a target threshold around 6500 mV is chosen, as it is covered by most channels at one point of the

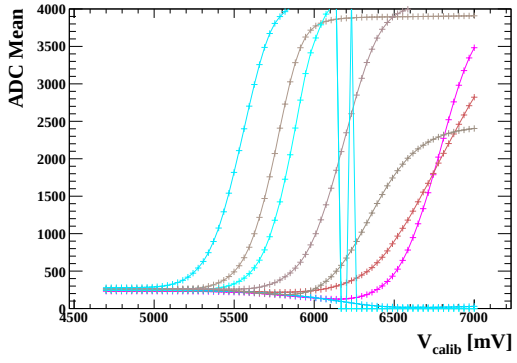


(a) *LED response.*

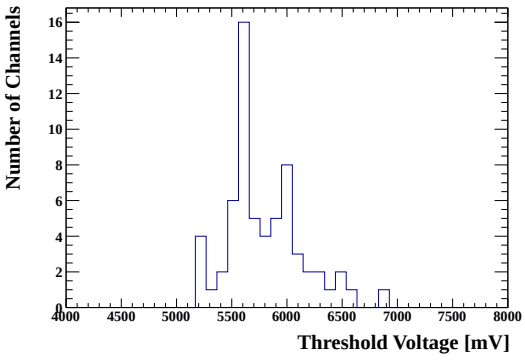


(b) *Threshold voltage distribution. Mean*= 5914, *RMS*= 327.4, $\frac{RMS}{mean} = 0.055$

Figure 3.6: *LED response in ADC counts versus V_{Calib} voltage and extracted voltage threshold distribution at CL = 237 pF.*

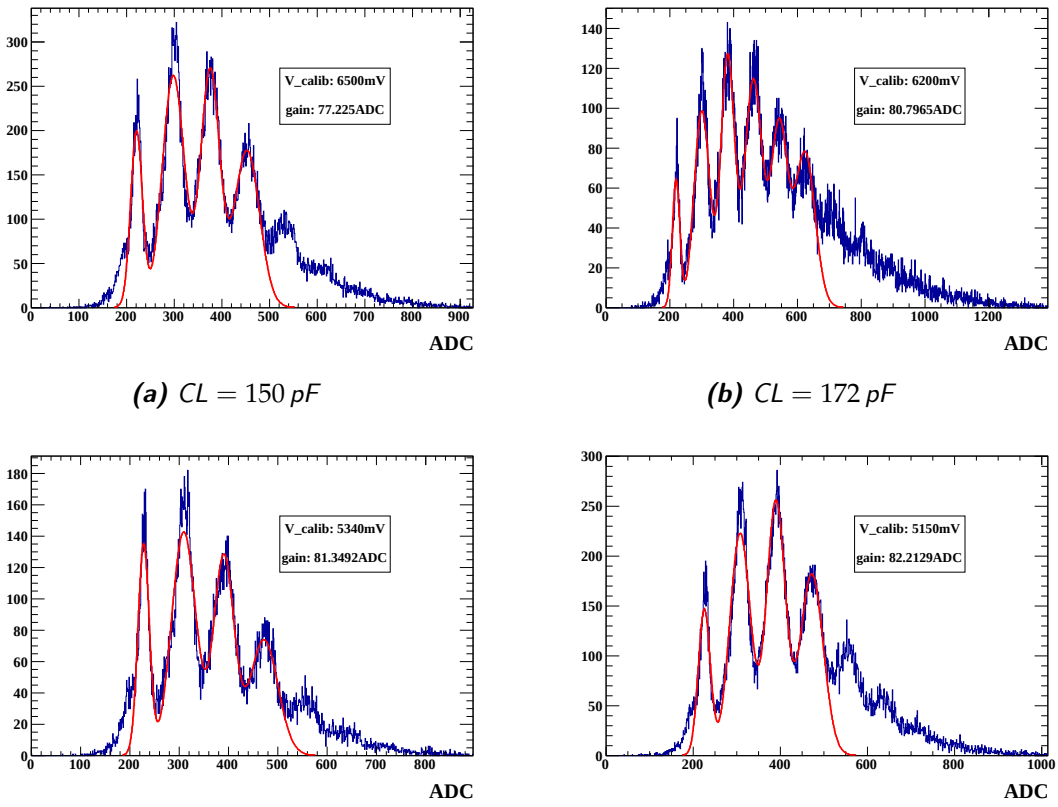


(a) *LED response.*



(b) *Threshold voltage distribution. Mean*= 5796, *RMS*= 352.1, $\frac{RMS}{mean} = 0.061$

Figure 3.7: *LED response in ADC counts versus V_{Calib} voltage and extracted voltage threshold distribution at CL = 259 pF.*



(a) $CL = 150\,pF$ **(b)** $CL = 172\,pF$

(c) $CL = 237\,pF$ **(d)** $CL = 259\,pF$

Figure 3.8: *Single photon spectra of the same channel taken with different calibration capacities, V_{Calib} chosen to give similar spectra.*

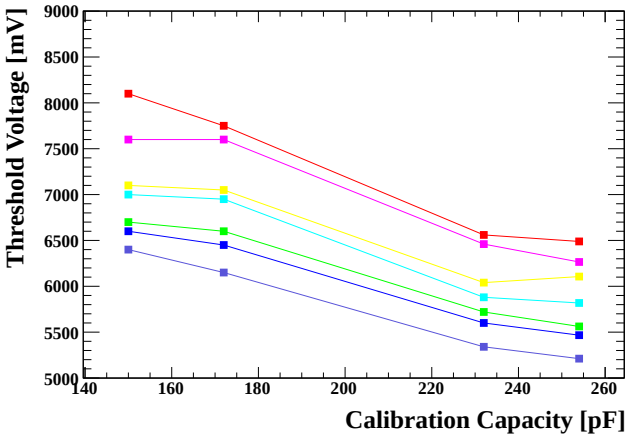


Figure 3.9: *Threshold voltage depending on calibration capacity for exemplaric channels. The highest and lowest curves roughly correspond to the extremes of the spectrum.*

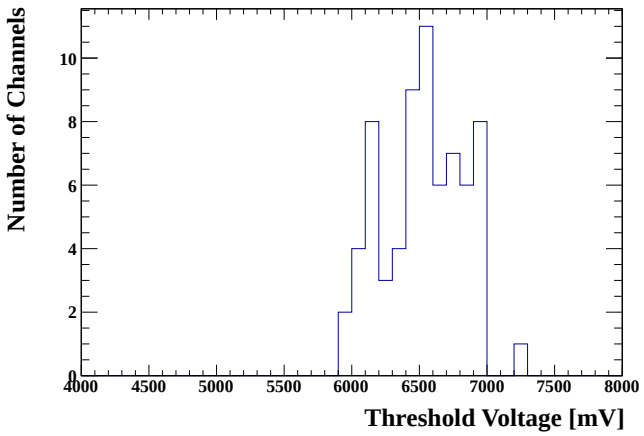


Figure 3.10: *Threshold voltage distribution after LED response equalisation procedure. Mean*= 6507, *RMS*= 285, $\frac{RMS}{mean} = 0.043$

capacity-threshold relation. A lookup is performed for each channel to calculate which available capacity comes closest to the target threshold. The optimal capacity for each channel is then set up manually on the HBU.

The optimal threshold distribution derived from this feature, as shown in Figure 3.10, shows an improvement in relative width while the mean is very near the defined target threshold.

The general spread in threshold voltages is too high to be explained by individual part variance like LED output, capacitor tolerances or coupling efficiency between tile and SiPM. Mapping threshold voltages per channel to their corresponding position on the HBU, Figure 3.11, suggests that LEDs on the outer parts of the HBU have higher threshold voltages and thus less light output. The HBU DAQ is not suited to further investigate this issue, as it is not possible to switch off single LEDs in software and hardware problems like pedestal shifts interfere with reliable quantitative measurements. The Wuppertal LED test stand described in section 3.4 is better suited to study the generated light pulses and issues of the system integration.

3.3 SiPM Saturation

For even higher values of V_{Calib} the light pulses generated from the LED system are expected to saturate the SiPMs. To test this the SPIROC chips are configured to run in lowgain mode, so that the generated signal does not exceed the dynamic range of the preamplifiers. A scan through the higher range of V_{Calib} values is performed up to the maximum of 10 V. The resulting LED response curves are shown in Figure 3.12.

At some point for each channel, increasing V_{Calib} (and such the light pulsed into each tile) does not increase the signal from the SiPM anymore. This can be explained by all illuminated pixels of the SiPM firing at once, thus giving the maximum output that SiPM

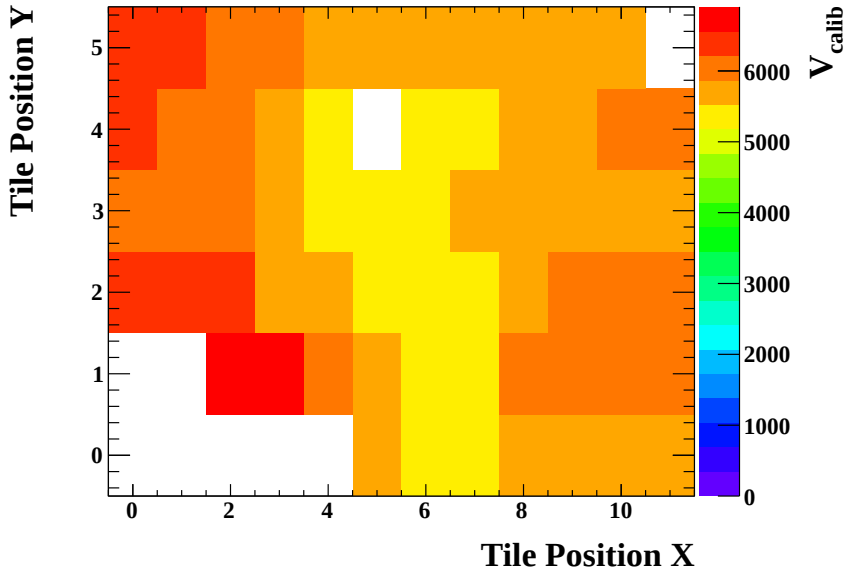


Figure 3.11: *Spatial distribution of threshold voltages for the lower part of the HBU2 (first revision). HBU oriented with DIF to the right side, ASICs facing up.*

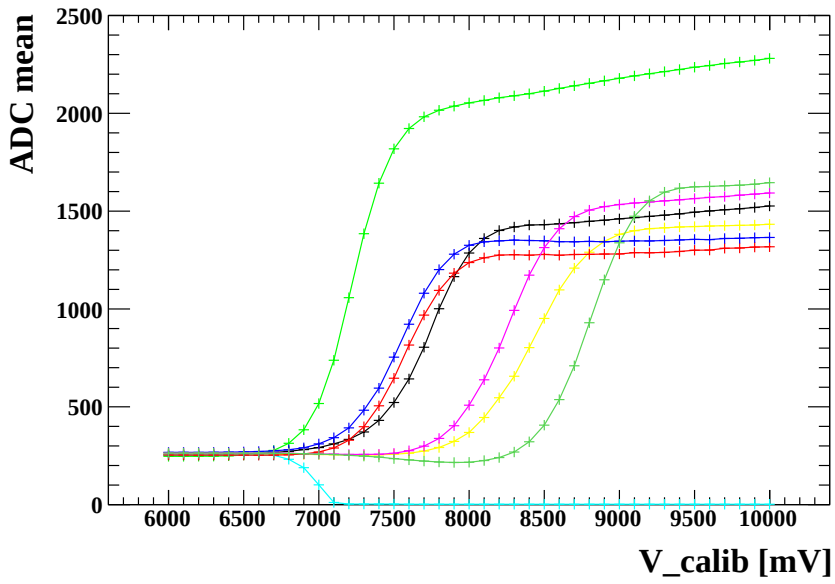
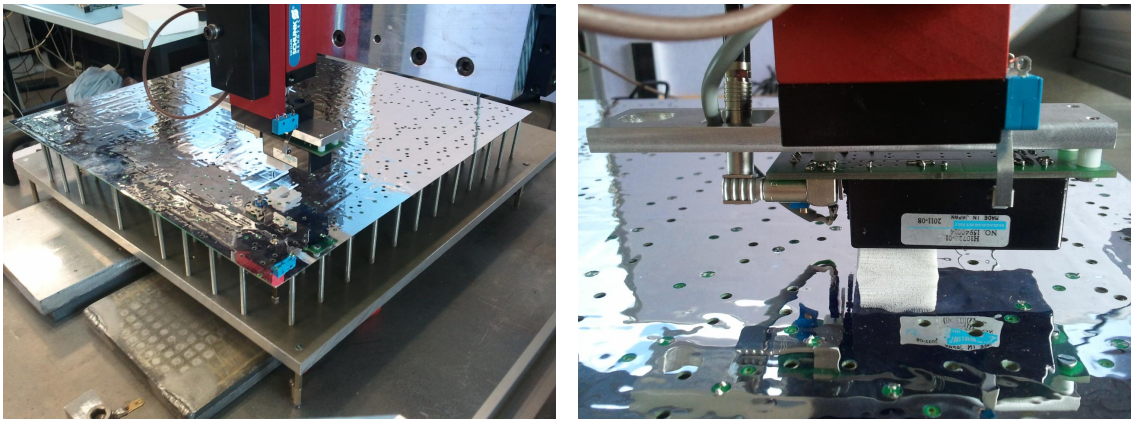


Figure 3.12: *LED response curve in lowgain mode for LED amplitudes up to SiPM saturation. Only some channels shown for readability.*



(a) *Overview* **(b)** *Detail of the PMT mount*

Figure 3.13: *Current setup of the Wuppertal LED system test stand. Shown with mounted HBU2 at the bottom, coated with reflecting foil.*

can generate. Some channels still show a slope in the LED response after the saturation point. This might be due to LED pulses becoming long enough for single pixels to regenerate their deadtime and firing twice from one pulse. The observed saturation is not a saturation of LED output, as previous measurements performed on single channel circuits with a PMT have shown the LED system to run well within its dynamic range at the currently assembled switchable CL capacities and V_{Calib} =10 V [33].

Analysis of such saturation curves needs to be performed to obtain parametrisations for channelwise corrections in a calorimeter prototype.

3.4 New Test Stand

In light of the results from the first LED systems tests on HBU2, the previously built Wuppertal test stand for LED pulse circuit and tile tests [34, 35] was modified to get a more detailed insight into the LED system. The test stand consist of an electronically translatable XYZ-table in a light-tight, temperature stabilised casing. An HBU can be mounted inside the test stand with the LEDs facing up towards the XYZ-head. The XYZ-head can be positioned with sub-mm precision over the full dimensions of an HBU. Depending on the measurement task, different instruments can be mounted on the XYZ-head. The current setup is depicted in Figure 3.13.

For the current measurement the XYZ-head is equipped with a Hamamatsu H10720-01 photomultiplier, featuring a low rise time of 0.5 ns and high photon efficiency. Signals generated by the PMT are digitised by a *PicoTech PicoScope6402* USB oscilloscope. The fast rise time of the PMT and the high oscilloscope sampling frequency of 5 GHz offers excellent time resolution for the whole setup. The oscilloscope features 32 megasamples internal memory and a fast trigger rate, so that up to 32000 waveforms can be acquired

and stored until readout. This enables very fast measurements of big numbers of single pulses for statistical analysis. However, for the first measurements shown here, only averaged pulse forms have been used.

To acquire light pulses from each LED on the HBU, the LED system is not driven by the usual setup of DIF, CALIB2 board and POWER2 board. Instead only the voltages and trigger pulses needed to activate the LED system are supplied from external sources. This allows for exact control over each parameter and circumvents the complications of setting up the full DAQ system, which is not needed with the PMT-oscilloscope combination either. The external LED trigger pulse is also fed into the external trigger input of the oscilloscope, fully synchronising operation of the LED system and the acquisition system. This enables the exact measurement of individual timing delays between trigger pulse and LED emission.

The PMT is automatically positioned over each LED of the HBU2 and the average of several hundred LED pulses is taken. This is done for a range of V_{Calib} voltages each, to cover a large range in LED amplitudes. From the resulting pulse shapes, information about amplitude and relative timing with respect to the trigger pulse can be obtained. The resulting pulse shapes for the sector used in the LED tests of the previous sections is shown in Figure 3.14. First tests from manual inspection of single pulses have shown no significant jitter in LED pulse timing and only a small variance in amplitude.

It is apparent that different positions give greatly differing LED amplitudes. Especially channels at the outer edges of the HBU show only very small light amplitudes even for the highest V_{Calib} settings. The OPAMPs driving the LED transistor bases are located along the center axis of the HBU2, the emission amplitude seems to be roughly correlated to the driver-LED distance on the board. Analysing the time delays between external trigger and onset of LED emission emerges a similar pattern, as shown in Figure 3.15.(a). The measured delay covers the range up to 9 ns. This is much more than the expected signal propagation offsets of ≈ 1 ns maximum.

To further analyse the amplitude and timing differences especially in light of their seeming correlation, the base and collector signals of the LED transistors have been measured for a number of channels. The resulting plots are shown in Figure 3.16. The base signal edge deteriorates from around 5 ns down to around 10 ns depending on the channel position. The slower edge channels also suffer from reflections along the signal line, causing a spike shortly after the signal edge. The collector signals show a less but still noticeable difference in edge slope, but exhibit a pronounced timing spread of up to ~ 6 ns. Channels that show shallow signal edges at the base correspond to a later collector signal and vice-versa.

This hints to the distribution of trigger signals as the source of the observed timing delays. During development of the LED system on single-circuit PCBs, similar problems from inductive effects in the signal lines have been observed [33]. Naturally this can be improved by increasing the physical width of the signal lines. Another idea of improving the transistor base signal uses a second transistor to reduce the load on the driver OPAMP. Tests are performed at time of writing and thus cannot be included here.

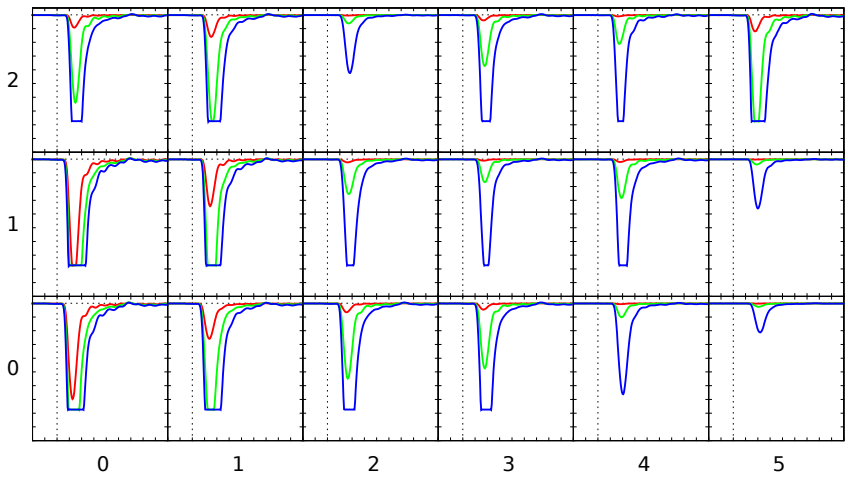
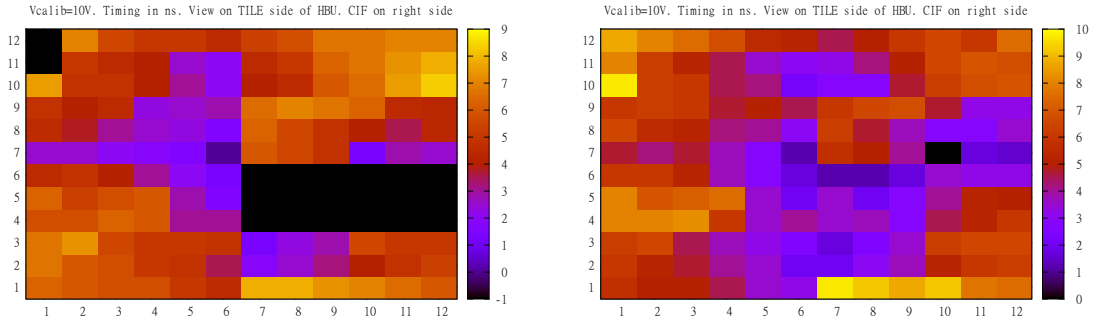


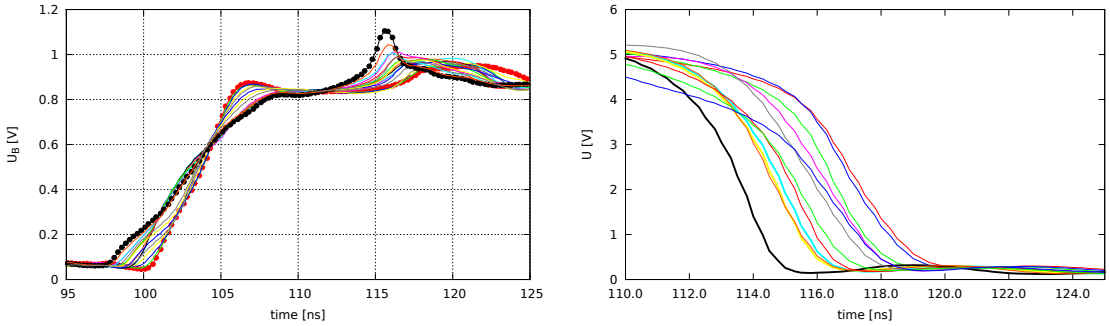
Figure 3.14: *LED system pulse shapes measured with the Wuppertal test stand for the channels of one quarter of the HBU2. The top left corner of the plot is the center of the HBU. The measured signal amplitude is given on the y-axis while the x-axis depicts time. The center Dotted vertical lines are the positions of the external trigger pulse. Line colors indicate different V_{Calib} values.*

Generally the results of the upgraded test stand only show the first tests performed. Future measurements will include analysis of pulse width and amplitude distributions for single channels and full boards.



(a) *HBU2 (first revision)* **(b)** *HBU2 (second revision)*

Figure 3.15: *Time delay between external trigger and LED pulse extracted from pulse shapes, earliest LED pulse set as t=0 to compensate for trigger and PMT line lengths.*



(a) *Transistor base* **(b)** *Transistor collector*

Figure 3.16: *Signal shapes measured at the base and collector of the driver transistor for different channels.*

3.5 Summary and Conclusion

The measurements presented in this chapter show, that it is possible to calibrate SiPM gains using the LED system integrated onto the HBU. The single photon spectra obtained from single channel measurements show good peak separation in a V_{Calib} range of 200-300 mV, depending on the number of events acquired.

Calibration of the whole setup at once proves to be more difficult, as the usable V_{Calib} range differs between channels because of differing LED responses between channels. This makes scanning over several V_{Calib} values a necessity for calibration of a full HBU. Homogenisation of LED responses by switchable extra capacitors in each LED circuit proves to be working, but the needed V_{Calib} range for a full calibration narrows by only $\approx$ 25%. The pedestal shift effect also interferes with the calibration, substantially increasing the total statistics needed.

The dynamic range of the generated light pulses is large enough to measure saturation curves for each channel.

From measurements of the LED response curves, a correlation of light amplitude and channel position on the HBU is observed. Generally channels further away from their respective trigger driver show less amplitude. This is confirmed by measurements with the upgraded Wuppertal test stand. Preliminary analysis of the first data taken with the test stand also shows a similarly correlated shift in LED pulse timings between channels. Direct measurements of the trigger signals arriving at the individual LED circuits show a degradation of pulse quality along the signal path. Future measurements will further enlighten this issue, as well as gaining insights into individual pulse widths as a function of V_{Calib} .

The currently implemented LED system fulfills the key requirements defined for a SiPM calibration system, with further improvements needed in output homogeneity. Apart from SiPM calibration, the LED system can be used to measure several HBU and SPIROC parameters as e.g. preamplifier gain curves. The upgraded Wuppertal test stand will greatly help in future development on the system scale.

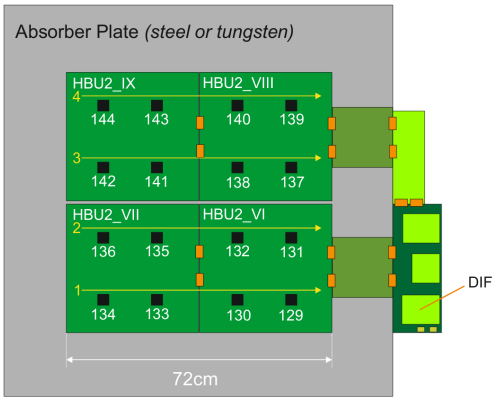
Apart from the measurements presented here, the LED system is a valuable tool for calibration of many parameters of the SPIROC chip and readout system, e.g. TDC offset calibration and hold time scans.

4 EPT Testbeam Commissioning

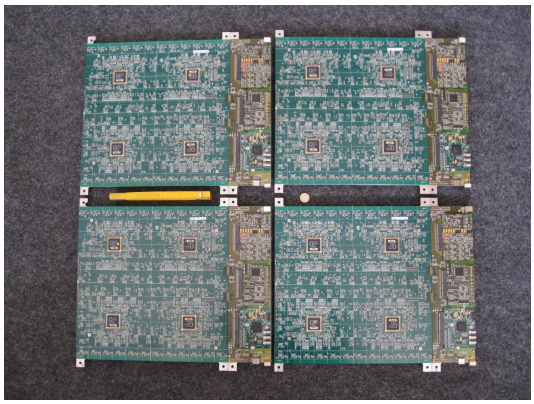
This chapter describes the procedures developed and applied for the commissioning of the EPT layer currently under construction at DESY for use in a timed hadron test beam at CERN in November 2012. For this 2×2 HBU2s, consisting of 16 ASICs and 576 total channels will be used as an extra layer of the CALICE DHCAL prototype. The HBUs will be assembled in two slabs of two boards each. As the absorber plates have bigger dimensions than the EPT layer, test beam extender modules have to be installed to have both the HBUs centered in the calorimeter and the DIF located outside. A schematic is given in Figure 4.1.(a).

Six new HBUs were ordered, four of them for the test beam layer, one for backup purposes and one for tests with the first SPIROC2c chips, that have arrived at DESY. The HBU PCBs are produced by an external contractor, while assembly of all on-board components is done at DESY. The used scintillator tiles with mounted SiPMs are supplied by ITEP.

For lab testing each of the four test beam HBUs is mounted on a separate baseplate, fully set up with a dedicated CIB, DIF, CALIB2 and POWER2 board. This enables doing different measurements with several boards in parallel. All four setups are shown in Figure 4.1.(b). The four used HBUs are numbered from HBU2_VI to HBU2_IX.



(a) *Schematic of the test beam setup. Yellow arrows indicate readout order.*



(b) *Photo of the four HBU2s used in the EPT layer*

Figure 4.1: *EPT layer schematic and photo.*

4.1 Commissioning Steps

Between HBU assembly and test beam operation several steps of setup and calibration have to be performed.

1. USB connectivity test to determine if the communication with the chip can be established.
2. Calibration of input DAC curves.
3. Equipping tiles and setting up input DACs accordingly.
4. Readout chain test to check if each tile gives signal.
5. Preamplifier setup to equalise SiPM gain on ADC scale.
6. Noise measurements for trigger setup.
7. MIP calibration.
8. Calibrations of other SPIROC parameters (e.g. TDC).

Steps 1..5 have to be performed in the order given above, as the ADC scale is only fixed after the preamplifiers are configured, which other parameters are dependent upon. The later steps are not bound to be done in the order given or can be worked on in parallel, e.g. the test beam MIP calibration can be performed without the optimised trigger settings, as described in section 4.4.

4.2 Input DAC Calibration

Each SiPM in the EPT has to be operated at its specified bias voltage to ensure correct SiPM quantum efficiency and thus lightyield. As explained in subsection 2.3.1, one input DAC per channel reduces the globally set bias voltage to match the specification of each SiPM.

To set each channels bias voltage with maximum precision possible, the DAC output curve has to be measured for each channel. This is needed as the DAC curves have inhomogeneous slopes between channels, because of their low power dissipation design. For measurement of a high resolution DAC response curve, the slowcontrol scan utility (see section 2.7) is used to automatically cycle through the full range of DAC settings. Acquisition of the generated DAC voltage is done with a Keithley 2000 multimeter, connected to the LabView PC via GPIB. As can be seen in the resulting plot, shown in Figure 4.2, the DAC curve is well described by the linear fit through the full parameter range and shows only very few outliers.

The procedure used for the full resolution scan can not be scaled to all channels of the EPT layer, as the update of slowcontrol configuration takes around 2 s. Also the DAC is not very fast in adjusting its output voltage, so after rewriting the slowcontrol another

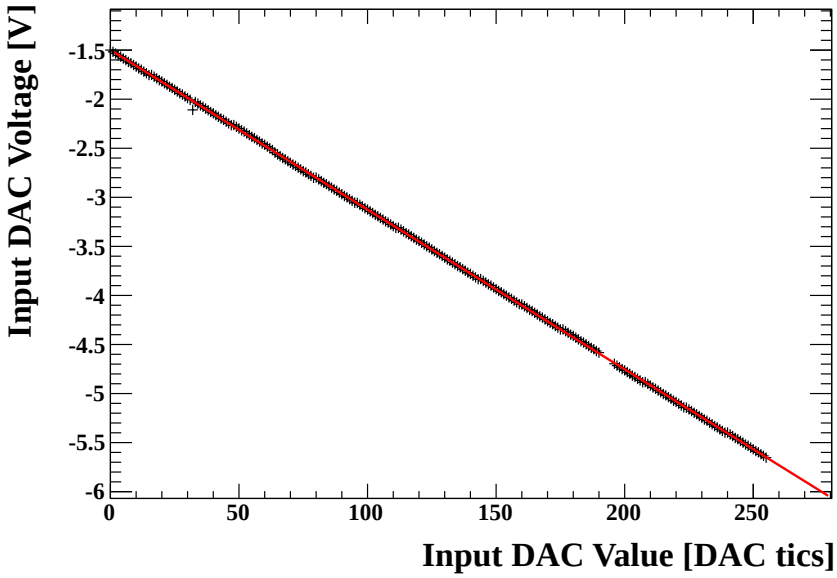


Figure 4.2: *High resolution input DAC response curve of a single SPIROC2b channel with linear fit.*

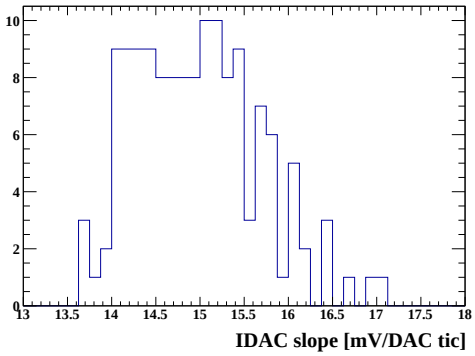
second should be waited for the DAC to settle to its new output. It would take a total of $576 \cdot 256 \cdot 3\,\mathrm{s} \approx 123\,\mathrm{h}$ to calibrate all input DACs. As no working channel with non-linear behaviour has ever been observed in test measurements, only the slope needs to be determined. This can be achieved with drastically less points than the full resolution. Defective channels either give the same output voltage regardless of configuration, or have no fixed potential and float.

For input DAC calibration of the full layer, three DAC values are taken for each channel. To circumvent potential problems at the extremal values of the DAC range, the DAC values 25, 125 and 230 are used. The full range is extrapolated from the linear fit. One HBU is used at a time, with one DAC value set for the whole board. The output voltage of each channel can then be acquired by hand in rapid succession. Acquisition of all three data points for each channel of one board takes around 45 minutes with this procedure, minimising the possible impact of temperature changes during the measurements.

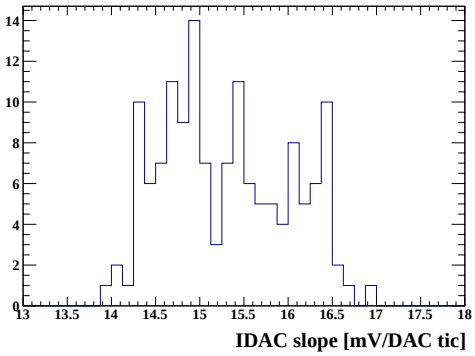
For each channel, the data points are fitted with a linear function. The distributions of slopes m for each board are given in Figure 4.3. The distribution of offsets b is very narrow and does not impact the DAC accuracy much. Omitting the input DAC calibration and using the mean of the fitted slopes, the average difference between set and actual voltage would be around

$$\frac{\sigma}{4m} \cdot 5\,\mathrm{V} \approx 117\,\mathrm{mV}. \tag{4.1}$$

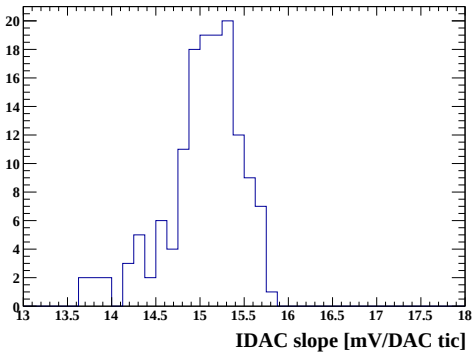
Tiles from two different batches manufactured by ITEP are equipped on the discussed HBUs. The *old* batch arrived at DESY around May 2011 and features tiles in the bias region around 37 V with a gain between 500k and 2000k. The *new* batch arrived in late



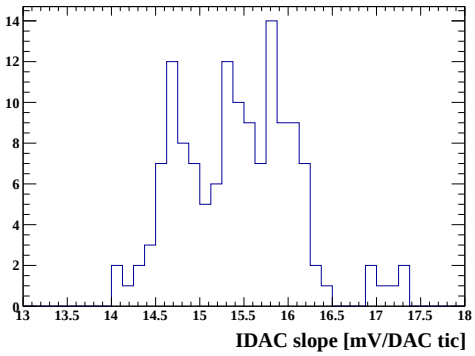
(a) *HBU2_VI, Mean = 14.98 mV/DAC tic, RMS = 0.70 mV/DAC tic*



(b) *HBU2_VII, Mean = 15.29 mV/DAC tic, RMS = 0.72 mV/DAC tic*



(c) *HBU2_VIII, Mean = 15.04 mV/DAC tic, RMS = 0.43 mV/DAC tic*



(d) *HBU2_IX, Mean = 15.43 mV/DAC tic, RMS = 0.66 mV/DAC tic*

Figure 4.3: *Distributions of the fitted slopes of the input DAC response curves for all HBU2 boards used in the hadron test beam layer.*

2011 has significantly higher bias voltage around 47 V and higher gain in the region of 1500k to 4000k. Higher gain tiles are preferred for better calibrateability, making the new batch the natural choice for equipping the EPT layer. Unfortunately, the new batch only includes around 460 tiles, just enough to equip HBU2_VI, HBU2_VII and HBU2_VIII. HBU2_IX is equipped with tiles from the old batch.

The tiles are grouped by bias voltage and equipped to the boards according to a *tile map* which documents each tile position on the HBUs. As the performance of the old tiles has proven to be significantly worse than the newer batch, the highest gain tiles of the old batch are equipped nearest to the center of the full layer, to increase the possible performance near the shower core.

From the distribution of SiPM bias voltages for each board, the setup of the bias voltage U_B for that board can be determined. The setup of bias voltages on the POWER2 boards is done by soldering voltage dividing resistors by hand, which makes the result dependent on the accuracy of the used resistors. The measured values for each board are tabulated in Table 4.1. Each HBU has its own POWER2 board and thus U_B during lab tests. In the full test beam layer only one POWER2 board will be available, limiting number of different U_B supplies to three. The tiles of HBU2_VI and HBU2_VII have similar enough bias voltages to be operated on the same bias voltage. The bias voltages for HBU2_VI and HBU2_VII are thus already very similar on their own POWER2 boards. Distributions of SiPM bias voltages with conservative estimations of the individual adjustment range from the DAC curve fits is shown in Figure 4.4.

Table 4.1: *Global bias voltages U_B for the test beam HBUs.*

Board	U_B[V]
HBU_VI	48.93
HBU_VII	48.60
HBU_VIII	52.00
HBU_IX	39.86

From the global bias voltages U_B, the fitted DAC curves $U_{DAC}(x) = mx + b$ (with the DAC setting x and fit parameters m, b) and the targeted SiPM bias voltage U_{ITEP} from the tile maps for each channel, the DAC setting for each channel can be calculated as follows:

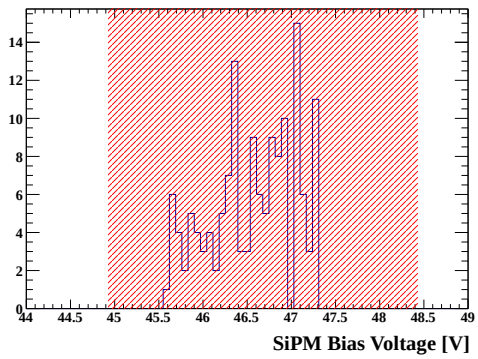
$$U_{ITEP} = U_B - U_{DAC}(x) \tag{4.2}$$

$$U_{ITEP} = U_B - mx - b \tag{4.3}$$

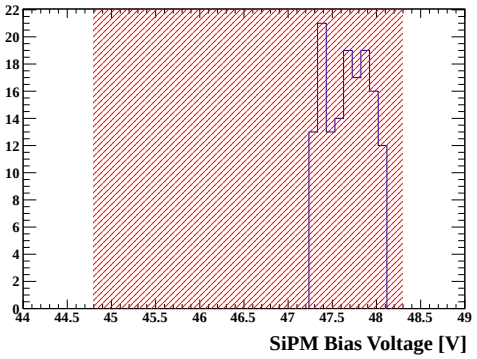
$$\Rightarrow x = \frac{U_{ITEP} + U_B + b}{m}. \tag{4.4}$$

The obtained DAC value x calculated for each channel, rounded to the next integer and written into the slowcontrol software.

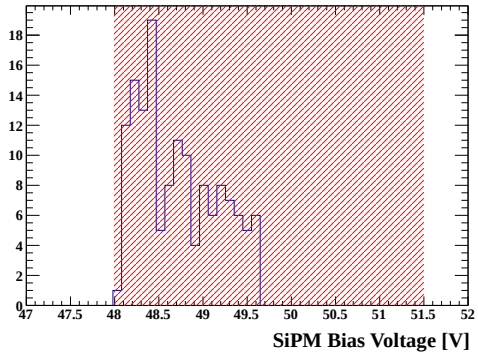
Defective channel DACs can be easily identified from their response curve fit parameters. Fit results outside of $\chi^2 < 0.01$, $0.1 < m < 0.2$ and $-5 < b < -4$ are counted as



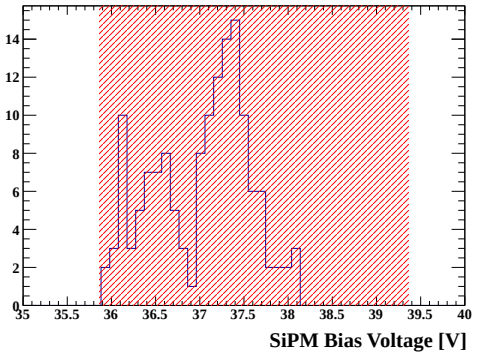
(a) *HBU2_VI, U_B = 48.93 V*



(b) *HBU2_VII, U_B = 48.60 V*



(c) *HBU2_VIII, U_B = 52.00 V*



(d) *HBU2_IX, U_B = 39.86 V*

Figure 4.4: *Distributions of SiPM bias voltages U_{ITEP} recommended by ITEP for tiles equipped on all HBU2 boards used in the hadron test beam layer. The area marked in red shows the conservative minimum coverage of the input DACs for individual bias voltage adjustment.*

a defect channel. Such channels are set to DAC value 0 to not damage the SiPM of that channel from overvoltage. The channel preamplifier is also switched off for these channels to not interfere with the measurements. 12 channels of out the total 576, around 2%, do not give proper DAC response curves (3 on HBU2_VI, 2 on HBU2_VII, 2 on HBU2_VIII and 5 on HBU2_IX).

While the procedure described is already optimised for measurement speed, it still relies on manual placement of the voltage probe on the SiPM connector of each channel of the HBU. There is no easy way of fully automatising the procedure. A robotic probe that automatically repositions itself on each channel is rather unrealistic and would not substantially decrease the time for the full procedure. If the issue of input DAC inhomogeneity persists on future versions of the SPIROC chip, the most realistic option seems to be a testbench that directly interfaces the in- and outputs of the packaged, unsoldered chip. Something similar would be needed for automatised quality control and could be incorporated into that process.

4.3 Preamplifier Setup

The general aim of setting up the preamplifiers is equalizing the ADC response to an incident MIP (*MIP response*) across all channels. Under the assumption that the distribution of *lightyields* in pixels/MIP is narrow, equalizing the cell gains achieves this goal. The assumption is reasonable, as the SiPM bias voltages provided by ITEP are specifically tuned for each tile to provide a lightyield of 15 pixels/MIP.

Measuring cell gains is possible with the onboard LED calibration system, whereas determining the MIP response takes at least a sophisticated coincidence triggered radioactive source setup, but better a test beam environment that gives true MIPs in the GeV energy range. Thus measuring cell gains is the far less complicated and a lot more time economical procedure.

The cell gain C of each channel is defined as $C = N \cdot G$ with the intrinsic SiPM gain G and the preamplifier conversion factor N. While G varies with the bias voltage U_{bias} applied to the SiPM, changing U_{bias} will also influence its photon conversion efficiency. Each scintillator tile is shipped with an exact value for U_{bias} optimised for a lightyield of 15 pixels/MIP, thus setting up cell gains by variation of U_{bias} is not an option. Instead N can be set up for each channel on SPIROC2b via slowcontrol. The SiPMs used in this setup vary in G in the range of $7 \cdot 10^5$ to $3 \cdot 10^6$, so N has to cover a range of around factor 5 to compensate for the variation in G.

The steps undertaken to achieve an equalisation of cell gains are as follows:

1. Determine cell gains for a fixed reference preamplifier setup.
2. Measure N in dependence of the preamplifier capacitor setup.
3. Define the target cell gain to be matched by all cells.
4. Calculate new, cell gain equalised preamplifier capacities from 1., 2. and 3.

5. Measure cell gains with the new preamplifier setup to verify the success of the procedure.

As the test beam measurements were done with single MIP-like particles that should never exceed the dynamic range of the highgain mode of SPIROC2b, all measurements are done in highgain mode exlusively.

4.3.1 Reference gain

For the determination of reference gains the onboard LED system is used to pulse each scintillator tile with short flashes of light. The average SiPM gain differs between the two batches of tiles equipped on the HBUs. A reference preamplifier capacity of 500 fF is used for the boards equipped with *new* tiles (HBU2_VI, HBU2_VII, HBU2_VIII). HBU2_IX, equipped with *old* tiles, is set up with 100 fF reference preamplifier capacity. The calibration is performed as explained in subsection 3.1.2.

All LED systems are set up with LED calibration capacity $C_{calib} = 150\,pF$ and scanned in a V_{Calib} range between 5700 mV to 8100 mV in steps of 100 mV. Each LED run consists of $\sim$ 40000 LED events.

The measured ADC spectra are fitted with a multi-Gaussian fit procedure provided by the AHCAL group. As up to 25 spectra are taken at different V_{Calib} for each channel, selection of optimal fits and determination of the total fitted cell gain has to be automated. For this a heuristic approach is implemented. To illustrate the selection procedure, Figure 4.5 shows the progression of a SPS for increasing values of V_{Calib} . Peaks are only evaluated within the fitting procedure, if their amplitude is at least 0.3 of the highest peak in the same spectrum. Spectra with less than two of such eligible peaks are not fitted at all. As the spectra are fitted in order of V_{Calib} , this makes the first fitted spectrum to consist of a large pedestal peak and a signal for one fired pixel with around 0.3 relative amplitude, as shown in Figure 4.5.(a). Only spectra up to 300 mV higher V_{Calib} than this first fit are used for calculation of the total gain, as spectra from higher V_{Calib} values tend to generate wrong fit results as shown in Figure 4.5.(f). The gains fitted from all spectra within 300 mV of the first fitted V_{Calib} value with at least 3 fitted peaks are averaged and used as the total cell gain of that channel.

Exceptions account for channels that never exhibit more than two fitable peaks. In such cases the fit with minimal amplitude diffences between the two peaks is selected.

Out of the total 576 channels 83 (25 on HBU2_VI, 16 on HBU2_VII, 17 on HBU2_VIII, 35 on HBU2_IX) give no fitable gain spectra, which equals 14.4% of all channels. In addition to that some channel gains are extracted incorrectly, as the heuristic approach described before does not always work perfectly. As HBU2_IX is equipped with old tiles, it performs notably worse than the other boards. However, on the quadrant equipped with tiles picked for high SiPM gain only 2 out of 36 channels are not calibrateable.

The correlations between measured cell gains and the gains specified by ITEP are shown in Figure 4.6. The correlations observed are worse than expected. Reasons for that could be the fit selection procedure, which picks wrong fits too often, resulting in too many outliers. Also uncontrolled and thus changing environmental conditions could

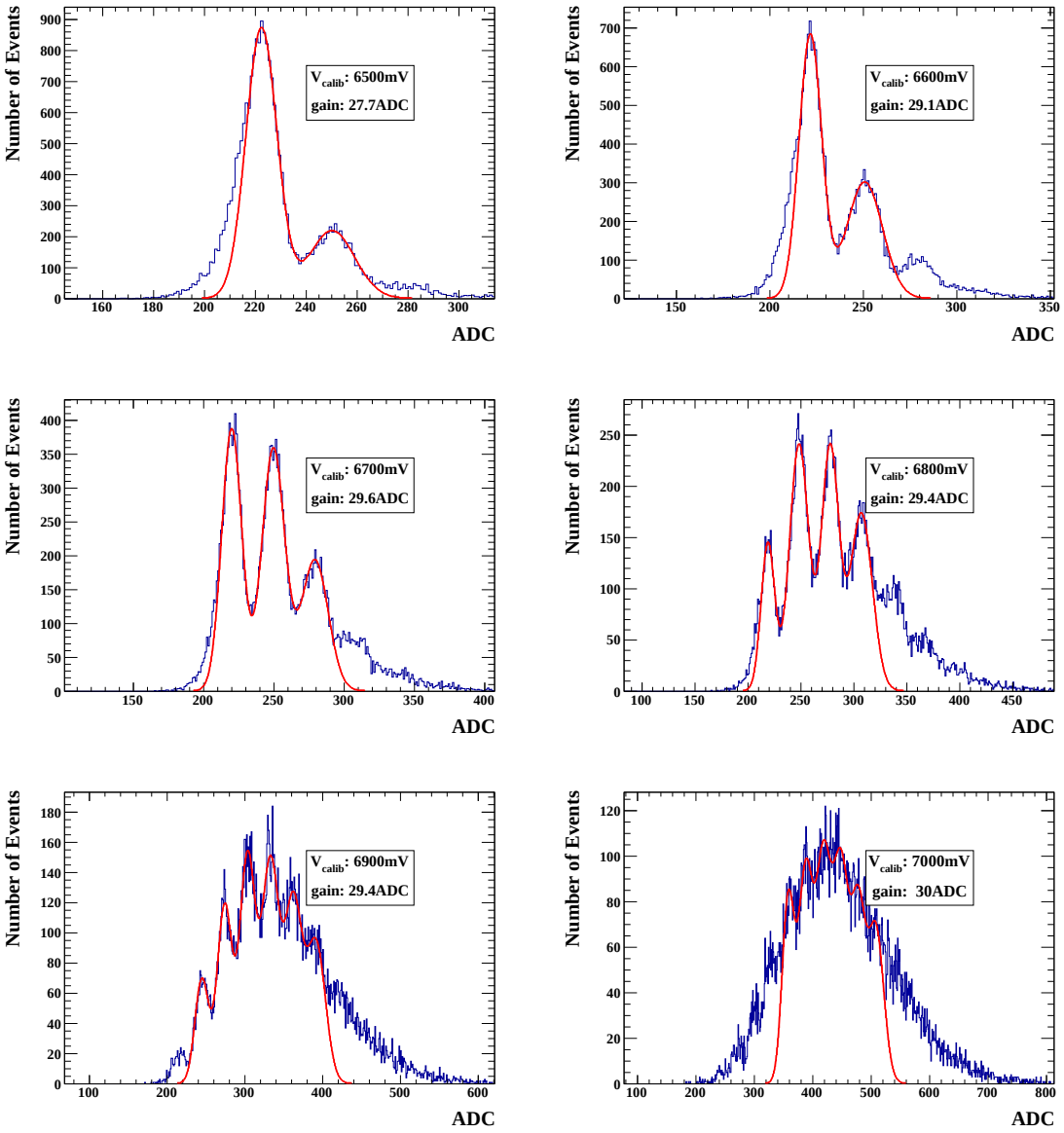
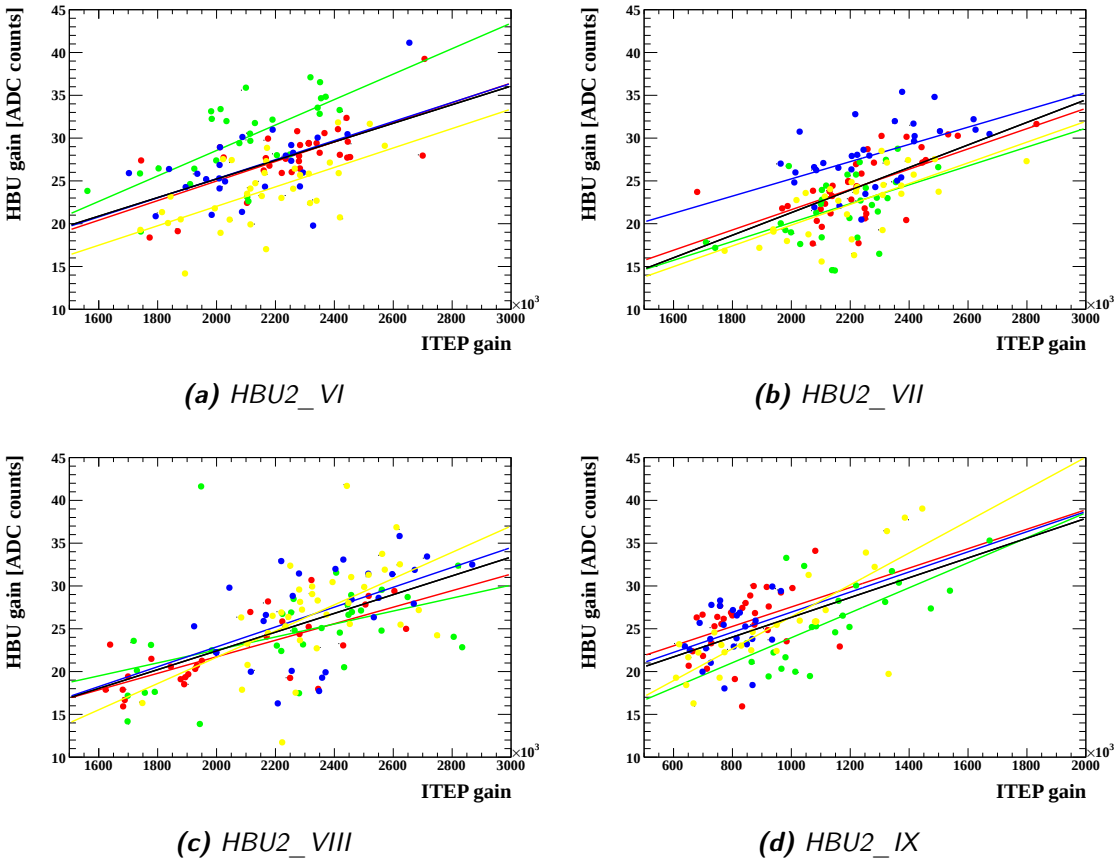


Figure 4.5: *Spectra of V_{Calib} progression with fits.*

lead to the degradation of the observed correlation. It is notable that while the slope of the linear fits seems to be fairly equal between different chips, relative large offsets are observed. The slopes of HBU_IX do not match those of the other boards, as it is measured at another reference preamplifier feedback capacity.



(a) HBU2_VI **(b)** HBU2_VII

(c) HBU2_VIII **(d)** HBU2_IX

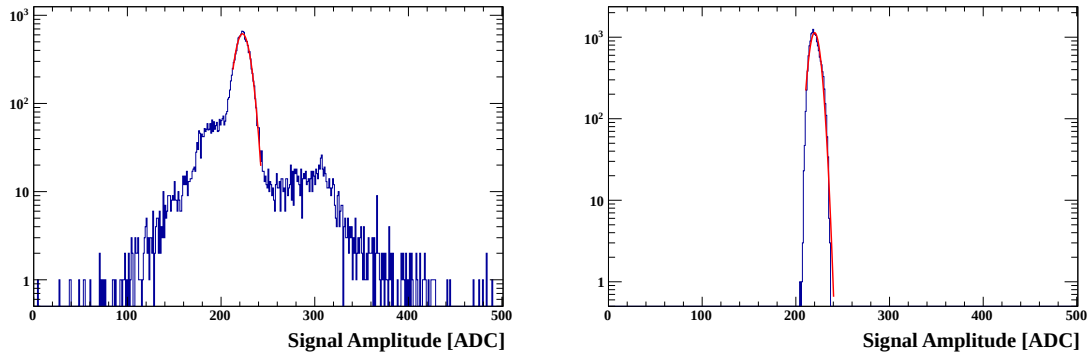
Figure 4.6: *Correlation between SiPM gains specified by ITEP and reference cell gains measured on the test beam layer HBUs. Colors indicate different ASICs of the same HBU. Colored lines are linear fits for that ASIC, black lines are linear fits for the full board.*

4.3.2 Pedestal Position

To determine $N(C_f)$ from the data acquired in the previous step, an exact understanding of the pedestal spectra is crucial. Pedestal spectra are measured with the same configuration as used for LED runs, but with the LED voltage reduced to 0 V, so that no light is emitted from the LEDs when triggered. The resulting ADC spectrum shows the pedestal peak surrounded by dark rate noise. Events with lower than pedestal ADC value are from undershoot caused by the shaper after a dark rate event has occured. By disabling the SiPM bias voltage pure preamplifier + ADC pedestal spectra can be obtained.

Pedestal peak position and width can be derived both from mean and RMS of the ADC spectrum and from a gaussian fit. The fitted mean should be used for pedestal subtraction in single events, while the mean pedestal value is used for subtracting pedestals from amplitude averages. Examples of measured pedestal spectra with and without active SiPM bias voltage are shown in Figure 4.7.

From the distributions of pedestal positions, as shown in Figure 4.8.(a), it is apparent that the positions derived from fitting and the mean ADC value do not differ much. It is therefore recommended to always use the fitted pedestal position, as the mean ADC position might be influenced by different feedback capacity setups. The distribution of widths is given in Figure 4.8.(b) and shows a much broader distribution of RMS values than fitted widths. This is expected as the fit is only performed on the pure pedestal peak and should be influenced by noise only minimally. However, the RMS width contains information about noise frequency and amplitude which may be useful for future applications.



(a) *SiPM bias voltage switched on* ***(b)*** *SiPM bias voltage switched off*

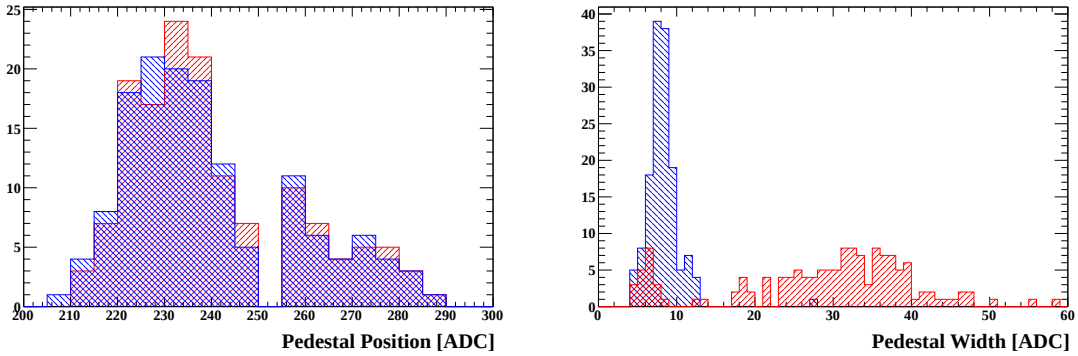
Figure 4.7: *Example pedestal ADC spectra for two different channels with Gaussian fit of the central pedestal peak.*

4.3.3 Gain Curves

N has to be measured as a function of the preamplifier feedback capacity C_f for each channel individually. Signals in the range well above pedestal and below saturation are generated by the LED system. $N(C_f)$ is obtained from the relative change in ADC response during a scan over a range of feedback capacities.

Setup of the LED Runs

For each channel a V_{Calib} voltage has to be chosen so that the resulting signal is somewhere between pedestal and saturation, in the center of the dynamic range. Optimal results would be obtained by tuning V_{Calib} for each channel individually, but this is



(a) *Pedestal positions, from Gaussian fit (blue) and ADC mean (red)*

(b) *Pedestal widths, from Gaussian fit (blue) and RMS of ADC values (red)*

Figure 4.8: *Distributions of pedestal positions and widths from Gaussian fit and the distribution itself. Measured on HBU2_VI with active bias voltage.*

unfeasible for the full 576 channels of the EPT layer. The procedure described here is optimised for minimum measurement time and would be completely automatable with a DAQ and slowcontrol system including an interface for external programs.

The devised procedure can be described as a simple algorithm. Algorithm inputs are the minimum mean ADC value (at the lowest capacity scanned) for a channel to be included in a feedback capacity scan ADC_{lower} and the upper mean ADC threshold ADC_{upper}. The output consists of a list of V_{Calib} values and corresponding channels with mean ADC value in the range between ADC_{lower} and ADC_{upper} for that channel.

1. Start with all preamplifiers and LED system active, V_{Calib} voltage set to minimum, all feedback capacities set to minimum of capacity scanning range.
2. Increase V_{Calib} until the mean ADC value of one channel exceeds ADC_{upper}.
3. Add V_{Calib} value and channels with mean ADC $>$ ADC_{lower} to output list.
4. Disable all preamplifier channels from previous step.
5. If active channels left and V_{Calib} not at maximum, go back to step 2.

The algorithm circumvents the problem of pedestal shift by deactivating all channels that generate a signal above the upper threshold. The number of output voltages can be controlled by adjusting ADC_{lower} and ADC_{upper}. Reducing ADC_{lower} decreases the achievable resolution of the gain scan and increases the susceptibility to differences in measured and actual pedestal level. Increasing ADC_{upper} increases the chance of single events saturating the preamplifier, thus biasing the ADC mean. The algorithm was performed by hand for $ADC_{lower} \approx 800$ ADC and $ADC_{upper} \approx 3000$ ADC, judging the ADC mean of the current V_{Calib} setup from the online monitor of the DAQ software.

From this, depending on the board, between 11 and 14 different V_{Calib} configurations are generated. Each V_{Calib} setting measures up to 7 channels per chip at once.

Using the list of V_{Calib} voltages and corresponding active channels, the slow control scanning utility is configured to scan through a range of feedback capacities for each setup. The scanned feedback capacity values should cover a range in N around the expected spread in SiPM gains. Also the feedback capacity values used for the reference cell gain measurements should be included, so that the normalisation reference is a data point and not interpolated from fits.

For these measurements, feedback capacities ranging from 100 fF to 1100 fF are scanned in steps of 200 fF. This includes both used reference feedback capacities and should cover enough of the needed range in $N(C_f)$.

Gain Curve Fit

From the mean ADC values of these measurements, the signal amplitude is derived by subtracting the pedestal position obtained from a separate pedestal run (see subsection 4.3.2). The signal amplitude is then normalised to the signal measured at the reference preamplifier capacity (500 fF or 100 fF depending on the tile batch mounted on the HBU) and plotted versus the used feedback capacity.

The resulting $N(C_f)$ curves can be described with a hyperbolic shape, as follows from

$$N \propto \frac{U}{U_{ref}}, Q = C \cdot U \Rightarrow N \propto \frac{1}{C}.$$

To account for parasitic capacities and offsets, the resulting $N(C_f)$ curves are fitted with a function of the form

$$N(C_f) = \frac{a}{C + b} - c, \tag{4.5}$$

with a, b, c as fit parameters. The function nicely describes the measured $N(C_f)$ curve as shown in Figure 4.9.

Examples of measured gain curves with fits are shown in Figure 4.10. Gain curves of most channels look similar to Figure 4.10.(a) and are well described by the function discussed above.

Some channels do not generate usable gain curves. Figure 4.10.(b) shows a very steep decrease from 100 fF to 300 fF, probably from a bad measurement of the 100 fF data point. A small number of channels does not give LED response, resulting in a flat curve as in Figure 4.10.(c) or other unusable curves as Figure 4.10.(d).

Channels that give fit parameters $a > 500$, $b > 0$ and $1 > c > 0$ ($a > 300$ for HBU2_IX measured with 100 fF reference capacity) are accepted as working. Out of the 576 total channels, 80 do not meet these criteria. However, most of these channels are located on HBU2_VI, of which 48 channels do not give proper gain curves. 20 channels of HBU2_VII result in bad fits, while on HBU2_VIII and HBU2_IX only 6 channels each do not seem to work.

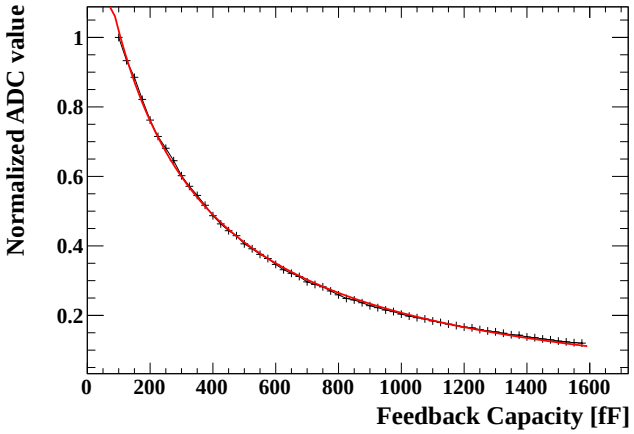


Figure 4.9: *High resolution $N(C_f)$ gain curve with hyperbolic fit.*

The reasons for the occurence of such channels is not fully understood yet, especially HBU2_VI needs to be analysed further. One possible reason is a global shift in LED output depending on the temperature, which would falsify the V_{Calib} values derived in the previous step from definition of measurements to capturing the gain curves. However, for small shifts in LED amplitude this should only lead to less accurate results and thus slightly worse fit results, and it is rather unlikely for the LED response to be influenced that much by temperature fluctuations of the scales observed in the laboratory. Also pedestal shifts are not compensated in the measurements shown here, which may influence the measured gain curves. The general effect of pedestal shifts should be small, considering the small number of channels measured per chip in one measurement. In addition pedestal shifting should result in an underestimation of N for small values of C_f.

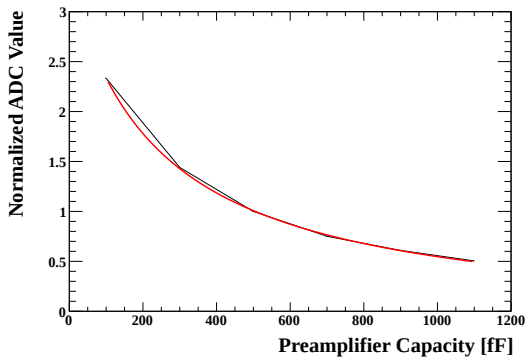
As not to disable all channels which give no proper $N(C_f)$ curve, the fitted average of the working channels of the same chip is used as an approximation.

The covered gain range in the domain of scanned feedback capacities C_f is calculated as $r = \frac{N(100\,\text{fF})}{N(1100\,\text{fF})}$. The distribution of r calculated from the fitted functions, is shown in Figure 4.11. The distributions peak around a gain factor of 4, slighty less than the required range of 5 specified above.

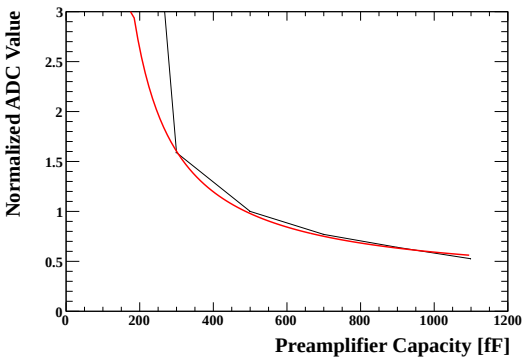
4.3.4 Calculating new Preamplifier Capacities

From the reference gains and the $N(C_f)$ curves, new preamplifier capacities can be calculated so that the spread in cell gains is decreased. One *target cell gain* has to be defined to be matched by all channels.

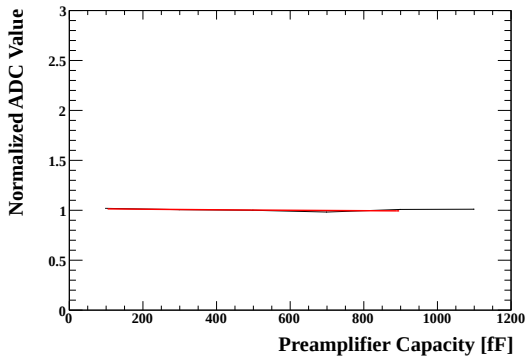
To use the maximum possible dynamic range of the low gain path in the SPIROC chip without risking to exceed the preamplifier input range, a fully saturated (all pixels firing at once) SiPM should generate a signal just below saturation of the low gain path.



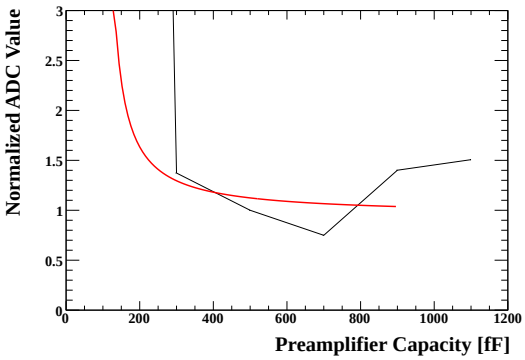
(a) *Normal gain curve.*



(b) *Gain curve with bad measurement at 100 fF.*

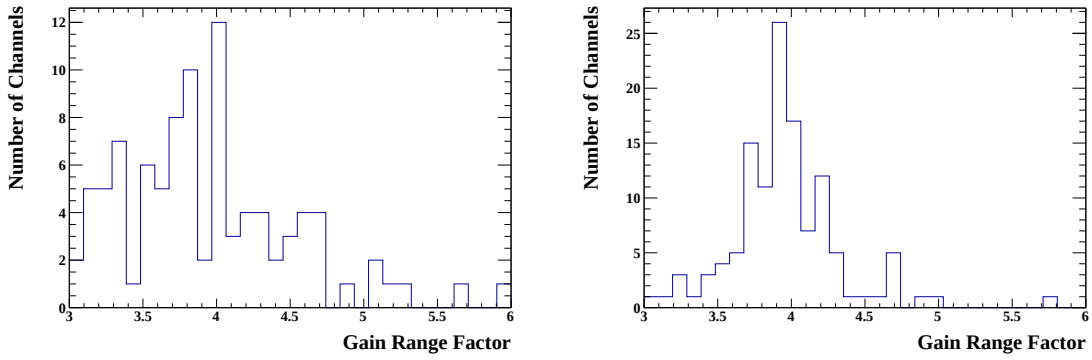


(c) *Flat gain curve from non-responsive channel or too low* V_{Calib} .

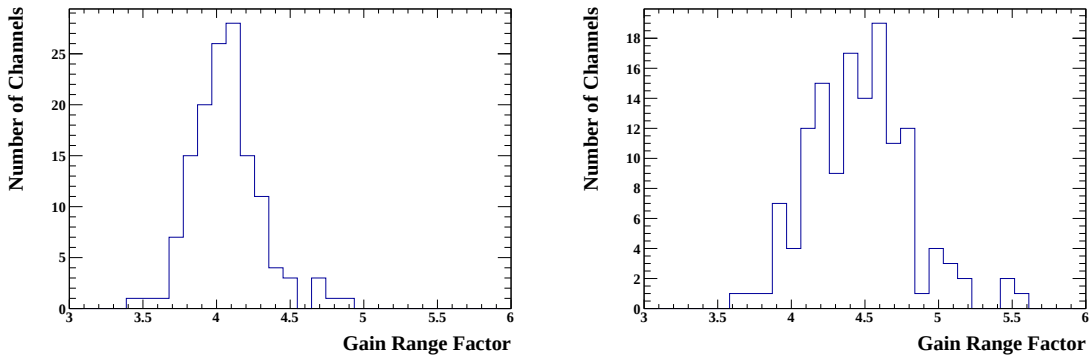


(d) *Completely unusable gain curve.*

Figure 4.10: *Measured gain curves showing different behaviors.*



(a) *HBU2_VI* ***(b)*** *HBU2_VII*



(c) *HBU2_VIII* ***(d)*** *HBU2_IX*

Figure 4.11: *Distribution of gain range factors in the measured capacity domain from fits.*

The SiPMs used in the EPT have 1000 pixels, while the dynamic signal range is around 3500 ADC tics (including pedestals and safety margins). This corresponds to 3.5 ADC tics per fired pixel in low gain mode, which, with a 1:10 gain relation on SPIROC2b, comes out to an optimal target cell gain of 35 ADC tics/pixel in high gain mode.

Several other factors also have to be considered while chosing the target gain. Only total feedback capacities $C_f \geq 100\,\text{fF}$ should be used, as the switchable smallest capacities $< 100\,\text{fF}$ are less exact, tend to take stronger influence from environmental conditions (temperature etc.) and thus are not intended for standalone use. As a consequence the target gain can not be higher than any of the reference cell gains determined in a previous step on HBU2_IX at $C_f = 100\,\text{fF}$. This also means that the mean cell gain will *decrease* from this reference measurement. Because of the limited granularity in capacities (especially at lower total values, as the stepwidth is constant but the resulting curve is roughly hyperbolic) accepting a reduction in mean cell gain will result in a lower gain spread after equalisation. Higher mean cell gain is preferred for calibration to make better use of the dynamic range in high gain mode.

In favor of reduced global gain spread and the relatively low intrinsic gains of SiPMs equipped on HBU2_IX, the target gain is defined as 22 ADC tics/pixel for all boards. Setting the target gains differently for the boards equipped with new tiles is possible, but ultimately similar cell gains and thus MIP responses are very useful for quick comparison of results at the hadron test beam at CERN and is thus decided against.

For each channel the ratio between reference cell gain and target cell gain is calculated and applied to the inverse of the fitted hyperbola

$$C_f(N) \quad = \quad \frac{a}{N+c} - b. \tag{4.6}$$

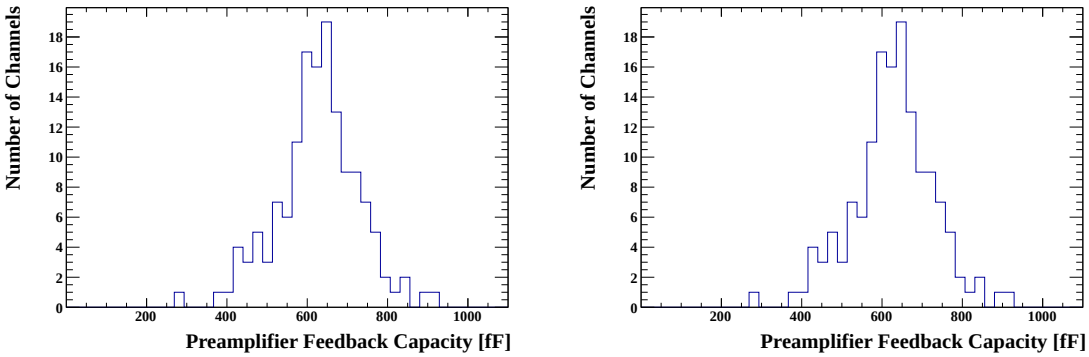
Cell gain values for channels that give no fitable spectra are interpolated from the specifications of each tile provided by ITEP using the fitted correlation between ITEP gain and gain measured on the HBU, shown in Figure 4.6.

The calculated optimal feedback capacity is compared to the two nearest possible values of C_f, and set to the one that gives a smaller deviation from the target cell gain. This is not necessarily the capacity nearest to the optimal value, as $N(C_f)$ is not linear. Distributions of resulting feedback capacities are shown in Figure 4.12.

4.3.5 Verification of New Cell Gains

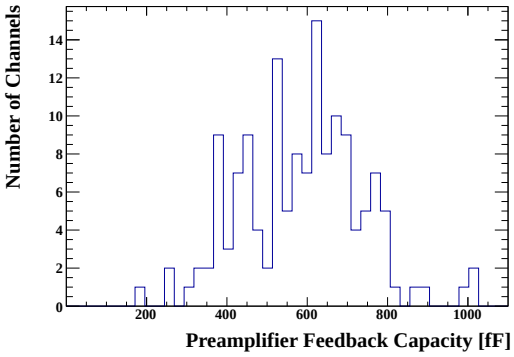
Similar to the reference gain LED runs, single photon spectra are captured for all channels. All parameters except the now individually configured preamplifiers are identical. The procedure for gain extraction is also the same as before.

In the comparison of two spectra of both channels at different feedback capacity setups, shown in Figure 4.13, the effect of a reduced peak-to-peak distance is clearly visible. 65 of the total 576 channels (11,2% total, 6 on HBU2_VI, 4 on HBU2_VII, 25 on HBU2_VIII, 30 on HBU2_IX) do not generate usable spectra for cell gain extraction. HBU2_VI and HBU2_VII show greatly reduced numbers of such channels, as the number of unusable channels on HBU2_VIII increases by half.

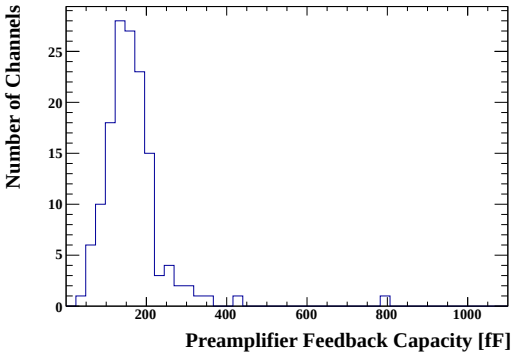


(a) HBU2_VI

(b) HBU2_VII

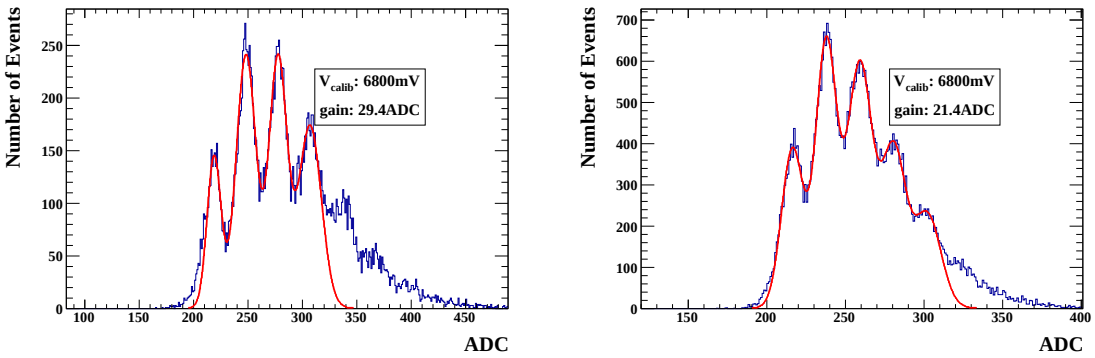


(c) HBU2_VIII



(d) HBU2_IX

Figure 4.12: *Distributions of preamplifier setup capacities as calculated to equalise the cell gain to 22 ADC tics/Pixel for all HBUs.*



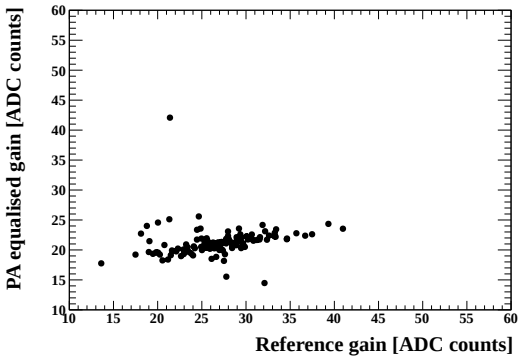
(a) $C_f = 500\,fF$ **(b)** $C_f = 700\,fF$

Figure 4.13: *SPS of the same channel at the same V_{Calib} voltage for different preamplifier setups.*

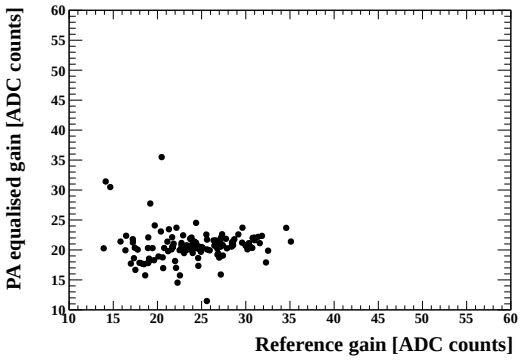
From the distribution of cell gains after preamplifier feedback setup, the spread in cell gains is shown to be reduced after the preamplifier setup procedure discussed here. The correlation between cell gains before and after preamplifier setup is shown in Fig. 4.14. However, the mean cell gain after preamplifier setup is lower than the targeted 22 for all HBUs. Also the spread around the target cell gain is wider than expected with 7.6% on HBU2_VI, 8.9% on HBU2_VII, 11.6% on HBU2_VIII and 7.8% on HBU2_IX. On a test HBU that was used to first derive the procedure described here, a spread of $\sim$ 5% was achieved with tiles from the old batch, resulting in feedback capacity ranges similar to HBU2_IX. Judging from the increased granularity in the higher C_f ranges, a spread better than 5% was thought to be achievable.

Several reasons might be responsible for this. From the amount of visible outliers in the correlation plots it is obvious, that the automated gain fit does not work as well as it should. It is also possible that the systematic uncertainty e.g. in fitting the $U(C_f)$ curves practically limits the achievable gain spread. The mean cell gains being lower than the target gain for all boards can be explained by different temperatures during the LED runs. An approximate deviance of 5% between mean and target cell gain corresponds to around 3 K temperature difference, which is not outside the possible range for the non temperature stabilised laboratory.

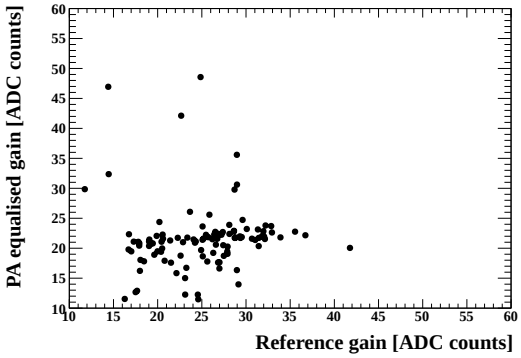
Channels that did not give a gain calibration in the reference setup, and thus had to be interpolated to calculate the optimal feedback capacity, show a surprisingly narrow distribution around the target cell gain, only slightly wider than for all channels. This proves that interpolating gains from the ITEP specifications is a feasible way of dealing with channels that are not initially fittable.



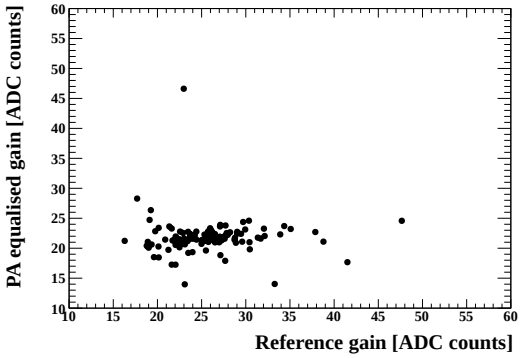
(a) *HBU2_VI, $mean_x = 26.90$, $RMS_x = 4.66$, $mean_y = 21.16$, $RMS_y = 1.60$*



(b) *HBU2_VII, $mean_x = 24.04$, $RMS_x = 4.51$, $mean_y = 20.53$, $RMS_y = 1.83$*



(c) *HBU2_VIII, $mean_x = 25.03$, $RMS_x = 5.42$, $mean_y = 21.11$, $RMS_y = 2.45$*



(d) *HBU2_IX, $mean_x = 25.84$, $RMS_x = 5.03$, $mean_y = 21.72$, $RMS_y = 1.70$*

Figure 4.14: *Distributions of preamplifier setup capacities as calculated to equalise the cell gain to 22 ADC tics/pixel for all HBUs.*

Signal to Noise Ratio

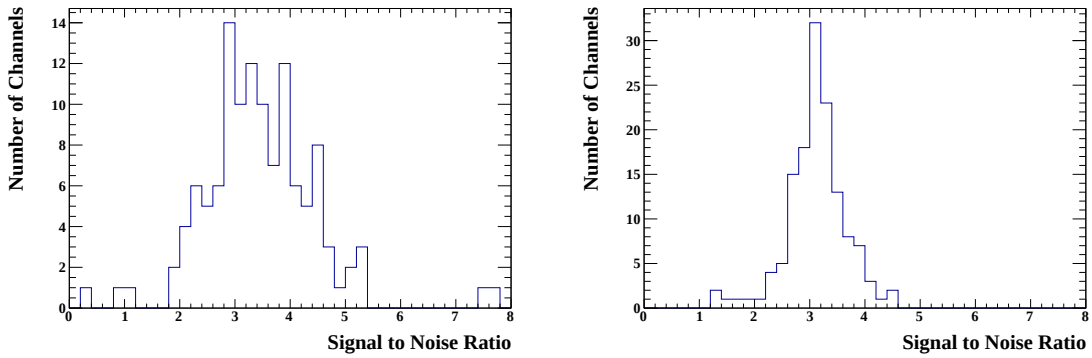
In the context of SiPM gain calibration and SPS the signal to noise ratio is defined as

$$S/N = \frac{C}{\sigma_{\text{pedestal}}}, \tag{4.7}$$

with the cell gain C as the SPS peak-to-peak distance in ADC counts and the fitted width of the pedestal peak σ_{pedestal}.

For an ideal preamplifier the S/N ratio would not change regardless of preamplifier setup, but under realistic conditions this is not achievable. The pedestal width not only depends on the preamplifier gain but also features a constant term from noise sources between the preamplifier and the ADC. The ADC also adds smearing to each measurement, but of less magnitude than the effect observed here [41].

The comparison in Figure 4.15 shows a general decrease in S/N ratios from reference setup to cell gain equalised configuration. The mean S/N is reduced by 9.8% from 3.46 to 3.12 on HBU2_VI. This hints to an undisclosed noise source between preamplifiers and ADC stages on the chip, which needs further investigation in the future. The decrease in S/N width roughly correlates to the cell gain distribution and is thus expected.



(a) *Reference preamplifier setup, mean = 3.46, RMS = 1.04*

(b) *Optimised preamplifier setup, mean = 3.12, RMS = 0.53*

Figure 4.15: *Distribution of signal to noise ratios before and after preamplifier configuration on HBU2_VI.*

4.4 MIP Calibration

For physical analyses of the data measured with the EPT, the ADC output has to be converted to the MIP scale (see 2.2.3). For this the most probable ADC value fitted from an acquired spectrum is used as well as pedestal information to rescale each event from ADC to MIP.

Measurements discussed here are not taken from the HBUs commissioned for the hadron test beam EPT layer, as the measurements for these boards were not finished at

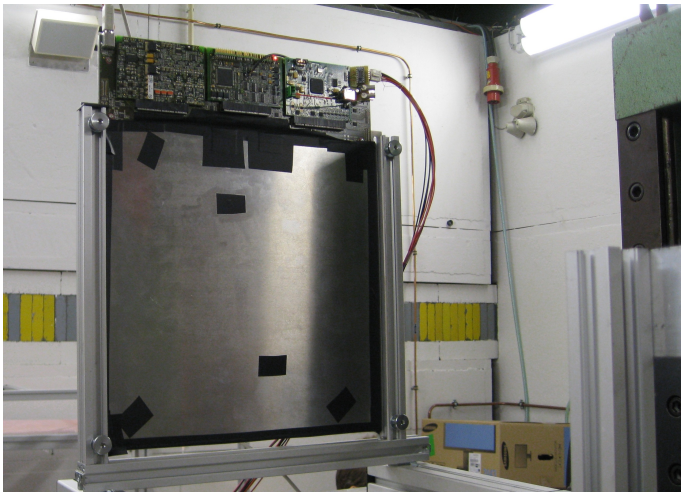


Figure 4.16: *Picture of the HBU2_II board encased in an aluminium cassette, mounted in the test beam area 21 at the DESY-II electron/positron test beam facility.*

time of this writing. This section thus describes the setup used for measuring MIP spectra, examples of the obtained spectra and analysis of tile lightyields and MIP efficiencies of an HBU used for first tests of the HBU2 in a test beam, measured in the spring of 2012.

4.4.1 Setup

The HBU used in test beam is a first generation HBU2 equipped with tiles from the first batch from ITEP numbered HBU2_II. As the DAQ system did not support readout of more than two SPIROCs at the time of test beam data taking, a total of 72 tiles are assembled on only one half of the HBU. Input DACs are calibrated and set up similar to the input DAC procedure described in section 4.2. Two sets of slowcontrol settings are available: A uniform preamplifier feedback capacity configuration of 100 fF and a cell gain equalised preamplifier setup, adjusting the cell gains obtained from LED runs to 21.89 ± 1.11 ADC tics/pixel.

The HBU is mounted perpendicular to the beam axis on a translatable stage. To prevent stray light entering the tiles, the board is encased in an aluminium cassette, with all openings in the cassette covered with black adhesive tape. Additionally the whole setup is wrapped in black light-tight cloth during measurements. A picture of the setup mounted in the beam area is given in Figure 4.16.

The particles used to generate MIP signals are 2..4 GeV positrons from the DESY-II test beam facilities [42]. A thin carbon fiber is placed inside the DESY-II positron beam, which generates bremsstrahlung-photons from positrons hitting the fiber. These X-ray photons are converted into e^+e^--pairs in a metal target. A dipole magnet fans out the particles, sorting their angles by energy. A collimator then cuts out the final beam for usage in the beam area. By setting up the dipole field strength, the energy of emitted particles can be configured. A schematic of the beam generation is shown in Figure 4.17. Depending

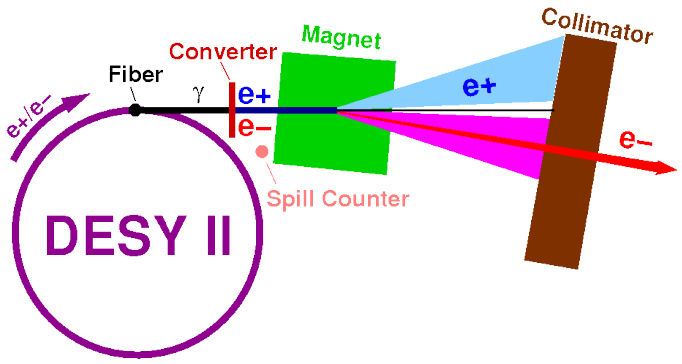


Figure 4.17: *Schematic layout of the DESY-II test beam generation [42].*

on the used collimators, accelerator setup, conversion target etc. particle rates around 2 kHz are expected. As DESY II also delivers beams to other experiments, the beam is interrupted regularly.

All measurements discussed in this section are taken in full self-trigger mode. Measurements in external trigger mode suffer from problems induced by the auto trigger comparators still engaging, as explained in 2.3.3. Each tile is measured on its own, the preamplifiers of all other channels being disabled. The stage position is set up so that the beam hits near the center of the measured tile. Exact positioning is not crucial, as the beam diameter is around 10 cm when hitting the HBU.

4.4.2 Lightyield

A MIP run of around 15000 events is taken for each channel for both preamplifier setups. When using the reference preamplifier setup, it is important to manually configure the trigger threshold for each run. Too high trigger thresholds cut into the MIP peak, which (considering the relatively low statistics taken for each channel) makes it difficult to distinguish between the MIP peak and the trigger edge, leading to possibly wrong fits. Setting the trigger threshold too low causes a high number of triggers from SiPM dark rate, reducing the amount of real data taken, which significantly increases the measuring time until enough statistics is accumulated in the MIP peak for fitting. For the cell gain equalised setup the same trigger threshold can be used for all channels, as the MIP position fluctuates less. Generally the measurements with individually configured preamplifiers are of better overall quality, as they were taken with the experience gained from the reference setup measurements.

The resulting spectrum can be fitted with the convolution of a Gaussian- and a Landau-distribution $LG(x)$. The MIP most probable value (MPV) in ADC tics is then extracted from the extremal position of $LG(x)$. An example high-statistics MIP spectrum is shown in Figure 4.18.

During test beam operation the beam is interrupted regularly, as the DESY-II accelerator is used to generate fills for other accelerators and experiments at DESY. During these

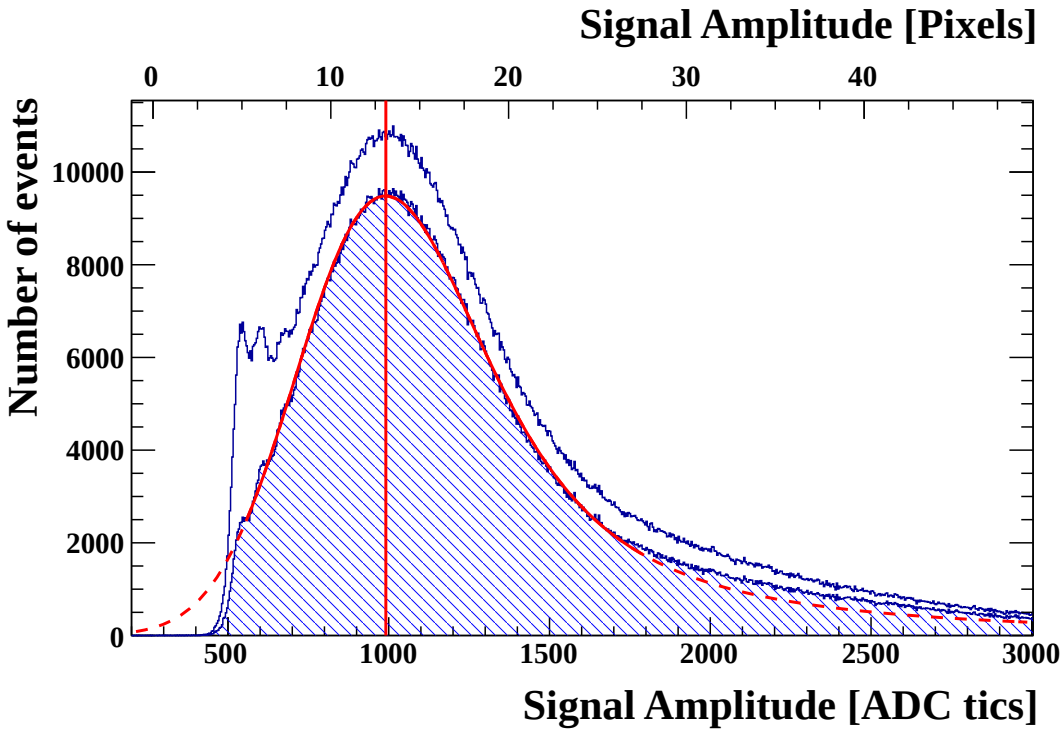
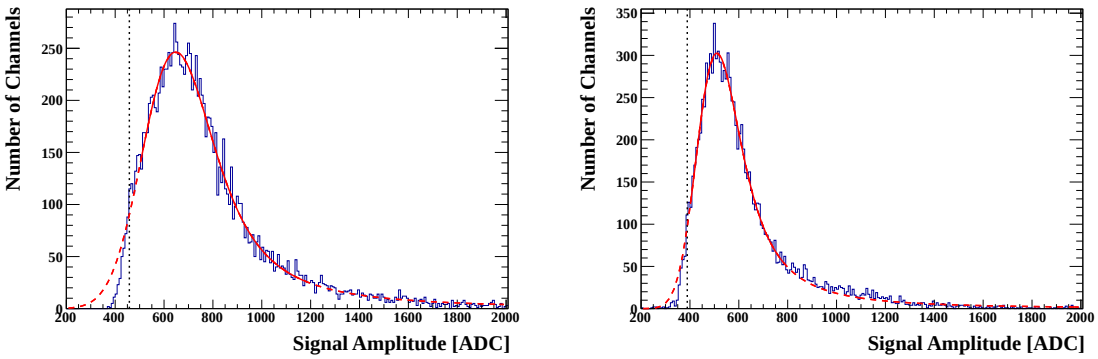


Figure 4.18: *High statistics MIP spectrum measured on a single channel of an HBU2. The upper curve is from raw data while the lower, shaded curve results from cutting readout cycles with less then 13 events. The dashed line depicts the best fit function, drawn solid within the fit range. The vertical line depicts the MPV position. Conversion to the pixel scale is calculated from separate LED gain calibration runs.*



(a) *Reference preamplifier setup* **(b)** *Optimised preamplifier setup*

Figure 4.19: *MIP spectra with fits for different preamplifier setups. The dotted vertical line indicates the 0.5 MIP position.*

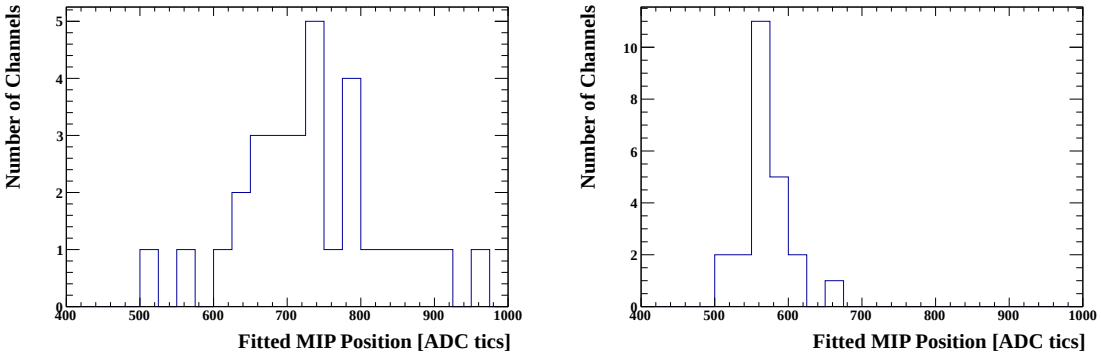
short time frames, only dark rate noise is acquired in the HBU. A simple noise suppression algorithm is implemented to cut events acquired during beam interruptions. The DIF stops the data acquisition and initiates digitisation and readout after a constant time or once all the memory cells are filled. As the beam frequency is usually higher than the noise rate on a single HBU channel, and pure noise is unlikely to generate 16 events in the time frame before the readout is enforced, a readout cycle with less than 13 events is not considered in the MIP spectrum. This visibly reduces the amount of dark rate noise in the spectrum with a cut efficiency of around 90%.

The fit range is chosen based on the trigger threshold for each channel. The applied fit represents a good description of the spectrum, with a small underestimation of the data in the first part of the tail (around 1800-2900 ADC tics in Figure 4.18), which might be explained by a small superimposed two-MIP signal. The fitted MIP position is relatively robust to shifts in the fit range.

Comparison of spectra from the same channel for both preamplifier settings shows a shift in MIP position as expected, spectra of one example channel are shown in Figure 4.19. Comparing the 0.5 MIP position with the position of the visible trigger edge shows that the trigger threshold used in the measurements was slightly below 0.5 MIP.

The distributions of fitted MIP positions confirm a reduction in spread from the preamplifier setup procedure, as shown in Figure 4.20. For an ideally narrow tile lightyield distribution, the relative spread in cell gains and MIP positions should be identical. The spread in cell gains for the board used here is 5.1%, while the spread in MIP positions is 5.2%. This is a weak confirmation of the initial assumption of a narrow lightyield distribution in section 4.3.

Individual normalisation of the fitted MIP positions to the pixel scale of each channel gives the tile lightyield distributions shown in Figure 4.21. For ideal measurements both distributions should look identical. Apart from the reference gain measurements generally being of worse quality than the optimised preamplifier spectra, which is a possible



(a) *Reference preamplifier setup, Mean = 736.3 ADC tics, RMS = 96.6 ADC tics*

(b) *Optimised preamplifier setup, Mean = 563.5 ADC tics, RMS = 29.4 ADC tics*

Figure 4.20: *Distributions of fitted MIP positions.*

explanation of the difference in distribution widths, temperature differences during gain calibration runs might be a reason for the difference in mean lightyields. The optimised preamplifier measurement gives a mean lightyield of 13.60 Pixels/MIP, around 10% less then the lightyield 15 Pixels/MIP specified by ITEP.

4.4.3 MIP Efficiency

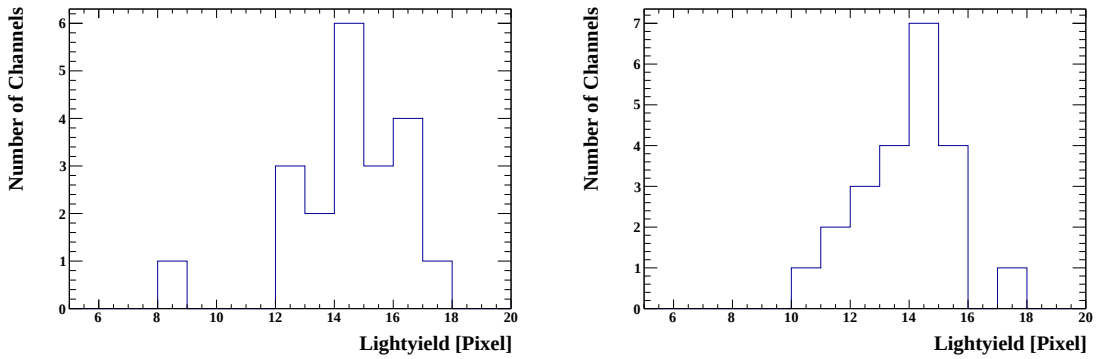
From the fitted spectra obtained in the previous section, the theoretical MIP efficiencies for different trigger thresholds can be obtained. The MIP efficiency is defined as the fraction of total events above the trigger threshold. Using the fit function $LG(x)$, the MIP efficiency as a function of trigger threshold t is defined as

$$e_{MIP}(t) \quad = \quad \frac{\int_t^\infty LG(x)dx}{\int_0^\infty LG(x)dx}. \tag{4.8}$$

The distributions of MIP efficiencies at the 0.5 MIP threshold show a mean MIP efficiency around 95% for both preamplifier setups, as depicted in Figure 4.22. The RMS of the distributions differs, with the reference gain setup featuring a wider range of MIP efficiencies.

Figure 4.23 shows the dependence of the MIP efficiency on the trigger threshold and the correspondent 1σ interval boundaries. The fluctuations observed for the reference preamplifier setup are of much larger scale than for the optimised feedback capacity setup. The estimated mean MIP efficiency does not differ much, als already observed for the 0.5 MIP point. At the 0.8 MIP threshold, the MIP efficiency is still around 80%.

The curve decrease of $e_{MIP}(t)$ is relatively shallow compared to the functional dependence of the dark rate versus trigger threshold, so the dark rate decreases much faster than the MIP efficiency. This makes it possible to increase the trigger threshold while



(a) *Reference preamplifier setup, Mean = 14.45 Pixels/MIP, RMS = 1.89 Pixels/MIP*

(b) *Optimised preamplifier setup, Mean = 13.60 Pixels/MIP, RMS = 1.44 Pixels/MIP*

Figure 4.21: *Distributions of tile lightyields.*

actually increasing the MIP efficiency in the acquired data, as less overall noise is measured. The main problem of this is, that for trigger thresholds $\gtrsim 0.7$ MIP the MIP peak is not reasonably well distinguishable from the trigger edge anymore (especially for measurements with less than 100000s of events).

4.5 Trigger Thresholds in External Validation mode

If the external trigger validation (see section 2.3.3) turns out as working in the current preparation test beam, auto-trigger thresholds have to be set up in a different way than for a fully self-triggered detector. Triggers thresholds for fully self-triggered operation are mainly determined from the dark noise rates of the detector, while the trigger rate does not depend on noise frequency for external validation.

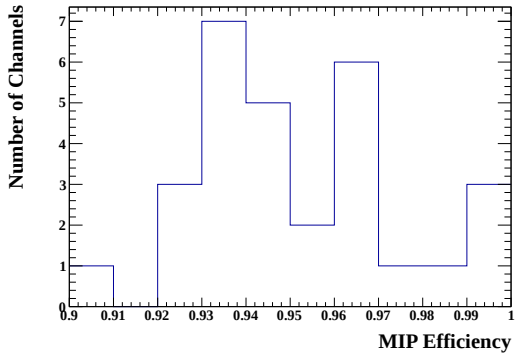
In a simple model disregarding timing and other intricacies of the external validation mode, the acquisition windows, arming the auto trigger comparators, is only activated for a short time after the external trigger fires. As the external triggers are uncorrelated to the noise hits, the noise amplitude distribution can be extracted from externally triggered pedestal spectra. The trigger threshold then follows from the definition of the maximum fraction r of captured noise events compared to total hits.

A noise fraction of $r = 10^{-3}$ is chosen, which roughly equates to ten noise events per cubic meter per external trigger. Determination of the corresponding trigger position is performed by solving

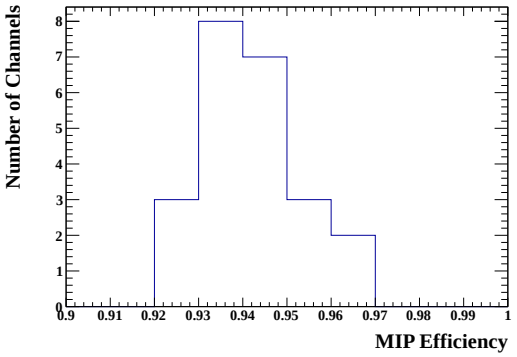
$$r = \frac{\sum_{i=t}^{max} p(i)}{\sum_{i=0}^{max} p(i)}. \tag{4.9}$$

for t, with the number of events in the i-th bin of the pedestal spectrum $p(i)$.

As the best possible approximation of a pedestal measurement done in external validation mode, which was not implemented in the DIF firmware at the time, the HBU is

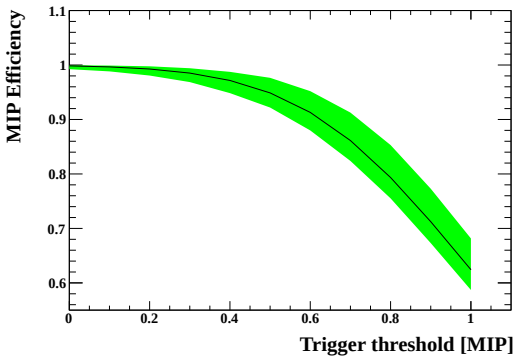


(a) *Reference preamplifier setup, Mean = 0.952, RMS = 0.0022*

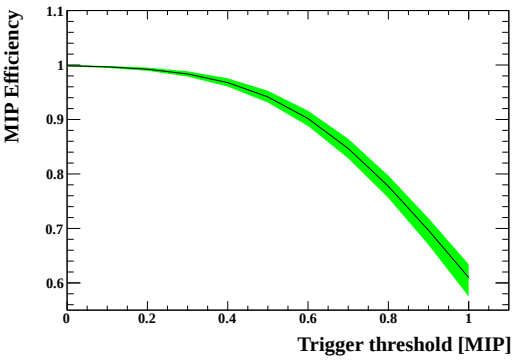


(b) *Optimised preamplifier setup, Mean = 0.954, RMS = 0.0008*

Figure 4.22: *Distributions of fitted MIP efficiencies at 0.5 MIP trigger threshold.*



(a) *Reference preamplifier setup.*



(b) *Optimised preamplifier setup.*

Figure 4.23: *MIP efficiencies as a function of trigger threshold position. The green area marks the* 1σ *interval boundaries.*

operated in external trigger mode. The problems of external triggering described in section 2.3.3 do not interfere with the pedestal measurement, as the pedestal measurement does not depend on correct hold times. The external trigger is set up in the beam area in the exact same setup as it would be used for measurement of externally triggered particles, generated from the coincidence of two scintillator paddles along the beam axis. A schematic of the applied trigger logic is depicted in Figure 4.24. The HBU is moved away from the beam as far as possible and shielded against stray electrons by lead bricks. Example pedestal spectra taken for both preamplifier setups are shown in Figure 4.25. As expected, the pedestal spectrum narrows for a higher feedback capacity.

Distributions of the extracted 10^{-3} threshold positions are given in Figure 4.26. A rough ADC to MIP conversion (assuming a pedestal position of 267 ADC tics and a cell

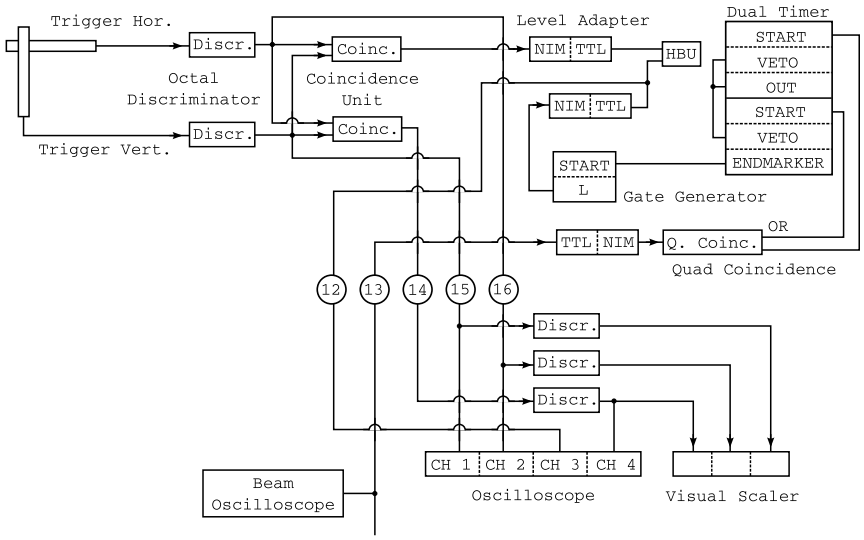
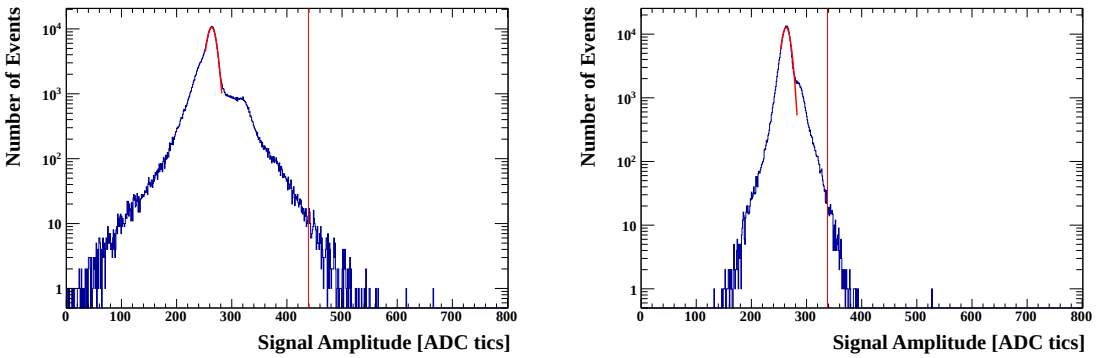
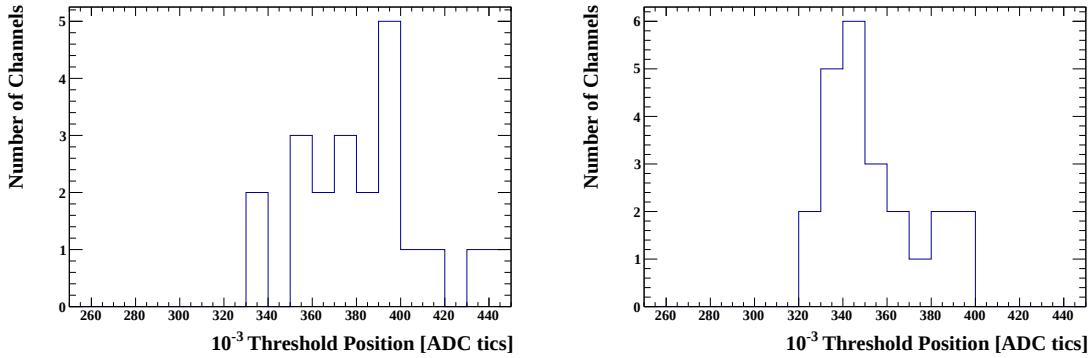


Figure 4.24: *Schematic of the trigger logic used in externally triggered measurements.*



(a) *Reference preamplifier setup, $C_f = 100$ fF.* ***(b)*** *Optimised preamplifier setup, $C_f = 400$ fF.*

Figure 4.25: *High statistics pedestal spectra of one channel measured with external trigger. The vertical line shows the position of the 10^{-3} threshold.*



(a) *Reference preamplifier setup, mean = 382, RMS = 27*

(b) *Optimised preamplifier setup, mean = 353, RMS = 21*

Figure 4.26: *Distribution of 10^{-3} thresholds obtained from pedestal spectra.*

gain of 22 $\frac{\text{ADC tics}}{\text{Pixel}}$) yields a mean threshold position of 0.27 MIP, corresponding to around 98% MIP efficiency (see subsection 4.4.3).

If the difficult timings of the external validation mode can be figured out, the data quality will be improved tremendously as the noise contamination does not depend on the data rate anymore. This is especially helpful for low event frequencies, as expected in the hadron test beam because of the rate limitation of the RPCs used in the DHCAL.

4.6 Pedestal Shift

To obtain a quantification of the pedestal shift effect observed in multiple measurements, the preamplifier load has to be gradually increased while observing the pedestal shift effect on an unloaded channel. This should be done in conditions as close to real operation as possible to get meaningful results, so direct charge injection is not preferred. The LED system is used instead to generate different signal amplitudes from the SiPMs. V_{Calib} should be chosen to generate signal in as many channels as possible without saturating the preamplifier. This is important, as the additional effects of preamplifier saturation on pedestal shifts is not known and hard to measure in the setup described here.

The shifted pedestal signal is extracted from a channel which has no tile equipped and thus can not suffer from SiPM dark rate, optical crosstalk and similar sources of interference. Electrical crosstalk in the SPIROC chip is still possible, but has never been observed to have a major impact on signal quality.

The selection of active channels is performed based on an LED response plot as shown in Figure 3.4. A V_{Calib} range of dense reponse curves is chosen to generate a SiPM signal, so that the LED response on these channels is relatively similar. This enables getting ADC readings on different channels over a wide range of total preamplifier loads without saturating single channels. The preamplifiers of all channels without signal in the used voltage range are switched off, as they would saturate either their preamplifiers

and cause more pedestal shift, or would not give any signal and suffer from pedestal shift. It is important to have as many channel preamplifiers active to measure in the most realistic conditions. For example if pedestal shifts are caused by breakdown of the preamplifier supply voltage due to overload, the number of active preamplifiers might be a factor.

The LED response scan for the used V_{Calib} range 6000 mV - 6800 mV is shown in Figure 4.27. It is scanned in steps of 20 mV for optimal amplitude resolution. Some channels saturate in the higher part of the voltage range, but most channels give a clean signal.

To analyse the measurements the correlation between total preamplifier load (as measured in ADC counts) and relative pedestal shift is plotted. The preamplifier load per event is defined as

$$L_{ADC} = \sum_{chn} (S_{chn} - P_{chn}) , \tag{4.10}$$

with the measured signal per channel S_{chn} and its pedestal position P_{chn}. Pedestal positions for each channel are extracted from a separate pedestal run before the V_{Calib} scan, see subsection 4.3.2. Before insertion into the 2D-histogram, signals of one cycle are averaged per channel.

The resulting correlation plot is shown in Figure 4.28. A linear relation between preamplifier load and pedestal shift is observed. The slope decreases around 25000 – 30000 ADC tics. This is caused by saturation in some of the active channels, thus not adding any more to the read ADC value while still increasing the contribution to the total pedestal shift. The analysis for individual memory cells does not show any dependence on the memory cell. Extrapolation of the linear fit gives a maximum of around 42000 total ADC tics before the pedestal value is effectively shifted into negative ADC regions, at which point data is lost instead of just shifted.

Conversion of the measurements to the MIP scale shows that less than 1% of the total MIP signal is lost per channel. This effect is no problem for single large hits, but for the extremal case of all 36 channels per chip being hit by a 1 MIP signal, this causes the signal to be measured as up to around 30% less.

The main problem of pedestal shifting occurs during calibration, as the scenario of most tiles being hit simultaneously by particles in a shower is rather unlikely. The influence of the pedestal shift effect on the auto trigger has not been investigated yet. If the effect causes a drop in preamplifier output, the trigger discriminator should also be affected.

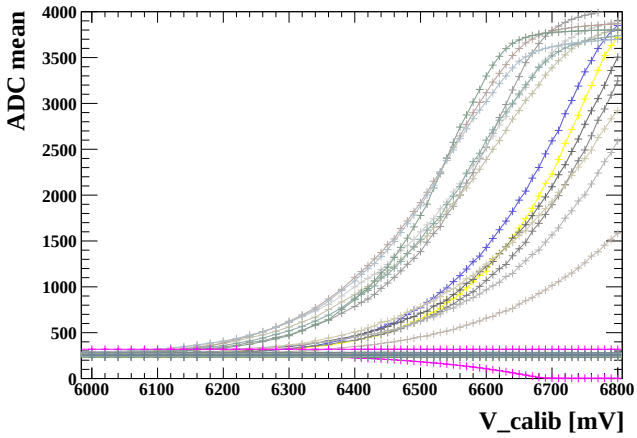


Figure 4.27: *LED response curve for the channels and voltage range used for the pedestal shift measurements. The bottom pink channel is the reference channel which is used to monitor the pedestal shift*

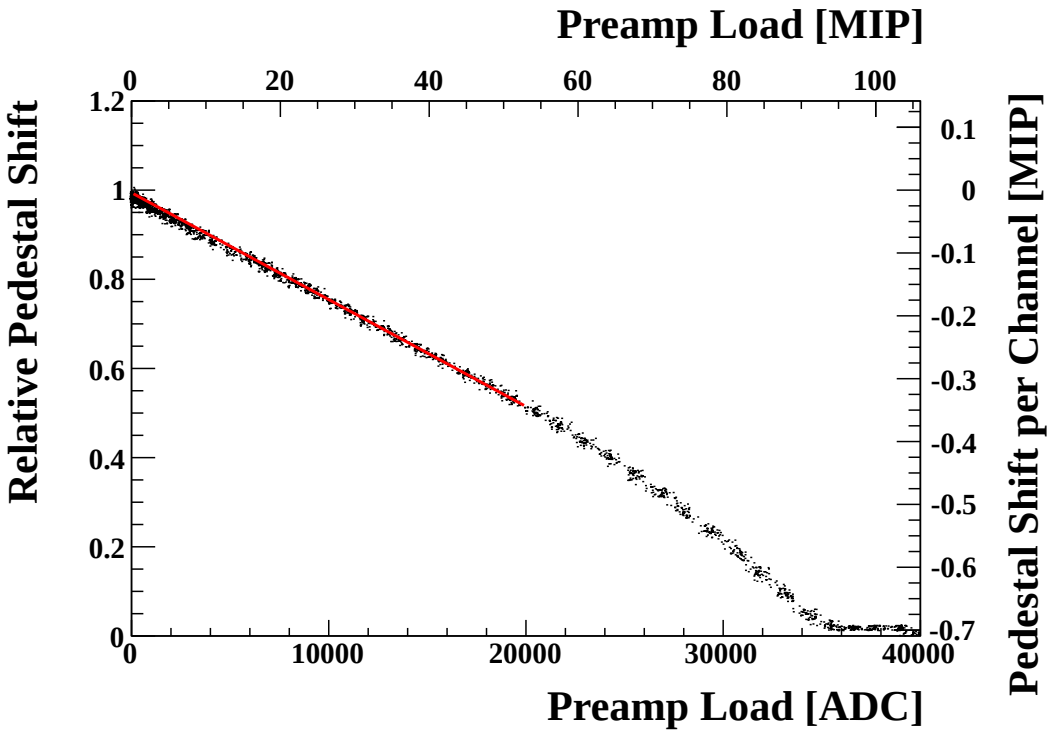


Figure 4.28: *Observed relative pedestal shift as a function of total ASIC preamplifier load. The MIP scale given is a rough estimation based on a lightyield of 15 Pixels/MIP and a cell gain of 25 ADC/Pixel*

4.7 Summary and Conclusion

Four new HBUs have been commissioned from tile assembly up to being ready for MIP calibration for use as an EPT layer in a hadron test beam. Procedures for MIP calibration and lightyield extraction are performed on a different HBU, as the MIP test beam data for the four HBUs used before was not yet available at the time of writing.

Three boards are equipped with tiles from the newer tile batch, while the fourth board is equipped with older tiles from the previous batch. To improve the performance of the board equipped with older tiles, the quadrant nearest to the assumed beam axis during test beam is equipped with the highest gain tiles of the older batch.

A quick, accurate procedure for setting up the input DACs for channel individual bias voltage generation is described. The manual measurement of a full HBU takes around 45 minutes. After correcting the slope deviations of around 5%, a bias voltage resolution of $\approx 20\,\mathrm{mV}$ is achieved.

To homogenise cell gains across the prototype layer, the preamplifiers are configured to compensate the differences in SiPM gains. The measured preamplifier curves as a function of feedback capacity are well parametrised by a hyperbolic function. The mean cell gain after equalisation is slightly lower than the target value of 22 ADC tics/pixel, in the range of 20.5 ADC tics/pixel to 21.7 ADC tics/pixel. The residual gain spread after applying the equalisation procedure is 7.6% to 11.6%, which is higher than expected considering the relatively high preamplifier capacities used. This is mostly caused by outliers which probably result from badly fitted LED calibration spectra. 83 of 576 channels do not give fitable spectra in reference gain setup, while for the optimised setup only 65 channels are not fitable. The mean signal to noise ratio of the LED spectra is decreased by setting up the preamplifiers, however that does not impede the spectrum quality enough to decrease the number of fitable channels. In the future, the calibration procedure has to be improved by a better automatic selection of the fits used for gain determination.

MIP runs are taken in the DESY-II test beam in full auto trigger mode, obtaining MIP spectra for several channels and both available gain configurations. The taken spectra are fitted with a Landau-Gaussian function. A MIP calibration for all measured channels can be extracted from the fitted MPV. The mean lightyield is determined as 13.6 ± 1.4 pixels/MIP. The MIP efficiency at 0.5 MIP threshold is calculated at 95%.

From considerations about the external validation mode, a threshold of 0.28 MIP at a noise contamination of 10^{-3} is extracted from pedestal spectra.

The measurements on pedestal shift show a linear shift in pedestal level for increasing ADC loads. The influence on single high amplitude events is rather low (around 1% for a single 10 MIP hit), but increases substantially for multiple low amplitude events at once. This especially concerns LED calibration runs, as a signal is generated in all channels simultaneously.

5 Conclusion and Outlook

This thesis describes measurements on the LED system and commissioning of the AHCAL
EPT, to be used as an active layer in an upcoming hadron test beam.

The performed tests of the integrated LED system prove, that it can be used to calibrate SiPM gains on the HBU. The performance of calibrating multiple channels at the same time suffers from inhomogeneities in the LED amplitude for different channels. This was initially suspected to be caused by part variances in the LED production process, but the spatial distribution of LED threshold voltages over the HBU suggest a systematic effect, probably depending on the signal distance between the driver OPAMPs and the LED circuit. Compensation of these differences in pulse amplitude via switchable capacities integrated onto the HBU helps to reduce the spread of threshold voltages, but does not fulfill the goal of one single V_{Calib} value for the whole setup.

Further tests on the LED system performed with an upgraded test stand at Wuppertal confirm the spatial distribution of LED amplitudes. Inspection of the trigger signals arriving at the channel pulser circuits show a degraded signal correlated to the observed pulse amplitude. The test stand setup also allows to measure the time offsets between LED pulses on different channels, which has to be incorporated into a possible TDC offset calibration using the LED system. The spatial distribution of timing offsets also shows similar characteristics as for the amplitudes.

Ongoing measurements and research with the test stand aim to improve on these issues, yielding a calibration system that meets all performance requirements.

From the commissioning phase of the EPT layer, many new insights about the HBU2 and the SPIROC chips arise. Many crucial parameters of the setup have to be calibrated for each channel separately, raising the need for efficient measurement procedures, optimised for automation and short measurement times. Such schemes are proposed for the input DAC setup and preamplifier configuration. While the realisation of the input DAC procedure is an overall success, the results of the preamplifer setup can be improved upon, mainly by refining the selection of gain calibration spectra.

Test beam runs of a similar HBU2 board prove the capability of the setup. From the data taken, fitted MIP efficiency curves and tile lightyield distributions are extracted. Inclusion of the data from the current test beam activities with the EPT layer HBUs is not possible, as the measurements are still ongoing at the moment. If the external trigger validation turns out to work in test beam conditions, very good MIP efficiencies and a low total noise fraction will be achieved independent of the signal rate.

A lot of work has been put into the EPT layer by many people, which will hopefully pay off by good results from the upcoming hadron test beam.

In the future, the LED system and commissioning procedures will be applicable in a larger scale EPT, consisting of several layers.

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List of Figures

Hiermit versichere ich, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt sowie Zitate kenntlich gemacht habe.

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