CDF/SEC_VTX/DOC/PUBLIC/1636
Version 1.0, February 16, 1993

Electrical Assembly and Testing of SVX Ladder Modules

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1 Introduction

The basic electrical subunits of the CDF Silicon Vertex Detector (SVX), are called the "ladder modules". Each consists of three silicon detectors serially bonded together to form a long (25.5 cm) sensitive strip which is finally bonded to the input of an SVX readout chip. This document describes the procedures by which these modules were electrically assembled and tested. It is organized in the following way. In Section 2 we describe the configuration of the ladder modules themselves. The overall assembly sequence is outlined in Section 3. In Section 4 we focus on the high density wirebonding procedures. In Section 5 the tests applied to the assembled and bonded ladders are discussed. The testing results are summarized in Section 6. Some of the ladders modules had individual regions with high leakage current. Often this resulted in a collective effect on neighbouring strips we dubbed the "black hole". These effects and their treatment are discussed in Section 7. Finally in Section 8 conclusions are given.

2 Description of the Ladder Modules

In this section we give a short description of the mechanical and electrical configuration of the SVX ladder modules. A general description of the entire SVX detector is given in references [1] and [2].

2.1 Configuration

There are four types of ladder modules used in the SVX detector, one for each layer. These are differentiated by the number of strips they contain (256 strips for layer 1, 384 strips for layer 2, 512 strips for layer 3, and 768 strips for layer 4). Here we keep to the original construction numbering scheme for layers of the SVX detector. Note that for purposes of offline analysis in CDF the layers are instead numbered from $0-3$. This is unfortunate. The readout of the current from the strips is done with the SVX readout chip (Rev. D) [3, 4]. Each chip has 128 inputs. On layers 1, 2, 3, and 4 we used 2, 3, 4, and 6 chips respectively. The mechanical dimensions and layout of the ladders are shown in Figures 1a and 1b. Each ladder module consists of three silicon detectors, a readout hybrid circuit called "ear" to hold and serve the SVX chips, and a composite backing which was fabricated from Rohacell foam (polyanacriline), epoxy, and carbon fibre strips. In the SVX detector array all the ladders are supported between two sets of beryllium rings called the "bulkheads". At one end, the ladder is connected to a bulkhead by a screw through a precision hole in the readout ear. To mount the opposite end a smaller piece of ceramic, the "dummy ear", is integrated into the ladder structure as well. This piece is patterned with a wire–bondable gold film and used to neutralize certain bad strips. This issue is discussed further in Sections 4 and 7 below.

Each ladder was identified by a unique number. This number was a composite of the ear serial number and the chronological ladder mechanical assembly number. A typical number would be "072-1A021" where "072" was the order of construction and "1A021" means layer 1 ear, version "A", assembly number 21.

Stages of the ear construction	Mass of the ear at each stage			
	Layer 1	Layer 2	Layer 3	Layer 4
Printed substrates, without parts and cable				2.55 g
Ears with parts and cable, without SVX chips				3.27 g
Fully assembled ears	1.35 g	1.78 g	2.25 g	3.60 g

Table 1: Material budget of SVX ears

2.2 Readout Hybrids

The assembly process of the readout ears is discussed in Section 3. Corresponding to the ladders there were four versions of the these hybrids [5]. Layers 1, 2, and 3 were fabricated in 0.015″ AlN (aluminum nitride), while layer 4 was fabricated in 0.025″ AlN. This unusual type of substrate was chosen for its good thermal conductivity (about 5 times higher than for the more commonly used Al_2O_3). Circuitry was patterned on both sides with through hole connections using a thick film technology. A larger number of layers were printed on the top side (SVX chip side) and consequently a small bowing of approximately 0.001″ was measured due to the higher coefficient of thermal expansion of the circuit dielectric layers over the AlN substrate. For layer 4, which had the largest aspect ratio, the thicker substrate material was chosen to limit this bowing.

The basic function of the ears was to distribute power, ground, and signals to the SVX chips. In addition, the ears contained bypassing capacitors for the power lines, resistors to set the current in the SVX chip integrator, and a simple RC filter for the detector bias line. An electrical schematic of the ear is shown in Figure 2.

In the design of the ear a natural tradeoff occurred between the minimization of material (radiation lengths) and the need for mechanical and electrical stability and reliability. Consequently, the substrate thickness was less than the fabrication vendor recommended. This led to occasional breakage of substrates and the adoption of particular handling procedures during processing. The material budget of the ear is given in Table 1.

The production yields of the hybrids was reasonably high especially after institution of good quality control and inspection procedures during processing. Typically 10 – 15% of the printed substrates would have random electrical defects. Following this another 10 – 15% of the parts would be lost at each major assembly juncture (mounting of solder components and cables, die attach and wirebonding, electrical test). We usually printed 100 substrates to have finally 40 fully assembled and functional units plus some unassembled spares.

2.3 The SVX Chip

Because much of the performance evaluation and testing of ladders discussed in this note is determined by the properties of the SVX chip we will describe it briefly here.

The SVX chip is a mixed analog and digital signal processing circuit. Revision D, which is used in the final SVX system, was fabricated in 3 μm CMOS technology. The CMOS process used was not radiation hard. A new version of this chip now exists which is radiation resistant and it is called SVX Revision H3. A block diagram of the SVX chip and timing pattern is shown in Figure 3. The chip contains 128 identical channels of charge integration, voltage amplification, sample and hold, and comparator/latch. These

are followed by a priority encoding circuit which allows a multiplexed analog readout to select only those channels for which the latch is set (or not set). This selective readout mode is called "sparse". Optionally, a global latch line may be asserted forcing a readout of all channels. This mode of readout is called "latch all". When the chip is read out, the address of the channel currently being read appears on a 7 bit address bus along with the corresponding analog level.

The charge integrator consists of a single cascoded stage with a reset switch. Contrary to usual practice, the output is taken off the center which is a relatively high output impedance in order to limit the preamplifier bandwidth and consequently the noise. The charge integrator operates off a supply voltage between 0 and 6 V. The input reset point is at 1.1 V. The cascode current can be set by an external resistor, one per chip. The standard operating current is between 80 and 100 μA per channel. The input to the integrator is protected by back to back diodes between 0 and 6 V. The integrator has a gain of 3.5 mV/fC and is followed by voltage gain stages such that the total gain product is 15 mV/fC. A test input per chip is provided with a calibration capacitor of 60 fF.

The SVX chip was designed to read out DC coupled silicon detectors. In order to have an efficient threshold comparison on a channel by channel basis it is therefore necessary to subtract the baseline shift due to varying strip to strip leakage current which will be integrated during the sampling time. This process is accomplished in the SVX chip through a quadruple sample and hold process. In this process the charge is integrated twice (once "on beam" and once "off beam"). The results of these two integrations are subtracted. If any particles had passed through the detector "on beam" an excess would remain at the nearest strip. In a charge integration and sample and hold circuit one integration from time t_1 to time t_2 would require two samples. This is called a double sample and hold measurement and an example is the CDF calorimetry before/after process. The leakage current subtraction described here requires two integrations and is consequently a quadruple sample and hold measurement.

In performing a quadruple sample and hold operation and reading out sparse data there are a number of options which may be selected. In addition to the latch all feature describe above, the SVX chip has the ability to read out either channels which are above the reset point of the latch ("postive sparse") or below the reset point of the latch ("negative sparse"). These options are selected by a bit set during chip initialization. Furthermore the user has a choice whether to integrate during collisions in the first or second of the two integation periods which comprise the quadruple sampling. The overall analog transfer function is an inversion of the voltage stored during the second integration period minus the first integration period. If holes are collected from the silicon strips and a particle passes through the detector during the first (second) period the analog out will increase (decrease) with respect to it's reset point.

When the analog system noise is measured, a double sample and hold will increase the intrinsic preamplifier noise by a factor of $\sqrt{2}$ for frequencies which are short compared to the inverse of the integration time. A quadruple sample and hole will contribute another factor of $\sqrt{2}$ to double the intrinsic noise. In Figure 4 we show the equivalent input noise (output noise voltage converted to input charge) of the SVX chip as a function of detector capacitance for both a double and quadruple sample and hold measurement. The fully bonded SVX ladders correspond to about 30 pF of detector capacitance.

The behaviour of the comparator circuit in the SVX chip which controls the sparse readout will be affected by the electronic noise. Rather than having a perfectly sharp transition at threshold, the transition will be spread. The threshold value and its width

can be measured by performing a quadruple sample and hold integration and observing the fraction of time a particular channel appears in the readout as the test input charge is varied for one of the two integration periods. A typical channel response is shown in Figure 14. It is possible to unfold the width of the underlying gaussian noise distribution from this curve by a method discussed in Section 5 and the Appendix. For good channels this quantity is 0.4–0.5 fC which corresponds to the quadruple noise shown in Figure 4.

The absolute value of the threshold itself is a quantity which will be affected by chip to chip variations in internal offsets, errors in the leakage current subtraction due to timing and preamplifier saturation, and parasitic charge injection related to the layout of the electrical system on the SVX. The requirement for efficient operation of the detector is to keep these variations at the same level as the threshold width. This is discussed further in Sections 5 and 6.

2.4 CDF Silicon Detectors

The silicon detectors used in the ladder construction are DC coupled and single sided. For layers 1, 2 and 3 the strips are on a 60 μm pitch. For layer 4 they are on a 55 μm pitch. The bonding pad pattern is indicated in Figure 5. The processing steps used in fabrication were optimized for low surface leakage current. In particular, a final sintering step at 400 C in forming gas served to lower the average strip leakage to 300–500 pA for an 8.5 cm strip at 20 C. Consequently the full leakage for a ladder strip was less than 2 nA. The detectors all have fully enclosing guard rings which were always grounded though the preamplifier ground on the SVX chip. Typical guard ring currents are much higher than single strip currents, in the few hundred nA range. It is important that the total detector current (including the guard ring) not be too high because shot noise can cause large fluctuating voltage drops across a 10 $k\Omega$ filtering resistor which is in the bias line. The drops will cause charge to be injected into the SVX chip through the detector capacitance which will appear as common noise on all read out channels connected to that detector.

An acceptance specification was applied to the silicon detectors used in the SVX. There were four basic categories (GOLD, SILVER, BRONZE, and FAIL) which are defined in Table 2. A basic principle of this specification was to limit the number of strips with current above 70 nA. These are useless and had to be skipped during wirebonding.

3 Assembly Sequence

This section describes the assembly sequence of the ladder modules, which is also sketched in Figure 6.

The silicon microstrip detectors used for the SVX were manufactured by Micron Semiconductor (United Kingdom). The manufacturer measured depletion voltage and individual strip currents and interstrip resistances for all strips. The detectors were shipped to Fermilab, where they were visually inspected and then all strips were probed again for leakage current and interstrip resistance. Generally the Micron and Fermilab measurements were in agreement although sometimes additional bad strips were identified at Fermilab. Disk files were kept of the strip leakages for all strips as well as ladder composites for the chosen triplets. In the case of bad strips detailed current–voltage characteristics were often saved as well.

The SVX readout chips (revision D, 3 μm CMOS technology) were manufactured by Hewlett–Packard Corporation. The wafers were fabricated in a four inch technology at

		Layer 1	Layer 2	Layer 3	Layer 4
GOLD	Max. # of strips with $I > 75\ nA$	1	1	2	2
	Max. # of strips with $I > 10\ nA$	2	3	4	6
SILVER	Max. # of strips with $I > 75\ nA$	–	1	2	3
	Max. # of strips with $I > 10\ nA$	–	4	5	9
	Max. # of strips with $I > 75\ nA$	1	2	2	4
	Max. # of strips with $I > 10\ nA$	3	4	6	10
	OR				
BRONZE	Max. # of strips with $I > 25\ nA$	0	0	0	–
	Max. # of strips with $I > 10\ nA$	5	7	10	–
	OR				
	Max. # of strips with $I > 400\ nA$	–	–	–	0
	Max. # of strips with $I > 10\ nA$	–	–	–	5

Table 2: Acceptance specifications for the SVX silicon detectors

the HP Corvalis, Oregon facility. Each wafer contained 110 SVX chips. Each wafer was evaluated at LBL using an automatic probe station. The chips were tested for basic digital function, power supply currents, noise, gain, and analog offset level, sparse readout, and for the presence of dead channels. Although the yield differed from wafer to wafer, typically 50 - 60 % of the chips were perfect. Notably, on a subsequent production run of the same chip for another customer the yields dropped to 15 % for no identifiable reason.

The printing and assembly of the four different readout hybrids was performed at Promex Inc. (Santa Clara, California) using the multilayer thick film technology on AlN substrates. After basic continuity checks of the boards, electronic components were mounted, a small kapton cable (to communicate with the data acquisition) was soldered to the external end of the board, and the SVX chips were attached and wirebonded. The chips attached to the same hybrid were selected in groups that had DC analog levels within 7 mV of each other. Then these multichip modules were brought back to LBL where their main electrical features (response to charge injection, stability, chip ID, channel addresses, positive sparse, negative sparse) were checked. Finally the readout boards were brought again to Promex for wire encapsulation, and then back to LBL for further electrical testing and burning in. The standard burn–in was to operate the modules at room temperature under clocking for 100 hours. No modules failed after this burnin.

Once ready, the readout boards were shipped to Fermilab where the mechanical assembly of the ladder modules was performed. The 3 detectors used for each module were matched to have similar depletion voltages. Furthermore, detectors were selected from among the acceptance categories GOLD, SILVER, and BRONZE to distribute bad strips as widely as possible amoung the ladders. The assembled ladders modules were then sent back to LBL.

The wirebonding took place at Promex, where the corresponding strips on adjacent detectors of the same ladder were electrically connected to each other, and then finally to the input of the corresponding channel on an SVX chip. The last step of the assembly of the ladder modules took place at LBL, where the back side of the detectors were connected to a bias pad on the back of the ear board. The ladder modules were then ready to undergo electrical testing, burning in, and eventually black hole fixing in some cases.

Finally the ladders were shipped back to Fermilab to be mounted on the SVX bulkheads

to form the two barrels of the final detector. At Fermilab the ladders were all retested twice, before and after mechanical survey was done to check for any slow shifts in detector positioning.

4 Wirebonding

The SVX ladders were wirebonded on a Kulicke and Soffa Model 1470 aluminum wedge bonder with a 30 degree wire feed. Although this machine had an automatic (programmable) bonding capability this was not used. All bonding was done in manual mode. The operator selected the first and second bond locations using crosshairs on a video monitor. After the second location was selected, the machine enacted the full bonding cycle. All bonds were done with a 1 *mil* diameter wire (99% Al, 1% Si). The bonding tool used was a Gaiser 2131-2025 (see Figure 7).

4.1 Bonding Parameters

We sought to minimize bonding power, time, and force to avoid damage to the silicon detectors. Damage to the detector could include microcracks in the junction, scratches and cracks in the oxide layer, and delamination of the bond pad. A particular parameter set is machine dependent even for the same model machine. For our machine the parameter set is given in Table 3. These can be interpreted somewhat absolutely by referring to Figures 8a and 8b.

4.2 Fixturing

A considerable effort was made to optimize the bonding fixtures used to support the ladders during bonding. The main issue was to rigidly support the silicon underneath the bonding point. If this is neglected, the silicon can yield under the wedge and bonding energy will be inefficiently transferred to the pad and wire. An example of the fixturing is indicated in Figures 9 and 10. Note the platforms under the bond area. The visible holes were for a vacuum which held the ladder down to the fixture. These fixtures were made of steel to prevent any small dents or nicks from forming which could affect the planarity of the fixture. During the bonding process the entire machine recoils against the rotating bond head. The bonding fixture was held rigidly on a pedestal so that it would not move independently of the rest of the machine nor oscillate due to the impulse. After a bonding session the fixture was removed and cleaned with acetone and blown dry. It was always stored in a plastic bag to prevent any rusting.

4.3 Procedure

The bonding procedure was guided by a bonding log and checklist which was followed for each ladder. A sample log is shown in Figure 11. Bonds were made on two levels (inner/outer). On each level we consequently bonded on twice strip pitch spacing for that detector type. Strips that were measured to have a leakage current in excess of 70 nA were not bonded to the SVX chips. After all the inner bonds were completed the ladder was removed from the machine and inspected under a microscope. Occasionally there would be shorts between adjacent wires which were easily separated with a fine needle. Sometimes the bonding machine would miss the pad and the bond would actually be on the silicon

Bonding hardware		
Machine	manufacturer	Kulicke and Soffa
	model	1470 30 degree wire feed
Tool (see Fig 7)		Gaiser 2131/2025
Wire	diameter	1 *mil*
	material	99% Al, 1% Si

Bonding parameter settings		
Bonding mode		Manual
Clamp control		Open at tear
Overtravel (OTV)		7
Ultrasonic generator		LO–LO
Ultrasonic power (see Fig 8a)	first bond	4.8
	second bond	5.0
Time	first bond	45
	second bond	40
Velocity (CVL)	first bond	7
	second bond	7
Loop height	inner wire, detector to chips	35
(see Fig 8b)	outer wire, detector to chips	80
	inner wire, detector to detector	30
	outer wire, detector to detector	50

Table 3: Bonding conditions and parameters

dioxide between pads. In this case the operator would pull the bond off with a small chisel like tool. This could usually be done cleanly and the missed bond could be redone (see section below on problems). After this inspection the upper bonds were done followed by a similar inspection. Microbonds were also made to connect the guard ring of each detector to a ground pad on the SVX chips. The typical time for the entire process depended upon the ladder type and was approximately 2 hours for layer 1, 2.5 hours for layer 2, 3 hours for layer 3, and 4 hours for layer 4. A total of 122 ladders were bonded (excluding tests), representing nearly 175,000 microbonds.

4.4 Problems

A number of problems were encountered during the wirebonding process worthy of note.

- **Falling wires.** If wires were too long they failed to hold a stable arc and would short to neighbors. A study of this indicated that the maximum reliable wire length was 0.140″.
- **Misaligned bonds.** Occasionally the machine would place the wire clearly off the targeted pad center. If the bond foot was more than about 25% off the pad we would remove the wire and rebond.
- **Missing wire.** Occasionally the machine would loose the wire and hit the detector on the silicon dioxide next to the pad. Two small marks would appear corresponding to the edges of the tool. This was very bad because that spot would generally source a large surface leakage current due to the induced defect in the oxide, eventually creating a black hole (see Section 7).
- **Bonds not sticking.** There were cases in which bonds would not stick to the ladder. In a number of instances this occurred after the machine had been used for a different job. Usually by putting in a new wedge or new spool of wire this could be fixed. On one ladder we were unsuccessful in bonding at all. Close inspection revealed brown spots on the bond pads which Micron later suggested might be nitric acid damage.

The only implication of these problems, is that sometimes good channels could not be connected to the front-end electronics, or got damaged by the bonding process. The rate of these problems still remained very low, as can be seen from Table 4.

4.5 Yield

Table 4 shows that among the 125 ladders that we put on the bonding machine, 108 ended up to be working ladders; in other words the electrical ladder assembly and testing had an overall yield of 86.4%. The losses were due to electrical failures observed after wirebonding (8.8%), accidents during which ladders were damaged or broken (3.2%), and situations where we failed to perform the wirebonding (1.6%).

5 Testing Procedures

Almost all the electrical tests made at LBL on the ear boards and the ladders consisted of automatic procedures driven from a computer. The data acquisition involved in these tests was made through a CAMAC interface, and a computer program calculated for each

	Layer 1	Layer 2	Layer 3	Layer 4
Number of SVX production ladders built	33	32	33	31
... built misaligned or broken before bonding	–1	–1	–2	
Number of ladders put on bonding machine	32	31	31	31
... unbondable		–1		–1
... broken by accident during bonding		–1		
Number of bonded ladders	32	29	31	30
... not working at all after bonding	–2	–1	–3	–1
... partly not working (one chip failure)			–1	–1
... with bad impedances on input lines		–1	–1	
... broken by accident after bonding			–1	–2
Number of ladder functioning reliably	30	27	25	26
... BH fixed by strip disconnection only	1	1	3	
... BH fixed by strip connection to guard ring			1	
... BH fixed by strip connection to dummy end	2	3	7	13
... fixed (but not because of BH)	1			1
Number of ladder used in the final SVX system	24	24	24	24
... BH fixed by strip disconnection only	1		3	
... BH fixed by strip connection to guard ring			1	
... BH fixed by strip connection to dummy end	1	3	7	11
... fixed (but not because of BH)	1			1

Table 4: Ladder yields

channel a number of characteristic quantities which were saved on disk in direct access files (HBOOK4 RZ files). The data contained in these files could then be graphically displayed or analyzed to look for bad channels. The results of these tests also allowed us to identify the strips that were responsible for black hole effects.

Before assembling an ear board to silicon detectors, the following testing procedure was applied to make sure the ear was functional:

a) check of the digital lines and of the response to charge injection;

b) burn in of the ear board for 100 hours and then checks a) again.

The sequence for the ladder testing procedure was more complete and involved quantitative measurements as well:

a) check of the impedances to ground on the output and control lines. If any input had suffered static charge damage it would have typically a small impedance to ground. Good inputs were always in excess of 400 $k\Omega$ to ground.

b) check of the digital lines;

c) measurement of some characteristics of each channel of the ladder; the following quantities were measured for each channel and the results saved to disk files:

- charge gain and offset in double sample and hold mode;
- charge gain and offset in quadruple sample and hold mode;
- differential noise in double sample and hold mode;
- differential noise in quadruple sample and hold mode;
- leakage current;
- sparse threshold and RMS of sparse threshold;

d) if needed, black hole fixing, and then measurements c) again;

e) burn in of the ladder module for 100 hours, and then measurements c) again;

f) if needed, black hole fixing, and then measurements c) again.

Steps b), c), and e) were performed at "full bias voltage". The full bias voltage was defined for each ladder as the maximum (or sometimes the average) value of the 3 detector depletion voltages, plus 15 V.

In the rest of this section, we describe the testing and burn in setup and then give a complete description of the measurements that were made on the ladder modules. The results of the tests, the interpretation of the data and the black hole fixing process are described in further sections.

5.1 Setup for Ear and Ladder Testing

The SVX testing setup at LBL consisted of two almost independent testing stations, one for ear boards and another one for ladder modules, each including a testing box connected to the two key CAMAC modules that allow the operation and readout of the SVX chips, the SRS and the SDA [6]. Figure 12 shows the setup used to test ladders.

The ladder testing box allowed us to operate 6 ladders simultaneously (all the chips are daisy chained like in a SVX readout wedge). In that box, each ladder was mechanically supported on its readout ear and dummy ear boards. The small flexible kapton cable coming out of the ear was connected to a test cable (also flexible kapton) that hooked up to a testing "mother cable". This mother cable was common to all the ladders in the box and transmitted input and output signals between the ladders and the port card also located in the testing box. The port card is a circuit which provides a number of support functions to the SVX ladders. These included digital interface and transmission, analog driving, calibration, and power regulation.

The electrical contacts between the ear board cables and the test cables were made with G10 plastic clamps identical to those that are used to connect the ladders to the real SVX mother cable. The port card used was a prototype version of the final SVX port card; since this prototype didn't carry the bias voltage lines, the box needed separate connectors for the bias voltages to be applied to the ladders.

The ladder testing box was initially equipped with a water cooling system although it was not finally necessary to flow water, because the metallic supports of the ear board were large enough to take away the power dissipated by the SVX chips (less than 0.2 W each).

It was also possible to flow dry air inside the testing box, and this had to be done constantly in order to obtain consistent measurements of the ladder properties (ladders are very sensitive to air moisture). In particular a subset of the ladders showed particular sensitivity to moisture. These ladders would have large leakage currents, especially near the edges, which persisted for up to one hour in a dry atmosphere. After that drying out period they behaved more like typical good ladders. Because of this easy improvement we never used this moisture sensitivity as a criteria for rejecting a ladder. Later during operation of the SVX detector in CDF, most of these ladders showed anomalous surface currents again. This effect, which in the end was more annoying than significant in terms of the successful operation of the detector, will be the topic of a forthcoming note.

Finally, since the SVX chips are photosensitive, the box was designed to be hermetic to light.

The SRS and SDA CAMAC modules were connected to the port card through a special receiver module. The SRS (SVX Readout Sequencer) generated all the input signals for the SVX chips and the SDA (SVX Data Acquisition module) collected and digitized the data sent back by the chips. The receiver module transmitted the signals between the SRS/SDA modules and the port card; it required also as input a voltage used to inject charge in the chips. This calibration voltage could be supplied by a DAC that was located in the same CAMAC crate as all the other modules.

The ear testing station is very similar to the ladder testing station. The corresponding testing box allowed to operate 16 ear boards at the same time and also had its own prototype version of the port card.

Finally an oscilloscope was used to display the signals received from the ears/ladders on the analog output line or on the digital lines.

The two stations could be operated simultaneously (and independently) during the burn in of ears and ladders. However, when doing measurements using analog information from one of the stations, the other station had to be turned off to avoid picking up noise from the other SRS clocking in an asynchronous way in the same CAMAC crate. This limitation had a negligible influence on the efficiency of the whole testing setup.

5.2 Digital Checks

The purpose of these checks were the following:

- verify that the chips can be operated and read out;
- verify that the individual channel addresses within each chip follow the correct sequence from 0 to 127 (7-bits addresses) in latch all mode;
- verify that a chip ID (6 bits) can be stored successfully in each chip.

These checks were performed by running into the SRS a two step program. During the first step all six chip ID bits of all chips are set to 0, and then a readout cycle was performed (in latch all mode) to check that a chip ID of 0 was returned by each chip and that all channel addresses were correct. The second step was similar, except that all six chip ID bits were set to 1, and that the chip ID returned during the readout cycle was checked to be equal to 63.

As shown in Table 4, some ladders or chips didn't work at all after wirebonding. For the other ladders modules, the yield of these tests was very good; most of the failures observed were in fact fake failures due to a bad contact between the ear cable and the test cable and these digital checks were practically in most case a check of the kapton cable connections.

All working ears and ladders successfully passed these digital tests, except one ear/ladder that has a single channel that cannot be readout, even in latch all mode, probably due to an internal failure in the corresponding chip. Chips with such failures had normally been rejected when they were tested on the wafers; this particular chip escaped that quality check, or it developed a failure after the wafer testing. Since the ladder on which that chip was mounted was otherwise a good ladder (above average) we decided to use this ladder in the final SVX detector. Subsequently the missing channel reappeared during operation of the full SVX detector for colliding beams at Fermilab.

5.3 Gain and Offset Measurements

The measurements of gain and offset are a basic quality test of the analog signal coming out of the SVX chips. The results of these measurements were a "calibration" of the device, in the sense that they allowed us to establish a relation between the voltage on the analog output line, V^{out}, and the charge deposited in the silicon by a particle passing through a ladder.

Charge injection was made by sending a voltage step, V^{cal}, on the calibration line of the ladder; for each channel in that ladder, this voltage step was converted into a charge by a capacitor, C^{cal}. The exact value of C^{cal} lays within 10% of a nominal value of $60fF$, but the difference between the calibration capacitors of any two channels in the same ladder was believed to be negligible; therefore, the injected charge,

$$Q^{inj} = C^{cal}V^{cal} \tag{1}$$

was the same for all the channels of the ladder.

The relation between V^{out} and V^{cal} was expected to be linear in some range. Therefore, for a given operation mode of the SVX, two calibration constants had to be determined for each channel: the gain $G^{(V)}$ (or $G^{(Q)} = G^{(V)}/C^{cal}$) and the offset V^{off}. The linearity of the response is expressed as:

$$V^{out} = V^{off} + G^{(V)}V^{cal} = V^{off} + G^{(Q)}Q^{inj} . \tag{2}$$

The nominal values of the offset and the gain are determined by the SVX chip properties, but the real values for a given channel are affected by the leakage current that is present on the strip connected to that channel: this leakage current directly affects the offset V^{off} in case a double sample and hold is performed (because the effective injected charge is equal to the sum of Q^{inj} and the charge due to leakage); furthermore, if the leakage current is high enough, the amplifier may saturate (and thus depart from its linear response) and this will result in a change of the gain $G^{(V)}$ which may eventually go to zero.

The gain and offset measurements were performed by stepping through M different values of V^{cal}. At each step j, corresponding to a voltage step V_j^{cal} on the calibration line, N events were read out in latch all mode. Then, for each individual channel, the mean values of the voltage on the analog output line was computed over these N events. This average (pedestal) was computed as

$$V_j^{out} = \frac{1}{N} \sum_{i=1}^{N} v_{j,i} \tag{3}$$

where $v_{j,i}$ was the voltage read out on the analog output line during event i of step j for a particular channel ($v_{j,i}$ was computed as a linear function of the number of ADC counts). After all the steps are completed, the gain $G^{(V)}$ and the offset V^{off} of each individual channel were computed as the slope and intercept of a linear fit through the points (V_j^{cal}, V_j^{out}).

Practically, we used $M = 10$ steps (with values of V_j^{cal} equal to 50, 100, 150, 200, 250, 300, 350, 400, 500, and 600 mV) with $N = 10$ events each, and the straight line fits were restricted to the first 5 points, because of a possible saturation of the amplifier chain. The gain and offset of all channels were measured (and saved to disk) for two different SVX operation mode, double and quadruple sample and hold, each with a 1500 ns integration time interval.

Figure 13 shows three typical analog responses to charge injection for both a) a double sample and hold program and b) a quadruple sample and hold program. The points are measurements of V^{out} as a function of Q^{inj} done on channels 042, 197 and 219 of ladder 106–4B032 (channels are numbered from 1 to 768 on this ladder, according to readout order). The straight lines are the linear fits done on the first 5 points (region where the lines are solid). As can be seen from that figure, channel 219 is a good channel, with low leakage current: its response for a double or quadruple sample and hold mode is about the same, showing that the leakage current does not provide a significant amount of charge at the amplifier input. Channel 042 has a low pedestal in double sample and hold operation mode, very likely due to a significant leakage current contribution; at high values of injected charge, the response even becomes nonlinear, indicating that the amplifier is starting to saturate. However, the leakage current contribution is reasonably taken out in the quadruple sample and hold mode, and channel 042 can be considered as a good channel when operated in this mode. Channel 197 has a very low gain both in double and quadruple sample and hold modes: it's a dead channel; the leakage current in this case is so big that it saturates the amplifier which becomes almost insensitive to an additional injected charge.

5.4 Noise Measurement

We define the noise on the analog output of a given channel as the standard deviation σ_v of the analog output voltage v for that channel:

$$\sigma_v^2 = \overline{v^2} - \overline{v}^2 \ . \tag{4}$$

Practically, the quantity σ_v can be estimated by computing the root mean square value of the analog output voltage of the considered channel over a big number N of events. This noise corresponds to a fluctuation of the analog output level; if the charge gain $G^{(Q)}$ of the amplifier is known (see gain and offset measurement), this fluctuation can be expressed as a fluctuation of the input integrated charge; we thus also define a noise

$$\sigma_Q = \frac{\sigma_v}{G^{(Q)}} \tag{5}$$

that can be expressed in fC or in units of the electron charge.

This measurement can be done in either double or quadruple sample and hold modes. The noise measured with a quadruple sample and hold program is expected to be higher than the noise measured with a double sample and hold program by a factor $\sqrt{2}$, because the analog output for a quadruple sample and hold program is the difference of two independent voltages that have the same standard deviation as the analog output for a double sample and hold mode.

The noise measurement is ideally a check of the electronic noise of the SVX chip amplifiers. The expected value of this noise with a full 30 pF detector capacitance is 2000–2500 electrons for a quadruple sample and hold. In a practical measurement this noise may be increased by a number of effects. Because of the specific modes of operation of the SVX chip different sources of additional noise will appear in particular ways. The SVX chip works by integrating charge in parallel on all inputs for a period of roughly 1 μs. Following this, each channel (or each latched channel) is then read out serially. Any one channel is typically driving the output bus for roughly 2–3 μs. The entire length of the readout scan depends upon the number of channels being read but for a Layer 3 ear would be typically 1–1.5 ms. These two operating modes and time scales determine the susceptability of the system to additional noise. High frequency noise which occurs during the parallel integration of charge will appear as a coherent shift on the analog output of all channels read out in a particular scan. A typical source of this noise would be fluctuations on the bias line of the silicon detector. The detector looks to the preamp as a capacitor in parallel with the input with a rough value of 1 pF. Low frequency noise (such as 60 Hz line noise) which occurs during readout will also appear as a coherent shift on the analog output of all channels read out in a particular scan. Finally noise with a frequency close to the readout clock but out of synchronization will appear as incoherent noise on a sequence of read out channels. All these sources of additional noise can to some extent be limited by the testing setup, grounding, filtering, and power distribution systems.

Because of the potential susceptibility of the system to external noise we defined also the "differential noise" of a given channel as $1/\sqrt{2}$ of the standard deviation of the difference between the analog output voltage v for that channel and the analog output voltage v' of a neighbor channel:

$$(\sigma_v^{diff})^2 = \frac{\overline{(v-v')^2} - \overline{v-v'}^2}{2} \tag{6}$$

Practically, the quantity σ_v^{diff} can be estimated by computing the root mean square value of $(v - v')/\sqrt{2}$ over a big number N of events. The differential noise can also be expressed as a charge,

$$\sigma_Q^{diff} = \frac{\sigma_v^{diff}}{G^{(Q)}} \tag{7}$$

and be measured for the two different modes of operation. Again, the differential noise measured with a quadruple sample and hold program is expected to be higher than the differential noise measured with a double sample and hold program by a factor $\sqrt{2}$. Assuming that $\sigma_v = \sigma_{v'}$, i.e., that the considered channel and its neighbor have the same noise, we have

$$\begin{aligned}(\sigma_v^{diff})^2 &= \frac{\sigma_v^2 + \sigma_{v'}^2}{2} - \overline{vv'} + \overline{v}\,\overline{v'} \\ &= \frac{\sigma_v^2 + \sigma_{v'}^2}{2} - \rho\sigma_v\sigma_{v'} \\ &= \sigma_v^2(1-\rho)\end{aligned} \tag{8}$$

where ρ is the correlation between v and v'.

The differential noise is thus equal to the noise if there is no correlation between the analog output of the channels, and it is less than the noise if there is a positive correlation between the analog output of the channels. A positive correlation can be due to a common component of the noise induced by external pickup. It was therefore important for us to measure both the noise and the differential noise, and check that they were close to each other in order to make sure that the external noise pickup in our testing setup was small. However, a small residual common noise component and the limited precision of our measurements (8-bit ADC used with low gain), did not allowed us to be sensitive to smaller order phenomena contributing to the correlation between neighbor strips. However, some of these phenomena, like the "readout effect" due to the slow risetime of the analog output line (positive contribution to ρ) or the interstrip capacitance (negative contribution to ρ), could be observed and studied in the final SVX system (12-bit ADC, careful reduction of the common noise).

The differential noise was measured for all the channels using data from $N = 250$ events; the results of these measurements using both double and quadruple sample and hold programs (with a 1500 ns integration time interval), were saved to disk.

Note again that the differential noise defined above may not necessarily coincide with the intrinsic noise from the strip and its front-end electronics; we indeed observed a ladder that had a chip with a non-negligible common noise (not due to external pickup in the setup). A method to measure the intrinsic noise of a channel is given in Sect. 5.6.

5.5 Leakage Current Measurement

An attempt to measure the leakage current on each strip was done in the following way: first, several different gain and offset measurements were performed for different integration time intervals; if the measured pedestals (for a nominal value of V^{cal}) and gains for the i^{th} integration time interval, τ_i, are V_i^{out} and $G_i^{(Q)}$, then the integrated charge is given by

$$Q_i = \frac{V_i^{off}}{G_i^{(Q)}} + Q^{(0)} \tag{9}$$

where $Q^{(0)}$ is an unknown "nominal charge". If $Q^{(0)}$ is a constant, then the leakage current can be estimated as the slope of a linear fit of $V_i^{off}/G_i^{(Q)}$ versus τ_i. Of course, this measurement should be made with a double sample and hold program (note that a quadruple sample and hold method would not be adequate here because it has precisely been designed to subtract the leakage current contribution).

For this measurement we used four different integration time intervals, 1650 ns, 1950 ns, 2150 ns, and 2300 ns, and the results were saved to disk file.

The method described above is meant to measure the leakage of all strips regardless of whether they were saturating due to high current or not. During the ladder testing we never got sensible results from this procedure. This was probably because $Q^{(0)}$ was not constant for different integration times. Such an effect could be due to additional parasitic charge injection effects on the chips which are related to the signal and power distribution on the ear. Consequently the results of the leakage tests were not used for ladder quality control. Other algorithms to measure the leakage current were implemented later on, once the final SVX system was put together. In particular a simple algorithm which ignores gain variation by just comparing the offsets for two double sample integration times was used extensively during the operation of the full SVX detector to monitor nominal radiation damage and other leakage current effects.

5.6 Sparsification Threshold Measurement

The goal of the sparse threshold measurement was to determine, for each channel, the mean value and the RMS of the amount of charge needed at the input of the front-end amplifier to set the latch. The results of this fundamental measurement allowed us to decide which "operating threshold" voltage step V_{op}^{cal} should be sent on the calibration line when taking data with the SVX. The value of V_{op}^{cal} was determined to accommodate the two following requirements:

- most of the channels should latch when a minimum ionizing particle crosses the corresponding strips, i.e., the SVX should be as efficient as possible;
- most of the channels should not latch when no particle crosses the corresponding strips, i.e., the amount of data containing only noise signals should be kept at a reasonable level.

Once the value of V_{op}^{cal} is known, the results of the sparsification threshold measurements can be used to predict the efficiency of each individual channel. In particular, a list of "dead" channels (channels that never latch) and "noisy" channels (channels that always latch) can be established.

The RMS of the injected charge needed to latch a particular channel is a measure of the noise of that channel. This measurement does not use the analog information sent by the SVX chip, and is an independent measurement of the noise of each channel, which, contrary to the noise measurement obtained from the analog data, will not be affected by any eventual contribution of the testing setup (port card, cables, receiver and ADC). If the noise is 2200 electrons, we expect the RMS of the sparsification threshold to lie around 0.35 fC, corresponding approximately to a difference of 6 mV in terms of the V^{cal} voltage.

The sparsification threshold measurement consists here of measuring a finite number of points on the "efficiency curve" of each channel (which is nothing else but the integral of the pedestal distribution, assumed here to be a gaussian distribution); in other words, the

probability to latch is measured for various values of the injected charge. To perform these measurements, the calibration voltage pulse is stepped through N different values, equally spaced between a value V_{low}^{cal}, where (almost) all the channels don't latch, and a value V_{high}^{cal}, where (almost) all the channels do latch. At each step i, the calibration voltage pulse is set to

$$V_i^{cal} = V_{low}^{cal} + (i - \frac{1}{2})\Delta V^{cal} \qquad i = 1, \ldots, N \tag{10}$$

where

$$\Delta V^{cal} = \frac{V_{high}^{cal} - V_{low}^{cal}}{N} \, . \tag{11}$$

A data acquisition program performing a quadruple sample and hold and enabling the "positive sparse" logic is run in the SRS, and a number N_{evts} of events are read out during a given step i; for each channel, the probability to latch, ε_i, is estimated as

$$\varepsilon_i = \frac{N_{latch}}{N_{evts}} \tag{12}$$

where N_{latch} is the number of times the address of that channel is present in the data collected on the digital lines during the current step (note that the analog data is not used).

At the end, the sparsification threshold, V_{thresh}^{cal}, and its RMS value, σ_{thresh}, are estimated using the following formulae:

$$V_{thresh}^{cal} = V_{low}^{cal} + \Delta V^{cal} \sum_{i=1}^{N} (1 - \varepsilon_i) \tag{13}$$

$$\sigma_{thresh} = \Delta V^{cal} \sqrt{\sum_{i=1}^{N} (2i - 1)(1 - \varepsilon_i) - \left(\sum_{i=1}^{N} (1 - \varepsilon_i) \right)^2} \tag{14}$$

The justification of these formulae, as well as a discussion of their validity, can be found in the Appendix.

The error on the estimate of the sparsification threshold V_{thresh}^{cal} is determined by the values chosen for ΔV^{cal} and N_{evts}. This error, δV_{thresh}^{cal}, has two independent sources whose contributions can be added in quadrature; the first contribution comes from the statistical uncertainty on the estimates ε_i and the second one is due to fact that the right hand side of Eq. (13) is only an approximation to the true value of the threshold. As shown in the Appendix, the standard error on V_{thresh}^{cal} can therefore be expressed as

$$\delta V_{thresh}^{cal} = \sigma_{thresh} \sqrt{\frac{r}{N_{evts}\sqrt{\pi}} + \mu^2(r)} \, , \tag{15}$$

where

$$r = \frac{\Delta V^{cal}}{\sigma_{thresh}} \, . \tag{16}$$

The function $\mu(r)$ is given in Figure 35 of the Appendix; it takes positive values less than 0.004 if r is less than 2.

When doing these measurements on the production ladders, the primary purpose was to detect failures and tag channels whose behavior during sparsification deviated from the average baseline. Therefore we needed to scan a rather big window to make sure that all (or at least most of) the channels of a given ladder be caught. A quick measurement was first

done with $N_{evts} = 8$, $N = 8$, $V_{low}^{cal} = -95.6\ mV$, and $V_{high}^{cal} = 91.8\ mV$, corresponding to $\Delta V^{cal} = 23.4\ mV$ (these odd values came about due to the calibration constants of various elements of the pulsing system). Then, a second more precise measurement was done with $N_{evts} = 50$, $N = 15$, and new values of V_{low}^{cal} and V_{high}^{cal} determined from the results of the first measurement; the algorithm used to determine this new window was designed to shrink the initial 187 mV window, if this was possible without loosing a significant number of channels. In most of the cases, we ended up with a window approximately equal to 112 mV centered around 7.5 mV, corresponding to a typical step $\Delta V^{cal} = 7.5\ mV$, that could allow meaningful estimates of V_{thresh}^{cal} and σ_{thresh} for about 97% of the channels (in the worst case, the window remained the same and the step ΔV^{cal} for the final measurement was thus never above 12.5 mV). Since σ_{thresh} was expected to be approximately equal to 6 mV, our measurements were made in a condition where $\mu(r)$ can be neglected; using Eq. (15), we estimate that the error

$$\delta V_{thresh}^{cal} = \pi^{-1/4} \sqrt{\frac{\sigma_{thresh} \Delta V^{cal}}{N_{evts}}} \tag{17}$$

is never above 1 mV for each channel satisfying $\varepsilon_1 = 0$ and $\varepsilon_N = 1$.

As a typical example, let us consider the measurement of the threshold for channel 219 of ladder 106–4B032. For this ladder, the window used when $N = 15$ was $V_{low}^{cal} = -38.5\ mV$ and $V_{high}^{cal} = 61.8\ mV$, corresponding to $\Delta V^{cal} = 6.7\ mV$, and using Eqs. (13), (14), and (17) we obtained $V_{thresh}^{cal} = 10.4\ mV$, $\sigma_{thresh} = 6.2\ mV$, and $\delta V_{thresh}^{cal} = 0.7\ mV$. Figure 14 summarizes this measurement: the circles are the measured efficiencies for the various values of the injected charge, and the curve is the integral of a gaussian distribution whose mean value is $C^{cal} V_{thresh}^{cal}$ and RMS width is $C^{cal} \sigma_{thresh}$ (the arrow in the center crosses the curve at this mean value and has a length of twice this RMS width).

6 Results of Testing

6.1 Examples of Results

The results of the ladder production testing consisted of a very large amount of data, which cannot be listed here in any detail. Thus, the complete sets of results is shown in this document only for some typical ladders. Figures 15 to 17 show the results of the measurements done on a typical layer 3 ladder after burnin. Figures 18 to 20 show the results of the measurements done on a layer 4 ladder where two "black holes" are visible; measurements done one the same ladder after it had been fixed are shown in Figures 21 to 23.

6.2 Quality of Channels

The results of the testing of each ladder were analyzed to get a list of "bad" channels. This list was useful for example to determine which particular channels were inducing "black holes" in the ladder and needed to be fixed (see Section 7 for a discussion about this fixing process). The "bad" channels were defined as channels that belong to one or more of the three following categories:

- Dead channels: channels with a gain (measured in quadruple sample and hold mode) that was less than 5 mV/fC in absolute value, or channels that had their 50% effi-

ciency threshold above the average by more than the averaged RMS of the sparsification threshold.

- Noisy channels: channels that had a probability to latch higher than 10% when the injected charge is equal to the average 50% efficiency threshold minus 3 times the averaged RMS of the sparsification threshold.
- Exceptional channels: channels that had at least one of the measured characteristics that deviated significantly from its expected value; more precisely, "exceptional" channels were those for which at least one of the following conditions were met:
  - the gain (in double or quadruple sample and hold mode) was less than 5 mV/fC in absolute value;
  - the offset in quadruple sample and hold mode deviated from the average by more than 4 σ;
  - the differential noise in double sample and hold mode was more than 3000 or less than 900 electrons;
  - the differential noise in quadruple sample and hold mode was more than 3500 or less than 1200 electrons;
  - the 50% efficiency threshold deviated from the average by more than 3.5 σ;
  - the RMS of the sparsification threshold was more than 0.7 fC or less than 0.2 fC;
  - the measured leakage current was more than 160 nA or less than -40 nA.

In the above definitions all the averaged values refer to "iterated averages" that were computed in the following way: first, the mean value and standard deviation were computed on the values of all the channels in the ladder; then, channels that had a value which was more than 3 standard deviations away from the mean were ignored, and the mean value and standard deviation were recomputed on the values of the remaining channels in the ladder; this procedure was iterated until the mean value didn't change anymore (but a maximum of 20 times); the "iterated average" is this final mean value, which was an average where the tails of the distribution had been ignored.

Note that dead and noisy channels are defined here in a rather arbitrary way, in the sense that they may not coincide exactly with what will appear to be real dead or noisy channels in the final SVX detector. In fact once installed in CDF the operation of the SVX detector was optimized in such a way that the number of dead or noisy channels was reduced further. The definition of exceptional channels is rather loose; as a consequence, an exceptional channel that does not meet the dead or noisy channel criteria should in principle be perfectly usable in the final SVX detector. However, the number of channels per ladder in each of these categories provided a convenient way of surveying the quality of the ladder production.

6.3 Summary of the Results

Figures 24 to 29 show result summaries, computed from the measurements taken on the production ladders after burn–in (and eventual black hole fixing). On Figures 24 to 28a, the iterated average of the various measured quantities are plotted as function of the ladder number (IB4 production number). Ideally, all the points on these plots should lie on a flat line, indicating that all the ladders have identical properties. In the real case, the observed

variations from ladder to ladder remain acceptably small (as seen in Figure 24b, 5 layer 3 ladders have a double sample and hold offset higher than 2.4 V, but this effect was due to the use of a different port card in the test of these ladders).

The variations in the 50% efficiency threshold, shown in Figure 27a, need particular attention. In the final SVX system, there are two separate calibration voltages per wedge; the first one is used to inject charge in the layer 1 ladder, and the second one is common to the ladders in layers 2, 3, and 4. It is thus very important that the layer 2, 3, and 4 ladders in a given wedge have the same 50% efficiency threshold; if it is not the case, then a whole ladder may appear as noisy or inefficient. Although the variations shown in Figure 27a are often bigger than 1 fC, it is possible to form wedges of ladders that have an acceptable match in threshold. Also, we believe that these variations are due in part by an inexact leakage current cancellation in the quadruple sample and hold mode, because we indeed observed a correlation between the 50% efficiency threshold and the offset (in double sample and hold mode). The threshold differences indeed got smaller once the two integration times were finely tuned to get the best possible leakage current cancellation (this adjustment was not possible with the SRS module, but was done with the Fastbus Sequencer module used in the final SVX data acquisition system).

Figures 28b, 29a, and 29b, show the percentage of exceptional, dead or noisy channels (using the definitions of Sect. 6.2.) as function of the ladder number. Most of the ladders have less than 2% dead channels and less than 5% noisy channels.

7 Black Holes

In the course of prototyping and constructing ladder modules for the SVX we observed that strips with a sufficiently large leakage current would share that current with neighboring strips in proportion to the distance between them. Because of the characteristic pattern of this sharing we called these areas "black holes".

The black holes are caused by the phenomenon of punch–through in a p^+np^+ structure [7] but only occur here because of the way the SVX chip behaves when it becomes saturated. In the classical punch-through configuration one p^+n junction is forward biased while the other is reverse bias. For a certain voltage across the structure, the depletion region of the reverse biased junction extends all the way to the forward biased junction. At that point a large current can flow. This situation is indicated in Figure 30 which is borrowed from the reference. The situation between adjacent strips in a silicon detector is similar and has been discussed in the literature [8].

For an integrated charge of about 60 fC the SVX integrator will saturate. The normal reset point of the integrator is 1.1 V. Once it saturates the input can charge up to 6 V plus a diode drop. At that point protection diodes, which connect the inputs to the AP=6 V line will turn on and the input will be fixed at that level. Under this condition, with the neighbors all at 1.1 V, punch-through can apparently occur (see Figure 31). Depending upon the magnitude of the current injected, the neighbors may even saturate as well. This will create a cascade like effect which may affect finally a large number of strips. An example of this is shown in Figure 18a, a double sample offset plot which is directly proportional to the strip leakage current.

We found that the black hole effect required a strip leakage in excess of a few hundred nA for our typical integration times. We also observed that leaving a known leaky strip unbonded prevented in most cases the black hole from appearing at that location. Since

the integrator saturated anyway at about 60 fC we chose to leave all strips with current in excess of 70 nA unbonded.

Occasionally, in the case of a very leaky strip, a black hole was observed centered on that strip, although it was skipped during wirebonding. This kind of black hole could be fixed by connecting the bad strip to ground, in such a way that the excess current would be drained without having to spread to the neighbor strips. The strip itself remained bad of course, but the good neighbor strips were recovered. Practically, the fix consisted of wirebonding the faulty strip to the dummy ear or to the guard ring itself.

During the wirebonding process another class of high leakage strips appeared. These were due to damage to the detector in the bonding process. In particular, when the bonding tool hit the silicon dioxide the effect was particularly pronounced. Interestingly subsequent removal of the bond wire at that strip did usually not remove the black hole. Instead the seed strip just moved to the next bonded strip.

These patterns can be understood by the following hypothesis (see Figure 32). Those strips which were delivered with high leakage probably contained a defect induced during ion implantation of the p^+ strips. This defect is perhaps a micron below the surface. Consequently, if the strip is unbonded the defect may remain in a relatively low field region and not contribute carriers to the neighbors. Those strips which have instead surface damage due to bonding may contribute a large surface current which persists even if the nearest strip is floating as long as the surface is depleted. That current will just sink to the nearest bonded strip.

In the case of the persistent black holes we found that the current could be satisfactorily drained if the strip was connected via a low impedance to voltage level near the nominal 1.1 V reset point of the integrator. This worked as long as the impedance was smaller than the apparent impedance into the saturated preamplifier. Thus it would not do to use a voltage divider consisting of 1 $k\Omega$ resistors. It was latter seen [9] that the same apparent draining effect came about if the offending strip was instead grounded through a capacitor of value in excess of 0.1 μF. This was the final procedure used in production for these strips. The effect of this bonding can be seen by comparing Figures 21 to 23 (after 2 black hole bonds) with Figures 18 to 20 (before black hole fixing). Generally, the two neighboring strips around a black hole would show increased noise after black hole fixing using this procedure.

The effect of the capacitor can be understood in the following way. During operation the charge integrator is repeatedly reset and activated. Consequently the large current only turns on the protection diodes periodically. The input is thus switching between 1.1 and 6.7 V at a typical frequency of 300 kHz. At this frequency the capacitor is a small enough impedance to shunt the excess current to ground.

Use of the capacitor to fix black hole is superior to an external voltage source because it is simpler and introduces no extra noise to the ladder. In practice we mounted 0.1 μF type 0805 surface mount ceramic capacitors to the dummy ear and wirebonded bad strips to the gold stripe on the dummy ear.

All black hole fixes were performed at LBL using a manual bonding machine. The strips that needed black hole fixing were identified during the testing procedures and their rate is listed in Table 5.

	Layer 1	Layer 2	Layer 3	Layer 4
Number of strips in bonded ladders	8192	11136	15872	23040
... unbonded (skipped or unbondable)	13	35	75	125
... partially bonded (1/3 or 2/3)		4	4	3
Number of fully bonded strips	8179	11097	15793	22912
.... disconnected to fix BH	2	2	15	1
... bonded to dummy end (capacitor) to fix BH	2	5		37
Number of strips skipped ($I_{leak}^{strip} > 70\ nA$)	13	35	59	111
... bonded to guard ring (ground) to fix BH			3	1
... bonded to dummy end (ground) to fix BH			1	3

Table 5: Bonded, skipped, and black hole (BH) fixed strips

8 Conclusion

The ladder modules of the CDF silicon vertex detector (SVX) have been successfully assembled and tested. The yield was high enough to provide enough modules for all 4 layers of the SVX plus some spares.

In order to monitor the ladder production, procedures have been developed and check the quality of the channels. Bad channels responsible for black hole effects were identified; an appropriate treatment of these black holes has been developed and applied in order to recover the good strips in the black hole neighborhood that otherwise would have been unusable.

Different quantities were measured to characterize each channel; these measurements were saved for later comparison with measurements taken during the final barrel assembly and with the first calibration data taken during the commissioning of the whole SVX system.

Acknowledgement: We naturally acknowledge the hard and careful work of all our collaborators in the CDF SVX group. In addition, there is a long list of individuals and institutions who provided support and cooperation throughout this project. We thank and acknowledge the following: the staff at Promex Inc. over a number of years, in particular Ms. Phansu Phong who performed all the wirebonding; the LBL Engineering Division, in particular Kaz Shimada for doing the many circuit layouts; the LBL Physics Division; and Mr. Bill Fujitsubo of Engineering Solutions Inc.

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Appendix

Estimation of the 50%-point and Width of an Efficiency Curve

An efficiency curve can always be described by a function $\varepsilon(x)$, the efficiency, that rises monotonically from 0 to 1 as some variable x varies from its minimum to its maximum value (or from $-\infty$ to $+\infty$). Here we consider the case where such an efficiency function is known at a finite number N of values of x, equally spaced between a value x_{low} such that $\varepsilon(x_{low}) = 0$ and a value x_{high} such that $\varepsilon(x_{high}) = 1$. More precisely, having defined a step

$$\Delta x = \frac{x_{high} - x_{low}}{N} \tag{18}$$

and the following values of x,

$$\begin{cases} x_0 = x_{low} \\ x_i = x_{i-1} + \Delta x \qquad \text{for } i = 1, ..., N \ , \end{cases} \tag{19}$$

we assume that the N efficiency values

$$\varepsilon_i = \varepsilon(x_i - \frac{\Delta x}{2}) \qquad \text{for } i = 1, ..., N \tag{20}$$

are known exactly, and that

$$\begin{cases} \varepsilon_1 = 0 \\ \varepsilon_N = 1 \ , \end{cases} \tag{21}$$

as shown on Figure 33.

The purpose of this appendix is to derive, from these N points $(x_i - \Delta x/2, \varepsilon_i)$ on the efficiency curve, expressions giving estimates for the 50% efficiency point and for some quantity describing the sharpness of the transition from 0 to 1.

The function $\varepsilon(x)$ is in fact the integral of an underlying probability density function $g(x)$ such that

$$\varepsilon(x) = \int_{-\infty}^{x} g(x')\, dx' \ . \tag{22}$$

Let m be the expectation value and σ^2 the variance of this distribution $g(x)$.

It is easy to show that

$$\varepsilon(m) = 50\% \tag{23}$$

if the function $g(x)$ is symmetric around m, i.e., if

$$g(m + x) = g(m - x) \qquad \text{for any value of } x \ . \tag{24}$$

We have indeed

$$\begin{aligned} 1 &= \int_{-\infty}^{+\infty} g(x)dx = \int_{-\infty}^{+\infty} g(m + x)dx \\ &= \int_{-\infty}^{0} g(m + x)dx + \int_{0}^{+\infty} g(m + x)dx \\ &= \int_{-\infty}^{0} g(m + x)dx + \int_{-\infty}^{0} g(m - x)dx \\ &= 2\int_{-\infty}^{0} g(m + x)dx = 2\int_{-\infty}^{m} g(x)dx = 2\ \varepsilon(m) \ . \end{aligned} \tag{25}$$

Thus, if we assume the symmetry of $g(x)$ (and this is what we will do here), the problem is reduced to find estimates for the mean value m and the variance σ^2. As can be seen below, the general idea will be to estimate the integrals defining these quantities by sums over the known values ε_i.

The mean value can be expressed as

$$m = \overline{x} = \int_{-\infty}^{+\infty} x\ g(x)\ dx = \int_{-\infty}^{+\infty} x\ \frac{d\varepsilon(x)}{dx}\ dx = \int_0^1 x(\varepsilon)\ d\varepsilon \tag{26}$$

and estimated as

$$\begin{aligned}
\widehat{m} &= \sum_{i=1}^{N-1} x_i(\Delta\varepsilon)_i = \sum_{i=1}^{N-1} x_i(\varepsilon_{i+1} - \varepsilon_i) = \sum_{i=2}^{N} x_{i-1}\varepsilon_i - \sum_{i=1}^{N-1} x_i\varepsilon_i \\
&= \sum_{i=2}^{N-1}(x_{i-1} - x_i)\varepsilon_i + x_{N-1}\varepsilon_N - x_1\varepsilon_1 = x_{N-1} - \Delta x \sum_{i=2}^{N-1} \varepsilon_i \\
&= x_{N-1} - \Delta x \sum_{i=1}^{N} \varepsilon_i + \Delta x = x_{high} - \Delta x \sum_{i=1}^{N} \varepsilon_i \\
&= x_{low} + \Delta x \sum_{i=1}^{N}(1 - \varepsilon_i)\ .
\end{aligned} \tag{27}$$

The variance σ^2 can be expressed as

$$\sigma^2 = \overline{x^2} - \overline{x}^2 = \overline{x^2} - m^2 \tag{28}$$

where

$$\overline{x^2} = \int_{-\infty}^{+\infty} x^2\ g(x)\ dx = \int_{-\infty}^{+\infty} x^2\ \frac{d\varepsilon(x)}{dx}\ dx = \int_0^1 x^2(\varepsilon)\ d\varepsilon\ . \tag{29}$$

This expectation value of x^2 can be estimated as a sum; we have

$$\begin{aligned}
\widehat{\overline{x^2}} &= \sum_{i=1}^{N-1} x_i^2(\Delta\varepsilon)_i = \sum_{i=1}^{N-1} x_i^2(\varepsilon_{i+1} - \varepsilon_i) = \sum_{i=2}^{N} x_{i-1}^2\varepsilon_i - \sum_{i=1}^{N-1} x_i^2\varepsilon_i \\
&= \sum_{i=2}^{N-1}(x_{i-1}^2 - x_i^2)\varepsilon_i + x_{N-1}^2\varepsilon_N - x_1^2\varepsilon_1 = x_N^2 + \sum_{i=1}^{N}(x_{i-1}^2 - x_i^2)\varepsilon_i \\
&= x_N^2 + (\Delta x)^2 \sum_{i=1}^{N}\left(1 - \frac{2x_i}{\Delta x}\right)\varepsilon_i = x_N^2 + (\Delta x)^2 \sum_{i=1}^{N}\left(1 - 2i - \frac{2x_0}{\Delta x}\right)\varepsilon_i \\
&= x_N^2 + (\Delta x)^2 \left[\sum_{i=1}^{N}\left(2i - 1 + \frac{2x_0}{\Delta x}\right)(1 - \varepsilon_i) - N\left((N+1) - 1 + \frac{2x_0}{\Delta x}\right)\right] \\
&= (x_0 + N\Delta x)^2 + (\Delta x)^2 \sum_{i=1}^{N}\left(2i - 1 + \frac{2x_0}{\Delta x}\right)(1 - \varepsilon_i) - (N\Delta x)^2 - 2x_0 N\Delta x \\
&= x_{low}^2 + (\Delta x)^2 \sum_{i=1}^{N}(2i-1)(1 - \varepsilon_i) + 2x_{low}\Delta x \sum_{i=1}^{N}(1 - \varepsilon_i)\ .
\end{aligned} \tag{30}$$

An estimate for the variance can then be defined as

$$\begin{aligned}
\widehat{\sigma^2} &= \widehat{\overline{x^2}} - \widehat{m}^2 \\
&= (\Delta x)^2 \left[\sum_{i=1}^{N}(2i-1)(1 - \varepsilon_i) - \left(\sum_{i=1}^{N}(1 - \varepsilon_i)\right)^2\right]\ .
\end{aligned} \tag{31}$$

Note that the quantities $\widehat{m}$ and $\widehat{\sigma^2}$ given by Eqs. (27) and (31) do not depend directly on the number of points N; it is indeed easy to check that changing the number of points (without affecting the step Δx) has no effect on $\widehat{m}$ and $\widehat{\sigma^2}$ as long as the hypotheses of Eqs. (21) remain in effect. The errors on these estimates are essentially determined by the step Δx, and the consistency of these estimates, which is guaranteed only if the conditions of Eqs. (21) are satisfied, is expressed by

$$\begin{cases} \lim\limits_{\Delta x \to 0} \widehat{m} = m \\ \lim\limits_{\Delta x \to 0} \widehat{\sigma^2} = \sigma^2 \ . \end{cases} \tag{32}$$

The quantity $(\widehat{m} - m)/\Delta x$ depends on two variables, r and α, which we define as

$$r = \frac{\Delta x}{\sigma} \quad > 0 \ , \tag{33}$$

$$\alpha = \left(\frac{m - x_{low}}{\Delta x} - \frac{1}{2} \right) \bmod 1 \quad , 0 \leq \alpha < 1 \ . \tag{34}$$

Because of the symmetry of the function $g(x)$, we have $\widehat{m} = m$ when $\alpha = 0$ (case where one of the values ε_i is equal to 50%) or when $\alpha = 0.5$ (case where one of the values x_i is equal to m), independently of the value of r. Figure 34 shows, for different values of r, how the quantity $(\widehat{m} - m)/\Delta x$ varies with α in the particular case where $g(x)$ is a gaussian distribution. One could easily show that, in any case (even if $g(x)$ was not gaussian), the absolute value of the difference between the estimate $\widehat{m}$ and the true value m does never exceed $\Delta x/2$.

Let us define $\delta\widehat{m}$ as the "standard error" on the estimate $\widehat{m}$, i.e, as the positive quantity that verifies

$$\text{prob}(m - \delta\widehat{m} \leq \widehat{m} \leq m + \delta\widehat{m}) = 68\% \ . \tag{35}$$

Given a step Δx, the error $\delta\widehat{m}$ on $\widehat{m}$ can be evaluated if one knows the shape of the function $g(x)$ as well as the shape of the probability distribution of the variable α; if the value x_{low} is chosen without any knowledge on the mean value m, then one can reasonably assume the quantity α to be uniformly distributed between 0 and 1. Figure 35 shows the quantity

$$\mu(r) = \frac{\delta\widehat{m}}{\sigma} \tag{36}$$

as a function of r in the particular case where $g(x)$ is a gaussian distribution. It is interesting to note that the precision on the estimate $\widehat{m}$ is better than 0.4% of the width of the gaussian if the step Δx is smaller than twice that width.

Let us now consider the more complicated case were the probabilities ε_i are not known exactly, but are estimated as

$$\widehat{\varepsilon_i} = \frac{\nu_i}{n} \tag{37}$$

where ν_i is the number of successes obtained during n independent tests, where the probability to obtain a success at each test is equal to ε_i. The quantity ν_i is nothing else than a binomial variable whose variance is $n\varepsilon_i(1 - \varepsilon_i)$; therefore, the error on the estimate $\widehat{\varepsilon_i}$ is given by

$$\delta\widehat{\varepsilon_i} = \sqrt{\frac{\varepsilon_i(1 - \varepsilon_i)}{n}} \tag{38}$$

We are now able to define new estimates of m and σ^2 as

$$\widehat{\widehat{m}} = x_{low} + \Delta x \sum_{i=1}^{N} (1 - \widehat{\varepsilon_i}) \,, \tag{39}$$

$$\widehat{\widehat{\sigma^2}} = (\Delta x)^2 \left[\sum_{i=1}^{N} (2i-1)(1-\widehat{\varepsilon_i}) - \left(\sum_{i=1}^{N} (1-\widehat{\varepsilon_i}) \right)^2 \right] . \tag{40}$$

The error $\delta\widehat{\widehat{m}}$ on the estimate $\widehat{\widehat{m}}$ is a quadratic combination of the error $\delta\widehat{m}$ defined above with N others terms coming from the propagation of the independent errors $\delta\widehat{\varepsilon_i}$ in Eq. (39); we have

$$\begin{aligned} \left(\delta\widehat{\widehat{m}}\right)^2 &= (\delta\widehat{m})^2 + \sum_{i=1}^{N} (\Delta x \; \delta\widehat{\varepsilon_i})^2 \\ &= (\sigma\mu(r))^2 + \frac{\Delta x}{n} \sum_{i=1}^{N} \varepsilon_i (1-\varepsilon_i) \Delta x \\ &\cong \sigma^2\mu^2(r) + \frac{r\sigma}{n} \int_{-\infty}^{+\infty} \varepsilon(x)(1-\varepsilon(x)) \; dx \,. \end{aligned} \tag{41}$$

In the particular case where the function $g(x)$ is a gaussian, the integral appearing in the above equation can be computed by analytic means,

$$\int_{-\infty}^{+\infty} \varepsilon(x)(1-\varepsilon(x)) \; dx = \frac{\sigma}{\sqrt{\pi}} \,, \tag{42}$$

leading finally to

$$\delta\widehat{\widehat{m}} = \sigma \sqrt{\frac{r}{n\sqrt{\pi}} + \mu^2(r)} \,. \tag{43}$$

Practically, this error can be estimated as

$$\widehat{\delta\widehat{\widehat{m}}} = \widehat{\sigma} \sqrt{\frac{\widehat{r}}{n\sqrt{\pi}} + \mu^2(\widehat{r})} \,, \tag{44}$$

where

$$\widehat{\sigma} = \sqrt{\widehat{\widehat{\sigma^2}}} \,, \tag{45}$$

$$\widehat{r} = \frac{\Delta x}{\widehat{\sigma}} \,. \tag{46}$$

List of Figures

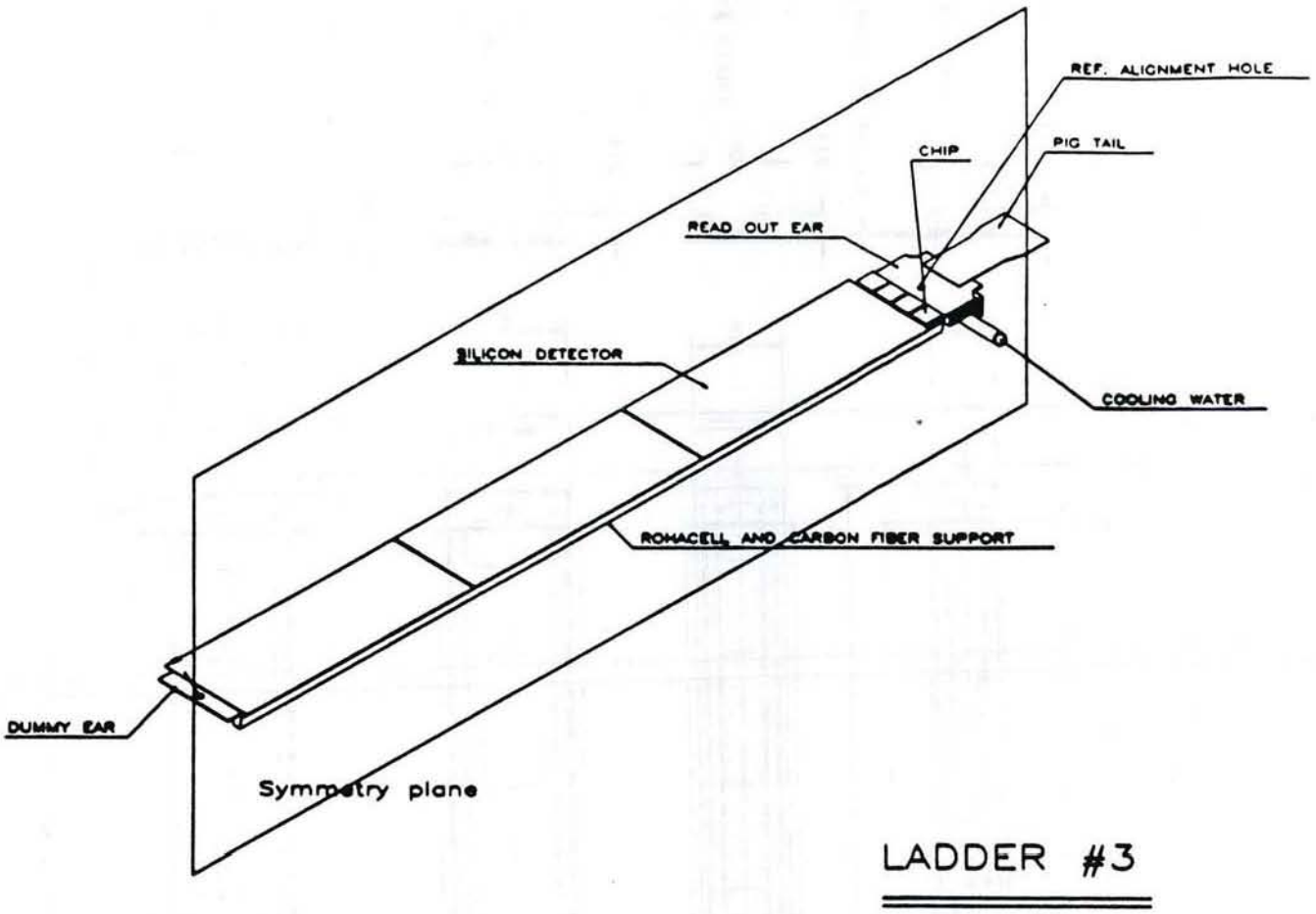

REF. ALIGNMENT HOLE
CHIP
PIG TAIL
READ OUT EAR
SILICON DETECTOR
COOLING WATER
ROHACELL AND CARBON FIBER SUPPORT
DUMMY EAR
Symmetry plane
LADDER #3

Figure 1a

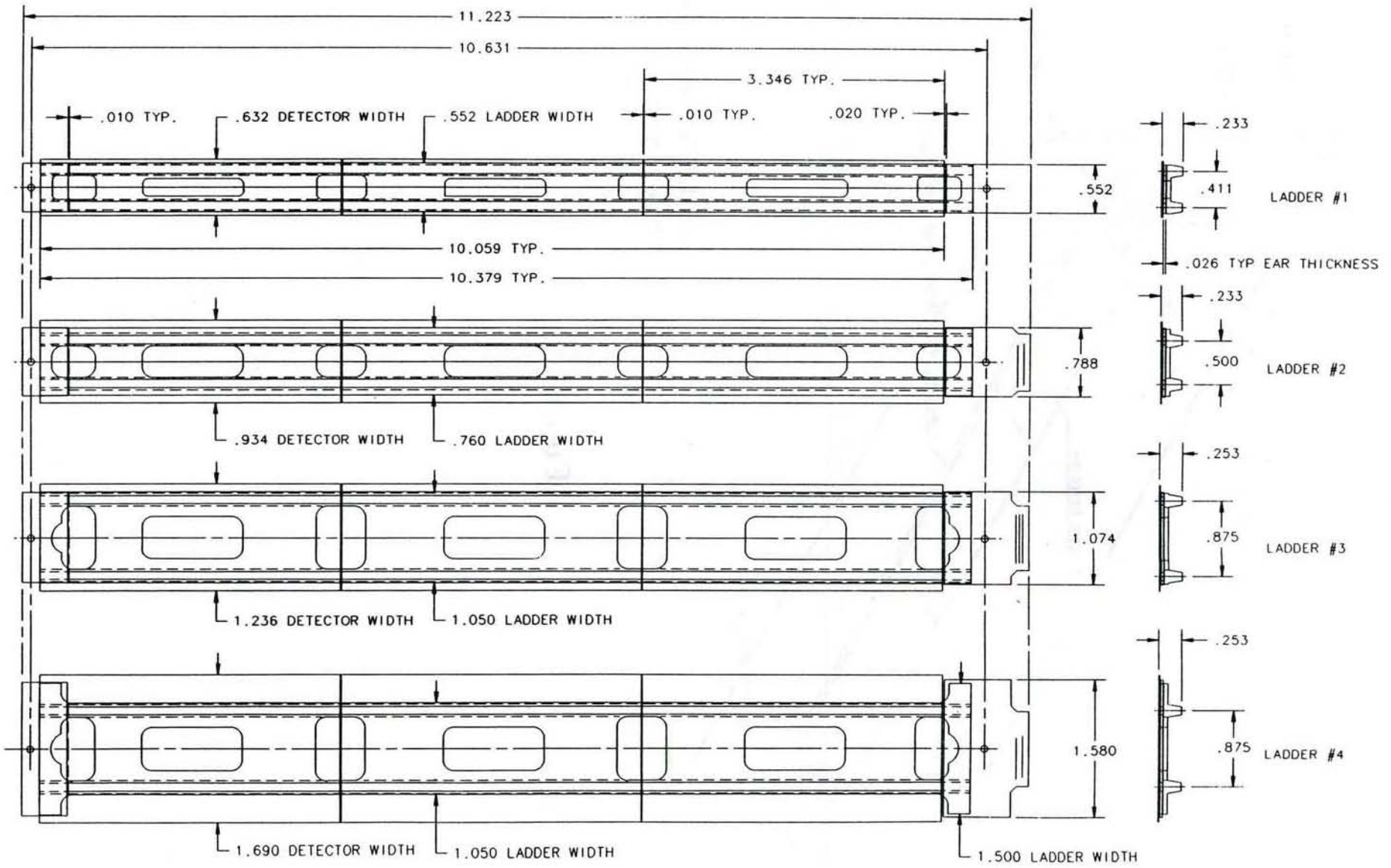
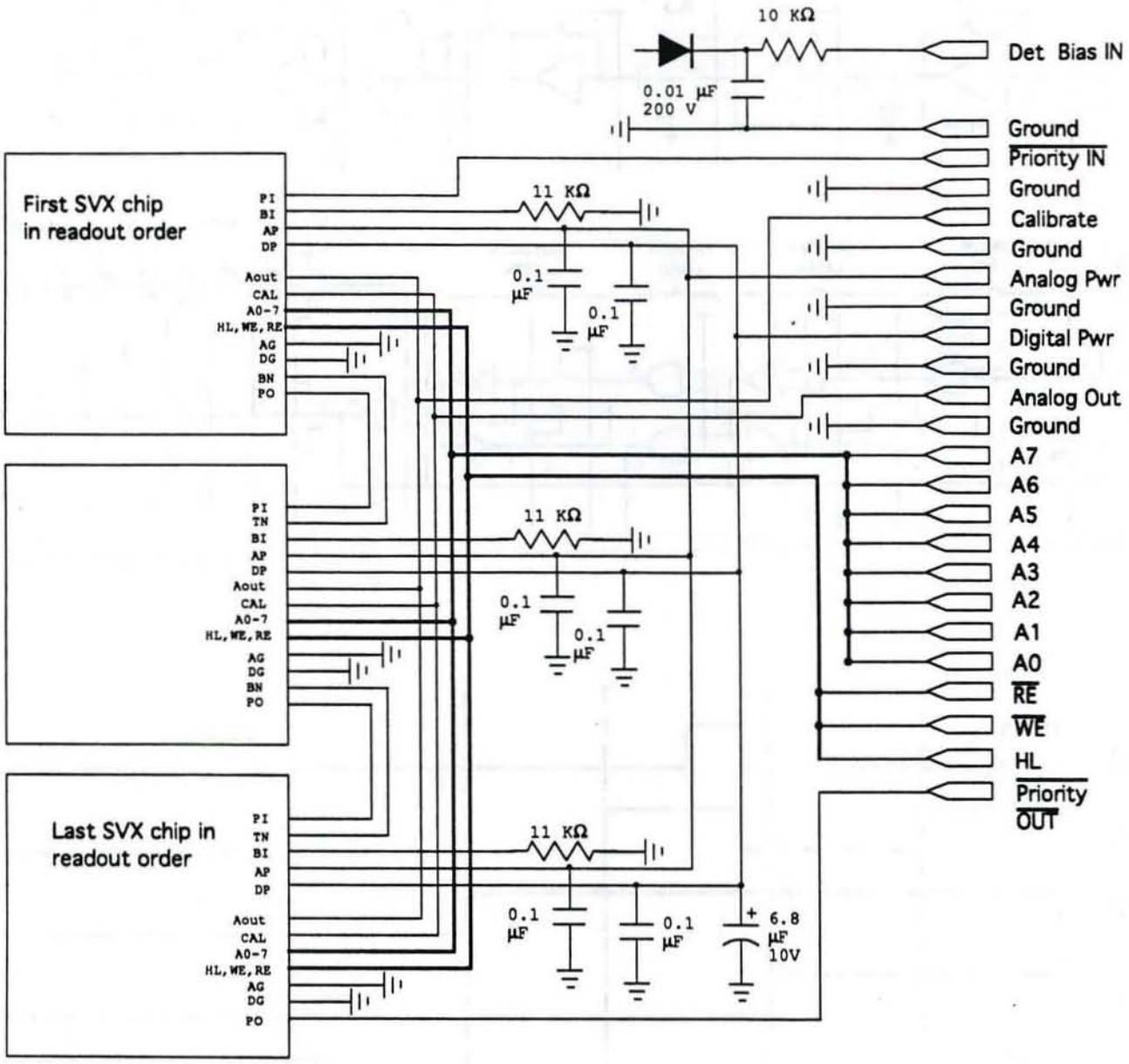

11.223
10.631
3.346 TYP.
.010 TYP.
.632 DETECTOR WIDTH
.552 LADDER WIDTH
.010 TYP.
.020 TYP.
.552
.233
.411
LADDER #1
.026 TYP EAR THICKNESS
10.059 TYP.
10.379 TYP.
.233
.788
.500
LADDER #2
.934 DETECTOR WIDTH
.760 LADDER WIDTH
.253
1.074
.875
LADDER #3
1.236 DETECTOR WIDTH
1.050 LADDER WIDTH
.253
1.580
.875
LADDER #4
1.690 DETECTOR WIDTH
1.050 LADDER WIDTH
1.500 LADDER WIDTH

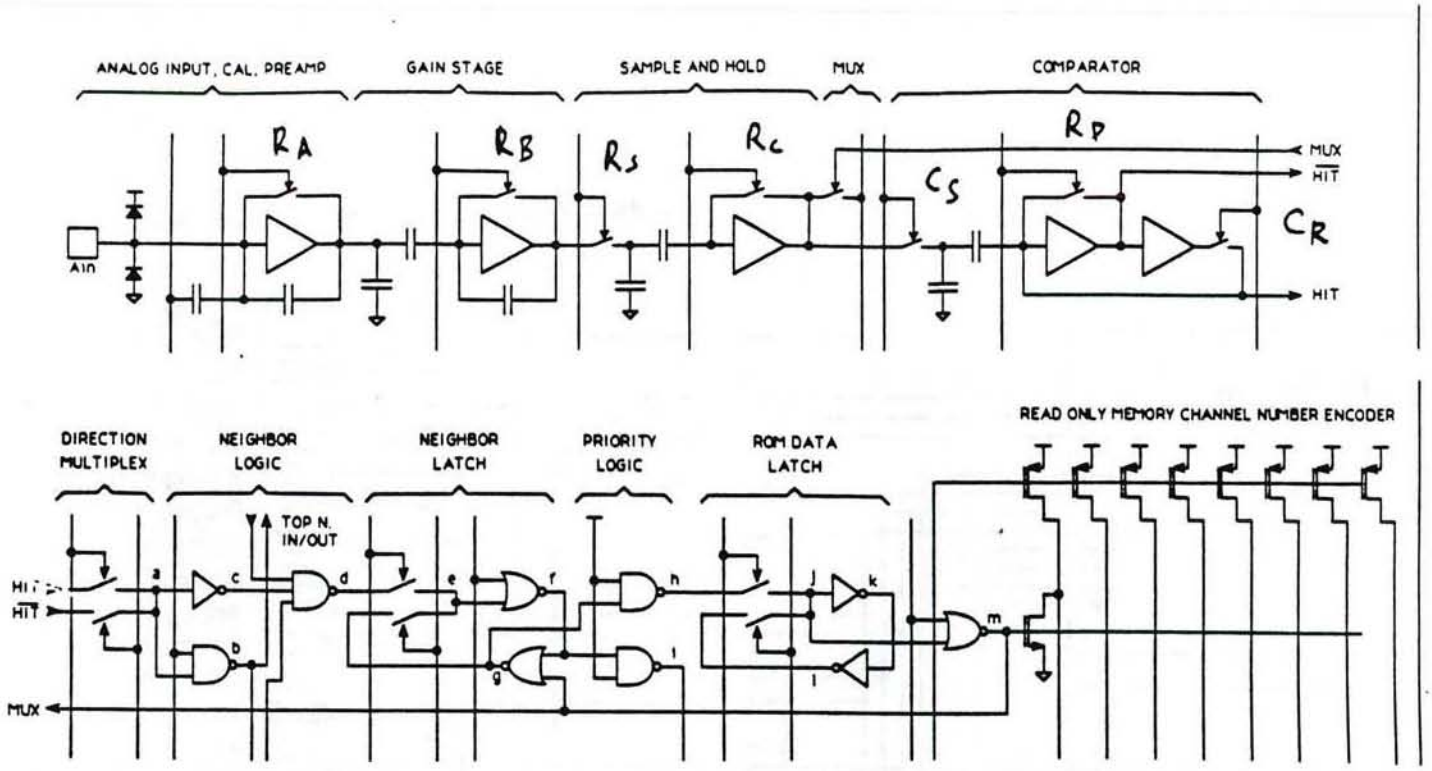
Figure 1b

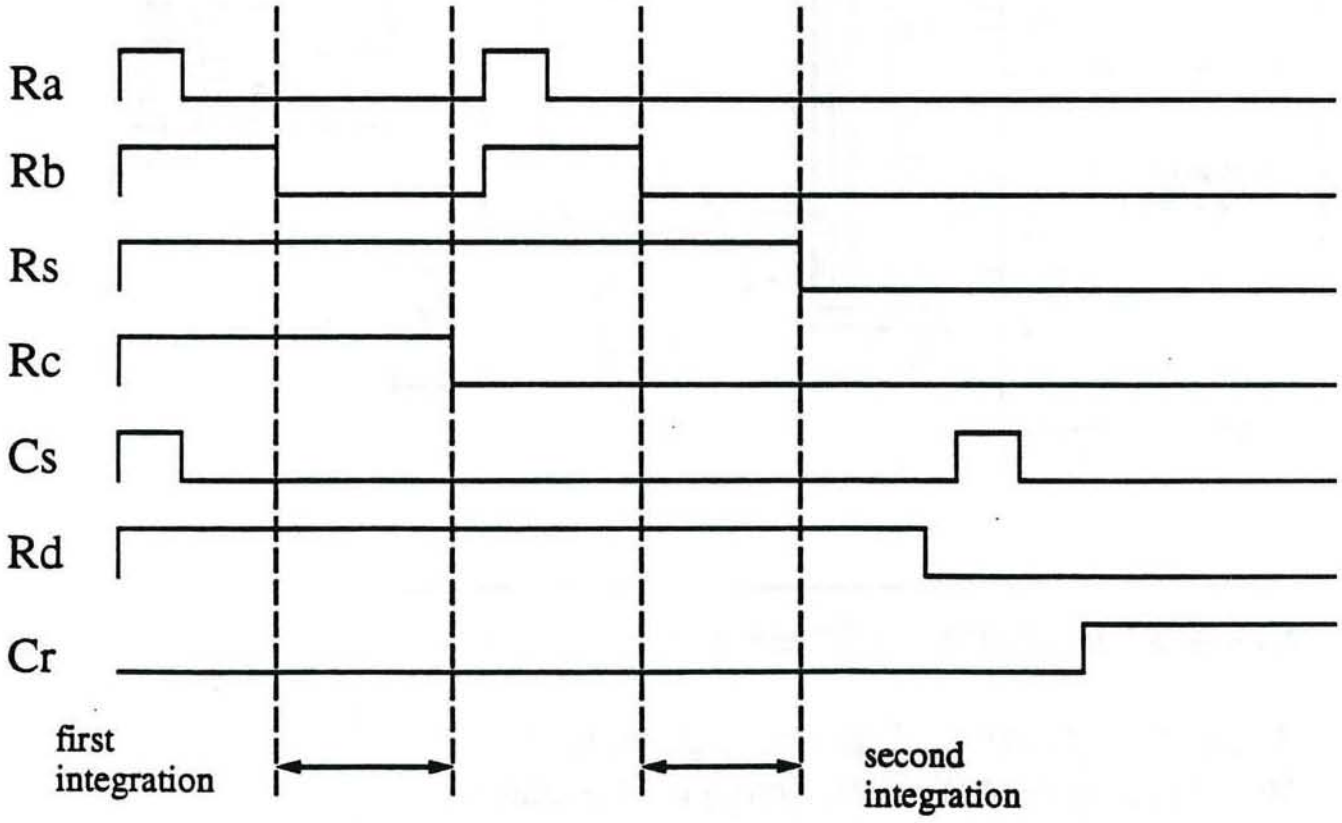


SVX Readout Hybrid "EAR" electrical schematic

3 chip configuration. This circuit generalizes to n chips by repeating the wiring of the middle chip.

Figure 2





Leakage current subtraction will have minimum error when time difference between two integrations equals risetime difference of sample and hold circuit for the two states of Rc (reset switch of Comp 2 (stage C)).

Figure 3

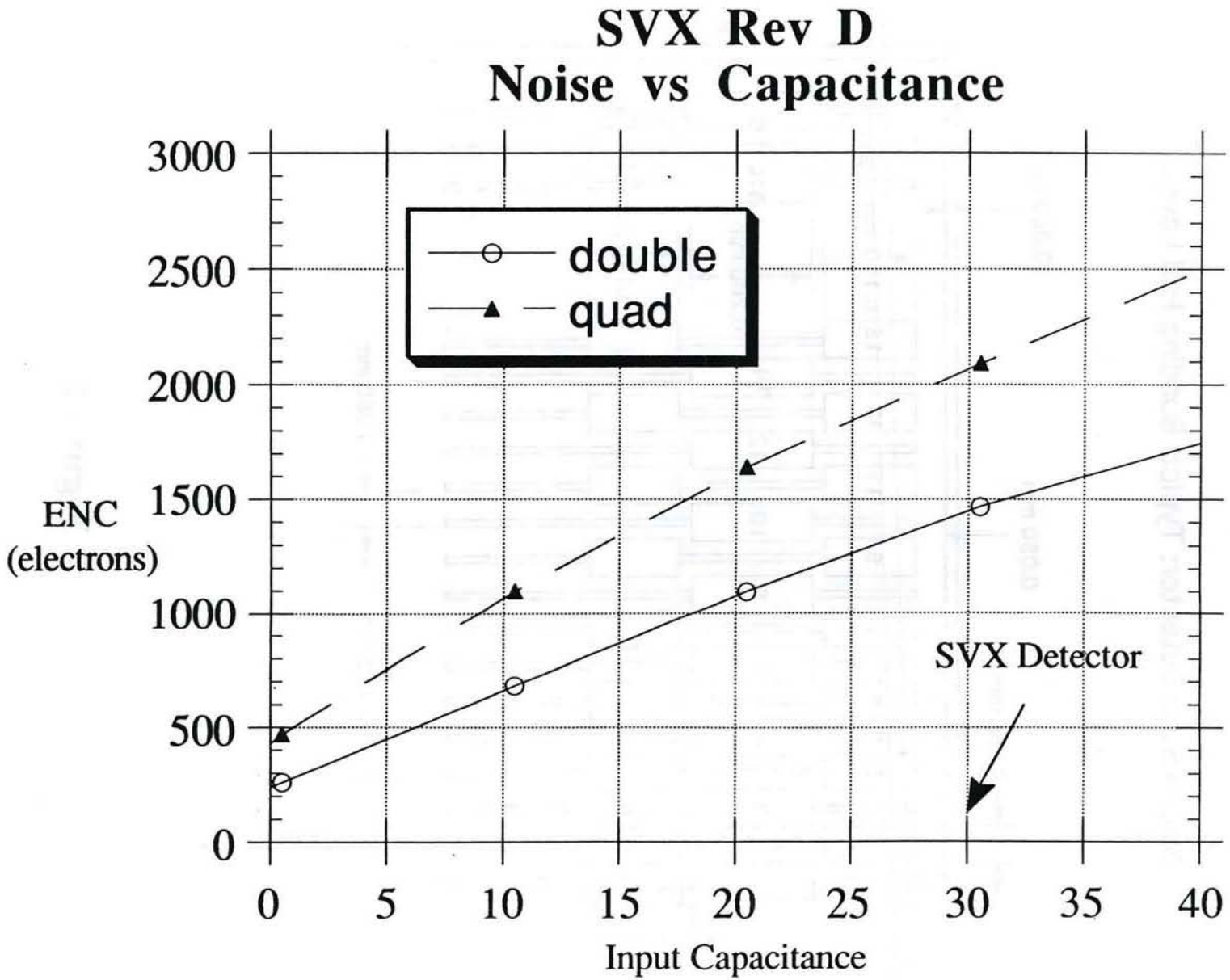

SVX Rev D
Noise vs Capacitance
3000
2500
2000
1500
1000
500
0
ENC
(electrons)
double
quad
SVX Detector
0
5
10
15
20
25
30
35
40
Input Capacitance

Figure 4

Silicon Strip Detector: Typical Bonding Pad Layout

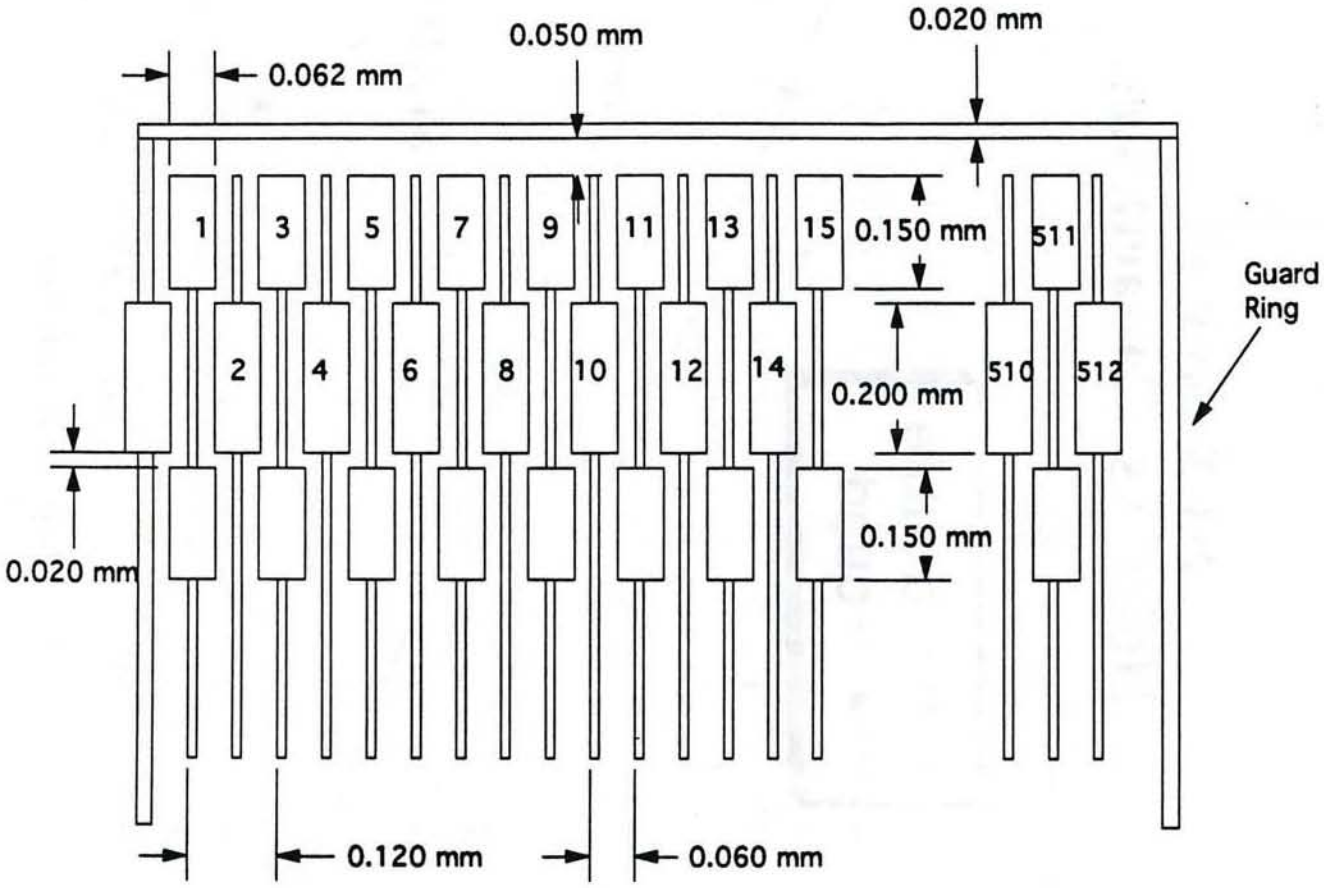


Figure 5

Assembly sequence for the SVX silicon microstrip detectors and associated front-end electronics

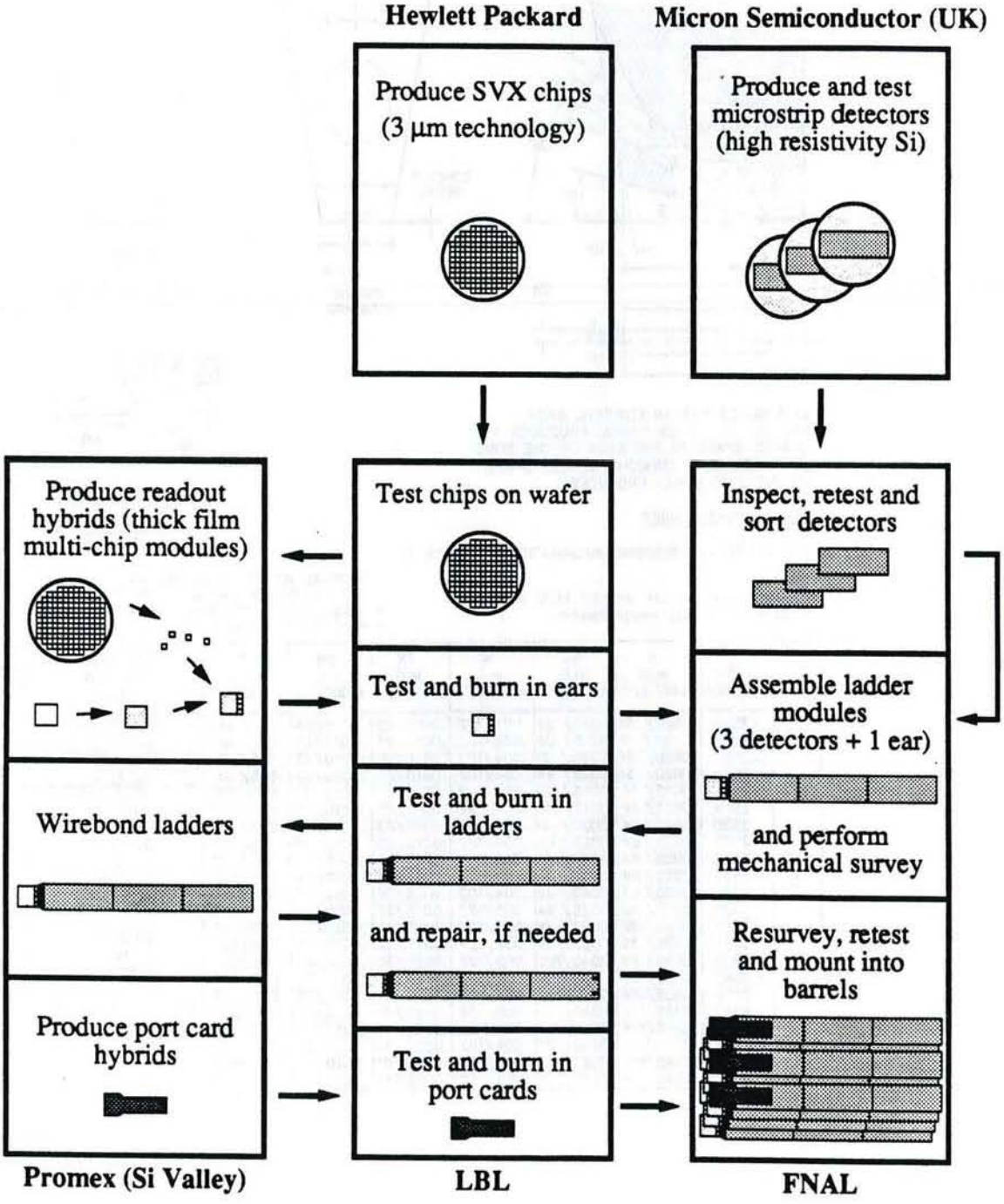


Figure 6

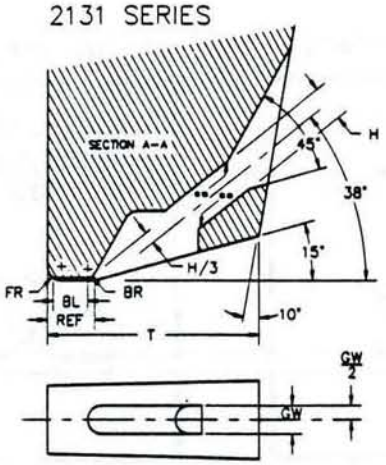
MAXIGUIDE
BONDING WEDGE
2131 SERIES

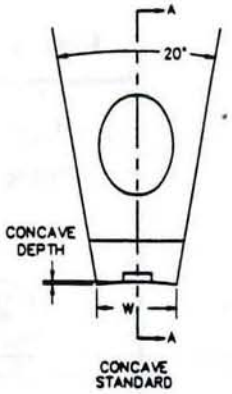
FOR ALUMINUM
OR GOLD WIRE

GAISER TOOL COMPANY

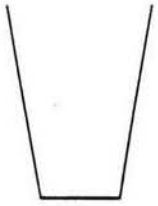
FOR TIP CLEARANCE MODIFICATIONS SEE PAGE 36.

2131 SERIES

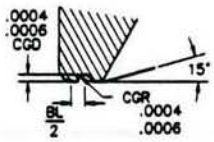




CONCAVE
STANDARD



OPTIONAL
FLAT FACE
ADD –F TO P/N



OPTIONAL CROSS GROVE
ADD –CG TO P/N •
(FLAT FACE ONLY)
RECOMMENDED FOR
GOLD WIRE

2131 SERIES HAS AN ELIPTICAL BACK RADIUS. THIS BACK RADIUS PRODUCES A CURVED SHAPE TO THE BACK OF THE BOND COMPARED TO A STRAIGHT ACROSS SHAPE. AS THE 2130 SERIES PRODUCES.

SAMPLE PART NUMBER
2131–2525–L
FOR ADDITIONAL ORDERING INFORMATION SEE PAGE 35.

Recommended for use on K&S 1470 and Mech El 9000 auto wedge bonders.

OPTIONAL VERTICAL ANGLE ADD –V TO P/N
OPTIONAL POLISHED BR ADD –PBR TO P/N
• CROSS GROOVE NOT AVAILABLE FOR BL <0.0015 in.
•• INDICATES POLISHED SURFACE

STYLE	DASH NUMBER	H in/μ ±.0002/5	BL in/μ ±.0002/5	W in/μ ±.0002/5	FR in/μ ±.0002/5	BR in/μ ±.0002/5	T in/μ ±.0005/13	SUGGESTED WIRE DIA. in/μ
2131	•2010	.0020/ 51	.0010/ 25	.004/102	.0010/25	.0010/25	.015/ 381	.0007/18 to .0010/25
	2015	.0020/ 51	.0015/ 38	.004/102	.0010/25	.0010/25	.015/ 381	
	•2020	.0020/ 51	.0020/ 51	.004/102	.0010/25	.0010/25	.015/ 381	.0010/25 to .0012/30
	2025	.0020/ 51	.0025/ 64	.004/102	.0010/25	.0010/25	.015/ 381	
	•2510	.0025/ 64	.0010/ 25	.004/102	.0010/25	.0010/25	.015/ 381	.0007/18 to .0010/25
	2515	.0025/ 64	.0015/ 38	.004/102	.0010/25	.0010/25	.015/ 381	
	2520	.0025/ 64	.0020/ 51	.004/102	.0010/25	.0010/25	.015/ 381	.0010/25 to .0012/30
	2525	.0025/ 64	.0025/ 64	.004/102	.0010/25	.0010/25	.015/ 381	
	2530	.0025/ 64	.0030/ 76	.004/102	.0015/38	.0010/25	.015/ 381	
	2535	.0025/ 64	.0035/ 89	.004/102	.0015/38	.0010/25	.020/508	
	2540	.0025/ 64	.0040/102	.004/102	.0015/38	.0010/25	.020/508	
	3525	.0035/ 89	.0025/ 64	.005/127	.0015/38	.0010/25	.020/508	.0013/33 to .0020/51
	3530	.0035/ 89	.0030/ 76	.005/127	.0015/38	.0010/25	.025/635	
	3535	.0035/ 89	.0035/ 89	.005/127	.0015/38	.0010/25	.025/635	
	3540	.0035/ 89	.0040/102	.005/127	.0015/38	.0010/25	.025/635	
	3545	.0035/ 89	.0045/114	.005/127	.0015/38	.0010/25	.025/635	
	3550	.0035/ 89	.0050/127	.005/127	.0015/38	.0010/25	.025/635	
	4540	.0045/114	.0040/102	.006/152	.0020/51	.0010/25	.035/889	.0030/76
	4545	.0045/114	.0045/114	.006/152	.0020/51	.0010/25	.035/889	
	4550	.0045/114	.0050/127	.006/152	.0020/51	.0010/25	.035/889	
	4560	.0045/114	.0060/152	.006/152	.0020/51	.0010/25	.035/889	
	4570	.0045/114	.0070/178	.006/152	.0020/51	.0010/25	.035/889	

Figure 7

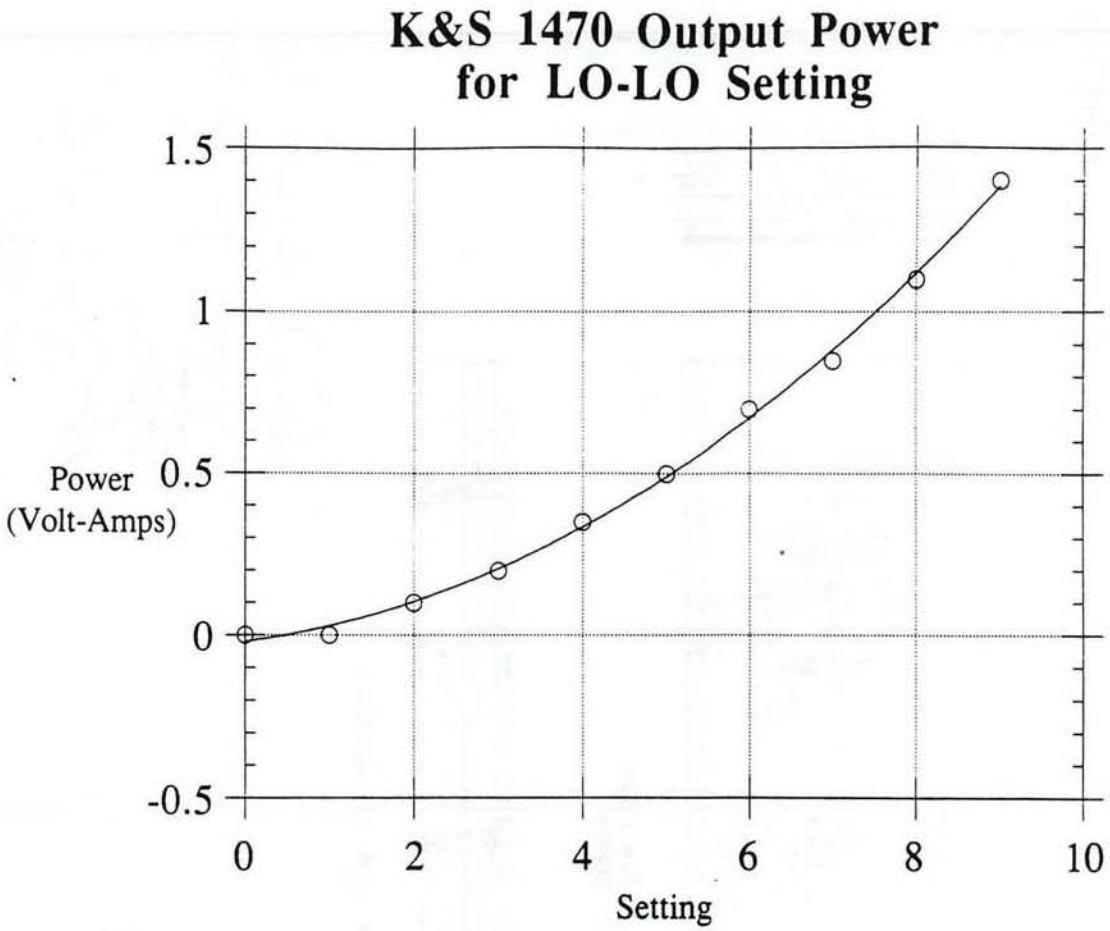


Figure 8a

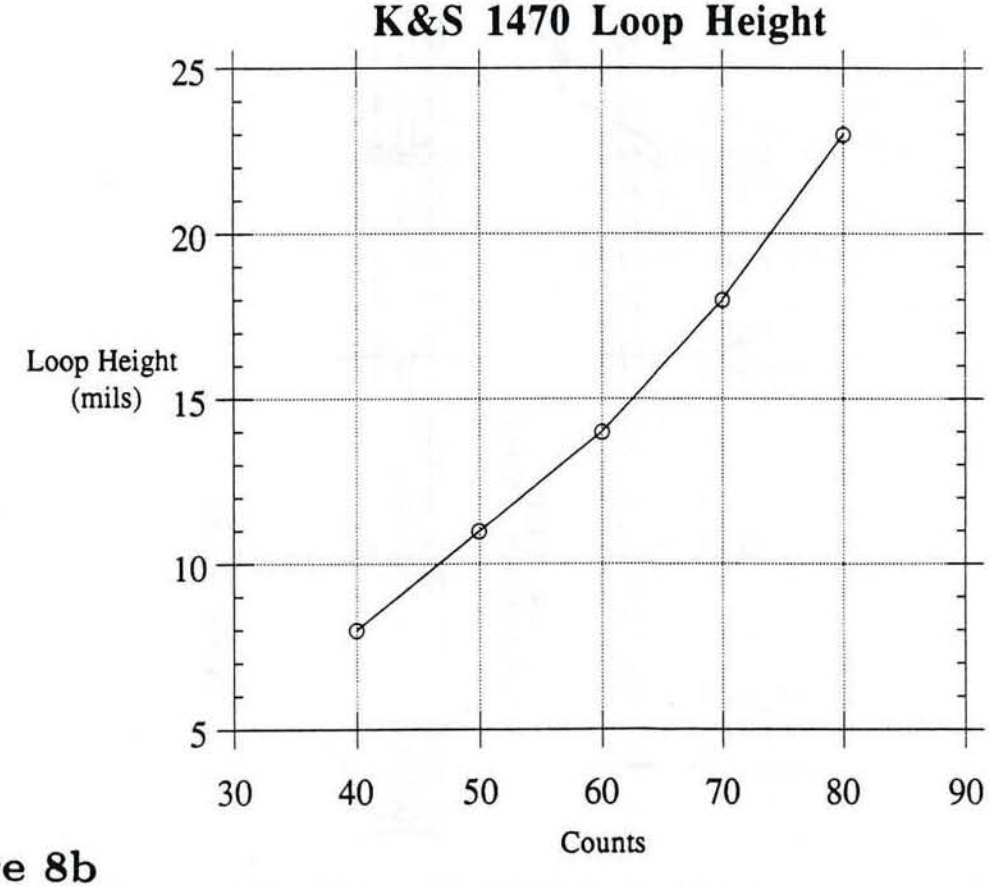


Figure 8b

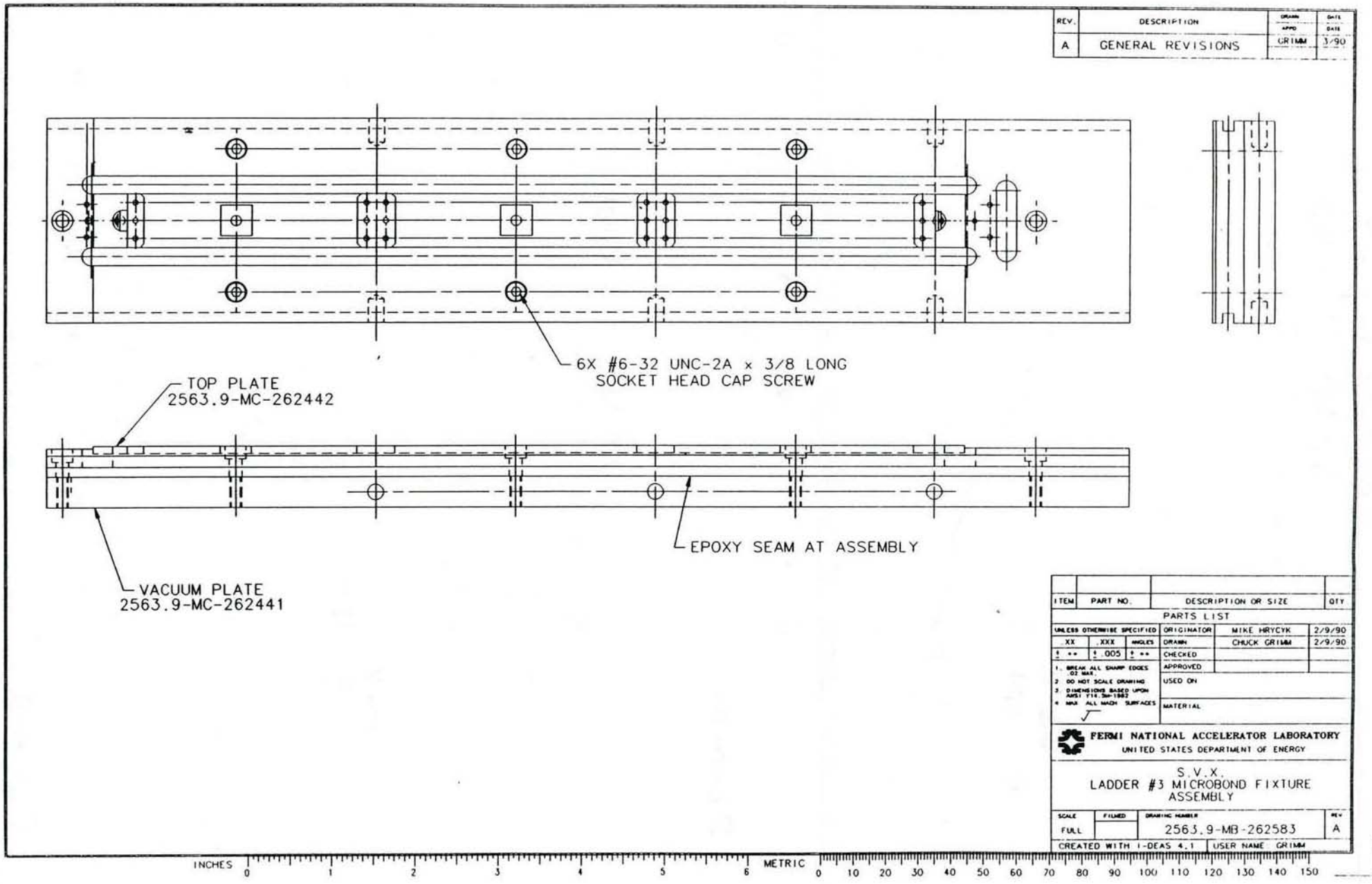

REV.
DESCRIPTION
DRAWN
DATE
A
GENERAL REVISIONS
GRIMM
3/90
6X #6-32 UNC-2A x 3/8 LONG
SOCKET HEAD CAP SCREW
TOP PLATE
2563.9-MC-262442
EPOXY SEAM AT ASSEMBLY
VACUUM PLATE
2563.9-MC-262441
ITEM
PART NO.
DESCRIPTION OR SIZE
QTY
PARTS LIST
UNLESS OTHERWISE SPECIFIED
ORIGINATOR
MIKE HRYCYK
2/9/90
DRAWN
CHUCK GRIMM
2/9/90
CHECKED
APPROVED
USED ON
MATERIAL
FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY
S.V.X.
LADDER #3 MICROBOND FIXTURE
ASSEMBLY
SCALE
FULL
FILMED
DRAWING NUMBER
2563.9-MB-262583
REV
A
CREATED WITH I-DEAS 4.1
USER NAME GRIMM
INCHES
METRIC

Figure 9

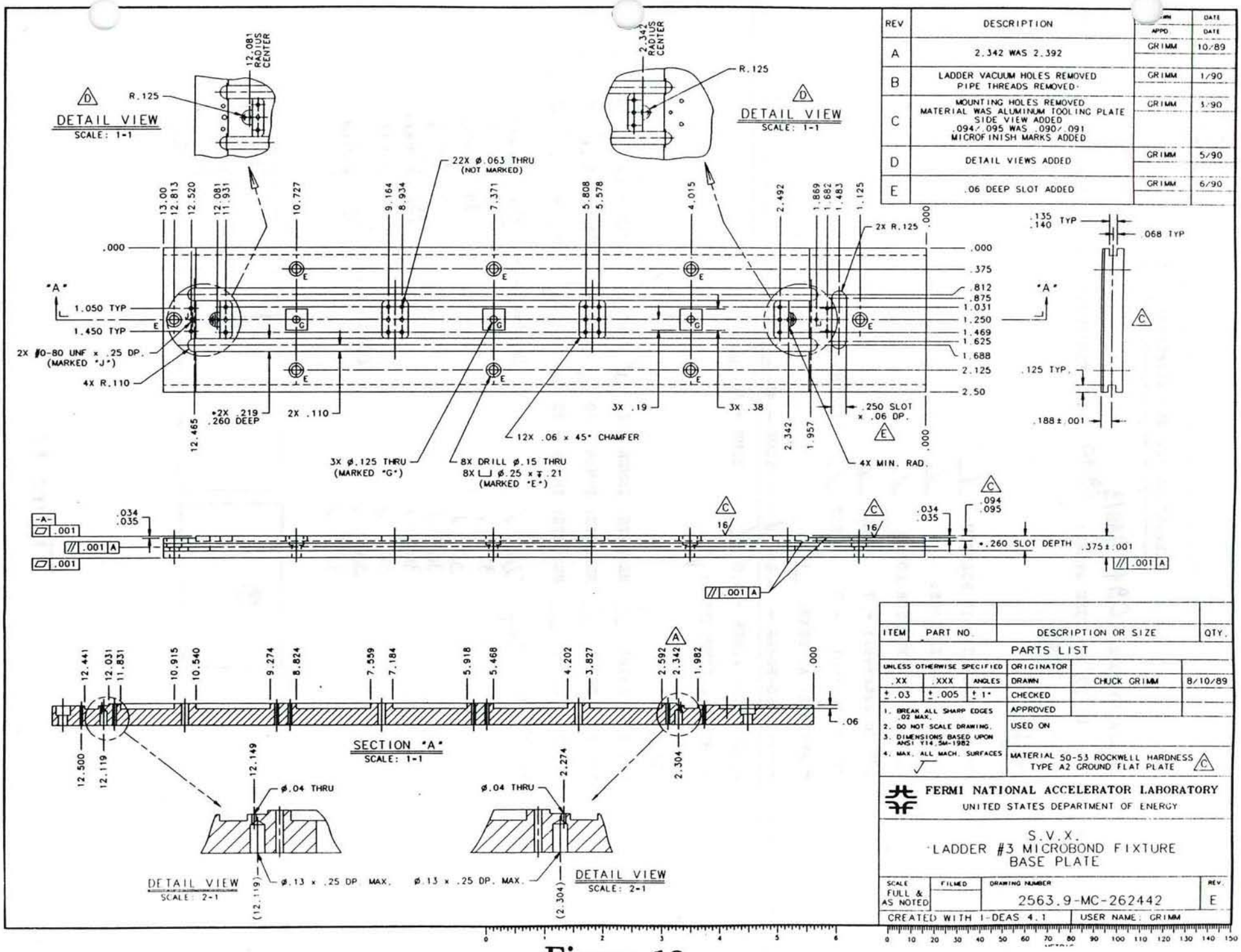

REV
DESCRIPTION
DRAWN
APPD
DATE
A
2.342 WAS 2.392
GRIMM
10/89
B
LADDER VACUUM HOLES REMOVED
PIPE THREADS REMOVED
GRIMM
1/90
C
MOUNTING HOLES REMOVED
MATERIAL WAS ALUMINUM TOOLING PLATE
SIDE VIEW ADDED
.094/.095 WAS .090/.091
MICROFINISH MARKS ADDED
GRIMM
3/90
D
DETAIL VIEWS ADDED
GRIMM
5/90
E
.06 DEEP SLOT ADDED
GRIMM
6/90
DETAIL VIEW
SCALE: 1-1
R.125
12.081 RADIUS CENTER
2.342 RADIUS CENTER
22X Ø.063 THRU (NOT MARKED)
2X R.125
1.050 TYP
1.450 TYP
2X #0-80 UNF x .25 DP. (MARKED "J")
4X R.110
2X Ø.219 .260 DEEP
2X .110
3X Ø.125 THRU (MARKED "G")
8X DRILL Ø.15 THRU
8X ⌴ Ø.25 x ↧.21 (MARKED "E")
12X .06 x 45° CHAMFER
3X .19
3X .38
.250 SLOT x .06 DP.
4X MIN. RAD.
.135 .140 TYP
.068 TYP
.125 TYP.
.188±.001
.034 .035
.094 .095
.260 SLOT DEPTH
.375±.001
.001 A
SECTION "A"
SCALE: 1-1
Ø.04 THRU
Ø.13 x .25 DP. MAX.
DETAIL VIEW
SCALE: 2-1
ITEM
PART NO.
DESCRIPTION OR SIZE
QTY.
PARTS LIST
UNLESS OTHERWISE SPECIFIED
.XX ±.03
.XXX ±.005
ANGLES ±1°
1. BREAK ALL SHARP EDGES .02 MAX.
2. DO NOT SCALE DRAWING.
3. DIMENSIONS BASED UPON ANSI Y14.5M-1982
4. MAX. ALL MACH. SURFACES
ORIGINATOR
DRAWN CHUCK GRIMM 8/10/89
CHECKED
APPROVED
USED ON
MATERIAL 50-53 ROCKWELL HARDNESS TYPE A2 GROUND FLAT PLATE
FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY
S.V.X.
LADDER #3 MICROBOND FIXTURE
BASE PLATE
SCALE FULL & AS NOTED
FILMED
DRAWING NUMBER 2563.9-MC-262442
REV. E
CREATED WITH I-DEAS 4.1
USER NAME: GRIMM

Figure 10

svx$docu:bond_chklst.txt
Carl Haber
CDF/LBL
8/15/90

Checklist for SVX Wirebonding V1.2

LADDER ID CODE: 091-4A013

DATE: 01/29/91 TIME START: 09:10 TIME FINISHED: 16:40 ELAPSED TIME: 7:30

PERSONNEL: Olivia

SETUP:

WIRE IS 1.0 MIL, 1% SILICON: ✓

WEDGE IS GAISER 2025: ✓

ULTRASONIC GENERATOR LO/LO ✓

OTV (overtravel) = 7 FIRST ✓

CVL (velocity) = 7 FIRST ✓ SECOND ✓

CLAMP OPEN AT TEAR: ✓

FIRST BOND POWER = 4.8 ✓ TIME = 45 ✓

SECOND BOND POWER = 5.0 ✓ TIME = 40 ✓

GUARD RING CONNECTION: ✓

POSITION:

DET 1 -> CHIPS	✓	HEIGHTS: INNER = 35	✓	VAC	✓	OUTER = 80	✓	VAC ✓
DET 2 -> DET 1	✓	HEIGHTS: INNER = 30	✓	VAC	✓	OUTER = 50	✓	VAC ✓
DET 3 -> DET 2	✓	HEIGHTS: INNER = 30	✓	VAC	✓	OUTER = 50	✓	VAC ✓

COMMENTS:

Skip: 206 ✓, 327 ✓, 366 ✓, 367 ✓, 368 ✓, 369 ✓, 530 ✓, 755 ✓

Det 1 → chips: 734 reboarded, 732 pushed, 24 reboarded, 4 lifted up, 255 reboarded, 191 pushed

Det 3 → Det 2: 435 pushed

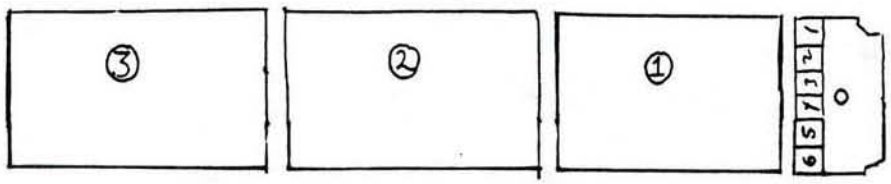


Figure 11

Ladder testing hardware configuration

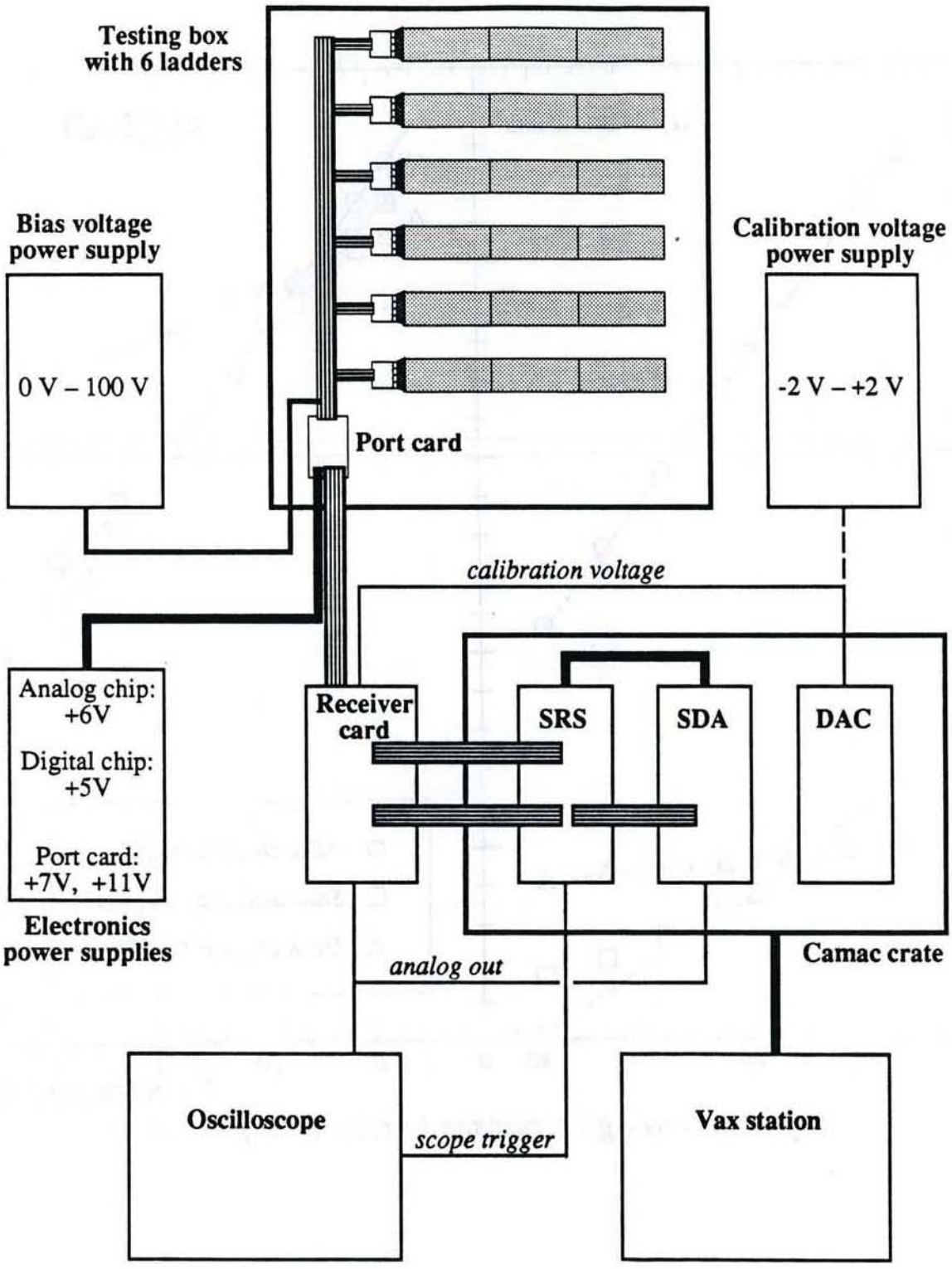
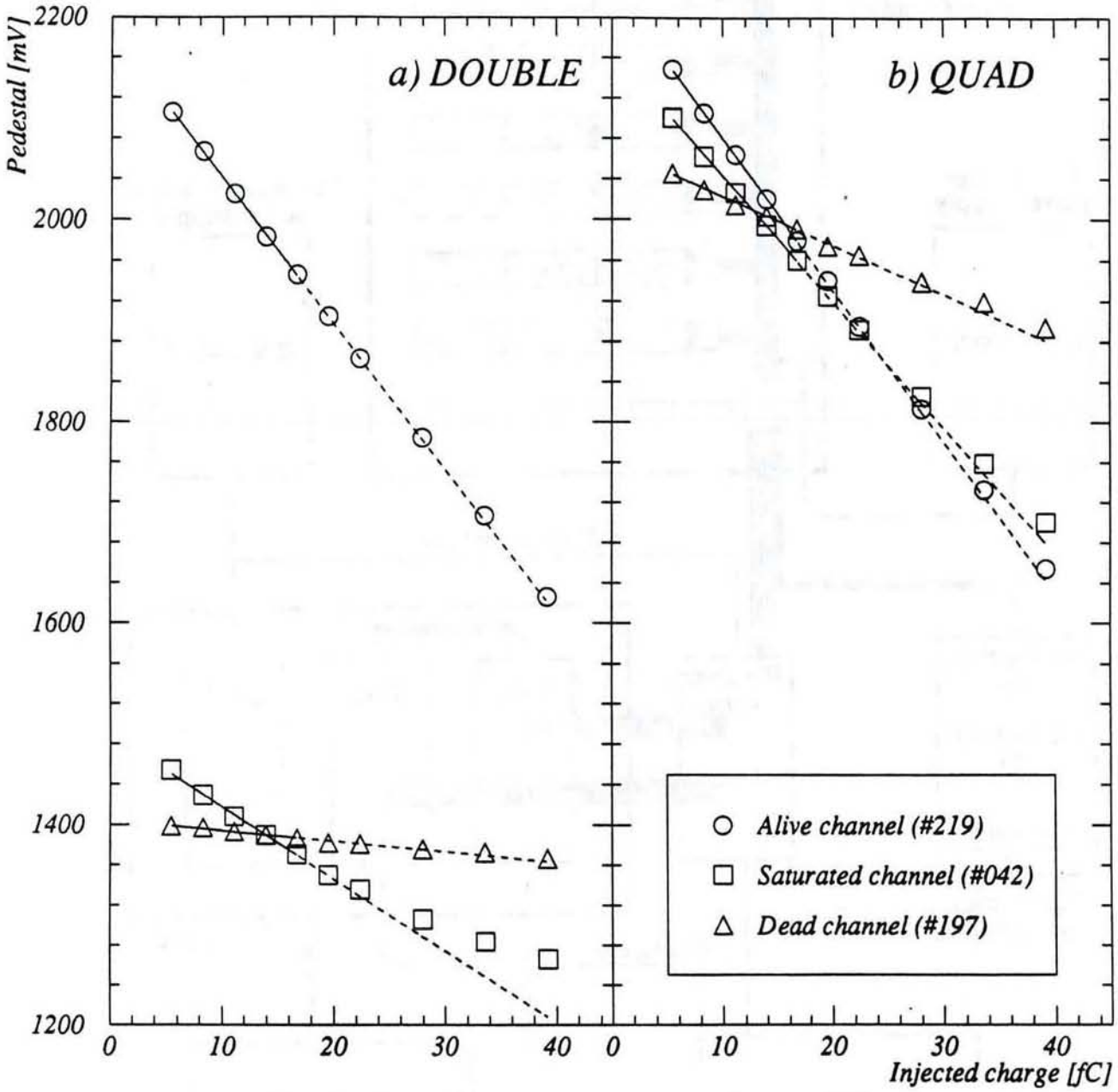
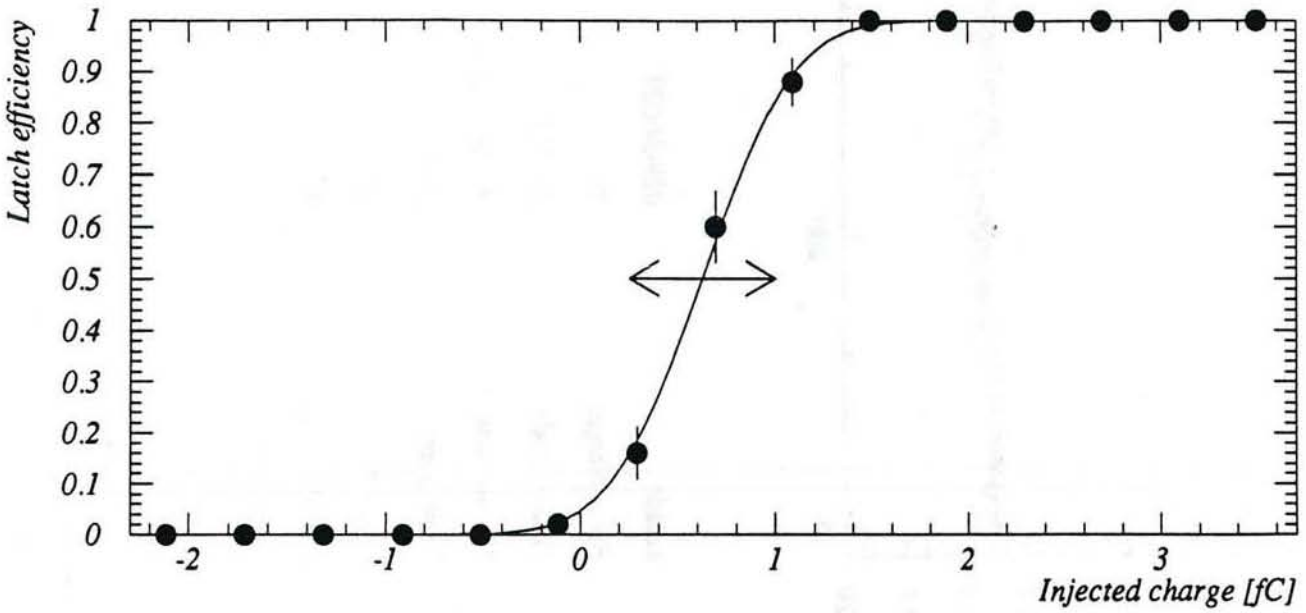


Figure 12



Typical analog responses to charge injection

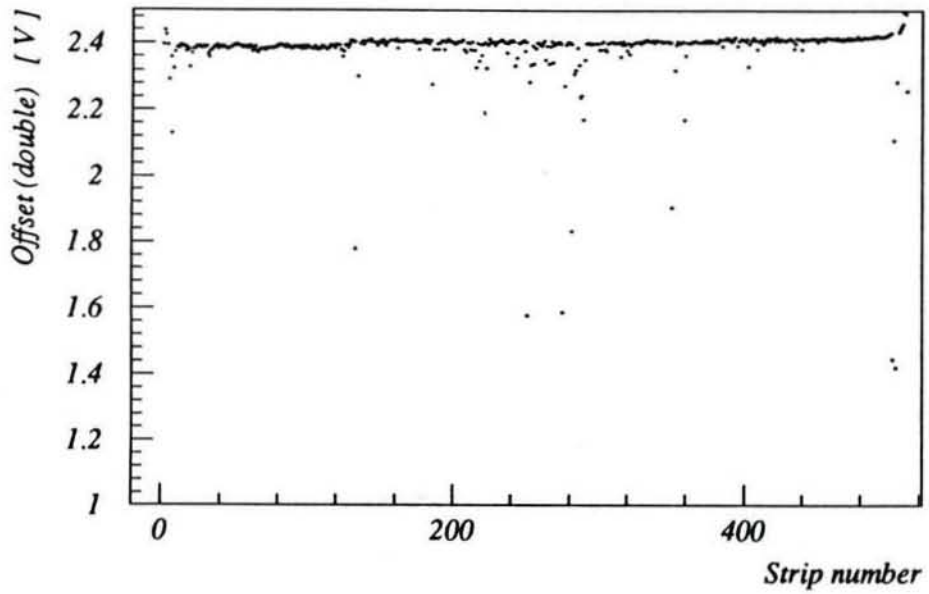
Figure 13

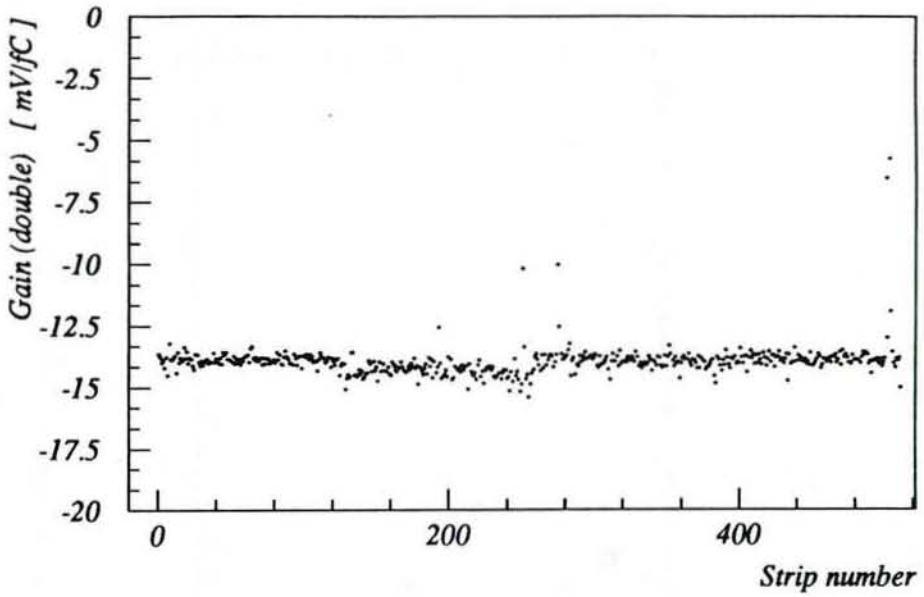


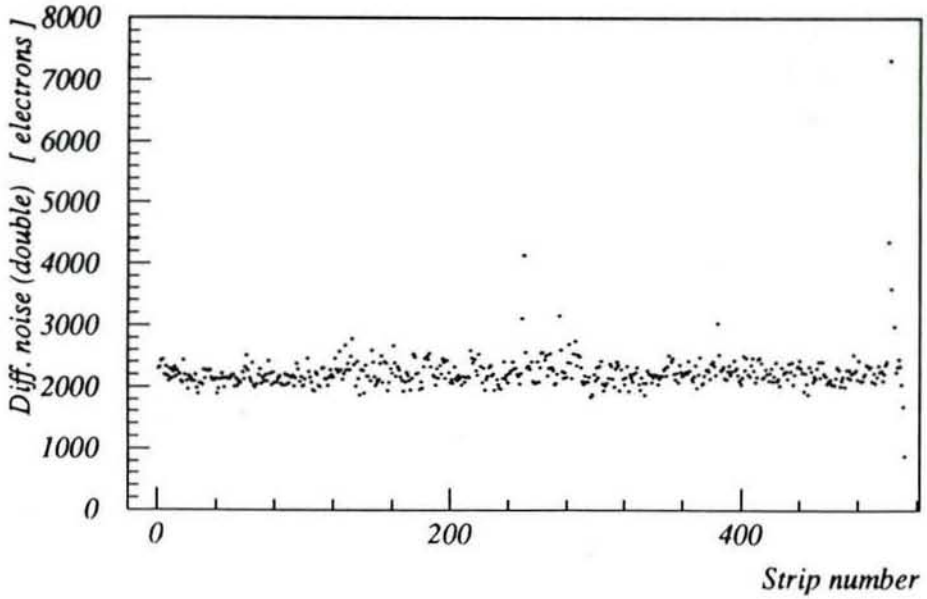
Typical digital response to charge injection

Figure 14

029-3F029



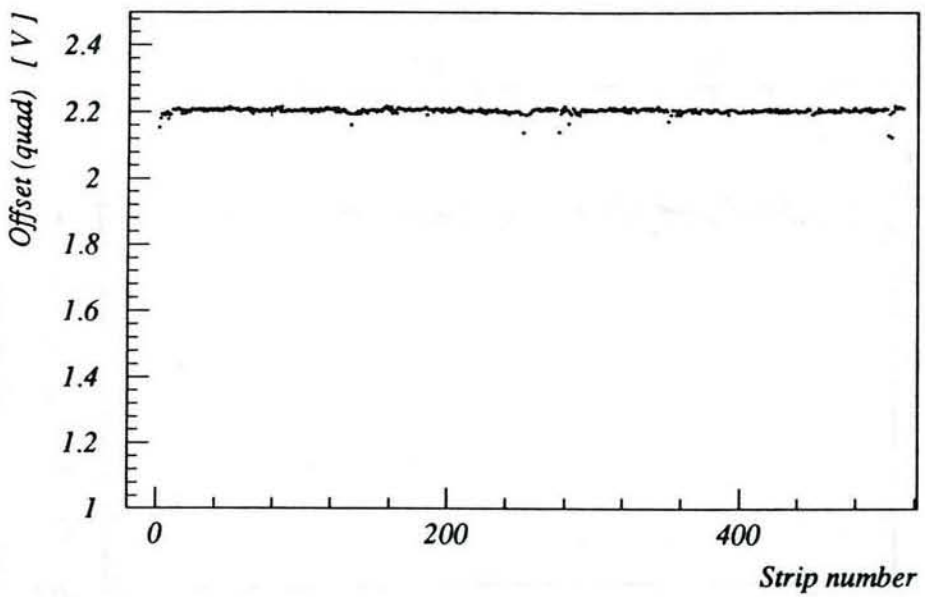


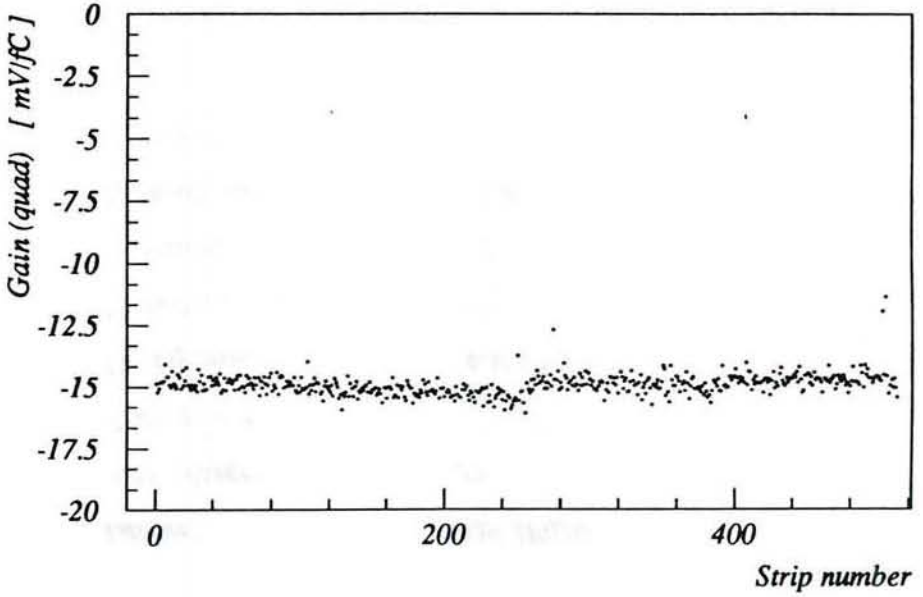


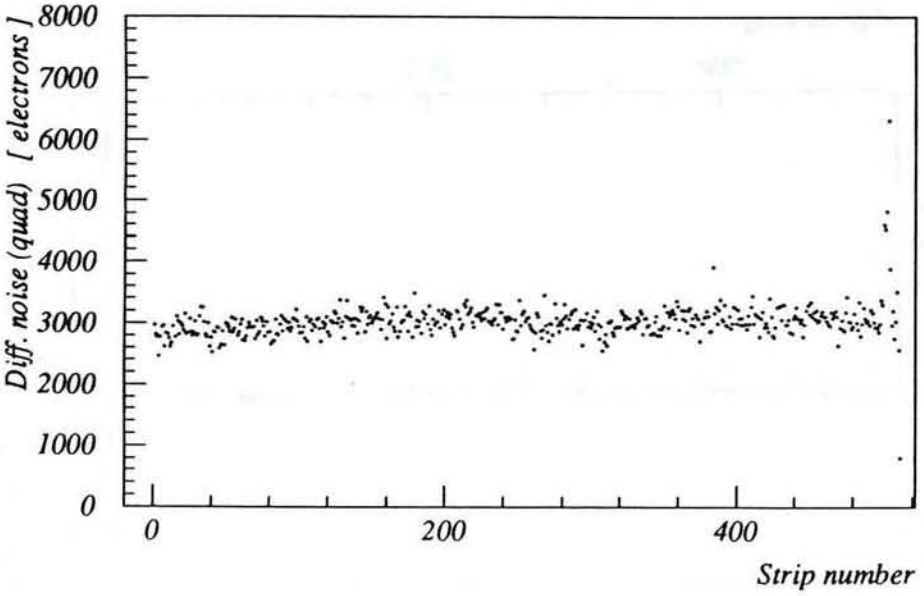
Ladder:	*029-3F029*
Bias voltage:	*35*
Testing code:	*225311*
Testing date:	*4-MAR-1991*
Testing time:	*16:06*
Operator:	*OS*
Logbook page:	*B168*
Comment:	

Figure 15

029-3F029



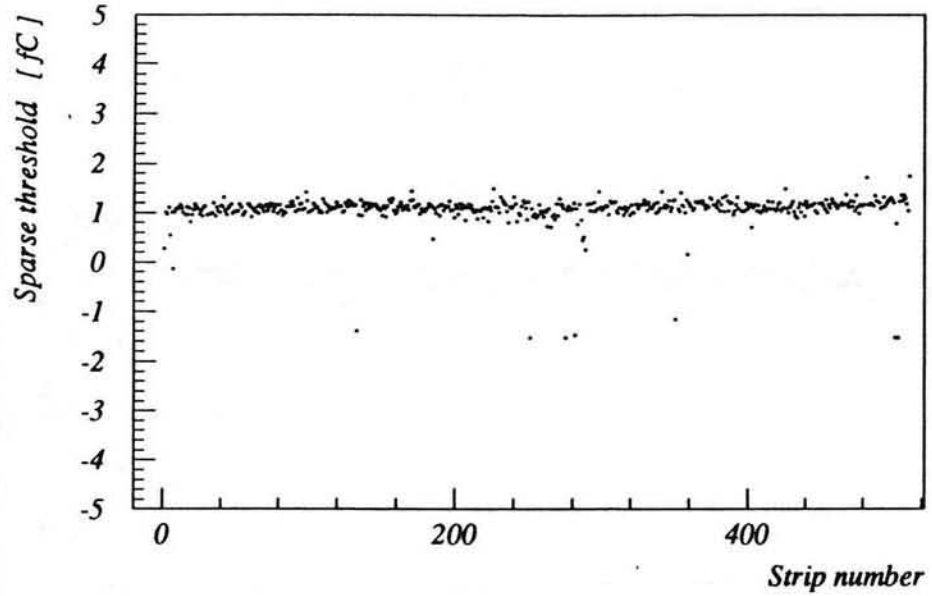


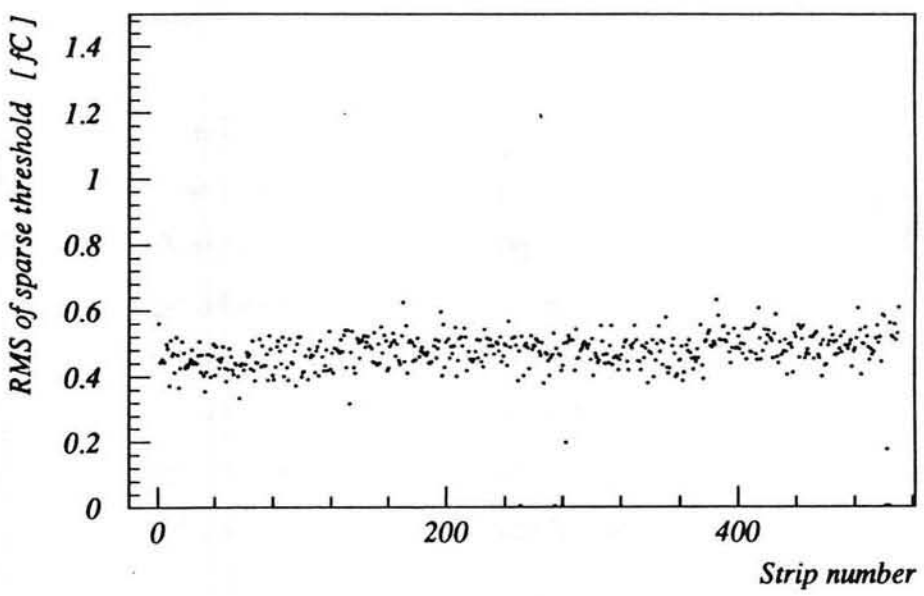


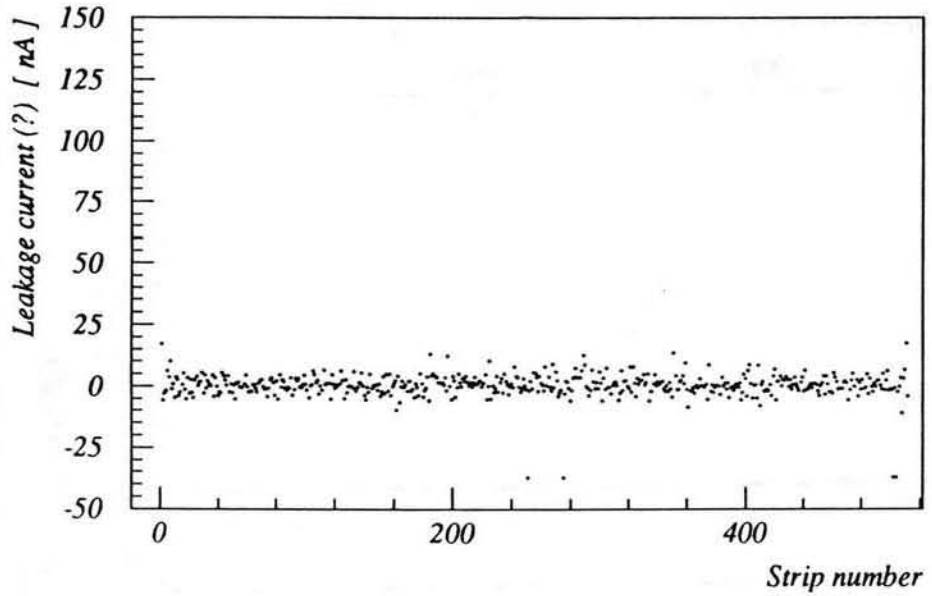
Ladder:	*029-3F029*
Bias voltage:	*35*
Testing code:	*225311*
Testing date:	*4-MAR-1991*
Testing time:	*16:06*
Operator:	*OS*
Logbook page:	*B168*
Comment:	

Figure 16

029-3F029



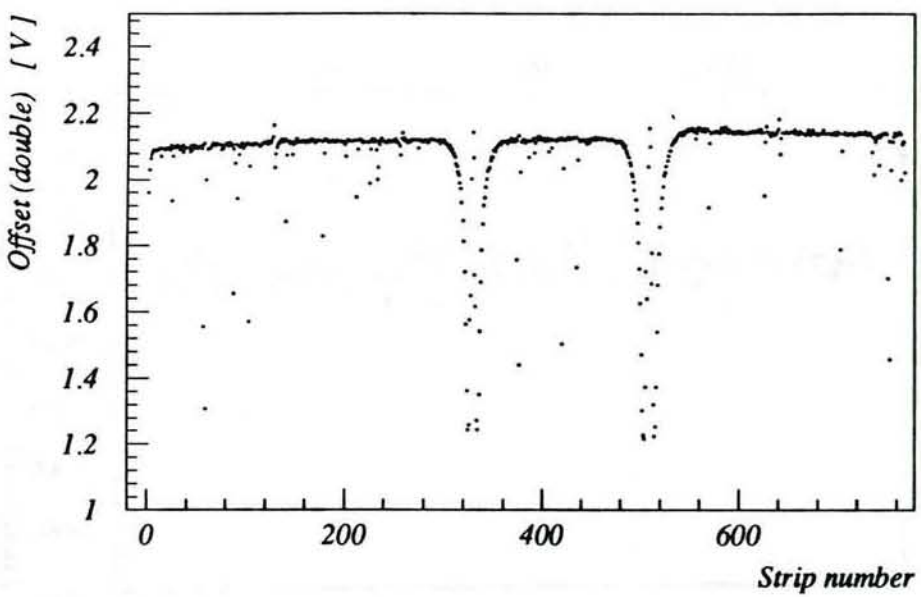


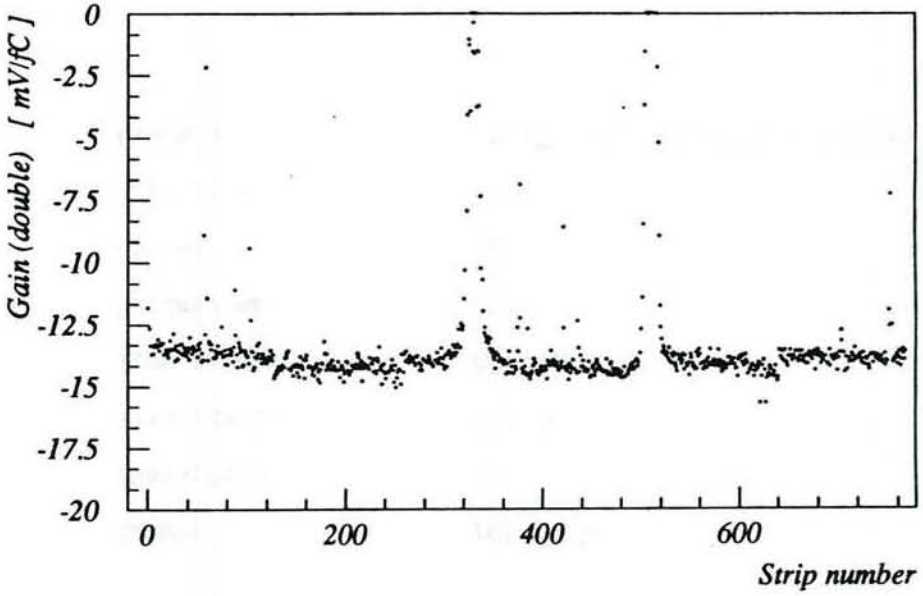


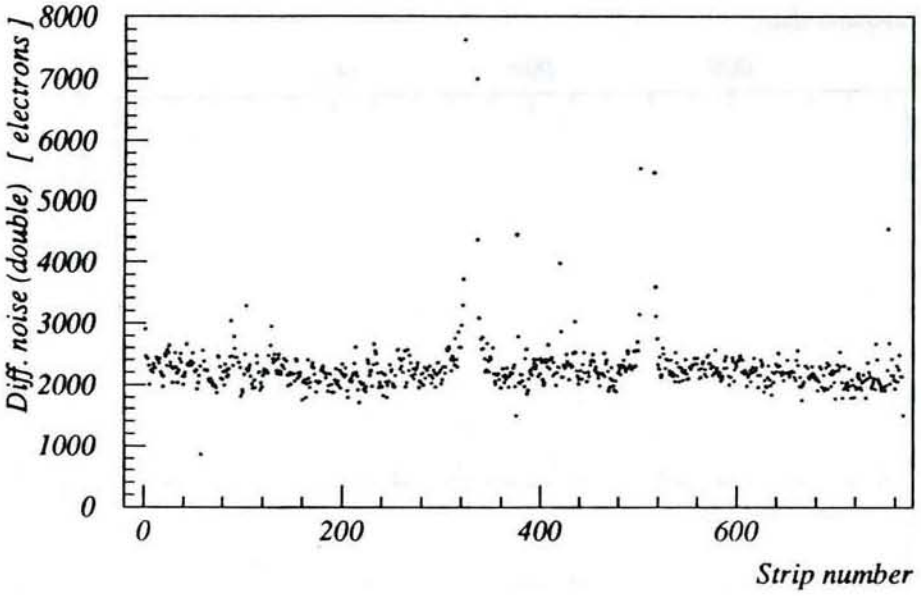
Ladder:	*029-3F029*
Bias voltage:	*35*
Testing code:	*225311*
Testing date:	*4-MAR-1991*
Testing time:	*16:06*
Operator:	*OS*
Logbook page:	*B168*
Comment:	

Figure 17

105-4B034



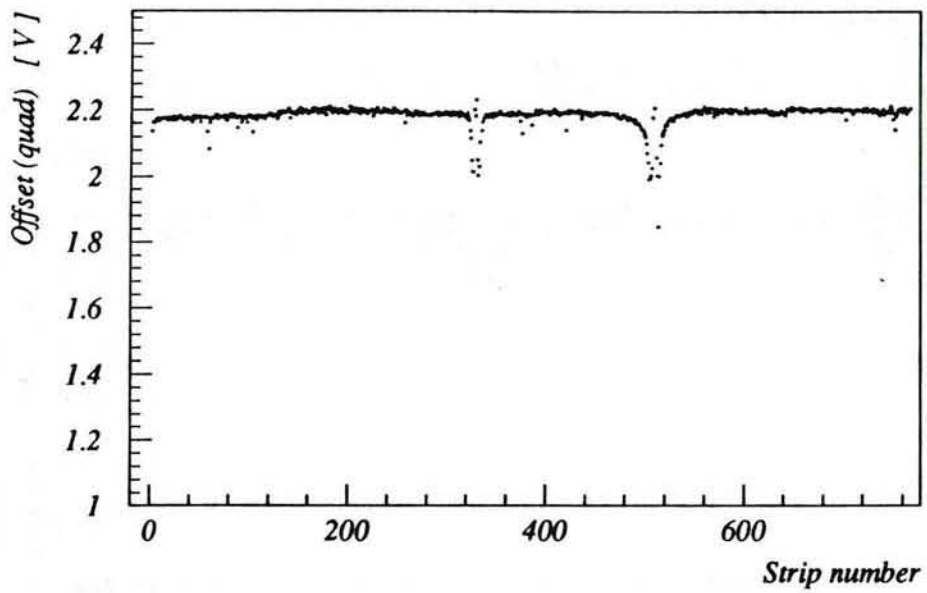


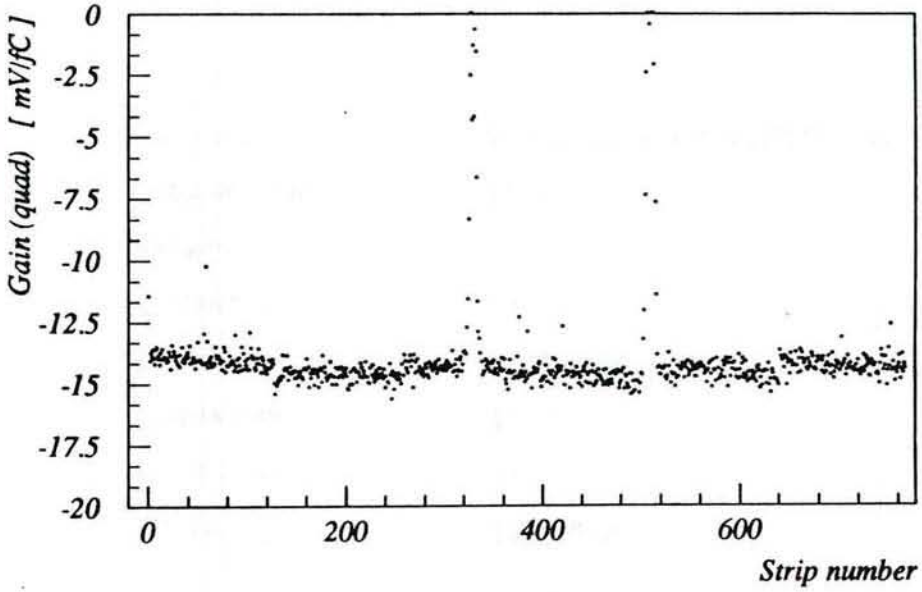


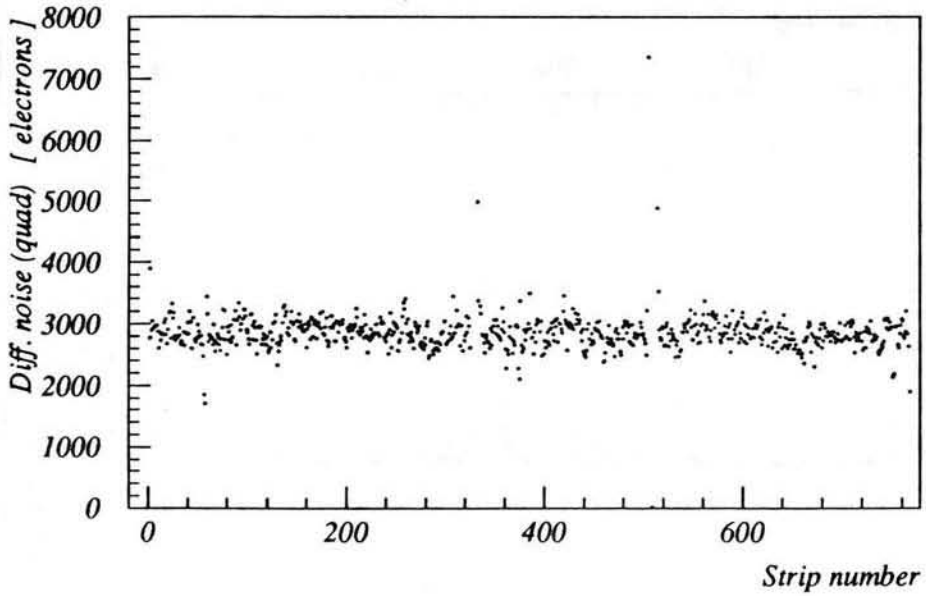
Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*22-MAR-1991*
Testing time:	*16:53*
Operator:	*OS*
Logbook page:	*B186*
Comment:	*BH AT 329_1, 509_1 NEED FIXING*

Figure 18

105-4B034



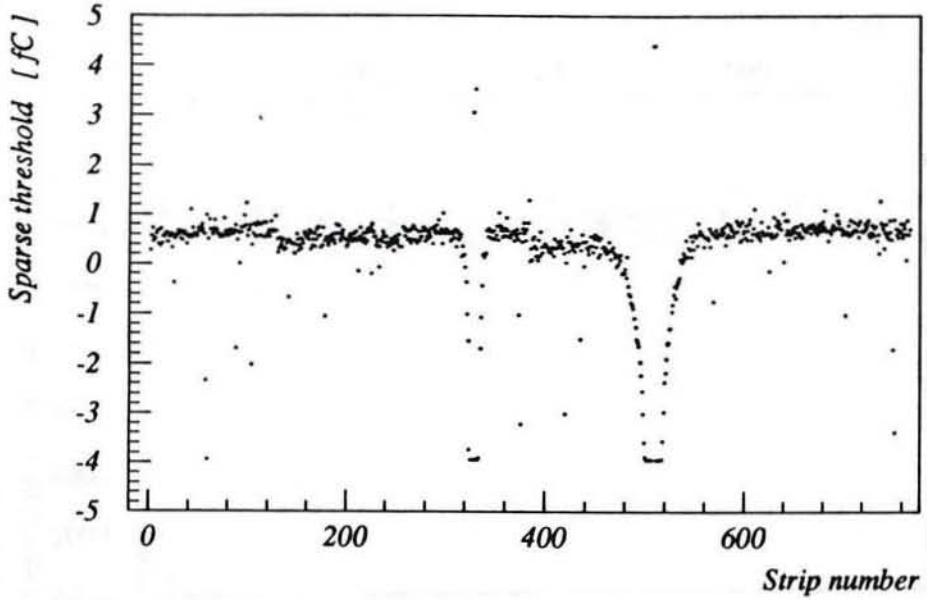


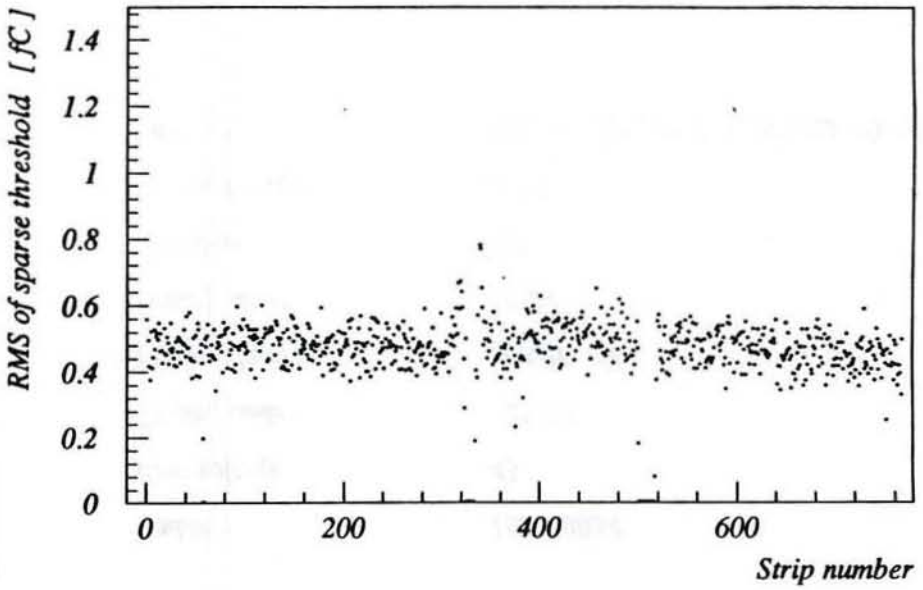


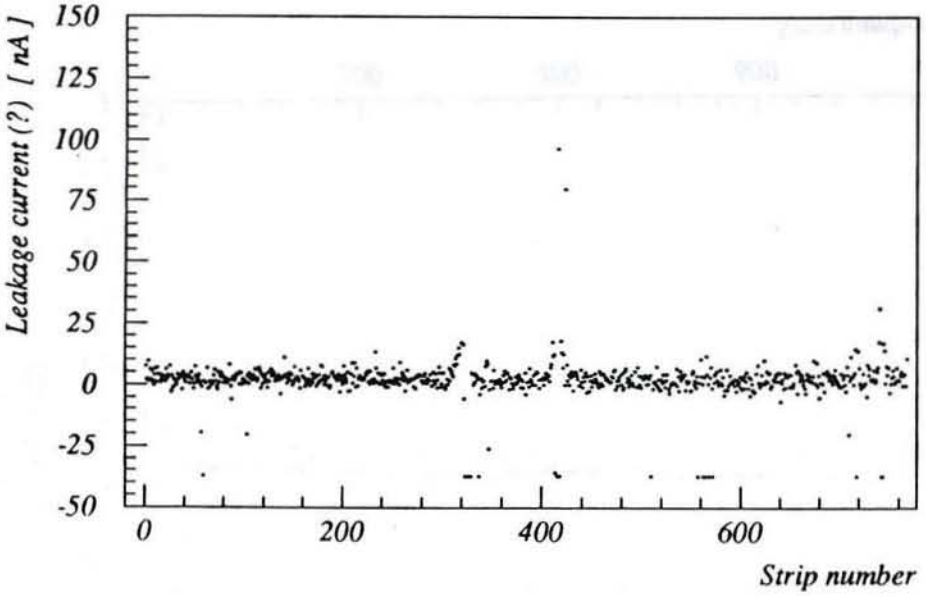
Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*22-MAR-1991*
Testing time:	*16:53*
Operator:	*OS*
Logbook page:	*B186*
Comment:	*BH AT 329_1, 509_1 NEED FIXING*

Figure 19

105-4B034



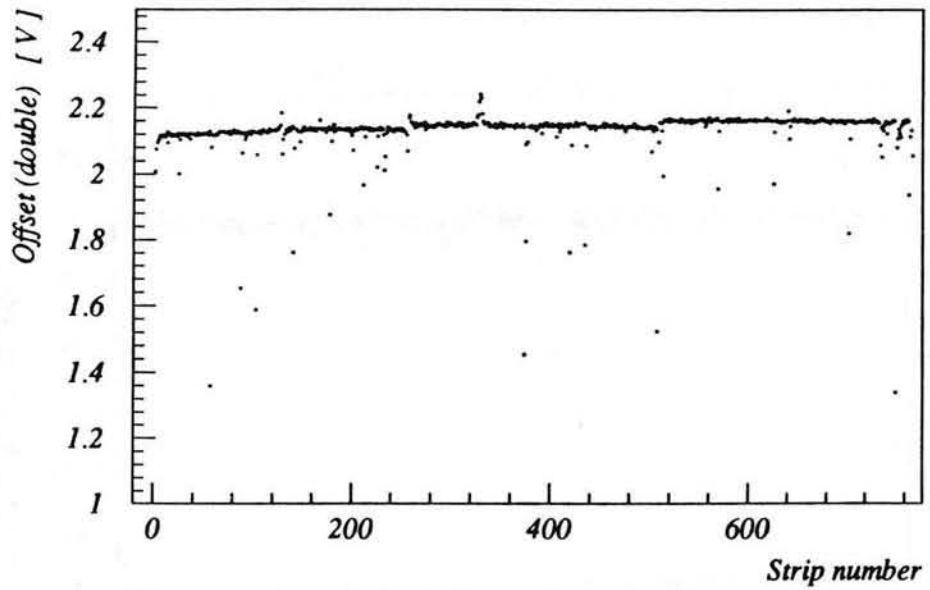


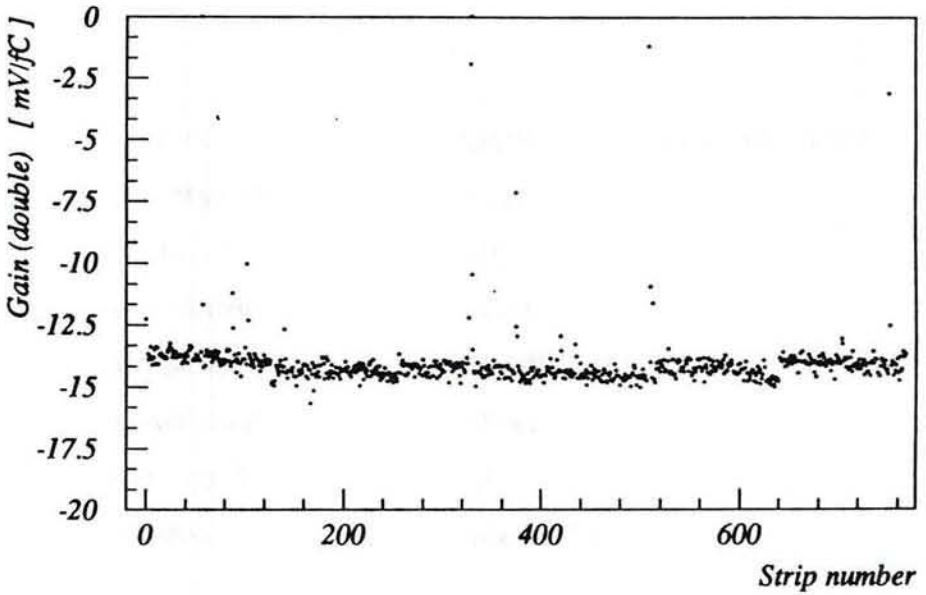


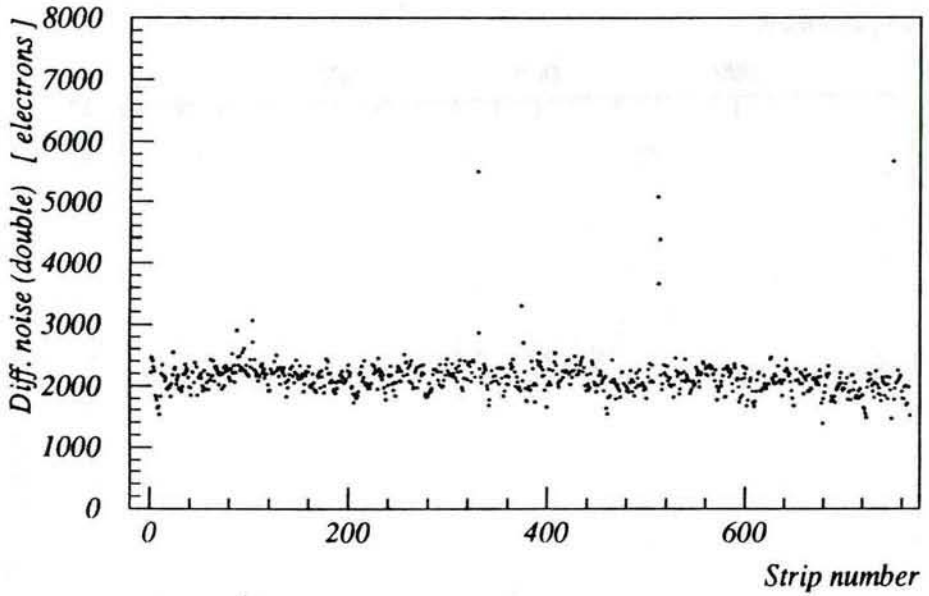
Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*22-MAR-1991*
Testing time:	*16:53*
Operator:	*OS*
Logbook page:	*B186*
Comment:	*BH AT 329_1, 509_1 NEED FIXING*

Figure 20

105-4B034



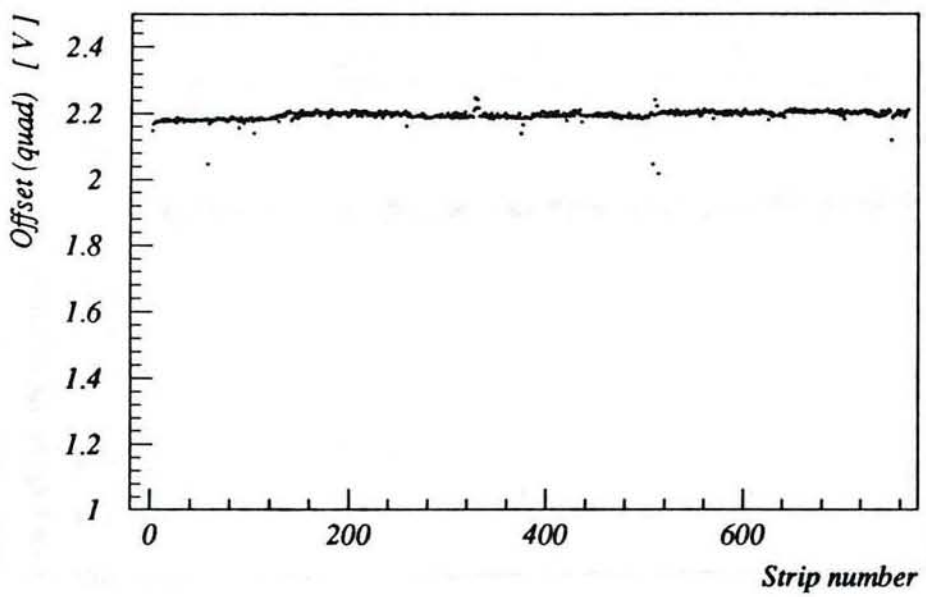


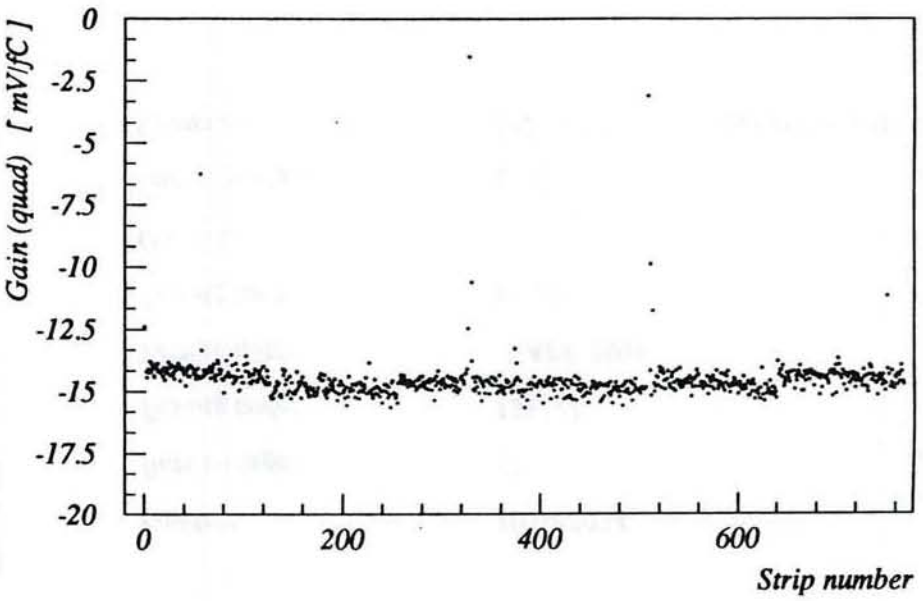


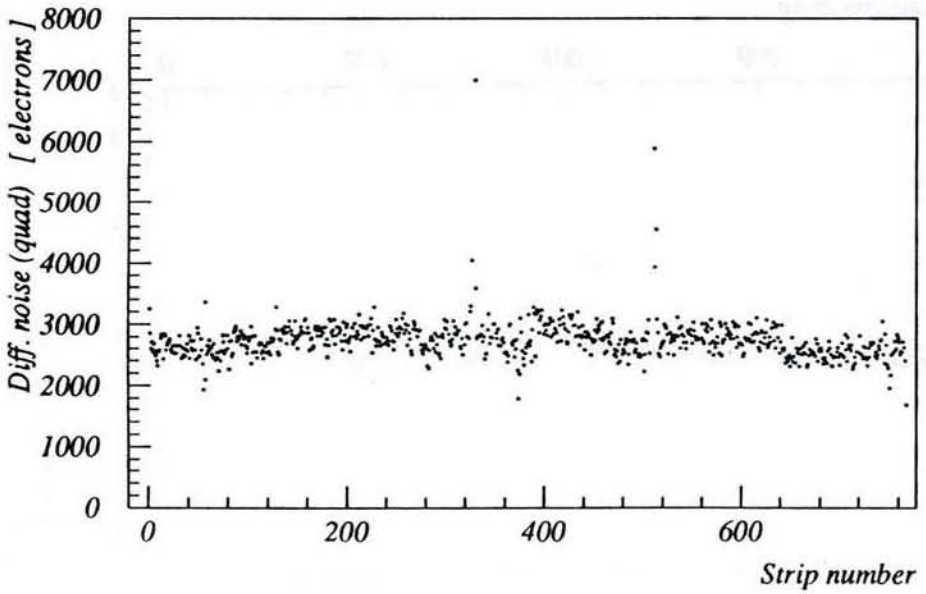
Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*3-APR-1991*
Testing time:	*11:29*
Operator:	*OS*
Logbook page:	*B195*
Comment:	*329_1 AND 509_1 BONDED TO CAP*

Figure 21

105-4B034



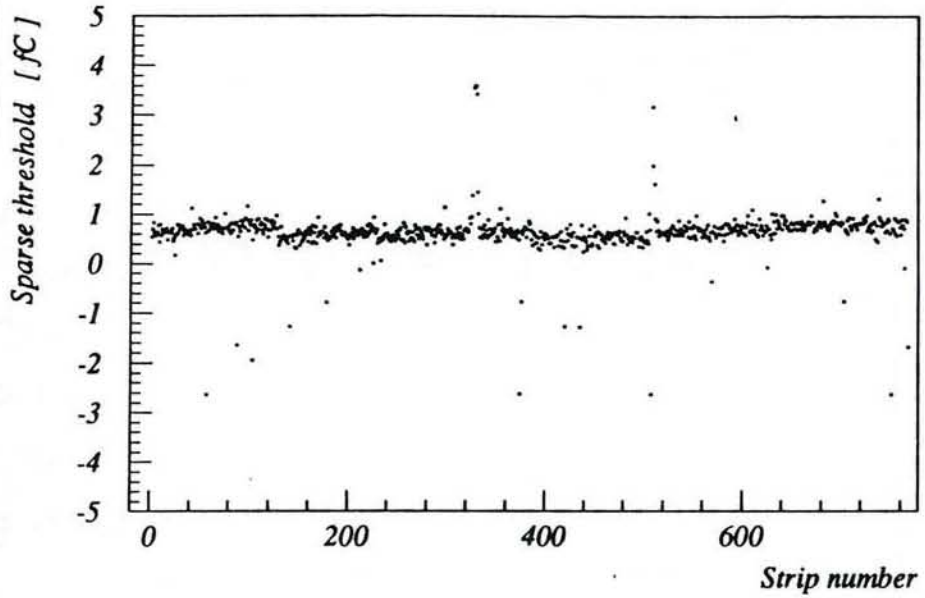


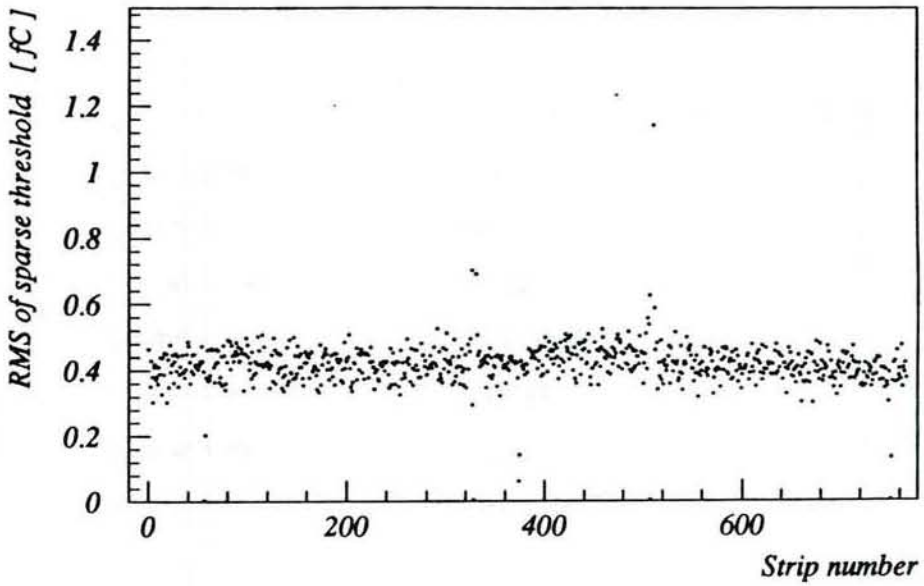


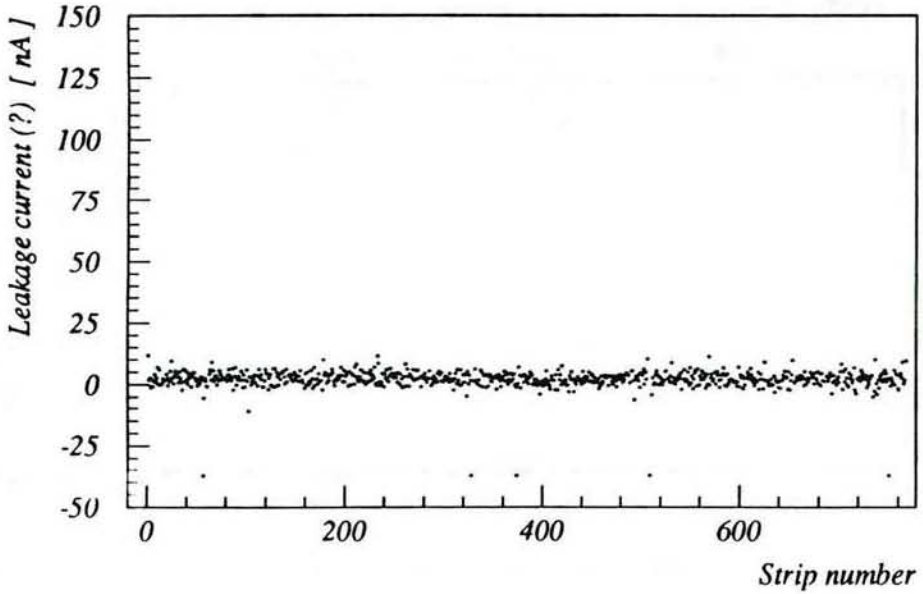
Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*3-APR-1991*
Testing time:	*11:29*
Operator:	*OS*
Logbook page:	*B195*
Comment:	*329_1 AND 509_1 BONDED TO CAP*

Figure 22

105-4B034







Ladder:	*105-4B034*
Bias voltage:	*43*
Testing code:	*125311*
Testing date:	*3-APR-1991*
Testing time:	*11:29*
Operator:	*OS*
Logbook page:	*B195*
Comment:	*329_1 AND 509_1 BONDED TO CAP*

Figure 23

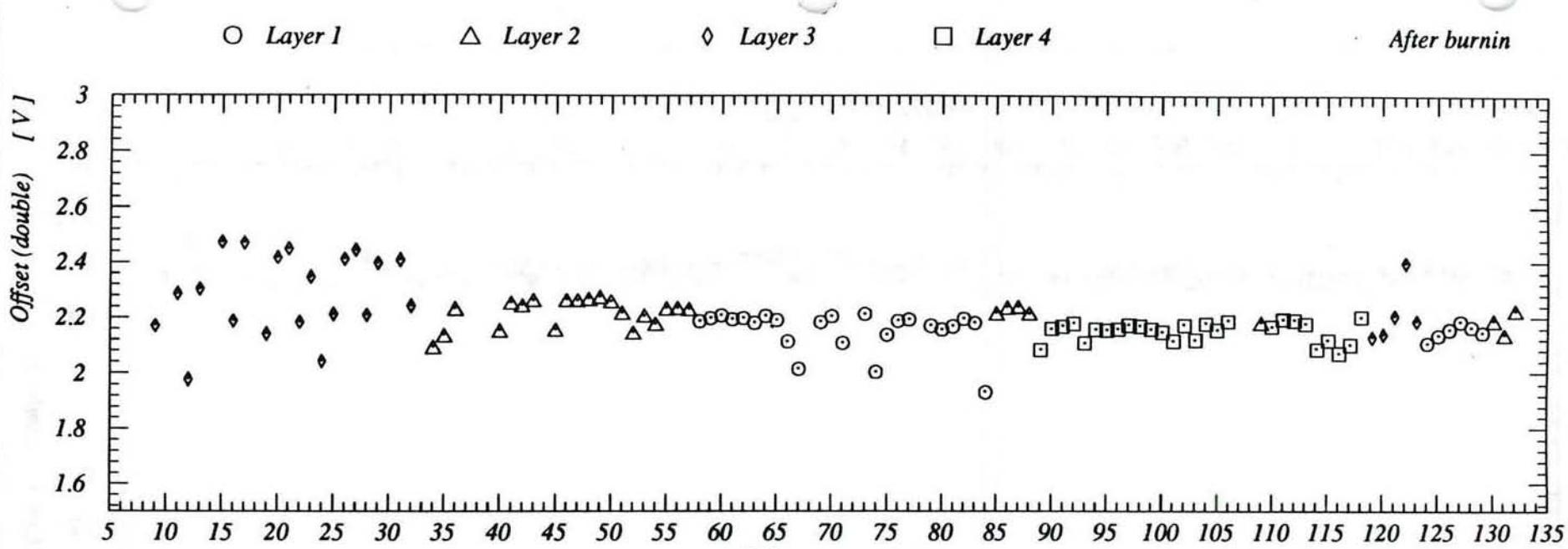


Figure 24a

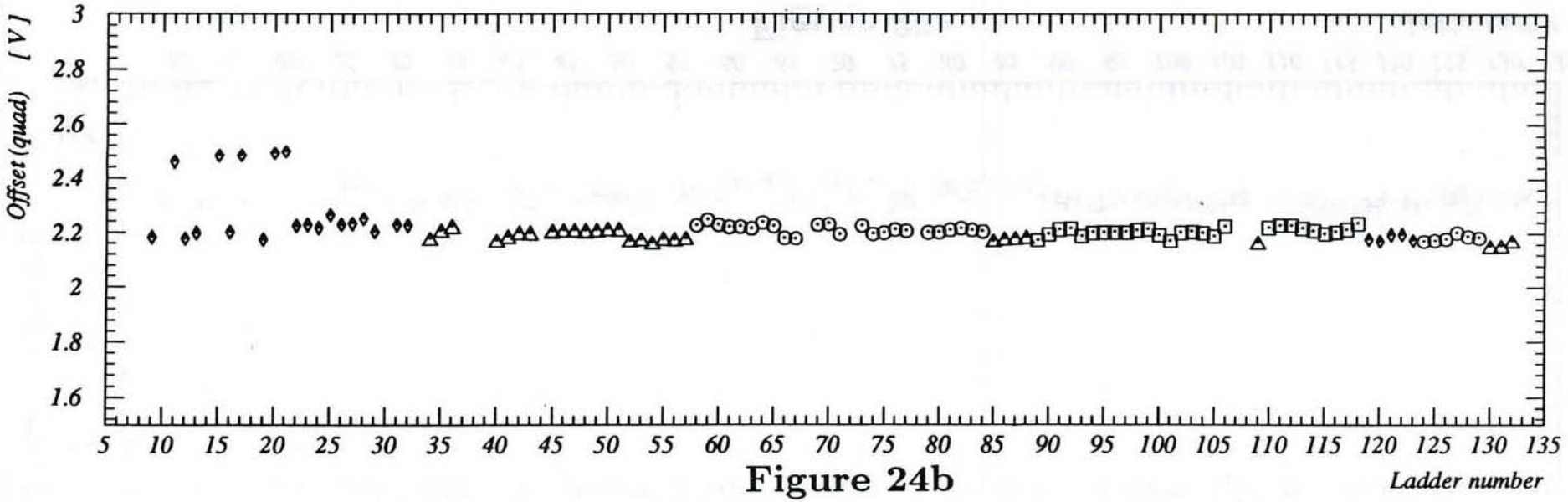


Figure 24b

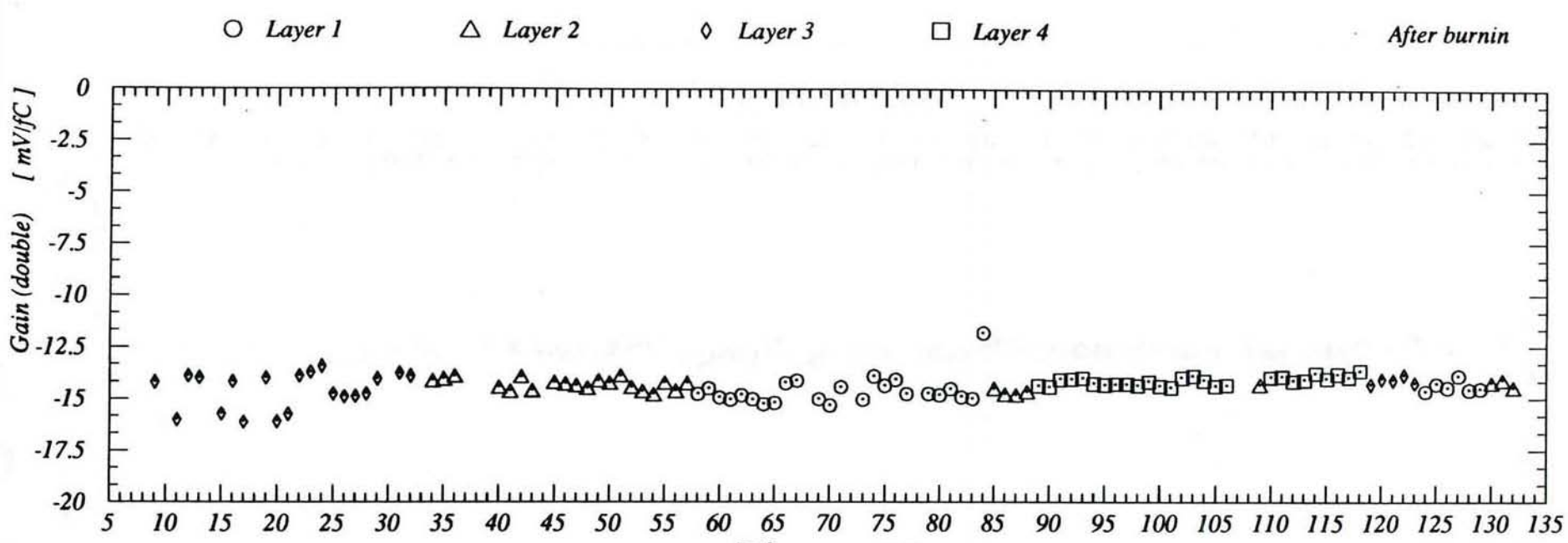


Figure 25a

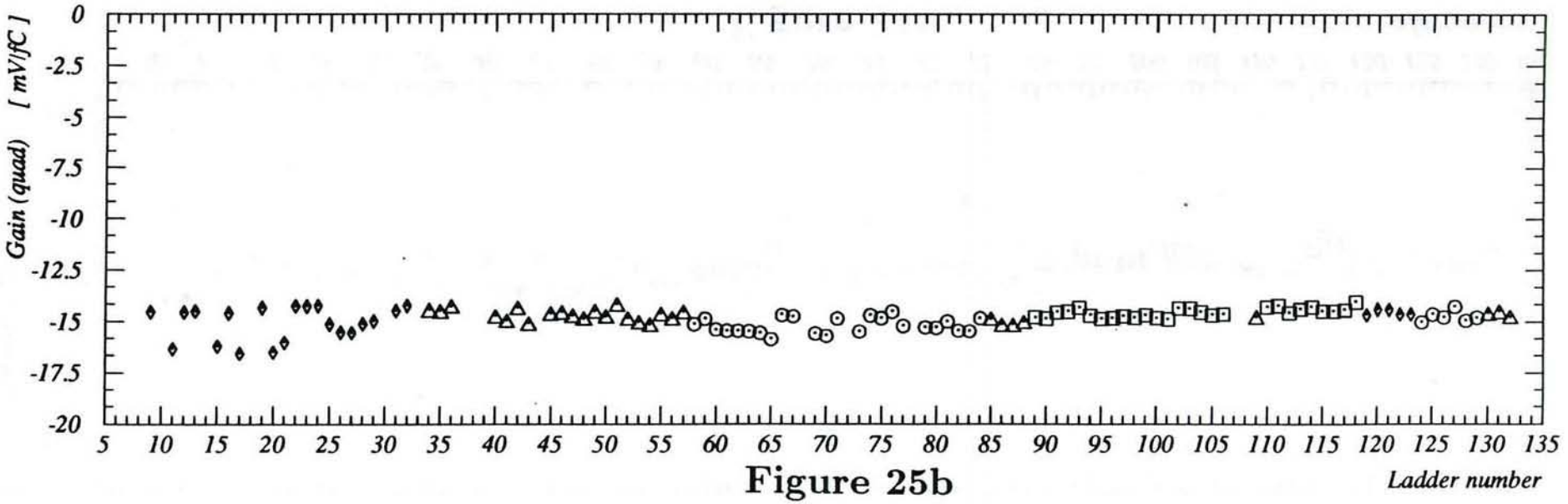


Figure 25b

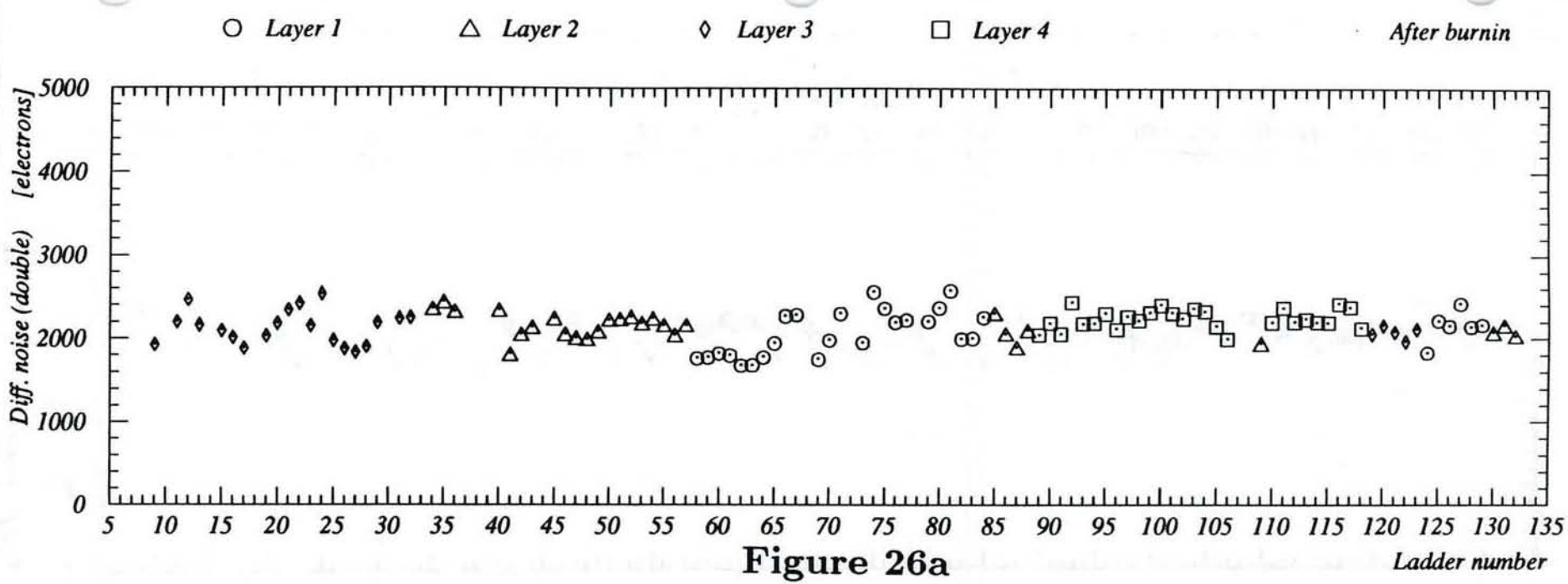


Figure 26a

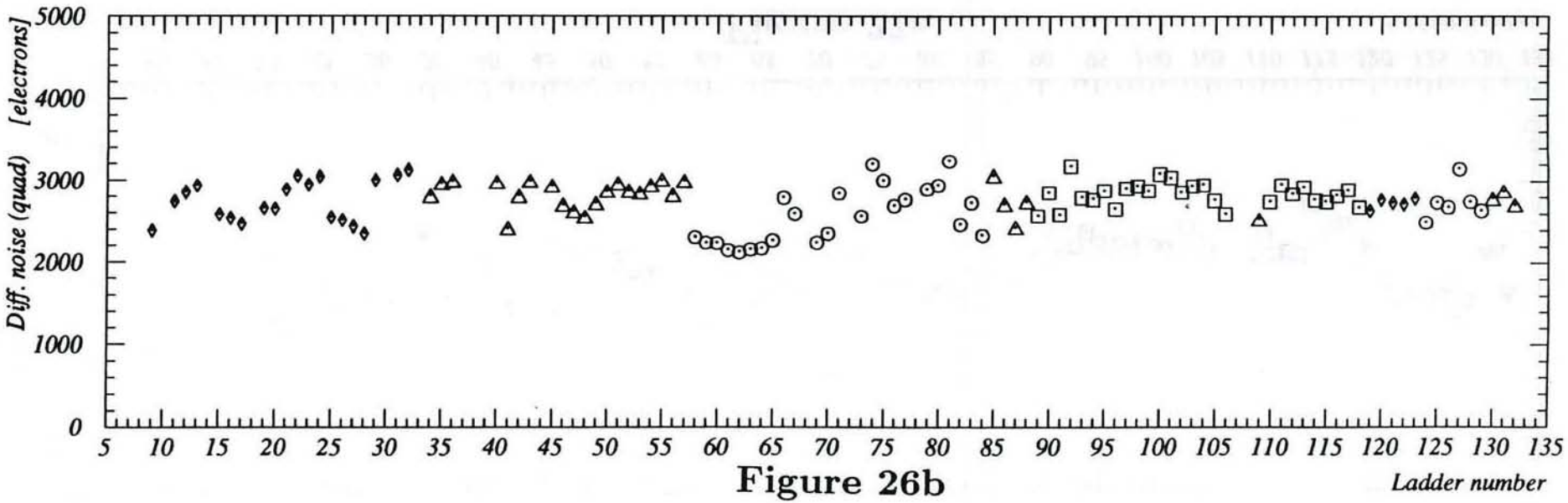


Figure 26b

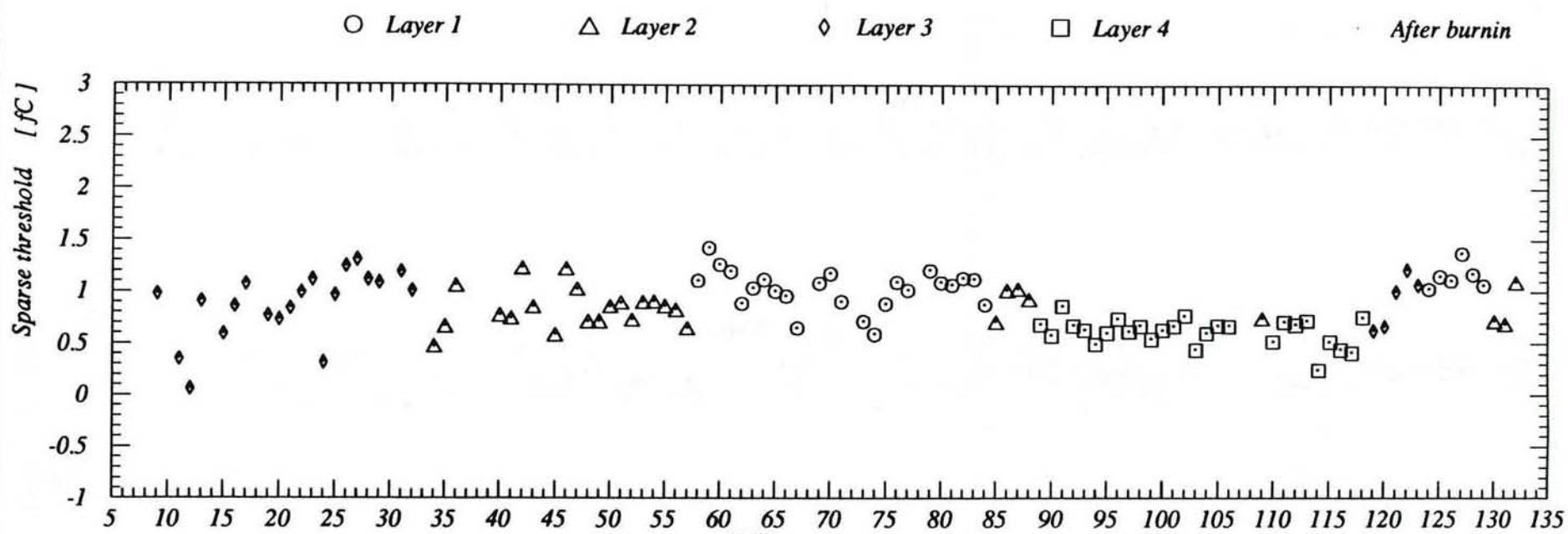


Figure 27a

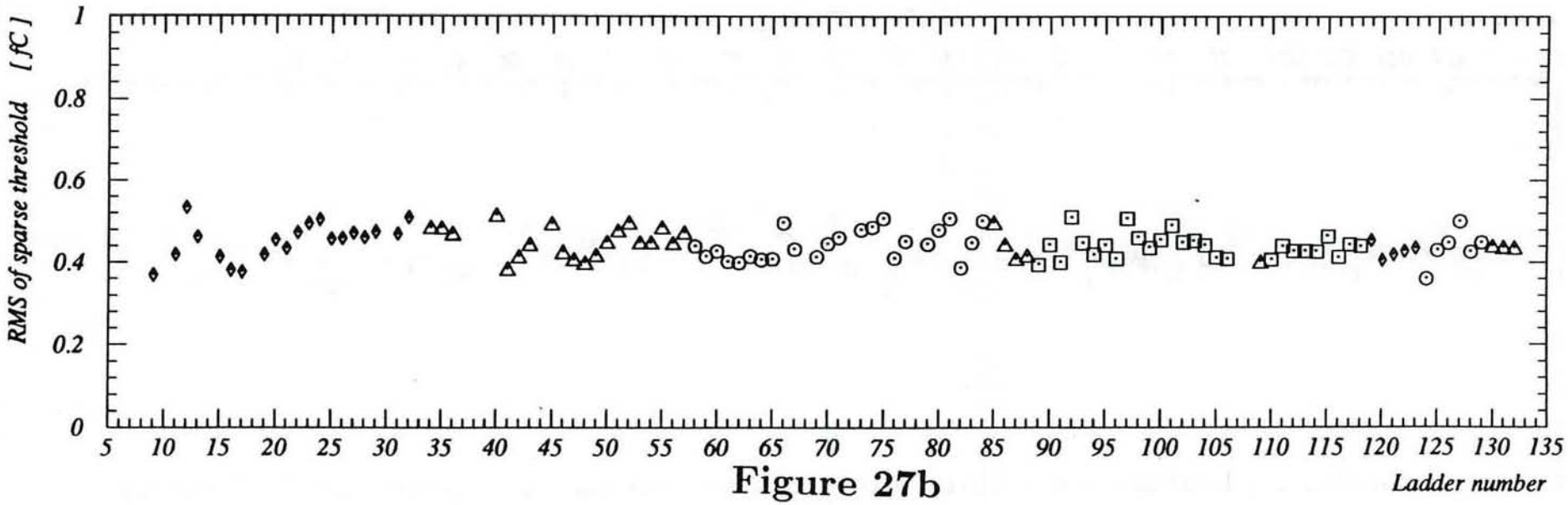


Figure 27b

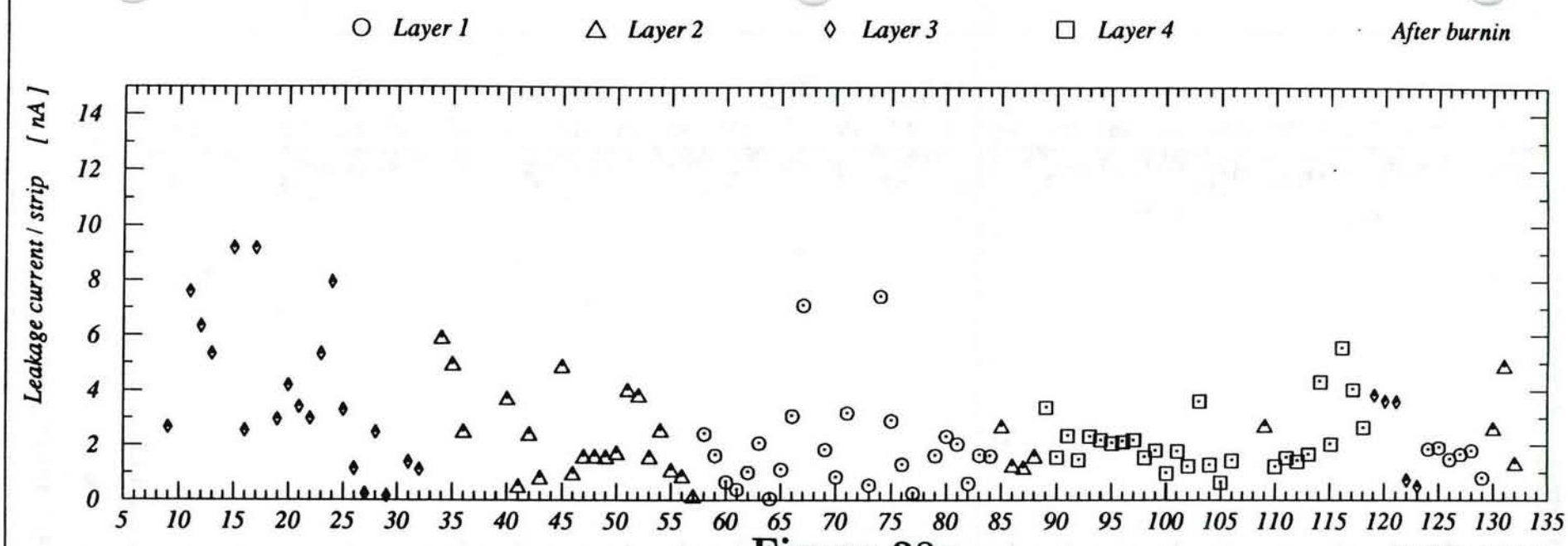


Figure 28a

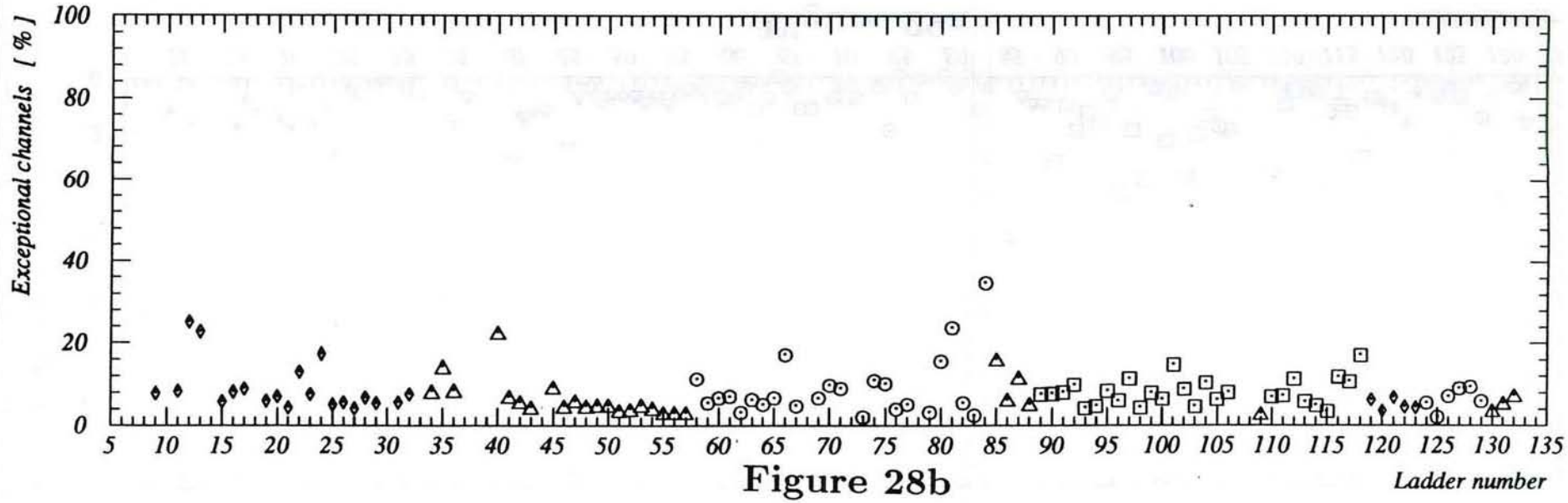


Figure 28b

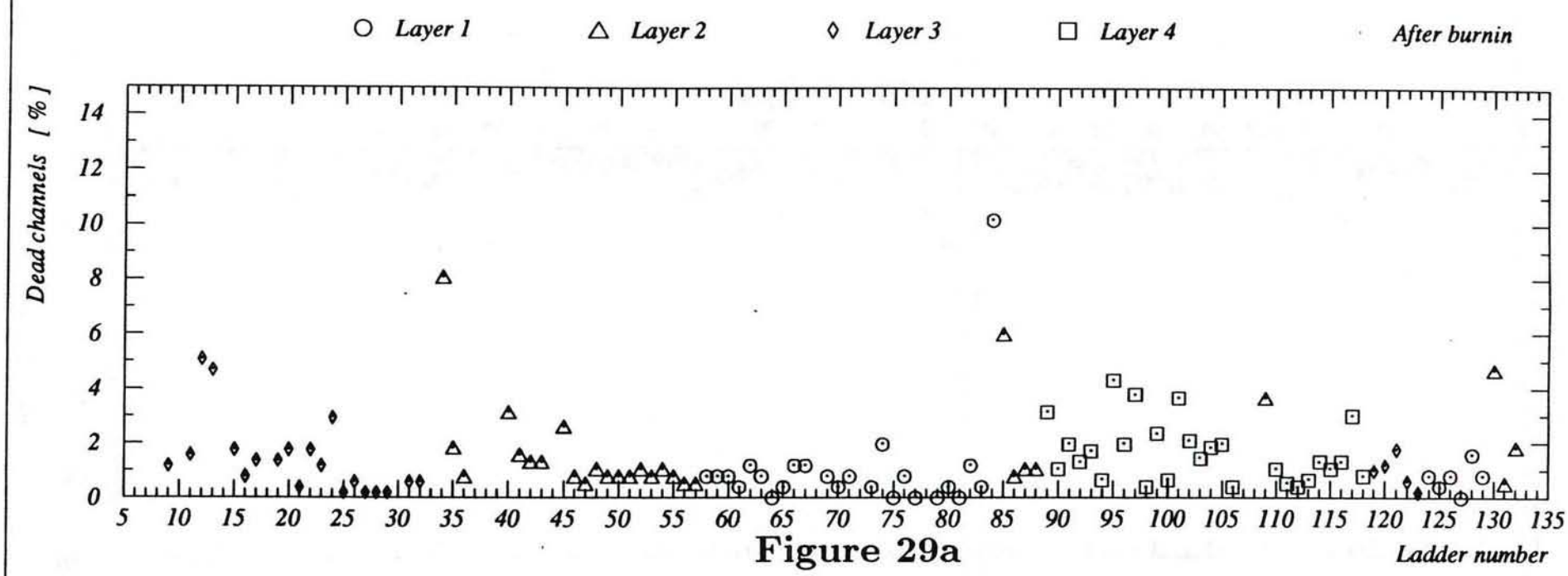


Figure 29a

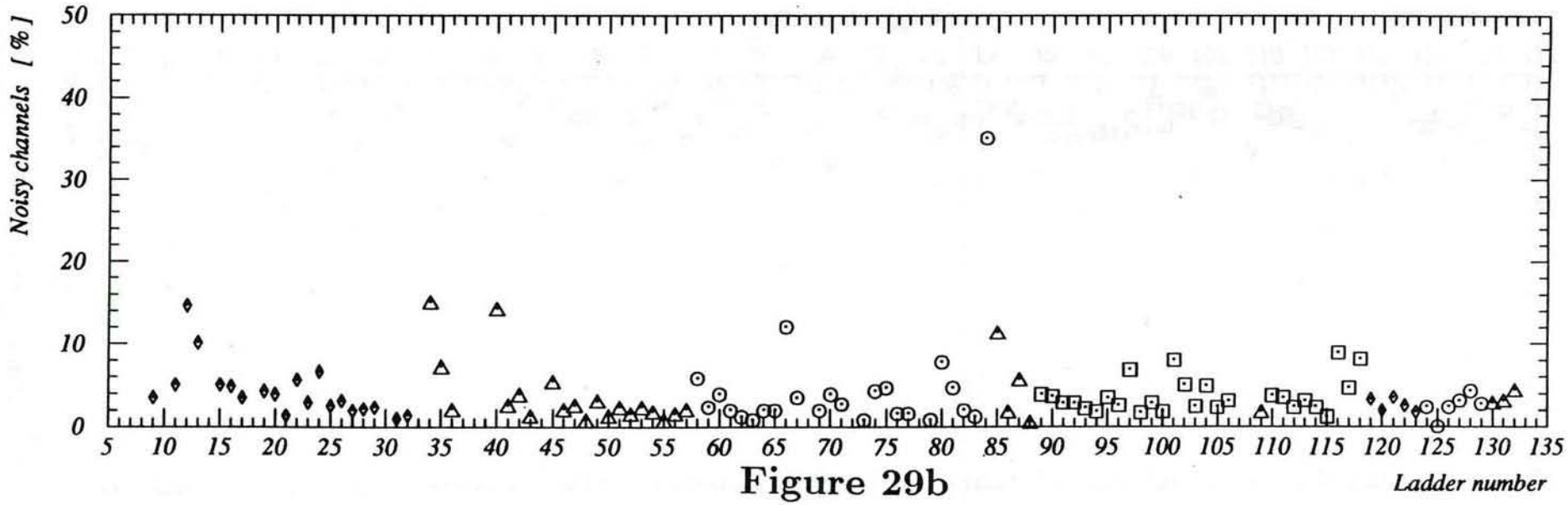


Figure 29b

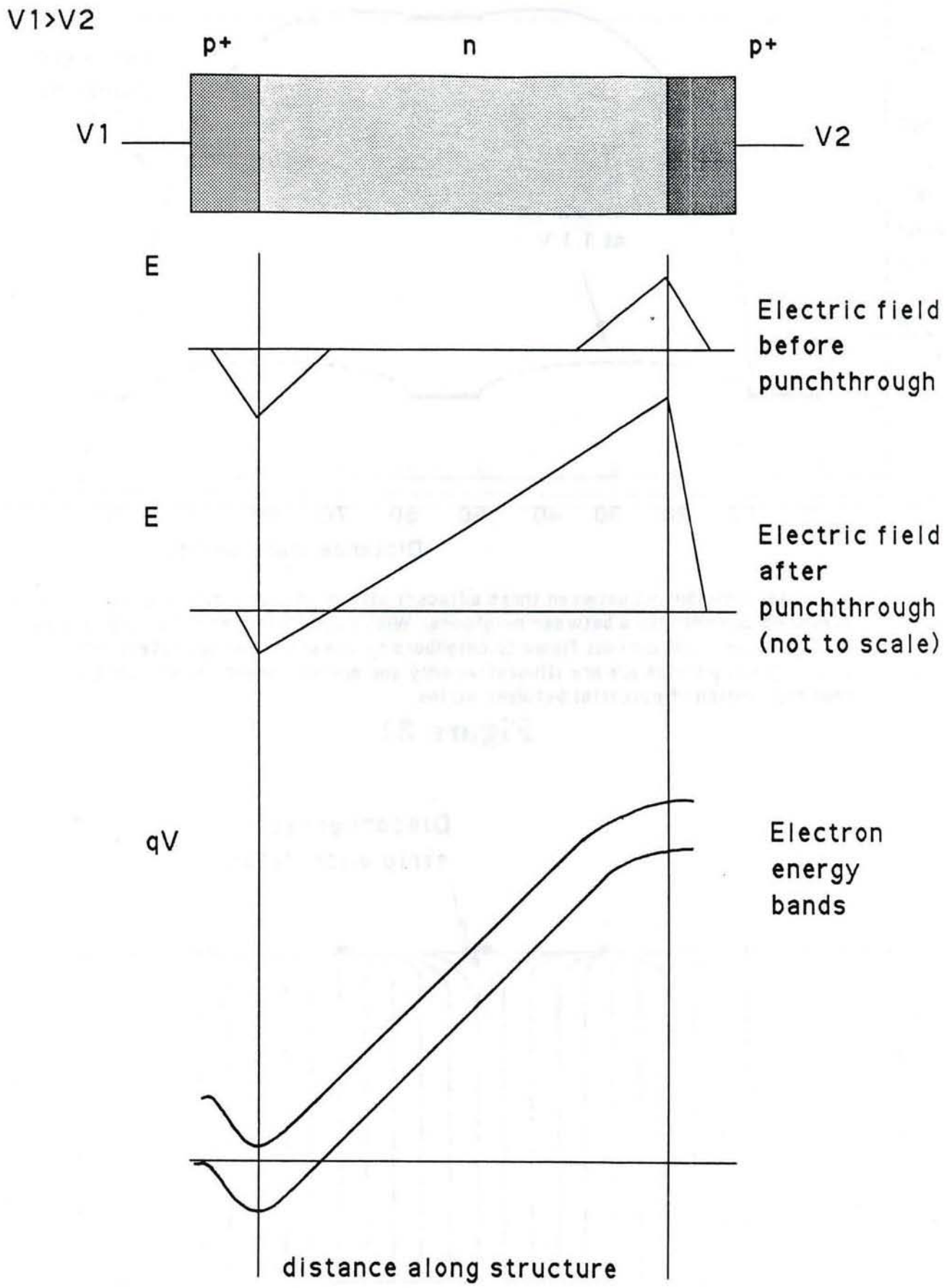
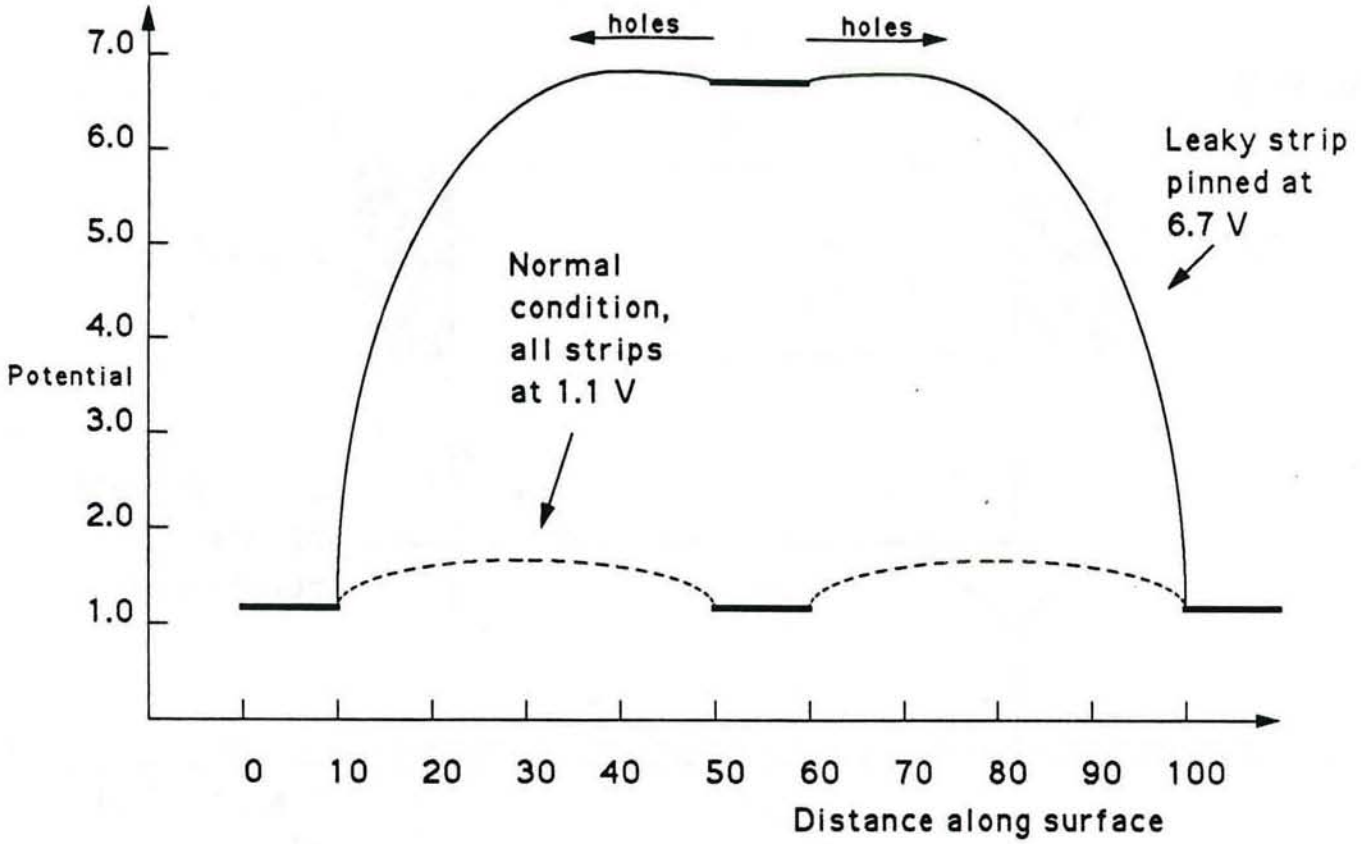

V1>V2
p+
n
p+
V1
V2
E
Electric field
before
punchthrough
E
Electric field
after
punchthrough
(not to scale)
qV
Electron
energy
bands
distance along structure

Figure 30



Potential distribution between three adjacent strips. With all strips at 1.1 V (dashed curve) no current flows between neighbors. With center strip at 6.7 V it becomes forward biased and current flows to neighbors by the punchthrough effect. Note: curves joining strips are are illustative only and are not meant to represent any real calculation of potential between strips.

Figure 31

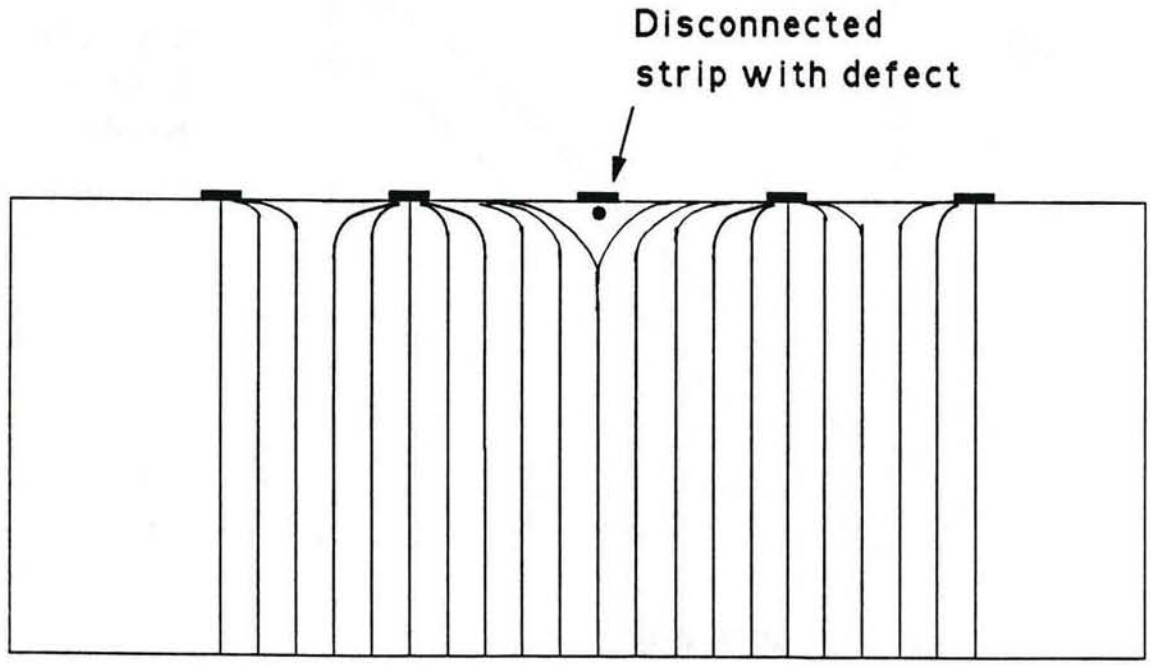


Figure 32

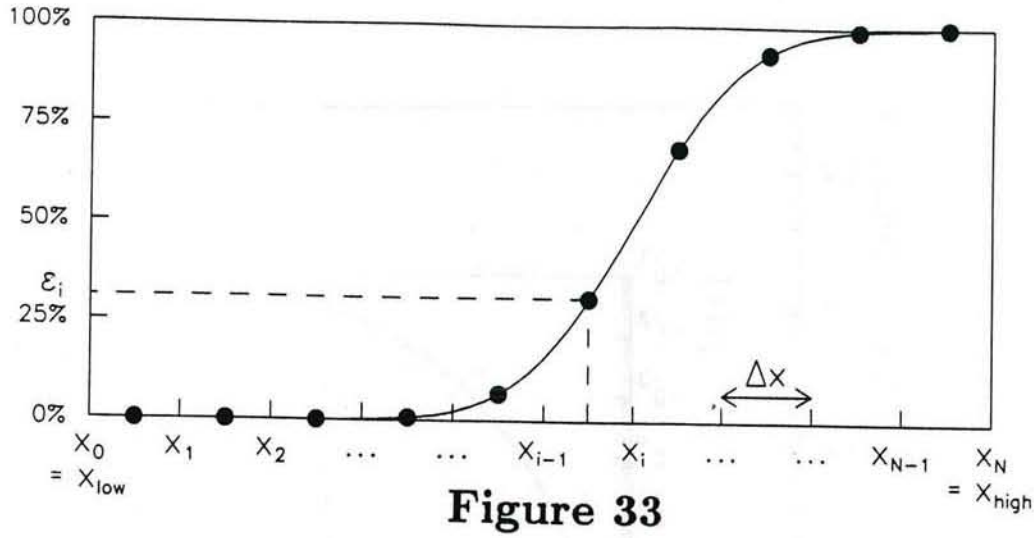


Figure 33

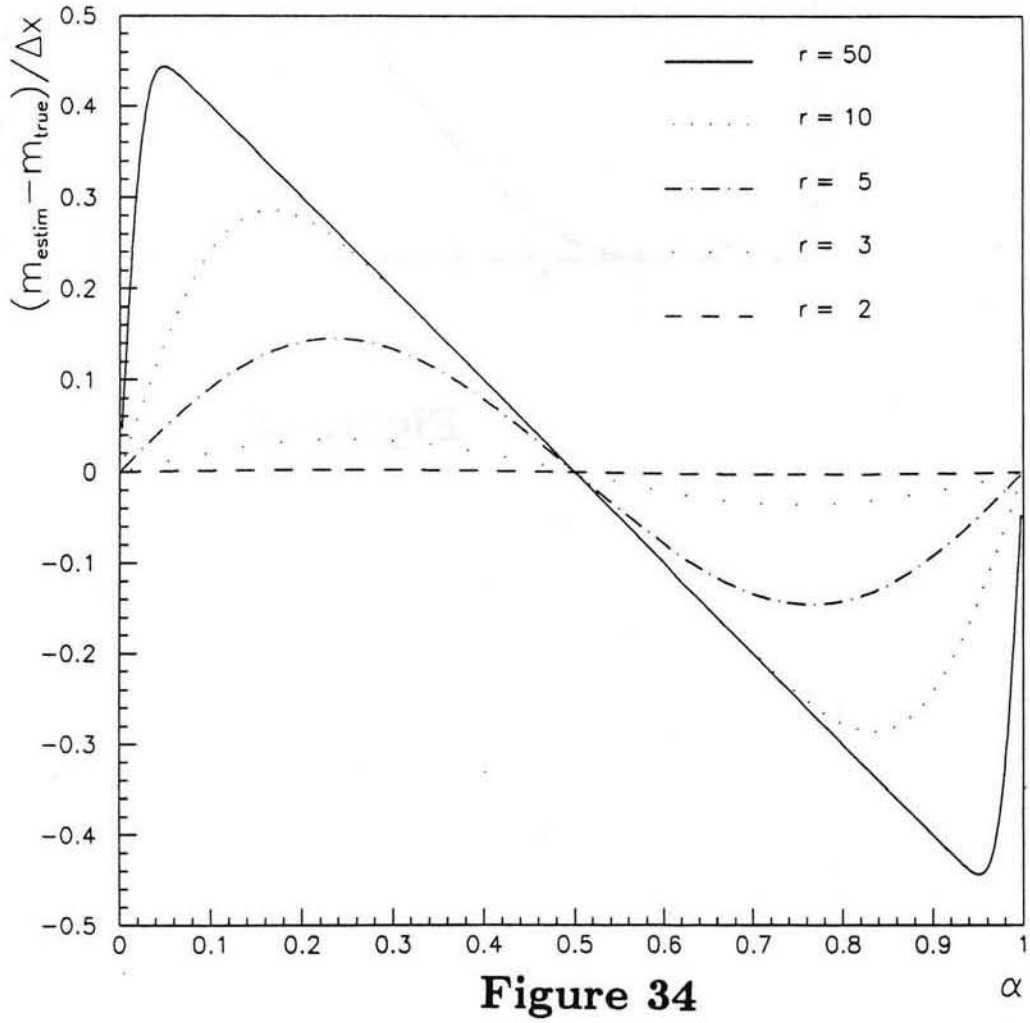


Figure 34

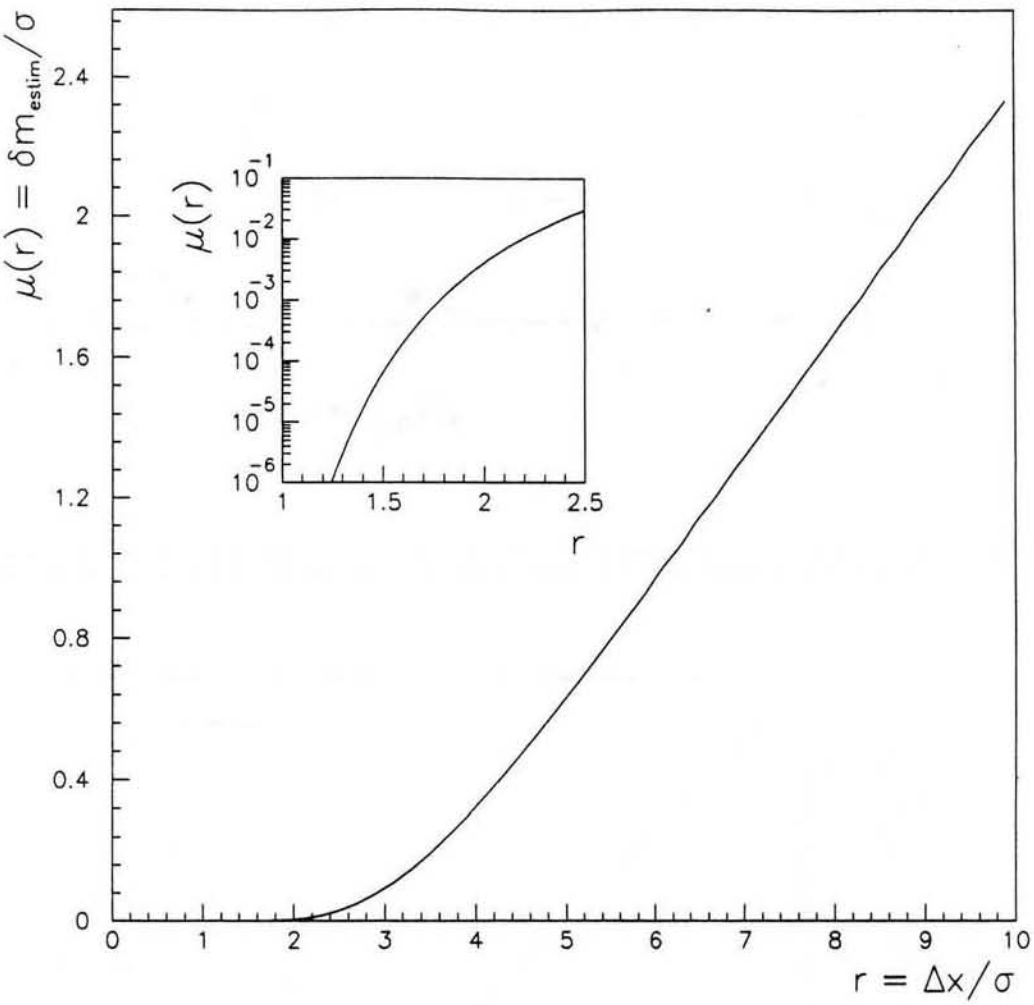

$\mu(r) = \delta m_{estim}/\sigma$
2.4
2
1.6
1.2
0.8
0.4
0
0
1
2
3
4
5
6
7
8
9
10
$r = \Delta x/\sigma$
$\mu(r)$
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
1
1.5
2
2.5
r

Figure 35