PERFORMANCE OF A CMOS MIXED ANALOGUE-DIGITAL CIRCUIT (APVD) FOR THE SILICON TRACKER OF CMS

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Abstract

The APVD is a rad-hard front-end readout integrated circuit in the DMILL technology for the silicon tracker of CMS.
The circuit contains 128 identical analogue channels, each one composed of a low noise preamplifier, a CR-RC shaper, a 160 cells deep analogue pipeline and a signal processing stage. A deconvolution filter at this point recuperates the initial fast response function of a silicon detector and confines it to one LHC bunch crossing. The 128 analogue channels are read-out by a serial output via a high-speed analogue multiplexer. Slow control is implemented on the chip using an I2C serial bus interface, which configures the chip and runs the internal calibration system. A dedicated block generates all the biases.
This paper presents the measured performance of the first APVD prototype.

1. INTRODUCTION

The CMS inner tracker contains approximately 10^7 channels from both silicon detectors and Micro-Strip Gas Chambers (MSGC). The main target is to build a system with minimum power consumption, minimum material and sufficiently low noise. An analogue readout system has been chosen for the following reasons: robustness, better resolution and easiness of testability. Existing rad-hard technologies have to be employed to meet the LHC time schedule.
The APVD is the first prototype for CMS of a rad-hard front-end readout chip developed in the DMILL process. It has been designed by a French-British collaboration of several laboratories. The design of the APVD is based both on the topology of the front end chip APV6 [1] fabricated in the Harris AVLSIRA technology and the design experience of the front-end chip FILTRES [2] developed in the DMILL process.
The DMILL technology uses an SOI substrate and integrates monolithically rad-hard, low noise, analogue-digital CMOS, JFET and bipolar transistors. This technology allows the design on the same chip of both analogue and digital fast circuits.
Submitted in summer 1997, the prototype of the APVD has been received in the beginning of 1998. Due to unexpected high values of one resistor type, the chip has been re-fabricated in a second run and has been received in September, two weeks before this conference.
After a brief introduction of the main design features of the APVD, this paper will present the measured performance of the first run.

2. APVD DESIGN FEATURES

The block diagram of the APVD [3] is shown in Figure 1.

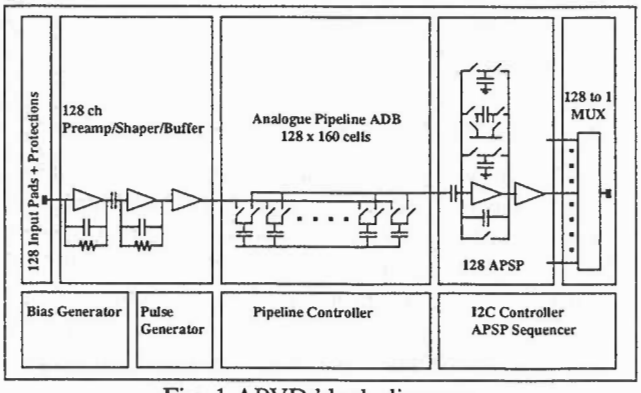


Fig. 1 APVD block diagram

The 128 analogue input pads are situated on the left-hand side of the chip. The silicon strip detectors are connected to the input pads by ultrasonic wire bonding. Standard DMILL ESD (Electro-Static Discharge)

protections scaled down to one third of their size have been added to the input pads. The current pulse is transformed into voltage by a charge preamplifier and then amplified and filtered by a CR-RC shaper. The signals are buffered by a source follower connected to the analogue pipeline ADB (Analogue Delay Buffer), where the signals are sampled and stored at 40 MHz. On receipt of a first level trigger, the signals are read and processed by the APSP (Analogue Pulse Shape Processor). The analogue output current signal is read-out serially at 20 MHz. The control of the circuit is provided by several blocks. On the right-hand side, the I2C interface allows programming of the main parameters of the circuit for the slow control and also generates the signals to cycle the APSP. The pipeline control logic controls the writing and the reading sequences of the analogue pipeline. The addresses of the tagged cells are stored in a FIFO. Further on the left, there is a pulse generation unit that internally generates calibration pulses for testing the analogue chain. The bias generator block is a set of RAM based registers and DAC's, and generates all the bias currents and control voltages for the analogue blocks and some digital patterns for the calibration pulse generator. It is programmed through the I2C controller. All digital processing of the chip and its pad layout are identical to the APV6.

3. TEST BENCH DESCRIPTION

An electronic test bench has been developed to characterise the chip (Figure 2).

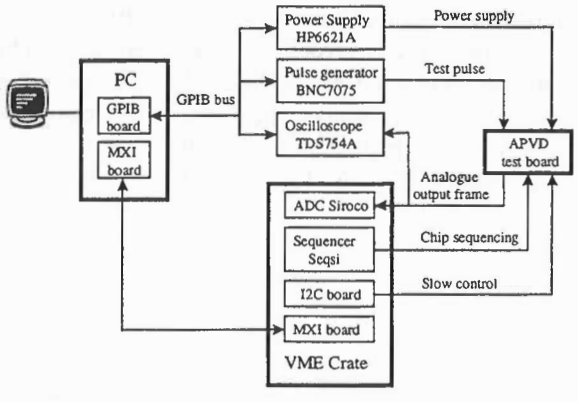


Fig.2 APVD test bench

This test bench is based on a PC equipped with LabVIEW, who drives a VME crate through a high rate MXI link, and commands measurement and control instruments via a GPIB bus.
In the VME crate, an I2C board allows the slow control of the chip and a sequencer board sends clock and commands to the chip under test via two differential links.
A precise electric charge is sent to a selected input channel of the chip by a pulse generator, whose delay is controlled via the GPIB.
After trigger reception, the APVD chip sends serially an output frame containing 128 multiplexed analogue values to an oscilloscope or to an ADC board [4] located in the VME crate for measurement. The data are then read and treated by the PC.
Several test programs developed under LabVIEW allow a complete characterisation of the chip.

4. BIAS AND INTERNAL CALIBRATION

There are seven analogue biases (4 currents and 3 voltages) to control the analogue chain (preamplifier, shaper, source follower and analogue processor). These currents are obtained in the bias generator by mirroring a reference current with different ratios controlled by the I2C interface. For the voltages, an internal conversion resistor is added. The reference current can be generated via an internal or an external resistor. The value of the internal resistors on the first run of the APVD was out of specification; an external reference current has to be used.
Test pads on the chip permit the measurement of the biases sent to the analogue chain. Figures 3 and 4 show respectively current and voltage biases as function of the slow control I2C code. These biases cover the whole application range with good linearity and the spread from chip to chip is below 2%.

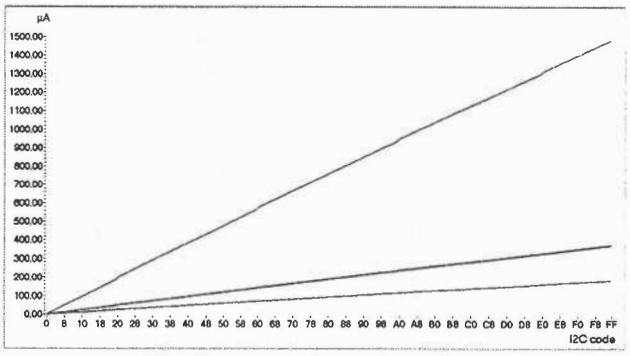


Fig. 3 current biases linearity

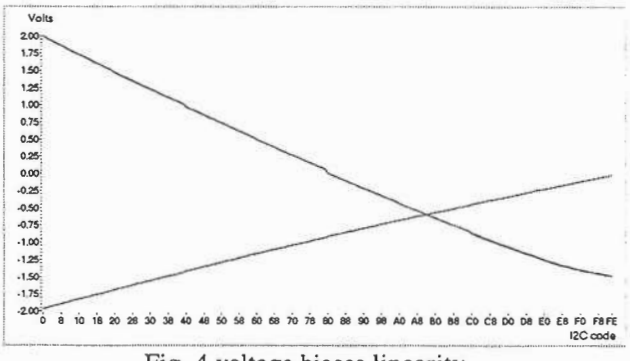


Fig. 4 voltage biases linearity

The internal calibration system can inject calibration charges up to 10 MIPs to all inputs of the chip through eight calibration lines. This allows the measurement of the amplifier pulse shape on the chip.
A request pulse sent by the APVD sequencer via chip sequencing link sets a calibrated pulse to selected channels. A trigger with an appropriate latency starts the read-out of the chip. Moving the calibration request by steps of 25 ns, a coarse reconstruction of the shape can be made. In order to obtain a better resolution, the calibration pulse can be delayed by steps of 3.125 ns by controlling the I2C programmed internal delay line.

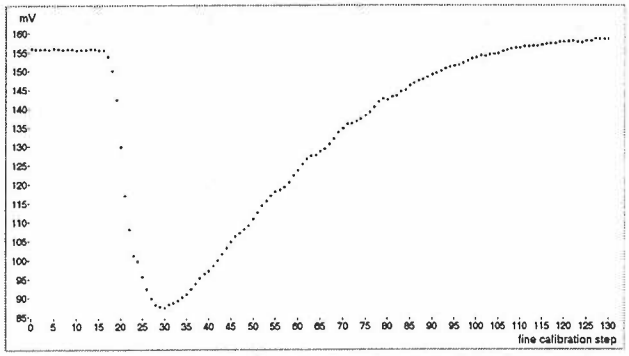


Fig. 5 Amplifier pulse shape generated by internal calibration pulse corresponding to about 2 MIPs

Figure 5 gives a pulse shape obtained with the internal calibration system. The curve is not totally smooth due to slightly larger internal delay line step.

5. ANALOGUE PERFORMANCES

Operating at 20 MHz, a 128 to 1 three-level multiplexer drives the analogue output current of the chip. The analogue data are preceded by a 4-bit header where the third bit indicates an internal logical error and an 8-bit address corresponding to the triggered pipeline column.
Although it is impossible to totally suppress the coupling between the analogue output frame and logical signals in the analogue multiplexer, precise sampling in the ADC reduces additional noise contribution.

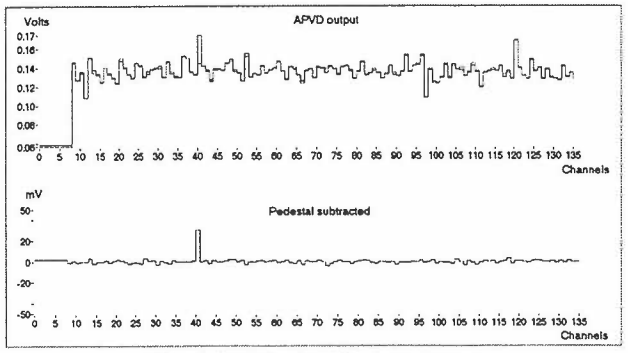


Fig.6 APVD output data frame

Two APVD data frames with and without a one MIP signal are shown in the top graph of figure 6. Dispersion of channel pedestals leads to a channel to channel non-uniformity. By subtracting pedestals, a one MIP signal injected on one channel can be clearly discriminated as shown in the bottom graph of figure 6.
An instability of the analogue output signal has been observed. It is due to a feedback loop via an insufficient ground connection in the front-end amplifier circuit. In order to cut this feedback loop, a modification by focussed ion beam technology has been performed on six chips. The measurement of the modified chips shows a better stability. Reducing current bias in the shaper stage by 20% allows to run the chip quietly.
Using the external pulse generator to inject a charge at an input of the APVD and changing its delay, the average amplifier pulse shape can be obtained both in peak and in deconvolution modes.
The average amplifier pulse shape in peak mode can be adjusted to an ideal CR-RC curve by changing the circuit biases as shown in figure 7.

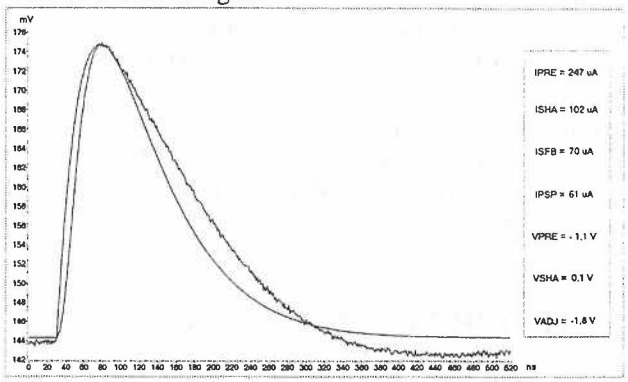


Fig. 7 Amplifier pulse shape in peak mode with -1MIP input

The difference in rise time between the two curves is typically due to the electronic response time of the chip. An undershoot of a few per cent has also be observed. An adjustment of the shaper parameters is needed to suppress this phenomenon in the next design. Nevertheless the shape is close to an ideal CR-RC.

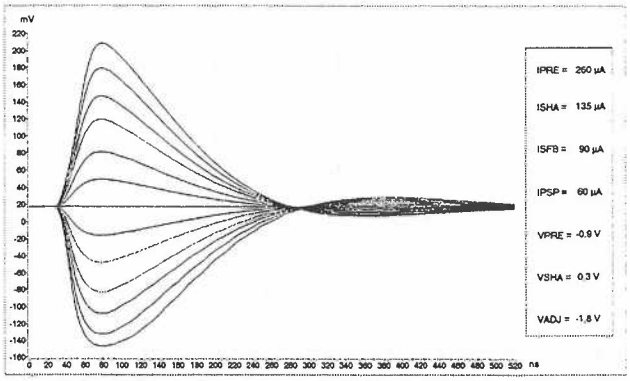
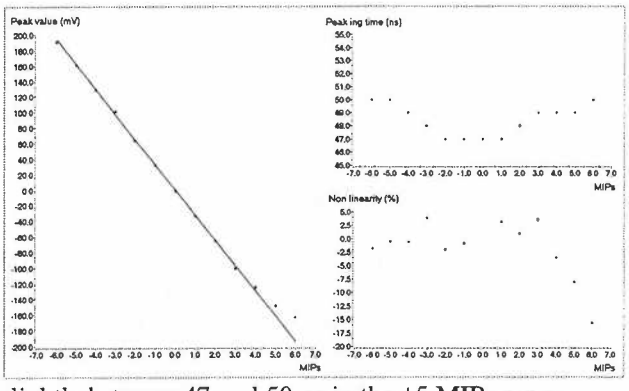


Fig. 8 Amplifier shapes versus input MIPs in peak mode

The linearity tested in peak mode over a dynamical range of ±6 MIPs is shown in figure 8.

Figure 9 shows a typical measurement from a set of different channels in the six modified chips. In peak mode the gain is 95 μA/MIP and the non-linearity is less than 8 % over ±5 MIPs range. The peaking time varies



slightly between 47 and 50 ns in the ±5 MIPs range.

Fig. 9 Linearity in peak mode

It should be noted that the amplifier pulse shape depends slightly on input capacitance. A gain variation less than 5% with a loss of 9 ns in peaking time is observed when a capacitance of 15 pF is added to a PCB line capacitor around 5 pF.

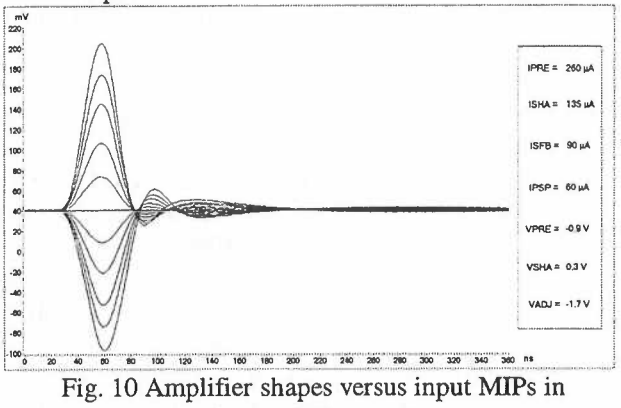
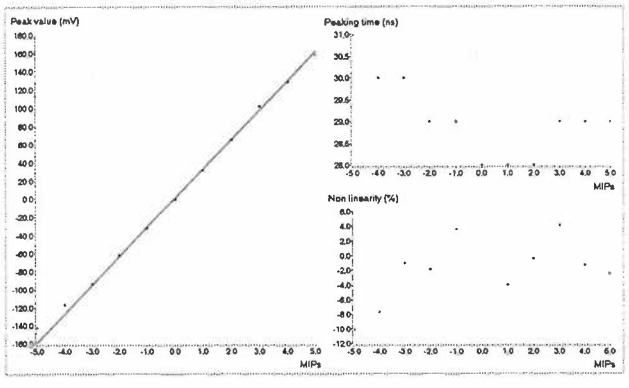


Fig. 10 Amplifier shapes versus input MIPs in deconvolution mode

Figure 10 gives the average shape of the deconvolution filter. The small undershoot is due to sensitivity of the deconvolution method to a non-ideal CR-RC amplifier response. A gain of 90 μA/MIP over ±5 MIPs is



obtained. The non-linearity is less than 10 % with correct rise time (Fig. 11).

Fig. 11 Linearity in deconvolution mode

6. NOISE PERFORMANCE

Two different noise measurements have been performed in peak and deconvolution modes. Using an oscilloscope to read-out the analogue pedestal of a selected channel in several thousand samplings with a precision of 100 ps, a Gaussian distribution of amplitude can be collected. The ENC of the APVD can then be calculated from this distribution. This method allows an accurate measurement of ENC. Figure 12 shows a typical noise performance of the APVD in peak mode and deconvolution mode respectively.

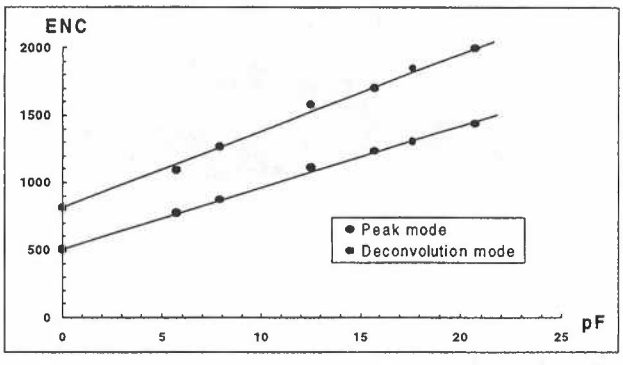


Fig. 12 APVD noise performance

The average values of the measured noise figures are:

505 + 45 e⁻/pF Peak mode

870 + 53 e⁻/pF Deconvolution mode

The noise measurement in peak mode agrees with our simulation. In deconvolution mode the noise is higher than in peak mode mainly due to multi-sampling. The APSP enters three times in this mode is also a possible noise source[5].

7. PIPELINE AND PROCESSOR PERFORMANCE

By changing the T1 trigger timing in 25 ns steps, a complete scan of the pipeline can be obtained. A typical outcome of this test is shown in figure 13 where the pedestal is plotted as a function of both the channel and the cell number.

From this measurement, three points can be verified:

Firstly, defective cells of the pipeline, caused by the technology problems or the sensibility of our design to the technology, can be correctly defined. We also observe a dispersion of pedestals from channel to channel.

Secondly, the contribution of the cell to cell fluctuation to the total noise can be measured and is less than 200 rms electrons. This value is negligible when added in

quadrature to the input noise obtained for a realistic detector capacitance.
Finally, by subtracting two measurements with and without input internal calibration pulse, channels can be identified in which preamplifier or shaper have a problem. This measurement allows also a check on the uniformity of the gain from channel to channel. From nearly 3000 channels in all tested chips, around fifteen preamplifier-shapers were defective. A good uniformity has been obtained.

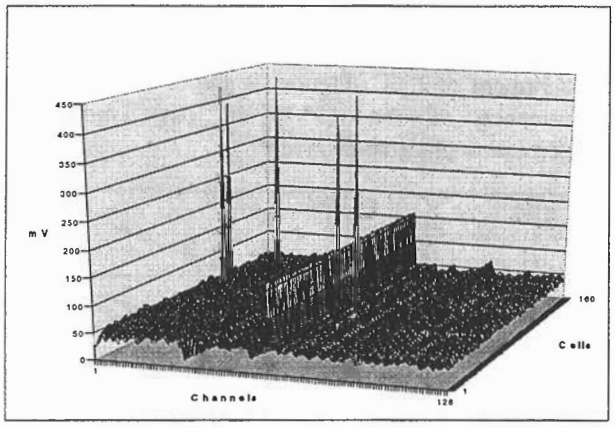


Fig. 13 APVD pipeline performance

Figure 14 represents the Analogue Pulse Shape Processor (APSP) performance. There are two curves on the figure. The first is directly obtained by using the deconvolution mode. Using the three-deconvolution weights and the amplitudes of three corresponding points measured in peak mode, the second curve was obtained. We can see that the APSP works correctly.

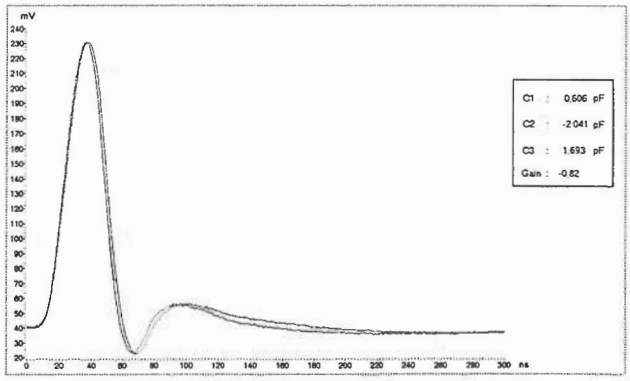


Fig. 14 APVD APSP performance check

8. CONCLUSIONS

The APVD is a 128-channel front-end readout integrated circuit in the rad-hard DMILL technology for the silicon tracker of CMS. The first version of the chip has been evaluated. The internal control system works correctly and a good analogue performance of the chip has been found. This version of the APVD is now under beam test at CERN for silicon detector. In spite of good functionality of the APVD, several potential problems, such as instability in certain bias conditions, sensitivity to technology variation, have been found. Further studies will be made to improve the APVD performance.
Evaluation of the chip in its environment will give us more conclusive information. A temperature test as well as an irradiation measurement will be performed as soon as possible. In order to evaluate large quantities of chips an automatic on wafer test bench will be developed.

ACKNOWLEDGEMENTS

We would like to thank the technical staff of our laboratories for their continuous and valuable support. In particular, we thank O. Runolfsson for his kind and very professional support of bonding many chips on their respective test-boards.

REFERENCES

[1] M. French *et al.*, APV6-RH A 128 Channel Read-out Chip For The Silicon Tracker In CMS, Proceedings of the 2nd Workshop on Electronics for LHC Experiments, Balaton (Hungary), September 23-27, 1996, pp.463-467

[2] F. Anstotz *et al.*, "Front-End Read Out Electronic Development for Microstrip Detectors in CMS: FILTRES", Proceedings of the 2nd Workshop on Electronics for LHC Experiments, Balaton (Hungary), September 23-27, 1996, pp.469-472

[3] R. Turchetta *et al.*, "APVD: a CMOS Mixed Analogue-Digital Circuit for the Silicon Tracker in CMS", Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, September 22-26, 1997, pp.163-167

[4] W. Dulinski, "ADC-Siroco version June 1998", Internal communication

[5] M. Raymond *et al.*, "The APV6 Readout Chip for CMS Microstrip Detectors", Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, September 22-26, 1997, pp.158-162