Development in a Novel CMOS Process for Depleted Monolithic Active Pixel Sensors

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Abstract*–Recent advancements in CMOS technologies enable Depleted Monolithic Active Pixel Sensor (DMAPS) realizations by exploiting high resistivity and/or high voltage biasing to deplete a large active sensing volume. DMAPS have emerged as a promising alternative for particle detection in high energy physics due to their low cost, reduced manufacturing complexity and high granularity. In the framework of the ALICE Inner Tracking System (ITS) upgrade, prototype sensors have been designed and characterized in the TowerJazz 180nm standard CMOS imaging process and in a novel modification of this process to achieve full depletion. Measurement results demonstrate that the sensors manufactured using the modified process are fully functional even after a dose of $10^{15} n_{eq}/cm^2$, which is the expected NIEL of the outer layers of the ATLAS Inner Tracker (ITk) during the future High Luminosity Large Hardon Collider (HL-LHC) operation. Based on these encouraging results, two highly granular, low power DMAPS chips with different readout architectures have been designed and are being proposed for the ATLAS ITk upgrade.

I. Introduction

MONOLITHIC Active Pixel Sensors (MAPS) that combine the sensor and readout electronics on the same silicon crystal have been successfully used in low radiation environments such as the STAR experiment at RHIC [1]. While in the design of hybrid pixels the sensor and the readout electronics can be optimized separately to cope with high radiation and high input rates, monolithic implementations were limited by the characteristics of the available CMOS processes. The key to radiation tolerance regarding charge collection efficiency and signal rise time is a strong electric field in the depleted active sensing volume that ensures charge collection by drift. The depletion depth of the sensing volume is enhanced by increasing resistivity and reverse biasing voltage [2].

Recently, CMOS imaging technologies have evolved independently from high energy physics, driven mainly by the smartphone market demands. Commercial processes offering high resistivity substrate and/or high breakdown biasing voltage can be exploited to design fully Depleted Monolithic Active Pixel Sensors (DMAPS). Additionally, multiple nested wells can be manufactured that allow complex circuits to be designed using both NMOS and PMOS devices. The development of radiation tolerant and high rate capable monolithic pixel devices for high energy physics experiments can significantly reduce cost since the complex assembly steps that are mandatory in hybrid detectors and include flip-chipping and bump-bonding are no longer needed.

In 2025, the Large Hadron Collider (LHC) will undergo a major upgrade and the luminosity, thus the hit rate and the particle radiation fluence will be increased by an order of magnitude [3]. To cope with these stringent requirements, a new tracking system (ITk) will be installed in the ATLAS experiment. A dedicated ATLAS CMOS development programme has been established to design, characterize and explore the feasibility of monolithic pixel sensors for the ITk upgrade.

Prototype monolithic sensors that were originally developed for the ALICE Inner Tracking System (ITS) upgrade in the TowerJazz[1] 180nm imaging process [4], combine small pixel size with low sensor capacitance and low analog power consumption. The sensitive volume of the sensor in the standard process is not fully depleted, and diffusion plays an important role in the charge collection. This leads to sufficient radiation tolerance for ALICE but not for more demanding applications. By employing a novel process modification [5], the whole pixel sensing volume is depleted and the sensor remains fully functional up to fluences of $10^{15} n_{eq}/cm^2$, which is the expected fluence in the ATLAS ITk outer layers.

These promising results encouraged the development of two large scale monolithic prototype chips for the ATLAS ITk, called "MALTA" [6] and "TJ-Monopix" [7]. TJ-Monopix is based on the well-established, synchronous column drain architecture, while a novel asynchronous readout architecture has been implemented in MALTA.

II. Sensor Design in TowerJazz 180nm Process

The size of the collection electrode is a crucial decision in the design of monolithic pixel sensors. A large deep n-well that also hosts the in-pixel readout electronics can be used as the collection electrode [7]. The short drift path over the entire pixel area, ensures that the trapping probability is small in the

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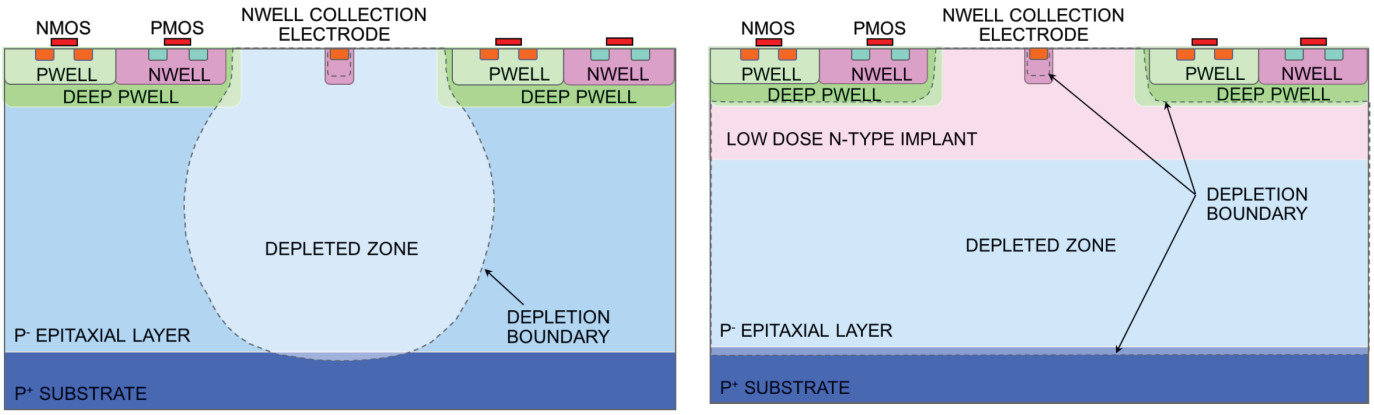


a) b)

Fig. 1. Sensor design in the standard (a) and modified TowrJazz 180nm CMOS process [5]

collection path. However, the sensor capacitance is usually large (~200-400fF) and high analog power consumption is needed to conform with a given signal to noise ratio specification. Furthermore, significant design efforts are required to reduce coupling from the in-pixel circuitry.

A sketch of the pixels designed in the TowerJazz 180nm process is shown in Fig. 1. [5] A small n-well is used as the charge collection node and is placed outside the CMOS electronics area. Therefore, crosstalk interference from the in-pixel digital activity is greatly reduced. The prominent advantage of this implementation is the very small sensor capacitance in the order of a few fF. Low capacitance is translated in high signal amplitude (Q/C) at the input of the Front-End (FE) amplifier and as a consequence in very low power consumption.

The cross section of the standard process is depicted in Fig. 1a. The depth of the high resistivity p-epitaxial layer is 25μm. Charge generated by ionizing particles is collected by the n-well collection electrode. To avoid charge collection at the PMOS transistor n-wells, a deep p-well is used for isolation. The depletion zone is increased by applying a reverse biasing voltage at the substrate. However, it is centered around the collection electrode and cannot extend laterally to the pixel edges. Charge generated in the undepleted region is collected mostly by diffusion and trapping probability is high.

To fully deplete the epitaxial layer, a process modification, shown in Fig. 1b has been developed in collaboration with the foundry [5] and can be implemented without altering the circuit layout. A planar n- implant layer is realized over the full pixel area. The p-n junction that is created, automatically extends the depletion over the whole epitaxial layer, even without reverse biasing. By applying a reverse bias voltage of a few volts (-6V), the depletion region is extended to the boundary of the n-well collection electrode reducing the sensor capacitance to approximately 3fF.

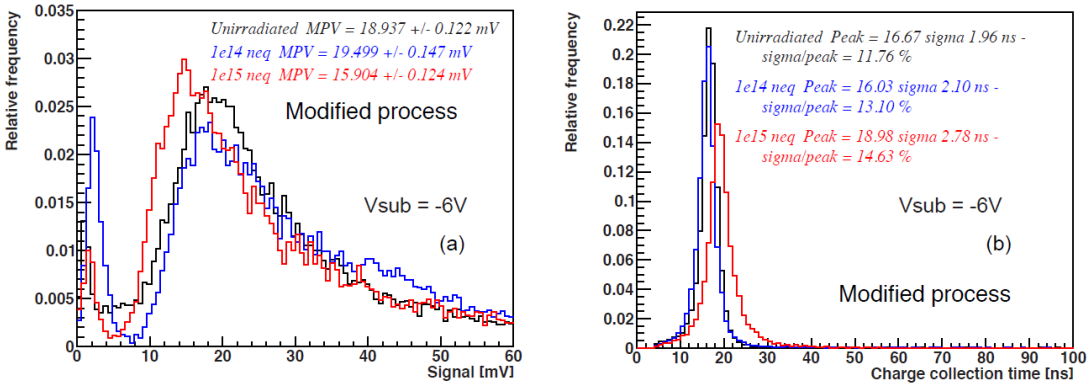
III. Characterization of the Pixel Sensor

Before the development of a large-scale prototype, the sensor performance and radiation tolerance must be measured and the impact of its geometrical parameters is essential to be identified towards an optimal design. The investigator chip was developed in the framework of the ALICE ITS upgrade to enable the characterization of the sensor analog performance [8], [9]. It includes 134 pixel sub-matrices, each consisting of 8x8 active pixels surrounded by dummy pixels. Geometrical parameters that affect the depletion region shape are different for each sub-matrix. Direct access to the analog output of the 64 pixels of each sub-matrix is possible through four source follower stages. Only one sub-matrix can be activated for measurement in any given time and simultaneous measurement of all the outputs of the selected sub-matrix is performed.

To study the effects of radiation damage on the sensor, a number of chips fabricated in the modified process were irradiated in the Triga reactor in Slovenia with total dose up to $10^{14}n_{eq}/cm^2$ and $10^{15}n_{eq}/cm^2$ (NIEL) [8], [9]. Due to the γ-background radiation, the samples also received a total ionizing dose of 100krad and 1Mrad respectively.

A. Characterization Using Radioactive Sources

Measurement of the sensor signal response with radioactive sources can reveal important details of the sensor performance such as gain, signal rise time, charge sharing and resolution. Due to the full depletion of the modified process sensor, significant improvement over the standard process is expected after irradiation to high doses. Electrons generated from a ^{90}Sr source were used to study the Landau spectrum of the charge deposited in the sensor volume and photo-absorption of photons emitted by a ^{55}Fe source were used for calibration [9]. The signal response of a 50x50μm^2 pixel produced in the modified process remains excellent as shown in Fig. 2, even after receiving a total dose of $10^{15}n_{eq}/cm^2$ (NIEL) [8].



a) b)

Fig. 2. Signal response of a 50x50µm^2 pixel manufactured using the modified process. Amplitude distribution for ^{90}Sr source tests is shown in (a) and signal rise time distribution in (b). The black curve corresponds to the signal response before irradiation, the red curve after a total dose of $10^{14}n_{eq}/cm^2$ and the blue curve after a total dose of $10^{15}n_{eq}/cm^2$ (NIEL) [8]

In comparison, no useful signal could be acquired from sensors produced in the standard process after receiving the same radiation dose. The slight decrease of the signal amplitude is a consequence of the reduction of the external amplifier gain after irradiation. The measured signal rise time is the convolution of the charge collection time and the amplifier response. It is slightly increased from 16,7ns to 19ns while the spread is also increased from 1,96ns to 2,78ns. However, the signal rise time and spread are still lower than the corresponding values of unirradiated samples produced in the standard process.

B. Beam test

Beam tests to measure the sensor efficiency were carried out in the CERN SPS test beam area by using a beam of 180GeV/c pions [8], [9] and reconstructing the tracks with the help of an FE-I4 based telescope [10] with 9µm resolution. The DUT consists of modified process pixels of the investigator chip and the applied reverse bias voltage is equal to -6V. Signals from 2x2 pixel groups were read out using broadband amplifiers. The efficiency obtained by this setup if the DUT efficiency was 100% has been simulated in order to apply corrections for each measurement due to the acceptance edge effects.

The charge collection efficiency measurement results of three different pixel groups are shown in Fig. 3 [8], [9]. The pixel groups have different size, collection electrode size and electrode n-well to deep-p-well distance (spacing). Due the increased noise in this setup, the threshold was set to a relatively high value (~600e$^-$). This threshold setting prevents the efficiency from reaching 100%. In the case of an unirradiated 50x50µm^2 pixel with 3µm electrode and 18.5µm spacing, the efficiency was measured equal to 98.5% ± 0.5% (stat.) ± 0.5% (syst.) with high uniformity. In the case of an 25x25µm^2 pixel with 3µm electrode and 3µm spacing irradiated with a total dose of $10^{15}n_{eq}/cm^2$, the efficiency was measured to be 98.5% ± 1.5% (stat.) ± 1.2% (syst.). If for the same parameters and radiation dose, the pixel dimensions are increased from 25x25µm^2 to 30x30µm^2, the efficiency is only slightly reduced to 97.4% ± 1.5% (stat.) ± 0.6% (syst.).

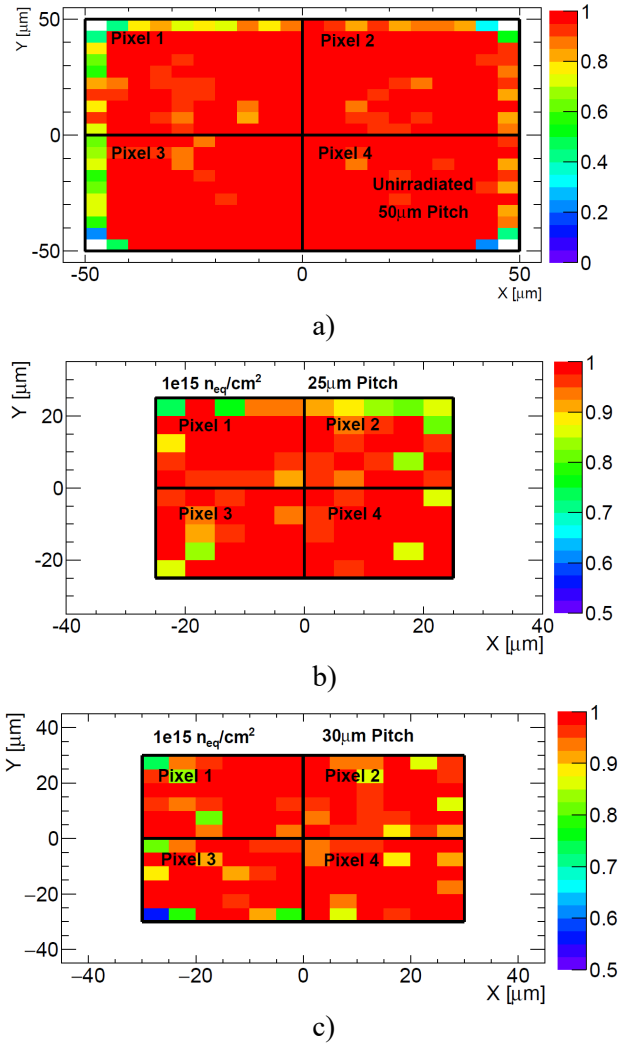


Fig. 3. Charge collection efficiency of a group of 2x2 pixels produced in the modified process: unirradiated 50x50µm^2 pixel with 3µm electrode and 18.5µm spacing (a), $10^{15}n_{eq}/cm^2$ irradiated 25x25µm^2 pixel with 3µm electrode and 3µm spacing (b), $10^{15}n_{eq}/cm^2$ irradiated 30x30µm^2 pixel with 3µm electrode and 3µm spacing (c) [8], [9].

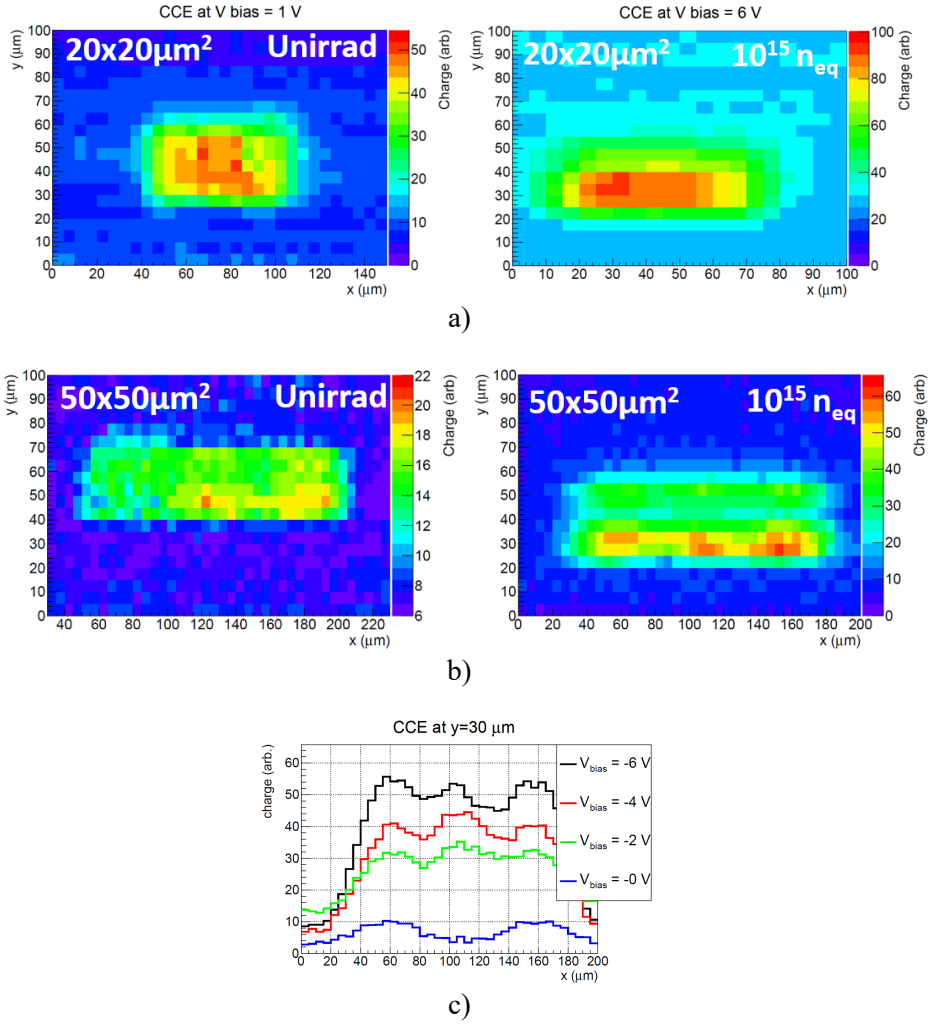


Fig. 4. Charge collection profile across the depth of the sensor of three adjacent pixels: 20x20µm^2 pixel size before and after irradiation to $10^{15}n_{eq}/cm^2$ (a), 50x50µm^2 pixel size before and after irradiation to $10^{15}n_{eq}/cm^2$ (b). Charge collection efficiency at y=30µm for different reverse bias voltages in the case of an irradiated 50x50µm^2 pixel [6].

C. *Edge TCT measurements*

The edge Transient Current Technique (e-TCT) is performed by directing short bursts of an infrared laser beam onto the side of the chip. It can be very useful in the characterization of the depletion region depth by scanning the beam across the epitaxial layer. In Fig. 4a the charge collection efficiency measurements are shown for a pixel of 20x20µm^2 before and after irradiation with neutrons to $10^{15}n_{eq}/cm^2$ [6]. The same results for a pixel of 50x50µm^2 are presented in Fig. 4b. In Fig. 4c, the charge collection efficiency of an irradiated 50x50µm^2 pixel for different reverse bias voltages is being studied. The measurements were done by combining the signal of 3 adjacent pixels to identify possible pixel boundary effects. The charge collection depth is measured to be about 25µm, which is equal to the thickness of the epitaxial layer. It is uniform with an error of 10% for a reverse bias voltage equal to -6V.

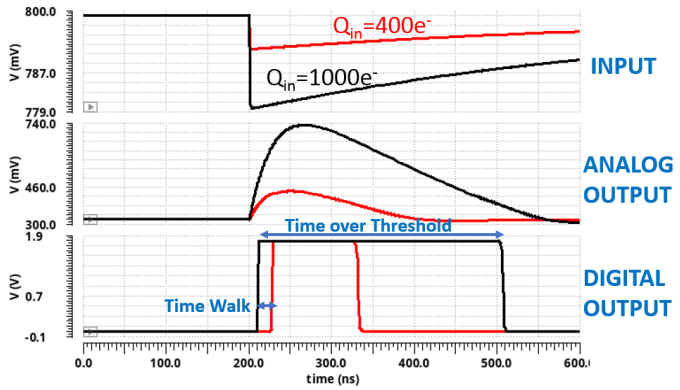
IV. Large Scale Demonstrator Chips

Sensors realized in the TowerJazz 180nm modified process combine very low sensor capacitance with radiation tolerance demonstrated by the measurements conducted with the help of the investigator chip. Design of pixels with small sizes is essential in achieving charge collection efficiency close to 100% and fast signal rise times. As a consequence, the granularity and spatial resolution of full scale chips based on these pixels will be high. The low sensor capacitance simplifies the analog front-end design and allows for very low power consumption. Furthermore, since the input signal is large, noise at the input that is quantified by the Equivalent Noise Charge (ENC) is expected to be very low.

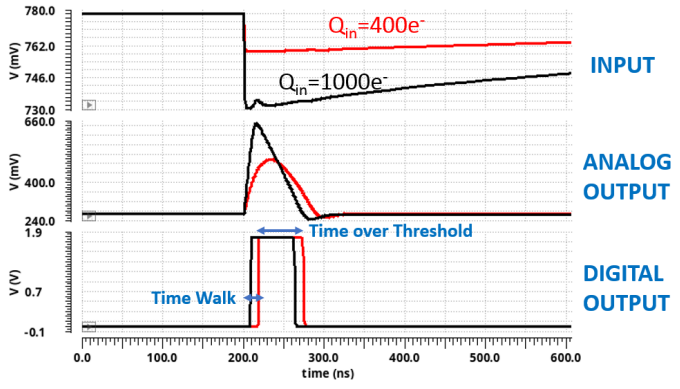
Two large scale demonstrator chips based on the modified process sensor, called “MALTA” and “TJ-Monopix” were designed and submitted for fabrication. MALTA is a full-scale chip with dimensions of 2x2cm^2 and consists of 512x512 pixels. TJ-Monopix size is 1x2cm^2 and it consists of 224x448 pixels. Both chips are designed with small pixel pitch: 36,4x36,4µm^2 in the case of MALTA and 36x40µm^2 in the case of TJ-Monopix. The collection electrode size of TJ-Monopix is 2µm surrounded by a spacing of 3µm. In MALTA slight variations of the sensor geometry are implemented for testing purposes.

The two demonstrator chips use a similar low power, low noise analog front end derived from the ALPIDE chip for the ALICE ITS upgrade [11]. It consists of a source follower to buffer the input signal, a cascode gain stage that shares the same current branch with the source follower, a low frequency feedback loop to stabilize the analog output dc potential and a simple common source discriminator. The front end was optimized for the fast timing requirements (25ns) of the ATLAS ITk. The power consumption of the front end is about 0,9µW, yielding an analog power density lower than 70mW/cm^2.

The analog charge information in the case of TJ-Monopix is encoded using the standard Time over Threshold (ToT) technique. On the contrary, the analog charge information in the case of MALTA is encoded by the Time of Arrival (ToA) difference of the hit pulses between neighboring pixels. This difference is called time walk. Therefore, a clipping mechanism is added in the MALTA front end to reduce the hit pulse width. The input node baseline restoration is achieved either by a diode or a PMOS current source. TJ-Monopix employs the PMOS reset scheme due to its improved ToT linearity and adjustable slope (resolution). These differences between the two otherwise similar front ends, leads to considerably different pulse shapes for MALTA and TJ-Monopix as illustrated in Fig. 5, for two different input charge values of Q_{in}=400e$^-$ and Q_{in}=1000e$^-$. The threshold is set to Q_{TH}=300e$^-$.



a)



b)

Fig. 5. Front end response of the TJ-Monopix (a) and MALTA (b) chips

In Fig. 6 the simulated noise performance of the front end with the PMOS reset scheme used in TJ-Monopix is shown. The equivalent noise charge is only about 11 electrons and well below 5% of the threshold.

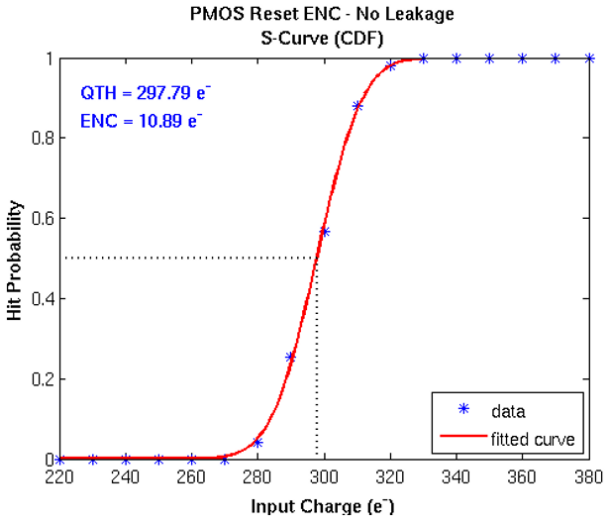


Fig. 6. Simulated ENC performance of the front-end with PMOS input reset (cumulative distribution function)

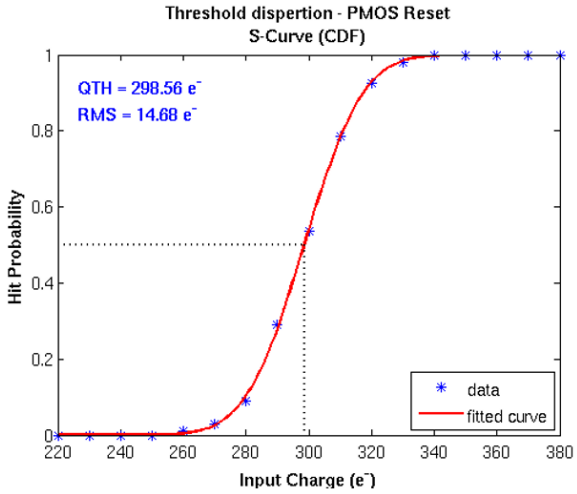


Fig. 7. Simulated front end threshold dispersion (cumulative distribution function)

Significant design efforts have been devoted into identifying the critical devices in terms of mismatch and adjust the transistor dimensions for an optimum performance to mismatch tradeoff. By increasing the area of the critical transistors, a simulated threshold dispersion below 15e$^-$ is achieved, with a threshold value equal to 300e$^-$, as shown in Fig. 7. Due to the low threshold dispersion there is no need for complicated programmable in-pixel threshold tuning.

Different readout architectures were implemented in the two prototypes. MALTA employs a novel asynchronous readout scheme that avoids the Bunch Crossing ID (BCID) time stamp distribution to the whole matrix to further reduce the power consumption, and that is also able to cope with high hit rates [6]. Each double column of MALTA is subdivided into alternating groups of 16 pixels. Each pixel generates a hit signal

of programmable width (0.5ns to 2ns). All pixels of the same group use a common 16-bit bus, to transmit the hit pulses asynchronously to the periphery. At the same time the group address information is sent over a 5-bit bus. At the end of the double column, all signals are merged on a common bus. An arbitration logic is used to time-sort simultaneous signals. After decoding of the data at the periphery, hit information is transmitted off chip via a fast serial link using a 5Gbps LVDS transceiver.

The readout architecture of TJ-Monopix is depicted in Fig. 8. It is based on the well-established column drain architecture used in the LF Monopix-01 [12] chip, that prioritizes the order in which the pixels can use the common bus to transmit the hit data. A 6-bit Bunch Crossing ID (BCID) time stamp is transmitted synchronously to every pixel in the matrix. When a pixel is hit, a hit flag is set and the time of the leading edge (LE) and the trailing edge (TE) of the hit pulse are recorded into a 2x6-bit in-pixel SRAM. At the same time a busy token signal with priority from top to bottom is set and propagates down the column. When it arrives at the End of Colum (EoC) logic at the bottom of the column, it becomes a busy token signal over the columns with priority from left to right, and is transmitted to an off-chip readout controller. The controller responds with two signals: Read and Freeze. The Freeze signal is global and disables the hit flag registers to avoid new hits disturbing the priority scan during the read phase. The Read signal initiates the read phase. Only the pixel that is hit and has the highest priority and also belongs to the column with the highest priority transmits data to the column bus. Apart from the 6-bit LE and TE information, the 9-bit pixel address is also transmitted. At the EoC, the 21-bit column bus values are identified by sense amplifiers and the 6-bit column address is added. The data packet is then propagated through the EoC logic of all the columns from left to right and transmitted off-chip. All signals are differential and carefully shielded to reduce crosstalk interference. To further reduce transient effects during the read phase, a source follower readout scheme is used for the column bus. In this configuration, the readout rate bandwidth of each double column is approximately 40MHz, without taking into account the EoC delays.

The full chip design of TJ-Monopix consists of four different flavors. Each flavor readout is independent. The output data rate can be as high as 40Mhz, thus the full chip data transmission rate of the serialized output data is 160Mhz. The first flavor explores the possibility of reducing the power consumption by modifying the column bus precharge circuit to eliminate the static power consumption of the source follower bus readout, while still limiting the transient effects. In the second flavor the unmodified precharge circuit derived from the LF Monopix-01 [12] chip is used. The third flavor incorporates a novel leakage compensation circuit designed specifically with the combination of the sensor capacitance and the front-end voltage preamplifier in mind. By compensating for the leakage current after irradiation, the baseline reset rate at the input does not change, improving noise performance and ToT resolution and linearity. In the fourth flavor, the possibility of using a positive high voltage to bias the sensor additionally to the reverse bias voltage of -6V is explored. The input of the front end is in this case AC coupled. The positive HV bias will increase the intensity of the electric field and can further increase the charge collection efficiency after irradiation.

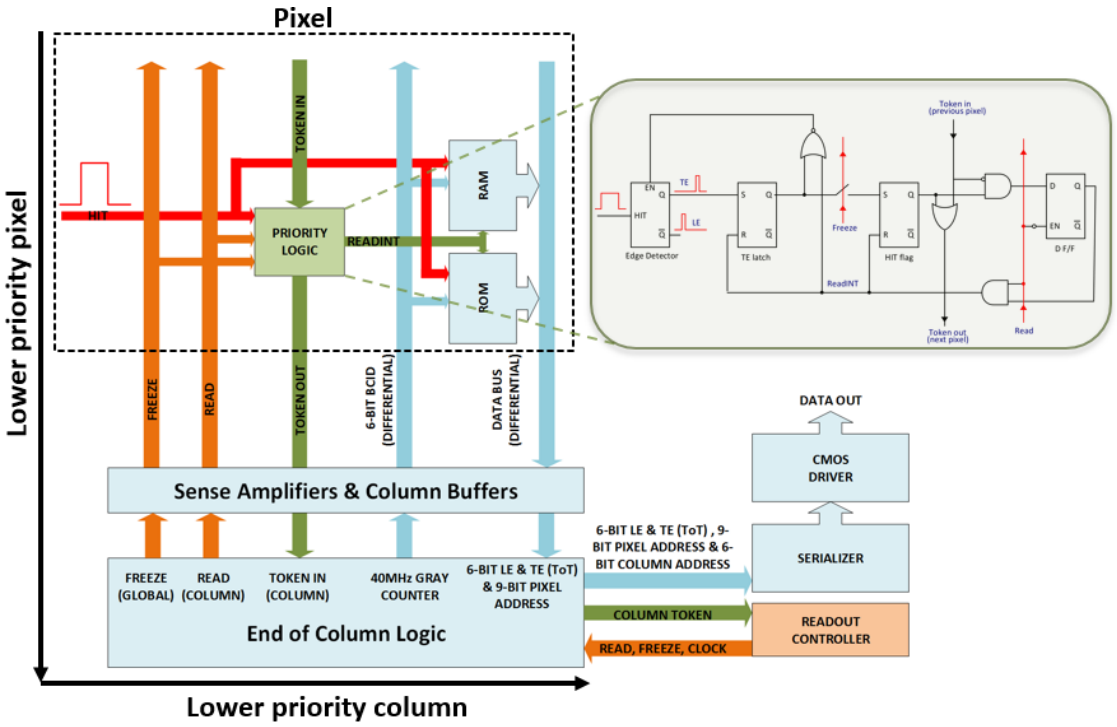


Fig. 8. The readout architecture of TJ-Monopix.

V. Conclusion

Depleted monolithic active pixel sensors have been developed in the TowerJazz 180nm technology using a novel process modification to increase radiation tolerance. The sensor was fully functional after a dose of $10^{15} n_{eq}/cm^2$, as demonstrated by measurements of the investigator chip. Two prototype chips with standalone fast readout architectures were designed to prove the feasibility of radiation tolerant, low capacitance, full scale DMAPS implementations for the ATLAS ITk upgrade.

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