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A silicon-based ion trap chip protected from semiconductor charging

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Abstract

Silicon-based ion trap chips can benefit from existing advanced fabrication technologies, such as multi-metal layer techniques for two-dimensional architectures and silicon photonics for the integration of on-chip optical components. However, the scalability of these technologies may be compromised by semiconductor charging, where photogenerated charge carriers produce electric potentials that disrupt ion motion. Inspired by recent studies on charge distribution mechanisms in semiconductors, we developed a silicon-based chip with gold coated on all exposed silicon surfaces. This modification significantly stabilized ion motion compared to a chip without such metallic shielding, a result that underscores the detrimental effects of exposed silicon. With the mitigation of background silicon-induced fields to negligible levels, quantum operations such as sideband cooling and two-ion entangling gates, which were previously infeasible with the unshielded chip, can now be implemented.

1. Introduction

Ion trap systems are among the leading platforms for quantum computation, as demonstrated by achievements in high-fidelity operations [1–7]. However, scalability remains a critical challenge [8, 9], requiring thorough consideration of numerous factors, including even the material of the trap [10]. As efforts to develop optimal ion trap architectures continue, silicon-based surface traps have been demonstrated as a strong candidate for achieving such scalability [11–14].

Their advantage is leveraged by mature semiconductor fabrication technologies, which allow for flexible trap design and integration of on-chip components essential for scalability. For instance, arbitrary chip shapes and junction fabrication are enabled by multi-metal layer structures where complex electric traces are routed in a three-dimensional layout beneath the chip surface [13]. This also facilitates ion shuttling, a key technique for realizing the quantum charge-coupled device architecture proposed for large-scale operations [15, 16]. Additionally, direct integration of optical and electrical components for on-chip beam delivery and detection is actively being pursued with ion trap fabrication [17–19].

While the benefits provided by this technological foundation are expected to outweigh certain drawbacks of surface traps compared to macroscopic traps—such as lower trap depth [20], increased susceptibility to dielectric charging [21], higher heating rates [22], and greater anharmonicity [23]—there is a significant yet

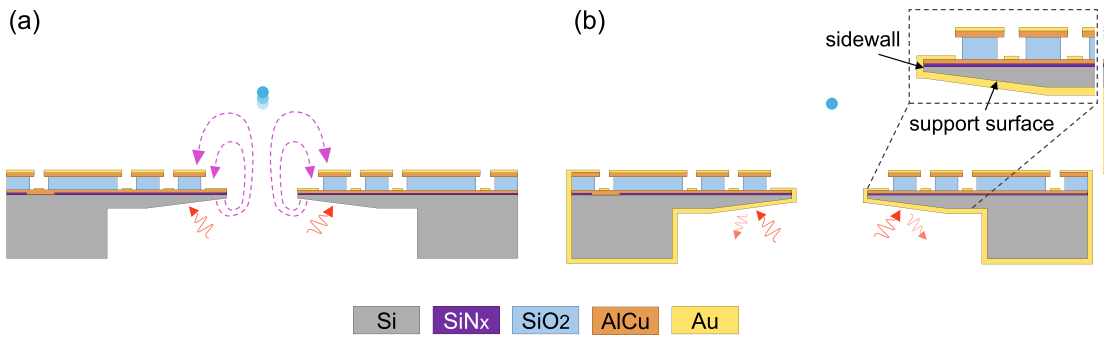

Figure 1. Cross-sectional view of the ion trap chips (a) without and (b) with gold coating. A protective gold layer is added on all exposed silicon surfaces in the new chip. The thickness is exaggerated for visual aid. The wavy arrows indicate light impinging on the surfaces of the slot structure. In (a), silicon-induced stray fields are represented as dashed arrows colored in magenta. The surfaces of the slot structure consist of the sidewall and support surface as shown in the inset of (b).

poorly understood issue specific to semiconductor-based surface traps. This issue, known as semiconductor charging, involves the photogeneration of charge carriers and their subsequent dynamics throughout the bulk and surfaces of a semiconductor [24]. Such charge carriers can generate strong stray electric fields at the ion position, scrambling the quantum evolution of motion-sensitive operations.

Recently, a microscopic model for the charge distribution mechanism and generation of surface photovoltage (SPV) has been presented and experimentally validated in a chip with exposed silicon surfaces [24]. Although optical shielding of the exposed surfaces was suggested as a potential method to mitigate semiconductor charging by suppressing photogenerated charge carriers, a chip with this feature was not previously demonstrated and tested to confirm the conjecture. In this work, we present results obtained from a chip specifically fabricated to verify this mitigation method and assess its effectiveness.

The new fabricated chip features metallic shielding on all exposed silicon surfaces as shown in figure 1(b), in contrast to the previous version without such protection in figure 1(a). Considerable effort is focused on coating the surfaces at the slot structure—the sidewall and the support surface—as these areas are sources of substantial SPV that originates from interface states formed during the deep reactive-ion etching (DRIE) process [24–26]. While the support surface is relatively easy to coat uniformly with gold, it is challenging to achieve full coverage on the sidewalls due to scallop patterns created during the DRIE process. A detailed description of the techniques associated with the removal of scallop patterns is provided in section 2. Although it has been quite common to shield non-metallic surfaces with gold in ion trap chips, including silicon chips, to improve dielectric shielding and reduce ion heating [13, 27], our approach is distinguished by its focus on suppressing semiconductor charging.

The paper is structured as follows: section 2 outlines the overall fabrication process of the ion trap chip. Section 3 demonstrates the effectiveness of our methods through experimental data that show suppressed silicon-induced stray fields and stabilized ion motion. Finally, section 4 presents results of quantum operations, including sideband cooling [28], heating rate measurements [29], and the implementation of the Mølmer–Sørensen gate on a pair of $^{171}Yb^{+}$ ions [30], all of which were not feasible in our previous chip without metallic shielding [24].

2. Trap fabrication

This section elaborates on the new fabrication process of the ion trap chip. The fabrication process involves a series of dielectric deposition, etching, and metal layer formation to produce the desired microstructures. The process flow is presented in figure 2.

The process begins with an anisotropic wet etch using potassium hydroxide (KOH) on the backside of the silicon wafer (a). The SiN_x layer serves as a protective mask during this step, allowing for anisotropic etching to define angled sidewalls on the wafer's backside. The primary function of the KOH etch at this stage is to shape angled sidewalls on the exposed silicon, which later defines the geometry of the slot structure. Following the KOH etching, an aluminum–copper (AlCu) layer is deposited and patterned (b). This metal layer acts as a ground and shielding layer between the silicon substrate and the metal layers to be deposited in step (g).

A silicon dioxide (SiO_2) layer of 10 μm thickness is deposited next (c), acting as an insulating barrier between the conductive AlCu layers and other structures. This layer is then patterned using dry etching (d). Step (e) employs DRIE on the front side of the wafer to control the remaining silicon thickness to around

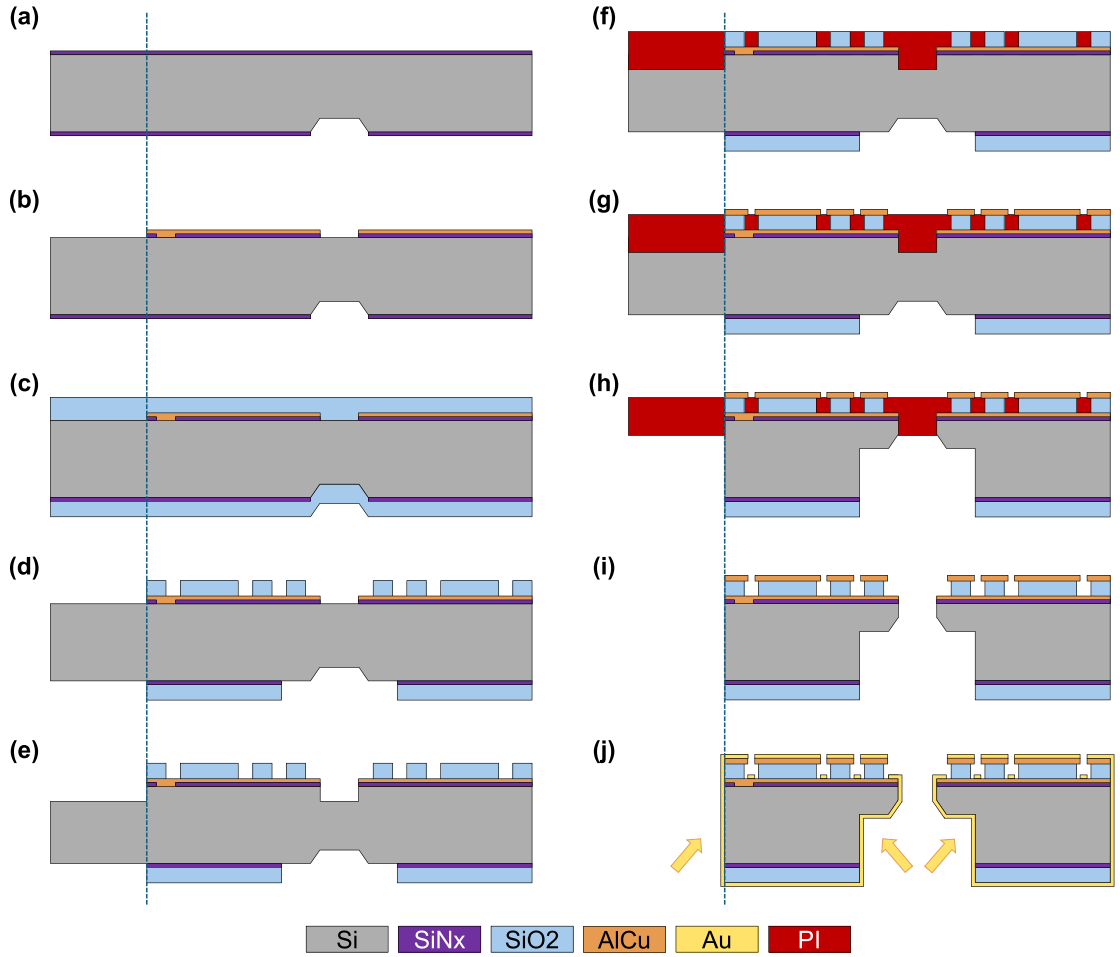

Figure 2. Fabrication process flow of the ion trap chip. It also illustrates the formation of the complex chip outline, where the vertical dashed lines represent the boundary of the chip. To the left of these lines, the area is etched to create the complex outer boundary, designed to minimize laser scattering. To the right of the vertical lines, a cross-sectional view of the chip shows the internal layers and structure formed during the fabrication process (not drawn to scale).

10 μm. In step (f), polyimide is coated and subsequently planarized using chemical mechanical planarization. The polyimide serves as a sacrificial layer for the subsequent steps. In step (g), AlCu is again deposited and patterned to form the electrodes, intentionally extending beyond the underlying SiO_2 pillars to create an overhang structure. While charges can accumulate on the SiO_2 surface, the AlCu overhang is designed to shield these charges from the trapped ions [11].

In step (h), DRIE is performed on the backside of the wafer to form a slot structure, which provides additional laser pathways. This step also completely etches the outer boundary of the chip, forming a complex-shaped outline that can minimize the scattering of lasers propagating parallel to the chip's surface. Further details on the formation of the chip's outer boundary are discussed in section 2.2. In step (i), the polyimide layer is stripped away, exposing the underlying structures, including the silicon within the slot structure. Once the polyimide is removed, the exposed silicon surfaces on the sidewalls of the slot structure undergo a scallop smoothing process to improve surface quality. The details of this scallop smoothing process are elaborated on in section 2.1.

The deposition of the gold (Au) layer is carried out in two stages (j), targeting both the front and back sides of the wafer. During the gold evaporation for the backside deposition, the wafer is tilted to ensure that the gold fully covers the exposed silicon within the slot structure. To enable gold coating along the outline of the chip, the wafer is diced into individual chips prior to gold deposition. The gold layer on the top prevents oxidation of the underlying aluminum layer, while the gold on the bottom ensures comprehensive coverage of the exposed silicon.

2.1. Scallop smoothing

During the DRIE process, scallop patterns commonly emerge on the sidewalls of etched silicon due to the alternating etch and passivation cycles. While these scallop patterns are a typical characteristic of DRIE, they

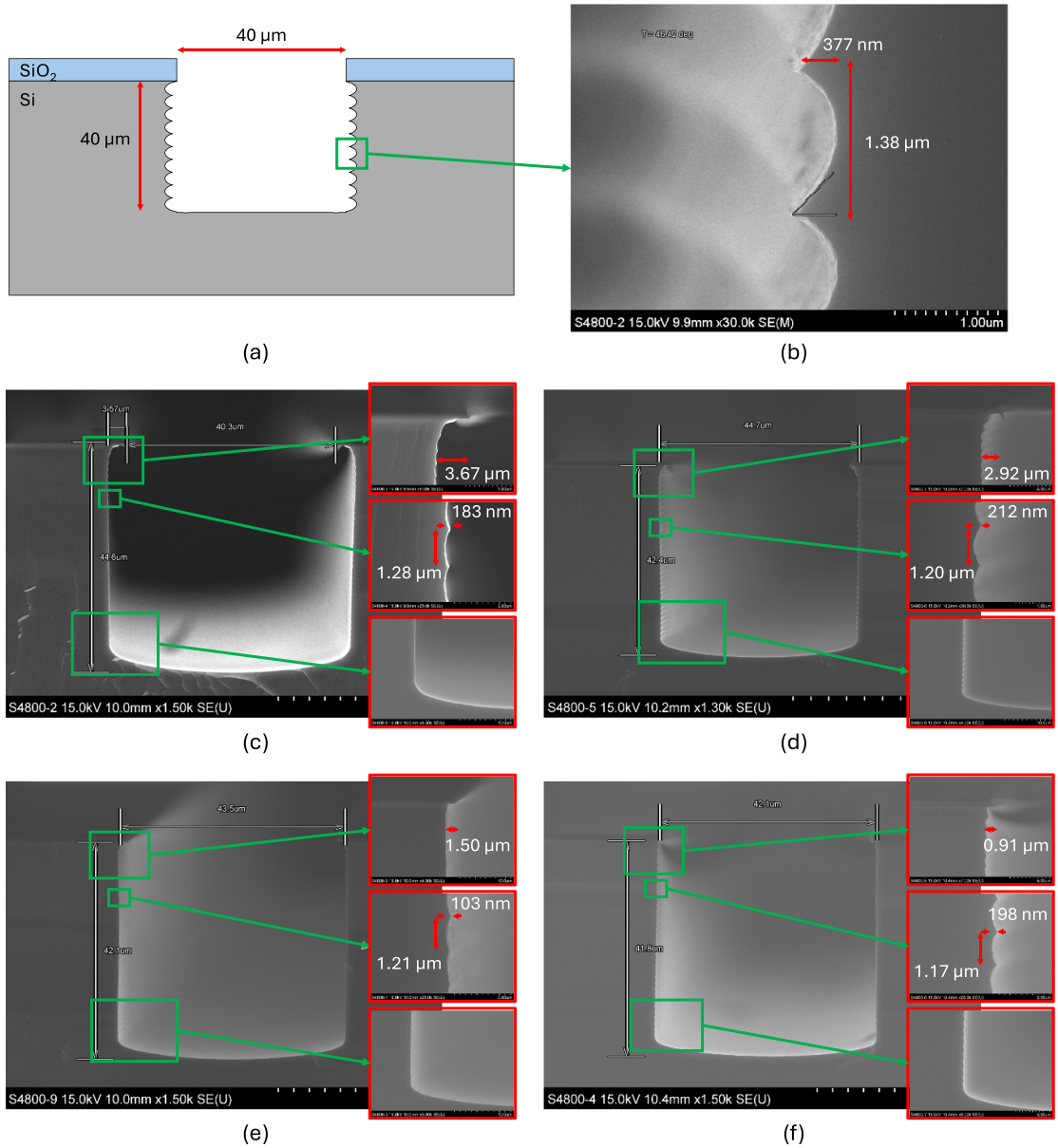

Figure 3. Results of the scallop smoothing test. (a) Schematic of the test sample. (b) Scanning electron microscope (SEM) image of the scallop on the sidewalls after DRIE. (c)–(f) Scallop dimensions on silicon sidewalls after scallop smoothing using different RIE process conditions. (c): RF power: 200 W, SF_6: 16 sccm, O_2: 8 sccm, pressure: 200 mTorr, 600 s. (d): RF power: 200 W, SF_6: 16 sccm, O_2: 8 sccm, pressure: 200 mTorr, 300 s. (e): RF power: 200 W, SF_6: 30 sccm, pressure: 200 mTorr, 300 s. (f): RF power: 100 W, SF_6: 30 sccm, pressure: 200 mTorr, 300 s.

pose significant challenges during the subsequent gold deposition step. The scallop-shaped surface can prevent complete coverage of the silicon sidewalls formed during step (e) in figure 2, as the irregularities cause a shadowing effect, leaving certain areas of silicon exposed.

To address this issue, an additional process is introduced to smooth the scallop patterns on the silicon sidewalls before gold deposition [31]. This step involves an isotropic etching process, which etches away silicon uniformly in all directions. By applying this isotropic etch, the sharp peaks and valleys of the scallop patterns are reduced, creating a smoother surface.

The scallop smoothing process is tested under four different RIE conditions using Oxford Instruments PlasmaPro 80 RIE, as shown in figure 3. To establish optimal process conditions, we first use a DRIE process to etch a standard silicon wafer to a depth of 40 μm with a pattern size of 40 μm, employing a 1 μm SiO_2 layer as a mask. The schematic of the test sample is shown in figure 3(a), and the scanning electron microscope (SEM) image of the scallop-shaped sidewall is in (b). The scallops formed during the DRIE process are measured at a depth of 377 nm, a height of 1.38 μm, and sidewall angles reaching up to 46°. Following the DRIE process, then RIE processes described in the caption of figure 3 are applied. Most of the fabrication conditions successfully reduced the sidewall angle of the scallop structures to a level that enables

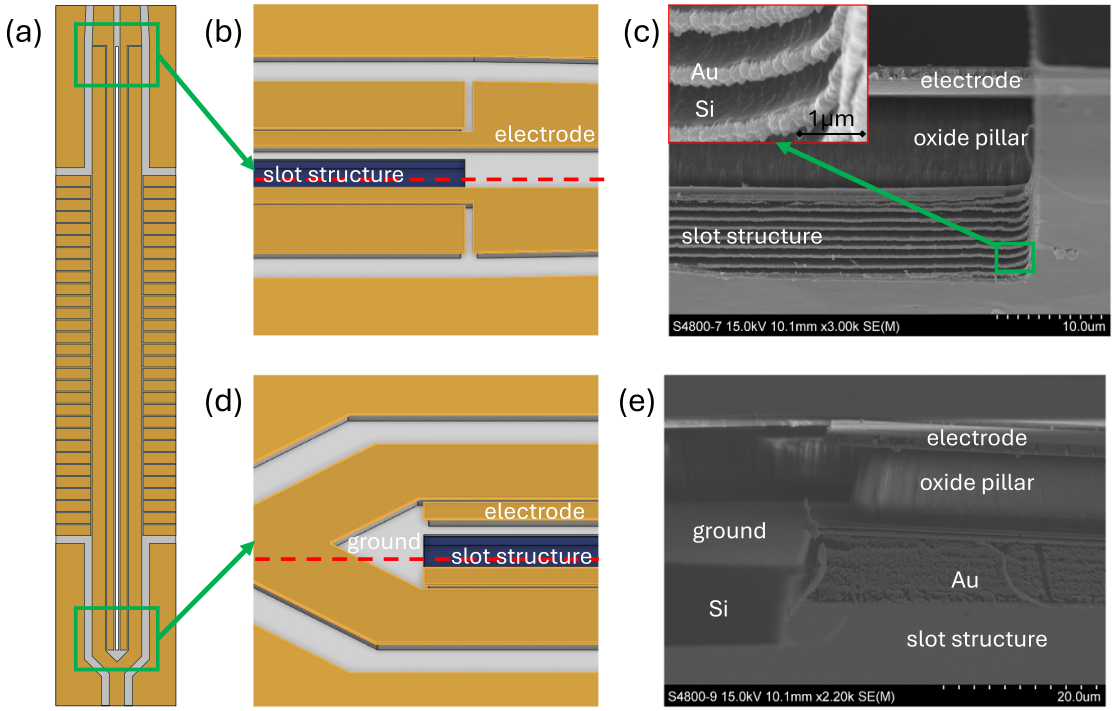

Figure 4. Comparison of gold-coated surfaces on the ion trap chips without and with scallop smoothing at the slot structure. (a) Layout of the electrodes near the loading slot. (b) and (d) Show close-up views of the regions in the green boxes of (a). (c) and (e) Are SEM images of the structures seen in (b) and (d), respectively. They are taken from different chip dies, without and with scallop smoothing. The samples are broken along the dashed red lines drawn in (b) and (d). (c) Shows incomplete gold coverage on the chip without scallop smoothing, where the shadow effect is evident. In contrast, a relatively evenly deposited gold-coated surface is observed in the chip in (e) that has undergone scallop smoothing.

sufficient gold coating. Notably, condition (e) yields the best results; the isotropic etching applied in this condition effectively removes the scallop patterns down to 103 nm and minimizes undercutting—critical for maintaining the integrity of the slot structure. This condition produces the smoothest sidewalls with minimal undercutting (1.5 μm), ensuring that the subsequent gold deposition achieves full coverage across the silicon sidewalls.

The optimized condition was subsequently applied to the ion trap chip, yielding successful results as demonstrated in figure 4. Figures 4(a), (b) and (d) present schematics indicating the locations where the SEM images were acquired. Figure 4(c) shows the result of gold deposition on an unsmoothed surface. The presence of scallop patterns results in incomplete gold coverage, with thinner or entirely uncoated regions. This incomplete gold coating may lead to the formation of photogenerated charge carriers at the slot structure. In contrast, figure 4(e) illustrates the gold coated after isotropic etching, which smoothens the scallop patterns and reduces surface irregularities. This result shows a more uniform surface that facilitates more coverage of metallic shielding.

Although achieving full gold coverage on the sidewalls of the slot structure in the chip was challenging, the support surface (see figure 1(b)) was uniformly coated with gold, shielding the largest portion of the exposed silicon responsible for semiconductor charging [24]. The overall fabrication process described in this section proved to be highly effective, as demonstrated in sections 3 and 4.

2.2. Fabrication of a chip with an arbitrary outline

In ion trap systems, precise control of the laser position is crucial for stable trapping and quantum gate implementation. One of the challenges arises when lasers, mostly aligned parallel to the chip surface and aimed at ions positioned at heights of typically 40–150 μm, cause scattering and clipping [32]. Long laser paths across the chip surface increase the likelihood of laser interaction with chip features, leading to scattering of the laser.

To address this issue, we have developed a new process for fabricating a chip with complex, arbitrary outlines designed to minimize clipping and reduce laser scattering. While chips with complex outlines have previously been reported [13, 14], we are not aware of any publications that detail their specific fabrication process. The design of the new chip is exhibited in figure 5(a). The beam paths are represented by blue dashed lines. The dimensions of the electrodes responsible for generating trapping potentials are denoted in

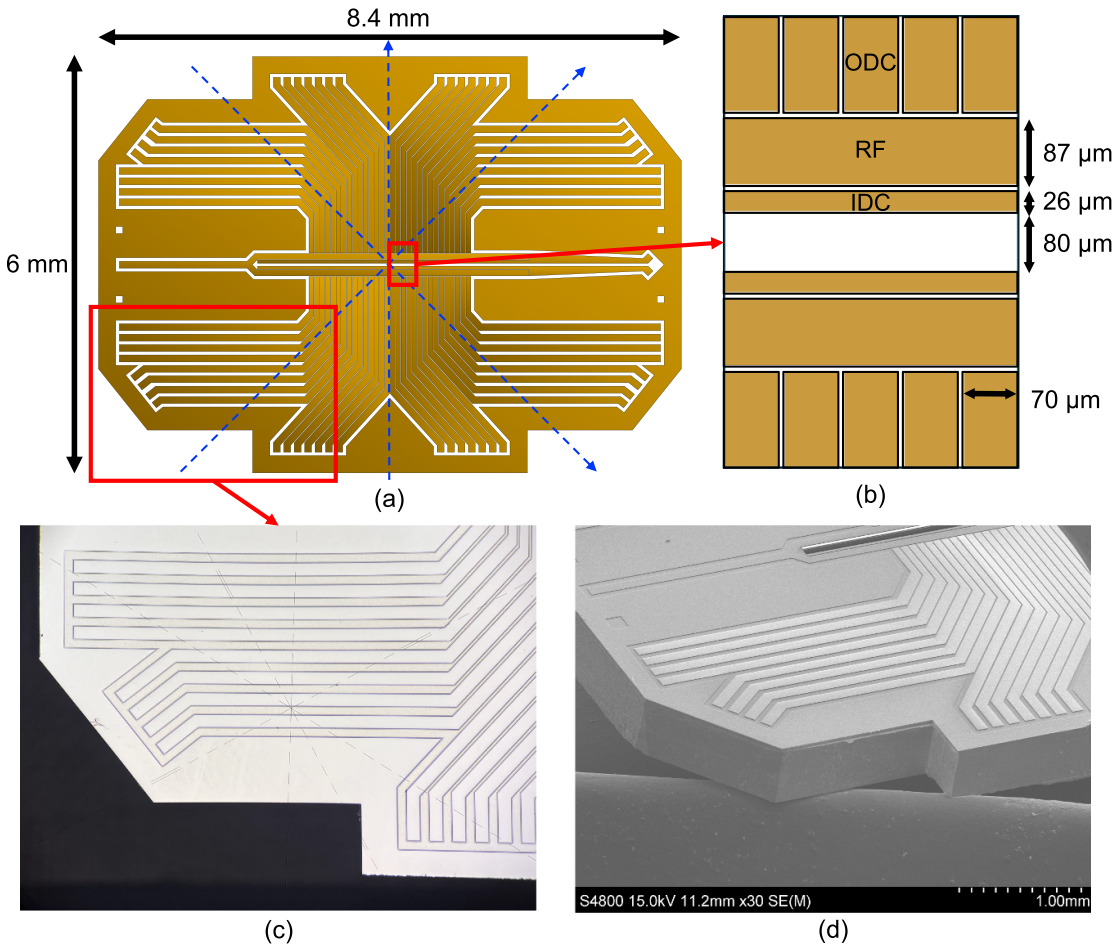

Figure 5. Images of the complex chip outline designed to minimize laser clipping. In (a), a schematic of the chip electrode layout is shown. Blue dashed lines represent the potential beam paths. The electrode dimensions are listed in (b). Electrodes are separated by gaps of width 8 μm. In (c), an optical microscope image shows the complex outer boundary of the chip, clearly displaying the design aimed at reducing laser clipping and scattering. The dashed lines in this image are artifacts of the optical microscope marking the origin and hold no significance. In (d), a SEM image taken at a similar magnification shows the outer boundary from a tilted perspective, revealing the cleanly etched edges of the outline.

(b), where IDC, RF, and ODC stand for inner-DC, radiofrequency, and outer-DC electrodes, respectively [33]. The complex chip outline is formed by selectively etching the regions to the left of the vertical green dashed lines shown in figure 2.

Importantly, while most of the outer boundary is defined during steps (d) to (h) in figure 2, complete singulation of the chip does not occur until the final dicing step. Conducting full outline etching using DRIE at step (h) would lead to premature singulation, disrupting subsequent wafer-scale fabrication steps and necessitating processing on individual dies. However, by etching only part of the outline at this stage, the remaining fabrication processes can continue at the wafer level. This approach preserves the integrity of the wafer until the final dicing step, ensuring that singulation occurs only after most of the fabrication processes are completed.

In figure 5, the results of the etched chip outline are shown. Figure 5(c) presents an optical microscope image from a top–down view, displaying the clean-cut outer boundary. Figure 5(d) is an SEM image taken at an angle, highlighting the etched outlines achieved through the fabrication process. Notably, no residual structures or unwanted protrusions were formed during the etching, and we obtain a clean and sharp outer boundary. These images demonstrate the effectiveness of the fabrication process in creating the precise and detailed outline required to minimize laser clipping.

3. Silicon-induced stray field measurement

In the chip with no metallic shielding, a peculiar optical absorption spectrum attributed to the physical properties of the defect states at the silicon surface has been reported [24]. There is strong absorption in the near-infrared range near the silicon band gap, with a monotonically weaker response extending through the

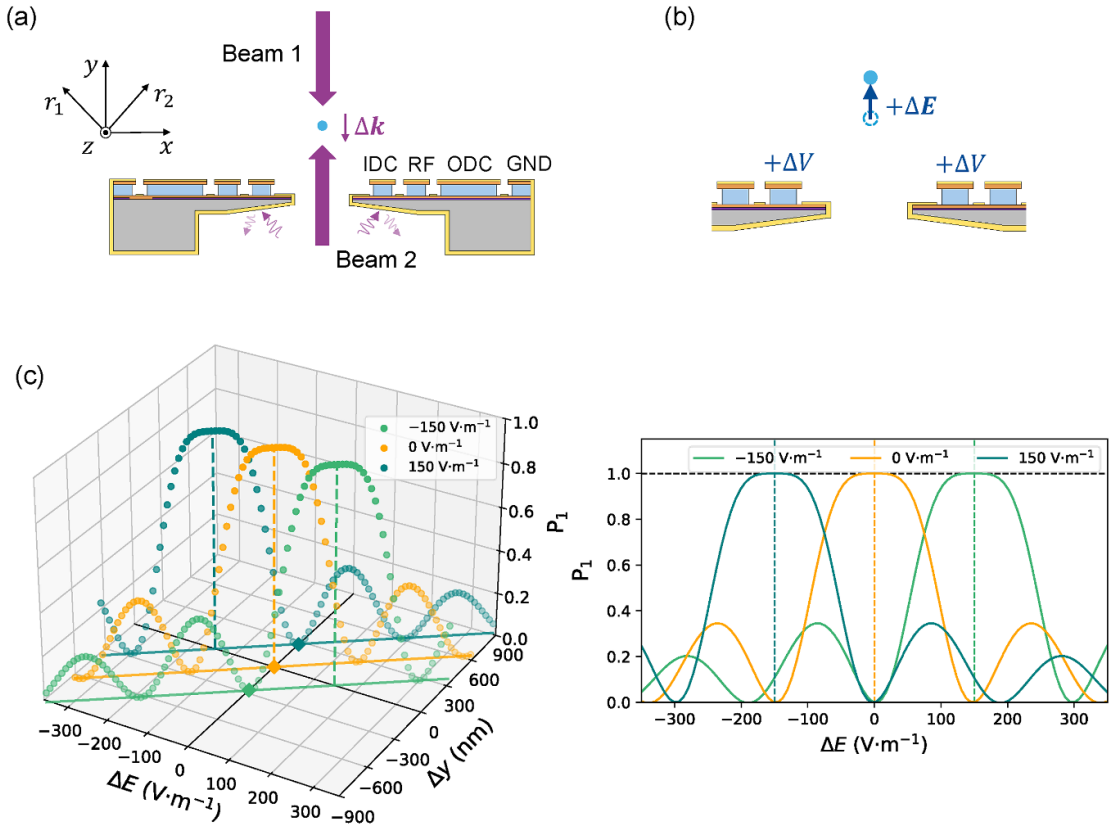

Figure 6. Experiment scheme for measuring silicon-induced stray fields. (a) Counter-propagating Raman beam configuration. IDC, RF, ODC, and GND stand for inner DC, radiofrequency, outer DC, and ground electrodes, respectively (see section 2.2). (b) Schematic of the DC scanning method. A voltage ΔV is applied to the IDC electrodes and scanned. (c) Visualization of the stray electric field measurement via the DC scanning method. (Left) A three-dimensional plot about the compensation field ΔE, the ion displacement Δy, and the qubit transition probability P_1, given background stray field values of $E_y \in \{-150, 0, 150\}\,\mathrm{V \cdot m^{-1}}$ denoted in the legend. (Right) The projection of the three-dimensional plot onto the ΔE–P_1 plane. Bessel-type patterns occur due phase modulation arising from excess micromotion. The maximum of P_1 occurs when the compensation field exactly cancels out the stray field.

visible and ultraviolet ranges. Photon flux in the range of $10^{14} - 10^{16}\,\mathrm{cm^{-2} \cdot s^{-1}}$ is sufficient to induce significant stray fields, depending on the wavelength. In the new chip with a protective gold layer, however, no such charging is observed across all previously tested wavelengths, even at higher power levels. This observation serves as evidence that charge carrier dynamics at the exposed silicon surface are responsible for the photoinduced charging observed in the chip without gold coating, further solidifying the experimental verification of semiconductor charging.

In order to characterize the reduced semiconductor charging more quantitatively, we use the DC scanning method to directly measure the silicon-induced stray fields [34]. The experimental scheme is shown in figure 6. We use Doppler-cooled $^{171}\mathrm{Yb}^+$ ions and a mode-locked laser with a center wavelength of 355 nm to drive a Raman transition [35]. As depicted in figure 6(a), two counter-propagating beams with a wave vector difference $\Delta\boldsymbol{k}$ oriented perpendicular to the chip are delivered to the ion through the slot structure. This configuration makes the Raman transition sensitive to electric fields along the y-axis. For the chip without gold coating, as shown in figure 1(a), semiconductor charging is primarily caused by beam 2, since the silicon surface can see its scattered light directly (see figure 6(a)). Note that $\Delta\boldsymbol{k}$ overlaps with both radial modes (r_1, r_2) of the ion.

The probe electrodes in the DC scanning method are the IDC electrodes shown in figure 6(a). As can be seen in figure 6(b), a voltage ΔV is applied to the IDC electrodes and scanned. This generates an electric field $\Delta\boldsymbol{E}$, defined as the compensation field, at the ion position. When ΔV is applied symmetrically to both IDC electrodes, the resulting compensation field, denoted as ΔE, is produced only along the y-axis. A visual description of the method is presented in figure 6(c), where numerical simulations have been performed with parameters detailed in section 4. In the three-dimensional plot, Δy is the displacement of the ion along the y-axis with respect to the RF null, and P_1 is the qubit transition probability. Three cases are shown, each with a different background stray field value E_y, as denoted in the legend. The markers along the Δy-axis represent the ion displacement due to E_y.

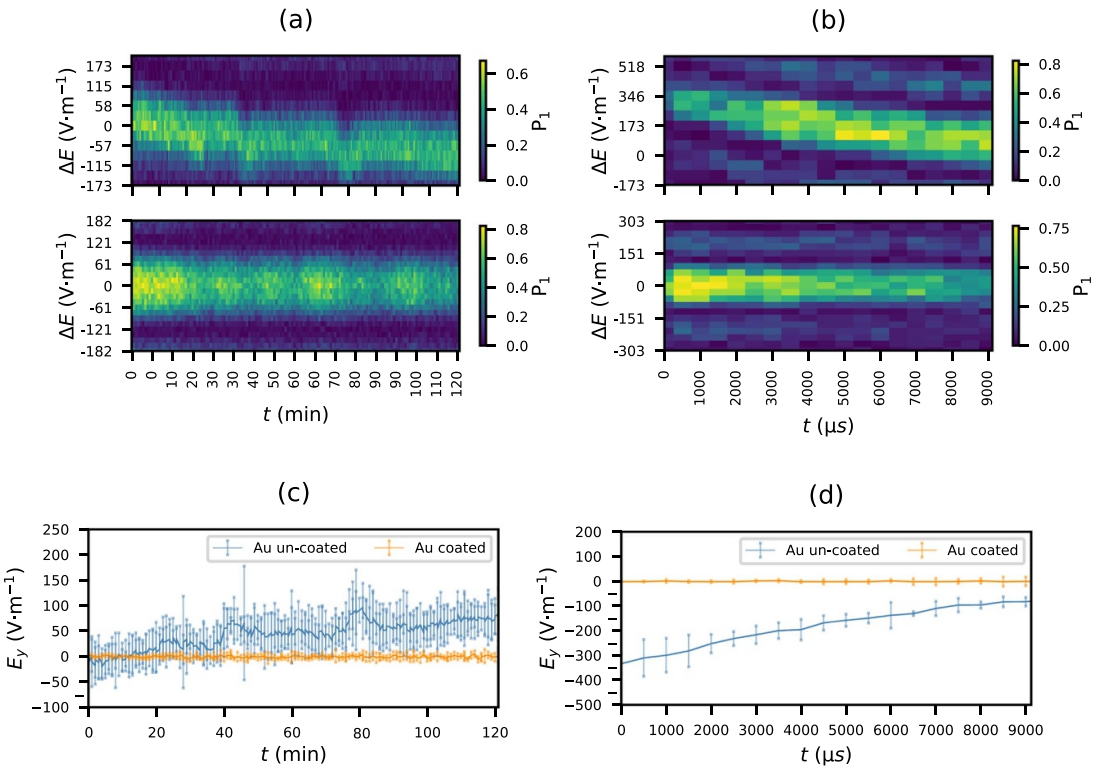

Figure 7. Stray field measurement results from ion trap chips with and without metallic shielding. (a), (c) Long term monitoring and (b), (d) short term evolution of the stray fields. The bottom and top plots in (a) and (b) correspond to the chip with and without gold coating, respectively. E_y represents the stray field along the direction normal to the chip surface. In (c) and (d), the compensation field values extracted from fitting the data in (a) and (b) to Bessel-type profiles are overlaid to directly compare the stray fields between the two chips.

Away from the RF null, the ion undergoes excess micromotion, which induces variations in the transition strength of the Raman transition. When the carrier transition is driven for a π-pulse duration as the compensation field ΔE is varied, the excitation probability P_1 is modified, resulting in a Bessel-type pattern [34]. The maximum occurs when the compensation field exactly cancels out the stray field, $\Delta E = -E_y$, restoring the ion back to the RF null. Note that the vibrational states of the ion have been assumed to be in the ground state for simplicity. Even when there are vibrational states other than the ground state, the maximum occurs at the same value of ΔE [24, 34]. The plot on the right in figure 6(c) shows the projection of the three-dimensional plot onto the ΔE–P_1 plane, which corresponds to what is measured in real experiments. The stray field E_y can thus be monitored by tracking the offset of the Bessel-type pattern as the compensation field ΔE is scanned.

Both long-term field drift and fluctuations, as well as short-term field generation when the laser is switched on [24, 34], are measured by applying the DC scanning method over time. The results are shown in figure 7, where (a), (c) correspond to the long-term monitoring and (b), (d) the short-term response immediately after a laser is turned on. The bottom and top figures in (a) and (b) are obtained from the chip with and without gold coating, respectively. By fitting each column of the time series data to a Bessel function with an offset (as shown in figure 6(c)), we determine the value of the stray field and its uncertainty from the fitted offset value, $\Delta E_{\text{fit}} = -E_y$. The fitted values extracted from (a) and (b) are plotted in (c) and (d), respectively, where the error bars represent the uncertainty of the fit at each instance. The magnitude of the stray field is calculated with the COMSOL Multiphysics® software.

As shown in figures 7(a) and (c), the long-term drift and fluctuations are suppressed to a negligible level. The error bars are also considerably smaller than those in data from the unshielded chip, where rapid stray field fluctuations occurring within the duration of a single DC scan increase the uncertainty of the fit. In the absence of such fast varying fields in the shielded chip, we are able to estimate the stray field with greater precision. The small fluctuations over time in (c) can be explained by drifts in beam parameters, such as beam pointing, which alters the π-pulse duration at each instance. These fluctuations also explain the variations of the transition strength over time in (a). The short-term field build up is also greatly suppressed, as shown in (b) and (d). Experiments with the chip lacking metallic shielding typically requires a pre-turn on

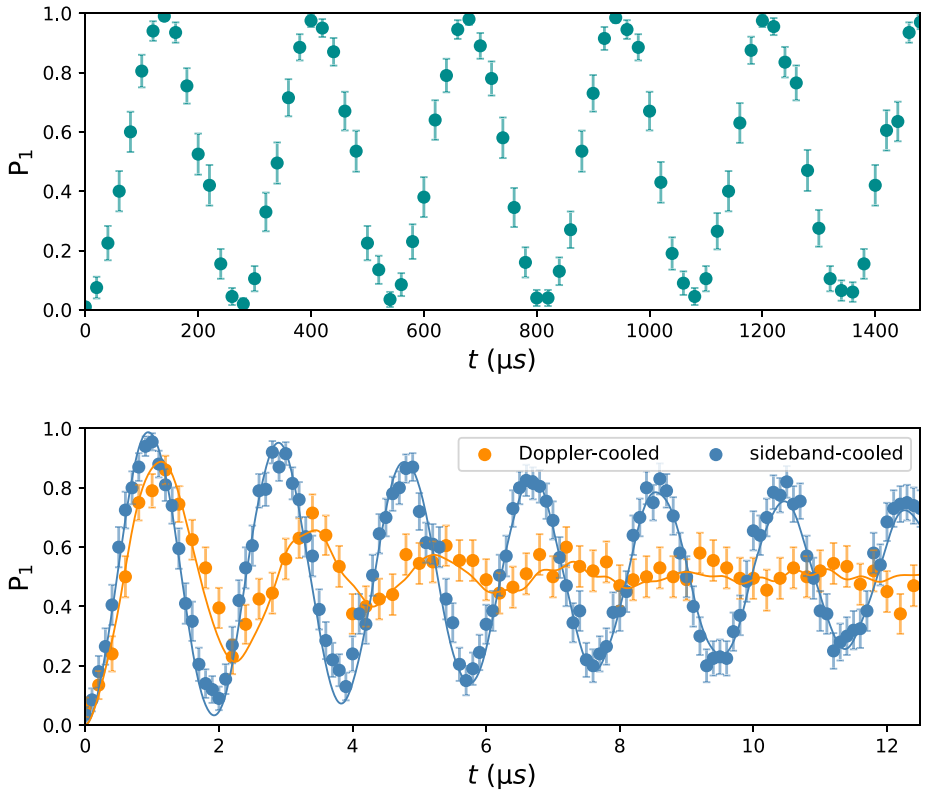

Figure 8. Carrier Rabi flopping in different beam configurations. (Top) Co-propagating configuration. This operation is motion-insensitive, flipping the qubit states independent of the vibrational states. (Bottom) Counter-propagating configuration. The qubit state and vibrational states are coupled in this geometry. P_1 is the population of the state $|1\rangle$. The mean phonon number of the vibrational states are fitted to thermal distributions, $(\bar{n}_1, \bar{n}_2) = (15.0, 14.0)$ after Doppler cooling, and $(\bar{n}_1, \bar{n}_2) \approx (4.0, 0.1)$ after sideband cooling (see solid lines). Heating is included in the simulation but has negligible effect during the evolution time.

procedure [24], where beam 2 is turned on for the field generation time prior to turning on beam 1, so that the Raman transition is driven after the ion has reached a new equilibrium position. As shown in (d), this sequence is unnecessary in the new chip as there is no observable photoinduced stray field.

4. Quantum operations as benchmarks of chip performance

The elimination of photoinduced stray fields leads to stable ion motion, enabling precise control of motion-sensitive operations. First, phase modulation of the Rabi frequency due to excess micromotion is removed [34]. Also, secular frequency shifts associated with stray field fluctuations, which are problematic in the unshielded chip, are not observed in the shielded chip. Such improvements allow the characterization of vibrational modes, sideband cooling, and qubit control via Mølmer–Sørensen interactions.

4.1. Sideband cooling and heating rate measurement

The trap parameters are chosen to set the radial mode secular frequencies of a single ion to $f_1 = 1.84(1)$ MHz and $f_2 = 2.11(7)$ MHz, corresponding to r_1 and r_2 in figure 6, respectively. The ion height above the chip surface is 100 μm. Figure 8 exhibits plots of Rabi flopping on the carrier transition driven by Raman beams in different configurations. The top plot was obtained using co-propagating Raman beams, which are insensitive to ion motion. The bottom plot shows Rabi flopping driven by a counter-propagating configuration as shown in figure 6(a), where the coupling of Raman beams to the vibrational states is maximal, before and after sideband cooling.

Due to the limited size of the instruction buffer in our current field programmable gate array controller, we are unable to implement fine-tuned sideband cooling, which is particularly important in systems with high heating rates, to reach the ground state of both modes. Only mode 2 is sufficiently cooled, while mode 1 is cooled intermittently. With a Rabi frequency of 545 kHz, the mean phonon number of each mode before and after sideband cooling are fitted to $(\bar{n}_1, \bar{n}_2) = (15.0, 14.0)$ and $(4.0, 0.1)$, respectively, assuming thermal distributions (see the solid lines in the bottom plot of figure 8). We expect to achieve ground state cooling of both modes once we are able to execute more instructions on an upgraded controller.

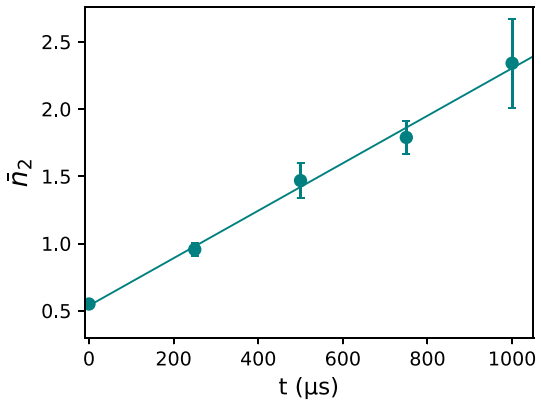

Figure 9. Heating rate measurement. The heating rate of mode 2, $\dot{\bar{n}}_2$, is measured using the sideband ratio method. t is the delay time during which heating occurs following the cooling of the ion. The fitted heating rate is $\dot{\bar{n}}_2 = 1.7(7) \times 10^3$ quanta $\cdot s^{-1}$.

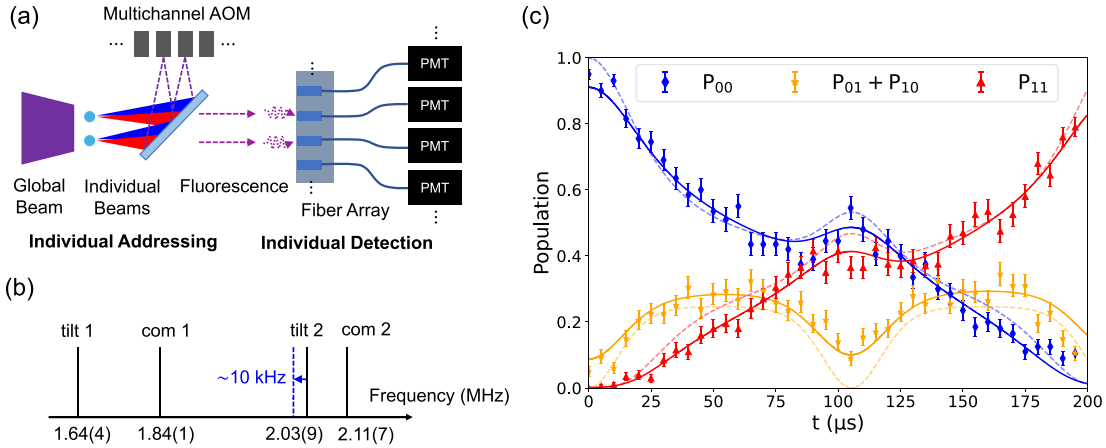

Figure 10. Implementation of the Mølmer–Sørensen gate. (a) The experimental set up for individual addressing using a multichannel acousto-optic modulator (AOM), and detection via a fiber array and photomultiplier tubes (PMTs). (b) The blue sideband frequencies of the two-ion chain. The tilt mode of mode r_2 is used for the operation due to its low heating rate of 6.2×10^1 quanta $\cdot s^{-1}$. The initial mean phonon number is $\bar{n}_{\text{tilt},2} = 0.2$ assuming a thermal distribution. (c) Result of the Mølmer–Sørensen gate, showing the populations of the two-qubit states. P_{00}, P_{01}, P_{10}, and P_{11} are the populations of the two-qubit states $|00\rangle$, $|01\rangle$, $|10\rangle$, and $|11\rangle$. The solid lines are fits to the data reflecting the limited detection fidelity. The dashed lines are obtained assuming perfect detection fidelity.

The heating rate of mode 2 is measured to be $\dot{\bar{n}}_2 = 1.7(7) \times 10^3$ quanta $\cdot s^{-1}$ using the sideband ratio method [29], as shown in figure 9. We observed that the dependence of the heating rate on the secular frequency appears random, without an evident scaling pattern of $f^{-\alpha}$ over the range $f_2 = 1.60(9)$ to 2.11(7) MHz, suggesting that technical noise predominantly influences our system [36]. In addition to reducing technical noise in our system, we are currently investigating other potential sources of heating, including imperfect gold coating on the sidewalls of the slot structure [13]. The partially exposed silicon surfaces on the sidewalls of the slot structure may contribute to the heating rate measured in our system [13], as space charge regions [37, 38], generation-recombination processes [39], and Schottky barriers [40] are known sources of electric field noise.

4.2. Mølmer–Sørensen gate

A Mølmer–Sørensen gate is performed with two ions [30], where beams 1 and 2 act as the individual and global beams, respectively. As shown in figure 10(a), the individual beams are controlled by a multichannel acousto-optic modulator (AOM) manufactured by L3Harris Technologies, Inc. The qubit states are individually detected via a fiber array, with each fiber connected to a dedicated Hamamatsu photomultiplier tube (PMT). Due to photon loss in the setup for multi-qubit detection, primarily due to high ultraviolet absorption in the low-OH fibers, the detection fidelity was limited to ~94%. This measurement error can be reduced by switching to a high-OH fiber array and optimizing the optical power and detuning of the detection beam.

The heating rates of the center-of-mass (com) and tilt modes of the two-ion chain along r_2 (see figure 6) are measured to be $2.3(6) \times 10^3$ and 6.2×10^1 quanta $\cdot s^{-1}$, respectively. Therefore, we operate at a frequency slightly red-detuned from the tilt mode, as shown in figure 10(b). After sideband cooling, we implement a Mølmer–Sørensen gate, the result of which is presented in figure 10(c). The data are fitted with Expans-ION, a simulator developed for the exact simulation of operations on an ion chain [41]. The fitted Rabi frequencies are 49.9(7) kHz for both ions, with a negative detuning of 9.4(6) kHz with respect to the tilt mode. The initial mean phonon number is fitted as $\bar{n}_{\mathrm{tilt},2} = 0.2$. The solid and dashed lines correspond to fitted curves with and without consideration of limited detection fidelity, respectively. The measurement errors are accounted for by incorporating $P(1|0)$ and $P(0|1)$, which represent the probabilities of misidentifying states $|0\rangle$ as $|1\rangle$ and $|1\rangle$ as $|0\rangle$, respectively. They are fitted as $P(1|0) = 0.04(5)$ and $P(0|1) = 0.06(1)$, in agreement with the overall detection fidelity.

5. Conclusion

A new fabrication process has been developed to mitigate semiconductor charging, as demonstrated by a chip featuring metallic shielding on all exposed silicon. Silicon-induced stray fields are observed to be significantly reduced in comparison with data from an unshielded chip. Using the shielded chip, we observe stable ion motion, and subsequently conduct motion-sensitive quantum operations, such as sideband cooling and two-qubit gates, that were not feasible in the absence of the gold layer. Additionally, fabrication techniques that produce complex chip outlines reduce laser scattering from the chip surface, further contributing to the suppression of photoinduced charging. The observed heating rate is primarily attributed to technical noise and some unknown sources, such as imperfect shielding of the sidewalls of the slot structure. In the context of ongoing efforts to develop increasingly complex and scalable silicon-based ion-trap chips, the results presented here offer an important means to address a significant source of infidelity inherent to semiconductor materials.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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