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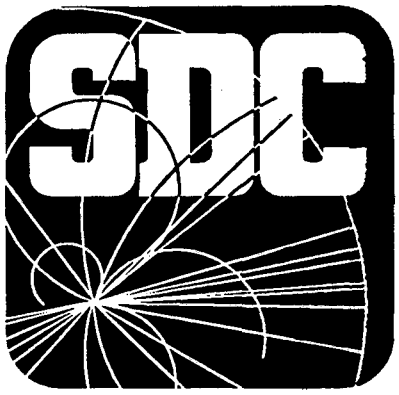

SDC
SOLENOIDAL DETECTOR NOTES

FIRST LEVEL MUON TRIGGER CIRCUITS USING XILINX FPGA

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FIRST LEVEL MUON TRIGGER CIRCUITS USING XILINX FPGA

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Abstract

Drift tubes of the SDC central muon detector in θ view are used to generate a first level muon trigger. In this paper, we will begin from describing the basic trigger concept developed by the SDC muon subgroup. Results from our Monte Carlo study will be given. A design for implementing the basic trigger concept using Xilinx FPGA will be discussed.

1 Trigger Concept

Drift tubes in the θ view measure the muon bend by the magnetized iron toroid. The θ tubes of layer 1 and 3 and those in layer 2 and 4 in a module form towers projecting to the interaction point. Offset is introduced between tube layer 1-3 and 2-4 to compensate the dead space in between tubes. For a pair of tubes behind the 1.5 m toroid, as shown in fig. 1(a), we have a simple relation

$$\delta t = \frac{3.2}{P_t \ sin\theta} \ \mu s,$$

where P_t is in GeV/c and the constant 3.2 is determined by the detector geometry and the drift velocity. The muon energy loss in the calorimeter and iron toroid is not taken into account here. The polar angle θ can vary from 30° to 90°. Trigger thresholds are set on δt's. The cuts must be adjusted accordingly to θ in order to maintain constant trigger response throughout the detector.

2 Monte Carlo Simulations

Single muons are generated at the interaction region and are propagated through the barrel toroid and drift tube arrays. The interaction region size (σ = 5 cm) and the multiple scattering in the calorimeter and iron toroid are dominating factors affecting the trigger turn on property. Our study shows that one meter thick toroid is insufficient whereas 1.5 m thick toroid provides a reasonable safety margin. It is also found that the time resolution of about 20 ns is sufficient for the trigger circuits. A more detailed description about these studies can be found in an earlier note.[1] Here, we will describe the results of trigger algorithm studies.

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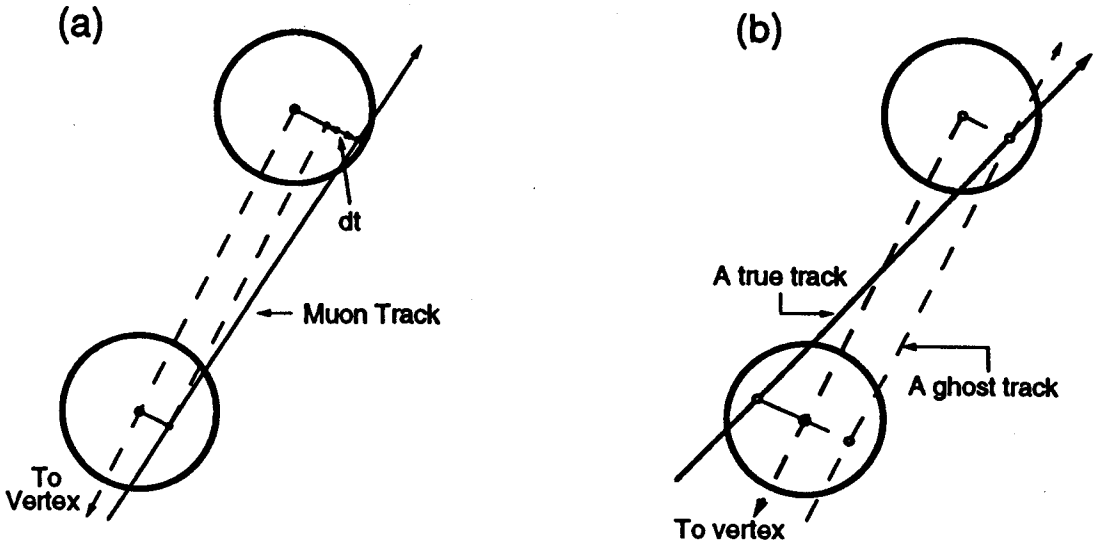

Figure 1: (a) A trigger tower consisting two projective drift tubes.
(b) A low P_t muon can fake a high P_t one.

The efficiency is low if only two layers of paired tubes are used. In addition, the background is high due to the fact that a low P_t muon can satisfy the trigger condition if it happens to cross the line joining the two wires as shown in fig. 1(b). The trigger efficiencies as functions of muon P_t calculated by Monte Carlo method is shown in fig. 2.

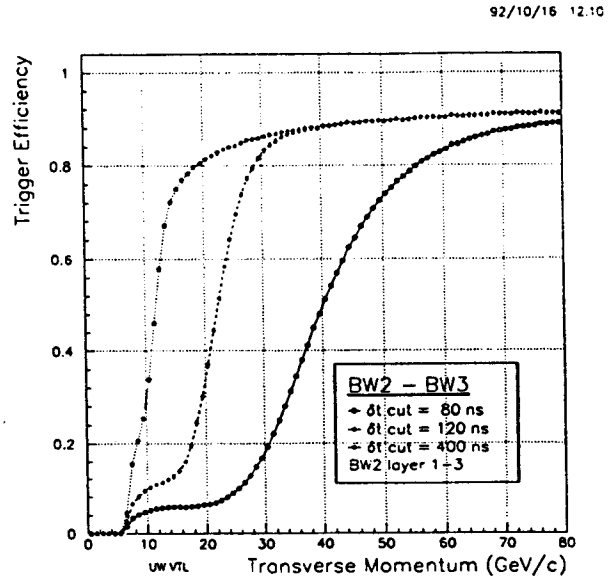

Figure 2: Trigger efficiency as functions of muon transverse momentum for three δT cuts. Only two layers of paired θ tubes are used.

There are eight layer of θ tubes in the two super modules outside of the toroid. Typically, four trigger primitives are produced by the four paired layers of drift tubes. We name them as T_1, T_2, T_3 and T_4. The problem of low efficiency and high background can be resolved if all four paired layers of drift tubes are used in the trigger. This method is first suggested by the Michigan group.[2] We can require that at least two out of the four δt's measured by the four paired layers of tubes are less than the cut. In other wards, we require at least two of the T_1, T_2, T_3 and T_4 to be set. This scheme is first suggested by the Michigan group.[2]

We can use another trigger algorithm which requires $(T_1 \oplus T_2) \otimes (T_3 \oplus T_4)$. Here, $\oplus$ refers to a logic AND and $\otimes$ is for logic OR. Efficiency curves for these two trigger algorithms are shown in fig. 3 and fig. 4. It is clear that the two out of four algorithm is very efficient at high P_t. But the background suppression is not very good at the low P_t end. On the other hand, the algorithm of $(T_1 \oplus T_2) \otimes (T_3 \oplus T_4)$ is less efficient at high P_t. But it can better suppress the low P_t background.

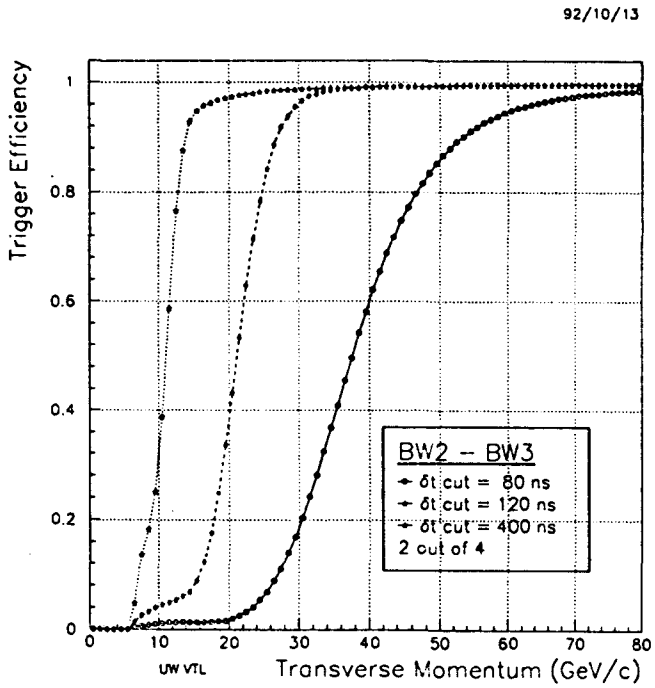

Figure 3: Trigger efficiency as functions of muon P_t. Two out of four of T_1, T_2, T_3. T_4.

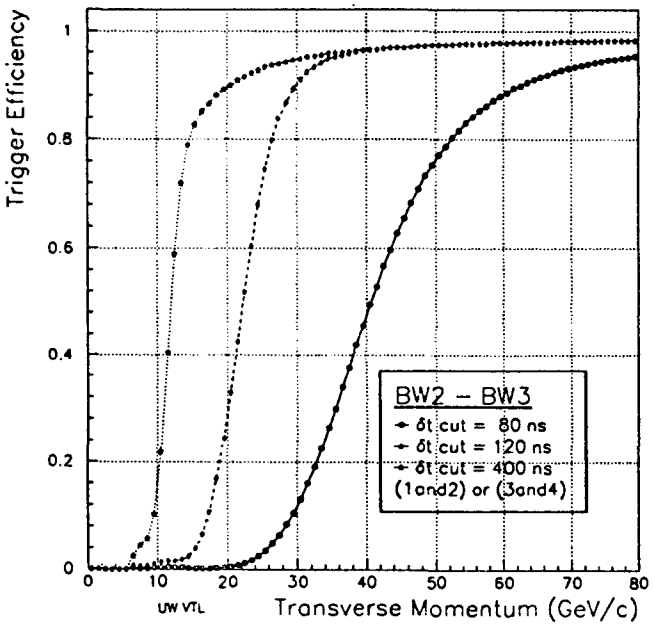

Figure 4: Trigger efficiency as functions of muon P_t for $(T_1 \oplus T_2) \otimes (T_3 \oplus T_4)$.
$\oplus$: logic AND, $\otimes$: logic OR.

3 Circiut Descriptions

A CAMAC trigger board intended for a beam test at KEK has been built and tested. This board is designed according to the trigger concept described above. The drift tube arrangement is assumed to be 32 tubes in two groups of 4 × 4 matrices. Discriminated signals from these 16 tube pairs are sent to the 16 XC2018-70 chips on the trigger board which set trigger flags according to the measured δt's. These chips are configured identically by parallel down loading. Three different δt cut circuits, circuit 1, 2 and 3, are shown in fig. 5, 6 and 7. The circuit design on the board can be changed by simply down loading a different design.

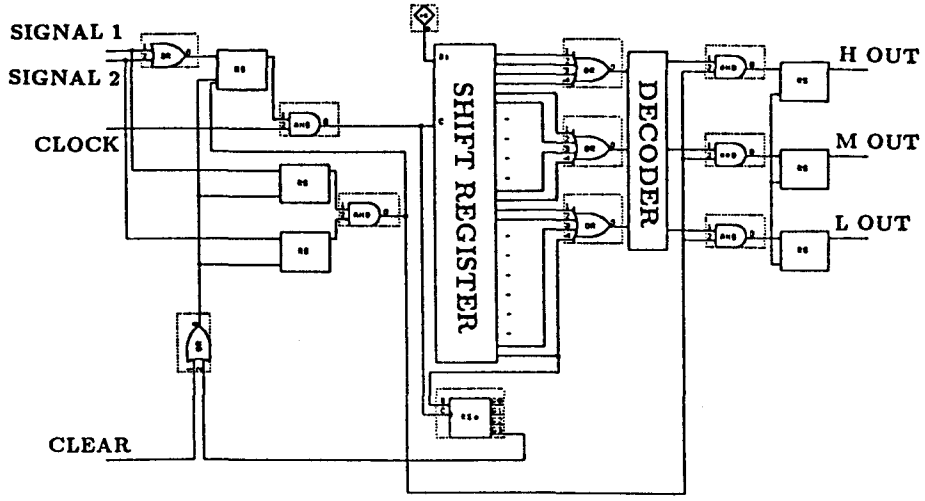

Figure 5: Circuit 1. The first arrival wire signal starts the clock of the shift register and the signal from the other wire stops the clock.

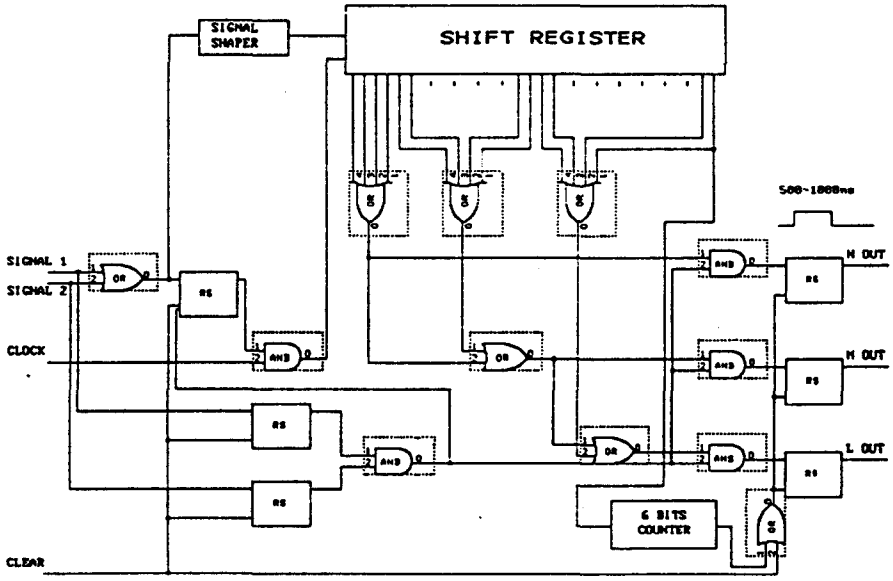

Figure 6: Circuit 2: The first arrived wire signal is sent in to a shift register and the clock starts. The δt is determined by the signal from the other wire in the trigger tower.

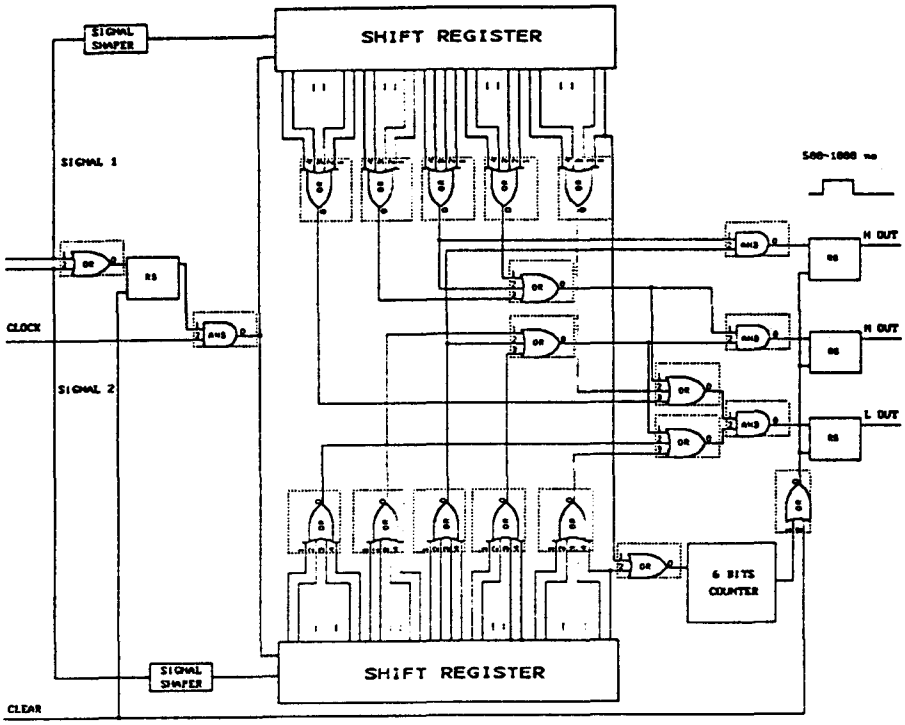

Figure 7: Circuit 3: Signals from the two wires are sent into two shift registers from opposite directions. δt cuts are made based on locations where the two signals meet.

These circuits consists coincidence logic and one or two 24 to 40 bits shift registers running at 65 MHz. The length of the shift register depends on the tube location inside the SDC muon detector. Signals are first clipped to one clock cycle wide before they enter the shift registers. This is necessary because the width of the discriminated signals from drift tubes can vary from few nanoseconds to few hundred nanoseconds depends on the amplitude of the analog signals. The signal clipping guarantees that only one bit is set at a given time ensures good time resolution. Three trigger flags, HIGH, MEDIUM and LOW, are generated for three P_t cuts. In order to maintain a constant P_t threshold, δt cuts must be adjusted at different θ. Such adjustments are easily made either by programming trigger circuits differently or running them at different clock speed. Computer simulation shows that such adjustments do not need to be continuous. [1] We can simply apply different δt cuts for different chamber modules. The registers for the trigger threshold outputs are cleared about 1 μs after the first tube hit is arrived. This ensures that there is enough time for making trigger decisions from trigger primitives generated in different tube layers.

Circuit 1 shown in fig. 4 is the simplest circuit. A disadvantage of this circuit is that it is possible to loose good triggers because of δ-rays associated with high P_t muons. Both circuit 2 and 3 do not have this problem. Circuit 3 is the most complicated and slowest one. The maximum time for setting trigger flags in this case equals to the total drift time plus the time it take for signal to travel through the half length of the shift register which can be as long as 300 ns. In the other two circuits, trigger flags are set in one clock cycle after signals from both wires are arrived at circuit inputs. Fig. 8 shows the measured threshold transitions of the circuit 2. The clock cycle used in the test is 15 ns. Without the presence of wire signals, the chip is at a static state requiring only 6 mA per chip. The current goes up to 40 mA when the chip is active.

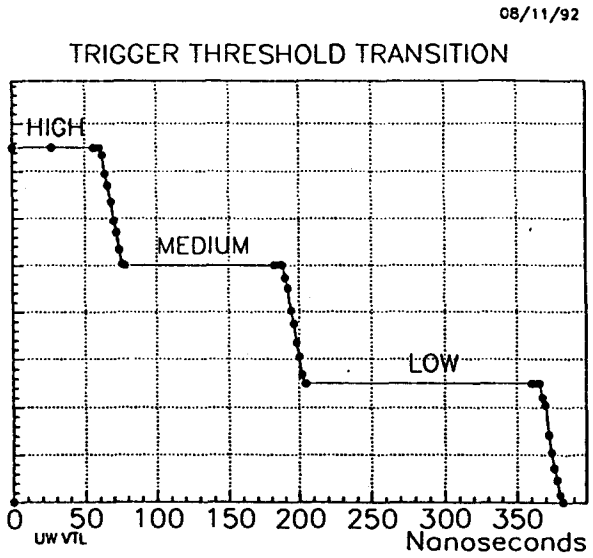

Figure 8: The threshold transitions from HIGH to MEDIUM and to LOW of circuit 2.

The total number of threshold signals is 3×16. These 48 signals are processed by a XC3064 chip. First, the neighboring tube pairs are grouped together logically. Trigger roads are then formed according to HIGH and MEDIUM or LOW threshold. Trigger flags are then set. The two out of four requirement is logically equivalent to $(T_1 \oplus T_2) \otimes (T_3 \oplus T_4)$ plus $(T_1 \otimes T_2) \oplus (T_3 \otimes T_4)$. In our trigger board, triggers using these three different trigger algorithms can be read out. Other trigger algorithms can be studied by reprogramming the XC3064 chip. The generation of the final trigger flags takes about 40 ns. The logic block diagram of the board is shown in fig. 8.

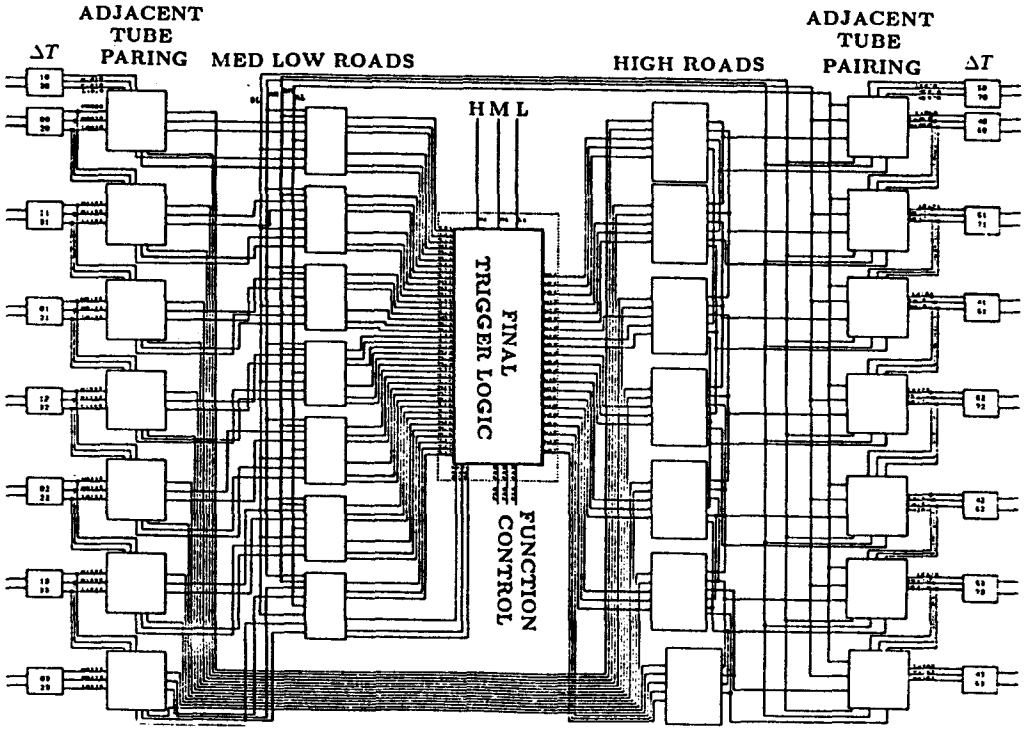

Figure 9: Block diagram of the trigger logic.

The addresses (tube pair numbers) of the trigger primitives are available for reading out. The association between the scintillator and the drift tube hits can be easily made. Such association is necessary because the 900 ns drift time corresponds to about 55 SSC beam buckets. Fast signals from a scintillation counter which are synchronized with the beam clock can be associated with the trigger flags generated by the board. Beam bunch tagging can be made this way. The concept of muon trigger is shown in fig. 10.

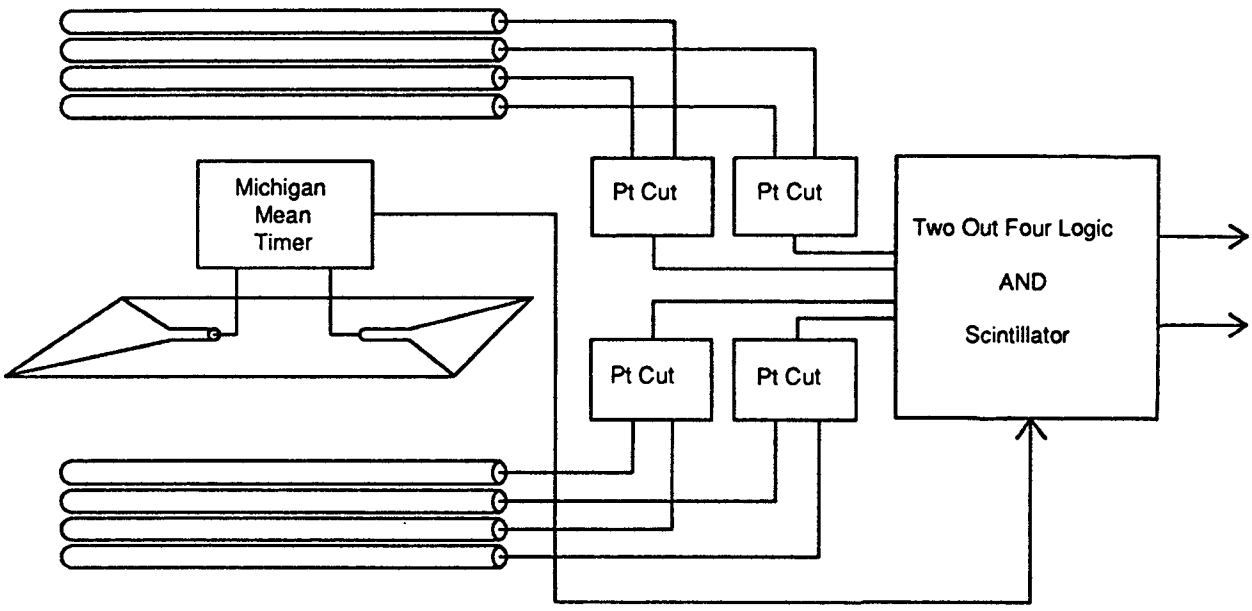

Figure 10: Level 1 Trigger Concept.

In addition, a XC3042 chip on board generates test pulse pairs of various delay time which are then distributed to the inputs of different chips. This pulse generator is operated at 65 MHz. The pulse pair separation and distribution are controlled by CAMAC commands.

4 Conclusions

A scheme of implementing the SDC first level muon trigger is demonstrated. In addition to the programmability, high speed and low power consumption, the low development cost, low chip cost and the fast turn around time are especially attractive. The complete flexibility of FPGA makes it possible to program the trigger logic after the experiment is turned on allowing us to overcome unexpected problems. This is very valuable for an expensive trigger system which will be operated for more than 10 years under different experimental conditions.

Acknowledgments

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References

[1] T. Zhao and Z. Jing, "Level 1 Muon Trigger Simulation", SDC-91-135, Jan. 1992.

[2] A. Simon and R. Thun, SDC-91-020, Jan. 1992.

[3] "Technical Design Report", SDC-92-201, SSCL-SR-1215 (1992).