CAPTURE CAVITY II RESULTS AT FNAL*

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Abstract

As part of the research and development towards the International Linear Collider (ILC), several test facilities have been developed at Fermilab. This paper presents the latest Low Level RF (LLRF) results obtained with Capture Cavity II (CCII) at the ILC Test Accelerator (ILCTA) test facility. The main focus will be on controls and RF operations using the SIMCON based LLRF system developed in DESY [1]. Details about hardware upgrades and future work will be discussed.

INTRODUCTION

Capture Cavity two (CCII) is a 9-cell high gradient TESLA Superconducting cavity intended to upgrade the existing Fermilab Photoinjector electron beam energy from 15MeV to 40Mev. DESY provided the cavity which was then shipped under vacuum to FNAL. After extensive preparation and conditioning, the cavity performed to 33MV/m at FNAL at the ILCTA test station. The first results with the complete LLRF system were presented at the LINAC 2006 conference [2]. These results include 4.5K and 1.8K operation with a 1.4 ms RF pulse and LLRF control. This current work reports on LLRF hardware and firmware upgrades and the resulting system improvements.

CAVITY TUNING

To match the ILC specifications, the cavity coupler has been adjusted to set the cavity loaded Q to $Q_L = 3.0\times10^6$. This mechanical tuning has to be performed inside the cave, outside of cavity operations. To perform frequency adjustments to the cavity and tune it to 1.3 GHz, a combination of a slow and a fast tuner are being used.

Stepper motor (slow tuner)

A stepper motor (Phytron) has been installed inside the CCII cryomodule to adjust the cavity's resonance frequency. The motor steps at 150 Hz at a tuning rate of 3690 steps / kHz. Although there is currently no read back for the motor position, controlling the motor and adjusting the cavity resonance frequency can be done remotely before RF operations.

Piezoelectric Tuner (fast tuner)

A single piezoelectric fast tuner (piezo) is also installed on the cavity and can alternatively serve as a longitudinal sensor or an actuator. This section provides an overview of some results obtained with this fast tuner at FNAL. A detailed description of the piezo and its performance on CCII is reported in [3]. The static piezo tuning range is around 1.3 kHz, corresponding to approximately 6.5 microns of cavity motion. When used as a sensor, the piezo tuner monitors the impact the RF pulse has on the cavity resonance frequency. When used as an actuator, it allows for compensation of any detuning due to the presence of Lorentz forces [4]. As shown in [3,5], exciting the cavity with a controlled mechanical stimulus milliseconds before the arrival of the RF pulse can pre-detune the cavity and effectively compensate any frequency shift induced by the RF pulse.

A phase detector was used to dynamically monitor the detuning during the RF pulse. Fig.1 shows the detuning experienced by the cavity at a gradient of 26.2 MV/m with and without piezo compensation. For these results, the cavity Q_L was measured to be around 2.0×10^6, the LLRF is running closed loop with a feedback gain around 20 and the flat top duration is 700 µs. As can be seen in Fig.1, without piezo compensation, the cavity experiences a resonance frequency drift in the order of 275 Hz. With the piezo correction this is reduced to approximately 20 Hz [3].

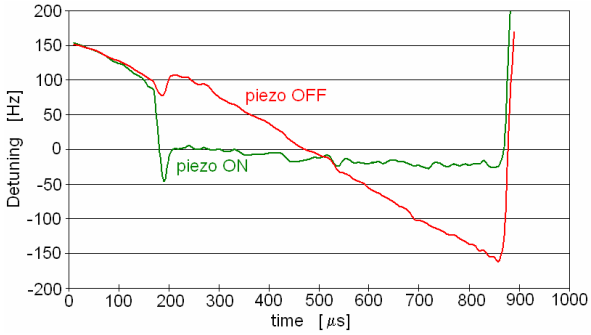

Figure 1: Cavity resonance frequency shift induced by Lorentz forces, without (red) and with (green) piezo compensation.

Furthermore, the piezo correction minimizes the required forward power while keeping the cavity gradient constant during the RF pulse. This has a beneficial impact for the feedback control of the LLRF and optimizes the RF power headroom, which can be critical when driving several cavities from a single klystron, as reported in [3]. In the plot shown above, the additional forward power required to maintain a flat top during the RF pulse peaks around 29% of the total forward power when no piezo

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correction is applied. This figure drops to 2% with the help of piezo compensation. The starting time and the amplitude of the piezo stimulus are adjusted to compensate Lorentz force detuning as the cavity gradient increases. Current work includes compensating Lorentz force detuning at higher gradients. Future work includes automation of the piezo control system.

LLRF UPGRADES

Hardware upgrades

The decision was made to move away from the 250 kHz direct IQ sampling scheme and to perform data sampling at a higher intermediate frequency (IF=13 MHz) [6]. To accommodate for this change, a new receiver was designed to perform the down conversion of the cavity probe signal from RF=1300 MHz to IF=13 MHz [7]. To account for the phase information, a 1.3 GHz signal coming from the master oscillator is also down converted to IF as a phase reference input to the SIMCON cavity controller. The local oscillator frequency 1313 MHz is generated locally, inside the receiver, while the master oscillator provides the 1.3 GHz and the 13 MHz signals. The block diagram of this new module is presented in Fig.2.

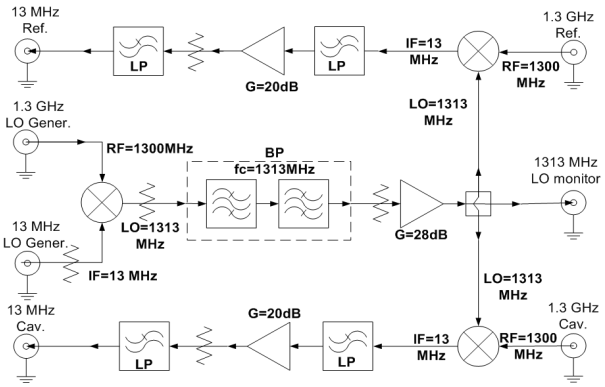

Figure 2: Block diagram of the 13 MHz IF receiver [7].

The master oscillator design is based on a 10 MHz crystal from Wenzel Associates used as a phase lock loop (PLL) reference for a 1300 MHz dielectric resonator oscillator (DRO) from Poseidon Scientific Instruments. The RF frequency is then divided down by a cascade of three low-jitter clock distribution chips from Analog Devices (AD9510) to provide the required frequencies. The MO provides a 1300 MHz signal with a phase noise of -93 dBc/√Hz at 100 Hz and -125 dBc/√Hz at 10 kHz. A detailed description of the master oscillator and its phase noise specifications was reported in a previous work [8]. The AD9510 is a programmable clock distribution chip that requires configuration at power up. This is performed through the chip serial port using an 8-bit PIC microcontroller (PIC12F675) from Microchip. This microcontroller is also used to send a pulse signal to synchronize the chip clock outputs. A schematic layout of the master oscillator is given in Fig.3.

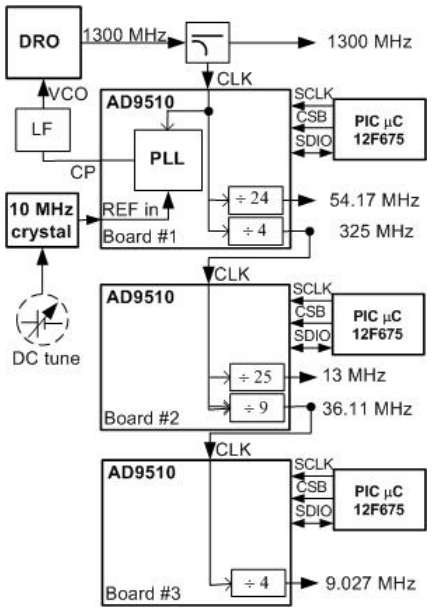

Figure 3: Master oscillator block diagram.

The LVPECL 54.17 MHz differential signal is used as an external clock for the ADCs of the SIMCON3.1 controller. The 9.028 MHz signal is sent to the timing module which provides in turn a 1 Hz repetition rate probe and a 1 MHz trigger to the SIMCON board. The 13 MHz output is the IF frequency used in the down conversion process taking place at the receiver. A good design practice consists of choosing a non-integer relationship between the ADC sampling frequency f_s and the IF frequency. In the scheme described above, we have f_s / IF = 6/25. This non IQ sampling scheme ensures strong linearity out of the ADCs. Preliminary results show the benefits of down converting the cavity probe signal to a higher IF. An RMS noise of 0.06% in amplitude and 0.07° in phase was measured on the digitized I and Q signals. Future plans include using a higher IF at the controller output as well. Currently, the SIMCON I and Q output signals are DC levels. A higher IF modulation of the RF frequency carrier should yield a quieter drive signal.

LLRF controller upgrades

In an effort to improve the noise associated with the SIMCON 3.1 hardware, Fermilab has been redesigning parts of the controller board [9], migrating from a VME32 to a VME64 crate standard. More specifically, the ADC front end has been redesigned, using dual channel 14 bits ADCs, optional DC coupling and replacing the input differential amplifiers with RF pulse transformers. The power distribution has been modified using a combination of DC-to-DC converters and regulators to minimize the

noise, the main FPGA has been upgraded from a Xilinx Virtex II Pro to a Virtex IV and the clock distribution has been redesigned for lower jitter and better layout. An internal PLL provides the clock for the ADCs and uses a reference clock signal provided by the master oscillator. Preliminary results show a SNR of 81 dB and an ENOB of 13.1 bits.

Firmware upgrades

In parallel, Fermilab has been working on integrating and modifying the SIMCON firmware originally developed at DESY. The down conversion to base band is now performed through a Numerically Controlled Oscillator (NCO) followed by a CIC filter. A combination of Simulink® and Sysgen® tools has been successfully used to build off from the original VHDL firmware and implement the additional features mentioned above. A schematic layout of the FPGA processing is depicted in Fig. 4.

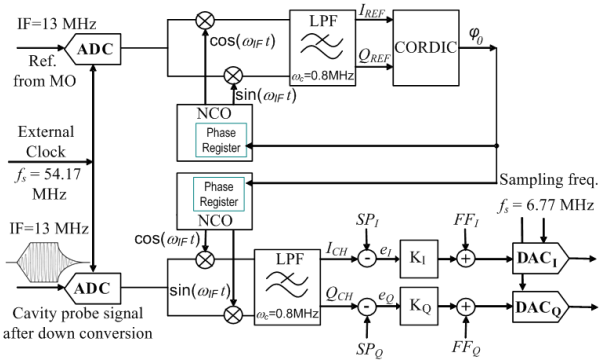

Figure 4: Digital down conversion scheme, performed by the SIMCON FPGA [6].

The current SIMCON firmware imposes an upper bound on the external clock frequency around 54 MHz. Future developments of the SIMCON firmware include removing this hard coded limit on the choice of external clock frequency. Another improvement consists of moving away from the use of the 1 MHz signal to clock internal FPGA operations. This will remove some of the process latency associated with the current firmware.

CCII STATUS

Recent CCII studies at ILCTA have identified some electron emission taking place at the input coupler of the cavity. This generates an arc when running at gradients above 16 MV/m. More information about operations with CCII and this electron activity issue can be found in [10].

For development purposes, the LLRF controls interface for the 13 MHz down conversion scheme described above is based on MATLAB®. Future plans include developing a graphical interface in the DOOCS environment, running on an INTEL based X86 VME controller, to replace the current Solaris unit.

CONCLUSION

This paper reports on the past and current studies performed with capture cavity 2 at the ILCTA test facility at Fermilab. The cavity is tuned using a slow stepper motor tuner, to adjust its resonance frequency to the ILC specification value of 1.3 GHz. Its coupling coefficient is also adjusted to meet the ILC loaded Q value of $Q_L = 3.0\times10^6$. A fast piezo electric tuner is used to understand the cavity mechanical modes during continuous wave (CW) operations, and to dynamically compensate Lorentz force detuning by pre-detuning the cavity just before the RF pulse. Preliminary results show that the additional forward power necessary to maintain a flat top during the RF pulse can be dramatically reduced when compensating Lorentz force detuning with the piezo fast tuner. The low level RF system is also changing from its original design, moving toward a higher intermediate frequency to down convert the cavity power signals, and to improve the overall system noise performance. Hardware and firmware changes have been presented in this work. The current system design is being used at difference test stations at FNAL and is expected to be used for future projects such as at the New Muon Laboratory test facility, where a total of three ILC type cryomodules and 24 CCII-like cavities are expected to be installed.

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