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Luminosity and beam-induced background measurement with the CMS Tracker Endcap Pixel Detector at HL-LHC

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Abstract. The High-Luminosity upgrade of the LHC (HL-LHC) places unprecedented requirements for background monitoring and luminosity measurements. The CMS Tracker Endcap Pixel Detector (TEPX) will be adapted to provide high-precision online measurements of bunch-by-bunch luminosity and beam-induced background. The implementation of dedicated triggering and readout systems, the real-time clustering algorithm on an FPGA and the expected performance are discussed.

1. Introduction

The CMS detector [1] will undergo a so-called Phase-2 upgrade [2] to meet the challenges imposed by the HL-LHC [3] operational conditions. Many of the instruments operated by the CMS Beam Radiation Instrumentation and Luminosity (BRIL) project during Runs 2 and 3 will have to be replaced [4] for HL-LHC. In addition to new dedicated luminosity instrumentation being designed, BRIL is also planning to extensively utilize the trigger data streamed from the other CMS subsystems at the bunch-crossing rate. Among the newly proposed luminosity measurement sources are the trigger paths of the Outer Tracker (OT), the muon systems, as well as the recently introduced 40 MHz level-1 (L1) trigger scouting system [5]. Another important subsystem in the scope of the BRIL Phase-2 luminosity upgrade is the Tracker Endcap Pixel Detector (TEPX), which is described further in these proceedings.

The upgraded TEPX will be located in the very forward extremity of the Inner Tracker (IT) volume, spanning a $|z|$ range from 175 to 265 cm and a radius between 63 and 255 mm. It will be composed of four large double disks per CMS side, each made up of five rings with a varying number of pixel modules. The occupancy in TEPX will be relatively low with respect to other parts of the IT (less than 10^{-3} [6]). This will allow the usage of the headroom in readout bandwidth for the luminosity measurement by sending dedicated luminosity triggers in addition to the nominally 750 kHz of L1 triggers for physics. The data corresponding to those luminosity triggers can then be separated from the normal data acquisition stream for online processing in a dedicated luminosity processing system. In addition, the innermost ring of the last disk in $|z|$ (D4R1) is beyond $|\eta| = 4$ and, because of the very few tracking points at that pseudorapidity, it is outside the nominal acceptance for efficient tracking. This will provide a possibility to exclusively use this part of the detector for luminosity and beam-induced background measurements utilizing the full trigger bandwidth.

2. Back-end electronics

The back-end system of the IT will consist of a set of ATCA cards, the so-called IT Data, Trigger and Control boards (IT-DTC) connected to the front-end electronics using optical links. The hardware platform for the IT-DTC is the so-called Apollo board [7], which among other elements hosts a System-on-Chip (SoC) and two processing FPGAs. The Xilinx Virtex Ultrascale+ VU13P FPGA is currently the prime candidate for the processing FPGAs. The back-end card will control and monitor the front-end modules, and acquire the triggered event data. Through the DAQ and TCDS Hub (DTH) placed in each crate, physics data from the IT-DTCs will be forwarded to the central CMS DAQ system.

The luminosity triggers will be generated by the so-called BRIL Trigger Board (BTB) and distributed to all CMS subsystems via the Phase-2 TCDS2 system [8]. The front end itself is totally agnostic to the type of trigger. The decision to forward an event fragment to either the central DAQ or the luminosity processing system will be taken at the IT-DTC level according to the trigger type sent by the TCDS2 system. Figure 1 illustrates the data flow within the TEPX system based on the kind of trigger.

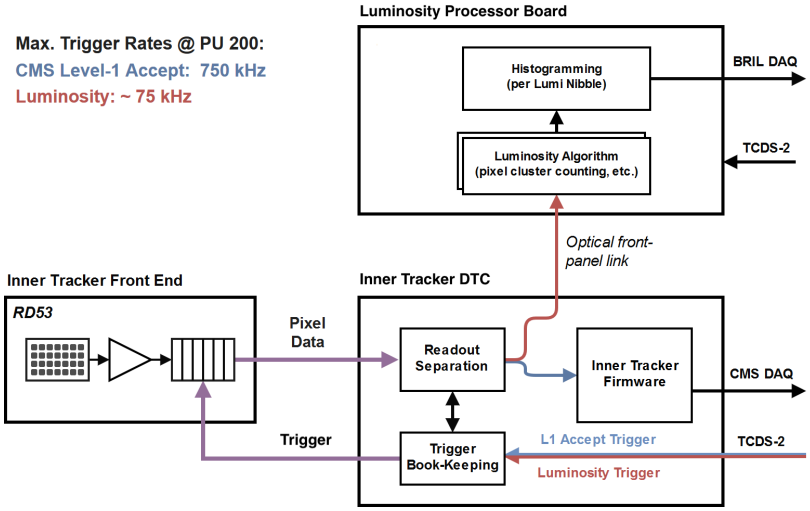

Figure 1. Block diagram of the data flow based on trigger types in the TEPX system [4].

3. Luminosity processing

The luminosity event fragments from the IT-DTC will be received by dedicated luminosity processing blades also based on the Apollo board, but utilizing independent firmware to perform real-time pixel cluster counting on its processing FPGAs. The IT-DTCs and luminosity blades will connect to each other through optical links on a one-to-one basis, so no duplication or sharing of data is necessary. After unpacking of the event data on the luminosity blades, the per-chip events will be distributed to the instances of the pixel cluster counting algorithm. Cluster counts for each event will be then grouped and summed per TEPX quarter ring and the total counts for each quarter ring will be transferred to the histogramming instances. The latter will transfer the accumulated histograms to the on-board SoC and further to the BRIL computing farm at the end of each integration period.

3.1. Pixel cluster counting algorithm

The BRIL-operated D4R1 read-out modules will be receiving triggers at a maximum rate of 1 MHz at at an average pileup of 200, which defines the minimal required event processing rate.

Larger trigger rates are possible during the Van der Meer (VdM) scans [4], when the sensor occupancy is significantly lower. On the one hand, the D4R1 will contain only 20 modules (80 chips) per z side that will be read out by a single IT-DTC. On the other hand, the IT-DTCs corresponding to the rest of TEPX will send event data from up to 704 chips per IT-DTC at a significantly lower trigger rate. Therefore, the FPGA pixel clustering module has to be fast to handle the D4R1 data and light in terms of FPGA resources utilized to handle the data from the rest of TEPX.

A test algorithm has been developed to prove the feasibility of the aforementioned task. Two hits were defined to form a cluster if they are horizontally, vertically, or diagonally adjacent. Thus, it is enough for them to share a single corner to form a cluster. The algorithm does not use the hit charge information from the front end and does not store cluster geometry information, such as cluster position or size, thus performing only cluster counting. The algorithm is split into six sequential processing stages operating at 320 MHz clock rate and performs tasks such as the chip data decoding, clustering of 4×4 pixel fragments, checking cluster isolation, merging of vertically adjacent clusters and merging of horizontally adjacent clusters. The latter three stages keep internal cluster counts for filtering nonadjacent clusters. Therefore, the next and last processor in this chain performs accumulation of the internal counts. Five out of the six described processing stages contain input buffers and finite state machines to perform the processing. Each input buffer implements a back-pressure mechanism to pause the processing in the earlier stages when the buffers in the later stages are close to overflow. This results in a dynamic buffer load balancing for compensating events containing larger clusters.

3.2. Algorithm performance

In order to qualify the performance of the algorithm, 1000 events simulated with an average pileup of 200 for the whole TEPX were split into 5 465 718 single chip events with at least one hit, and were injected into the clustering algorithm sequentially with a mean trigger rate of 1 MHz. The fraction of events where the calculated cluster count did not match the one obtained from the reconstruction algorithm used in the CMS offline reconstruction was measured to be 0.021%. In the events with mismatched counts, a typical mismatch is by one cluster. A significant fraction of the mismatched counts are expected to be caused by the fact that the offline algorithm uses charge information to apply thresholds and discard hits, which causes cluster splitting. Certain known limitations of the present algorithm may also cause some of the mismatches in the cluster count, whilst they will be eliminated in the final version of the algorithm.

The effect of various pileup conditions was studied by injecting the simulated event data for average pileup values in the range from 1 to 200 with a mean trigger rate of 1 MHz. In Fig. 2, the mean cluster count (left) and fraction of mismatched events (right) are shown as functions of pileup for TEPX D4R1. As expected, both values grow linearly with pileup.

In order to prove that the algorithm is capable of handling the required event rates, the mean event processing time was measured as a function of pileup and was later converted into the maximum trigger rate, as shown in Fig. 3. The maximum trigger rate at an average pileup of is 1.33 ± 0.44 MHz. This fully satisfies the requirements and also provides sufficient margins. A relatively wide standard deviation of the event processing time, and consequently the processing rate, is caused by larger clusters which require more processing time.

The number of algorithm instances sufficient to process data from a single IT-DTC (up to 704 chips) was placed on the VU13P FPGA. The resulting implementation did not contain any failing timing path and utilized only 45 % of logic resources and 27 % of memory resources. The present implementation of the algorithm can be easily placed on the target FPGA, and sufficient space is available for further improvement of the algorithm.

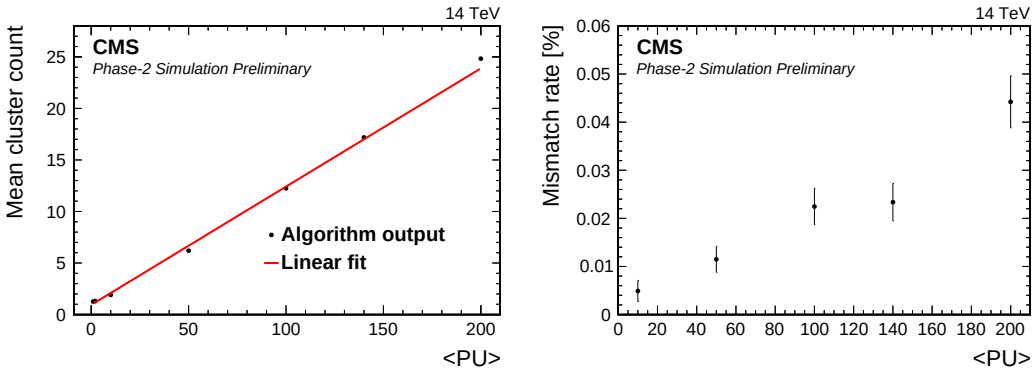

Figure 2. Mean per event cluster count (left) and fraction of mismatched events (right) at different pileup conditions for disk 4 ring 1 (D4R1) of TEPX.

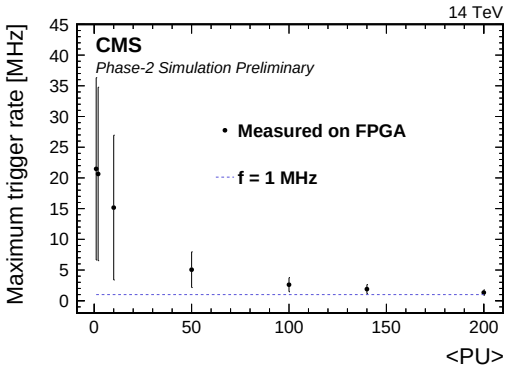

Figure 3. Calculated maximum trigger rate at different pileup conditions. The error bars represent the standard deviation of the distribution. The blue dashed line indicates a trigger rate of 1 MHz.

Summary

In order to prove the feasibility of using TEPX in real-time luminosity and beam-induced background measurements, a prototype version of the FPGA pixel cluster counting algorithm has been implemented and tested. The developed algorithm is fully able to perform online cluster counting at the required event rate of 1 MHz and provides cluster counts consistent with the ones obtained from the more precise offline reconstruction algorithm, with a low fraction of mismatches. Sufficient FPGA resource margin is available for further improvement of the algorithm. In particular, charge information and geometrical properties of clusters will be considered in the final implementation. The algorithm can already be used for luminosity measurement, however, in order to estimate with improved precision the deviation from linearity, more simulation samples should be produced and injected.

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