

New pixel-detector technologies for the ATLAS ITk upgrade and the CLIC vertex detector

VICENTE BARRETO PINTO, Mateus

Abstract

Characterization of novel silicon pixel detectors based on the new HV-CMOS technology, for the ATLAS ITk upgrade and the future CLIC vertex detector. Both ATLAS ITk and the CLIC vertex detectors are designed with high demanding requirements, pushing to the limits the standard technologies used for silicon pixel detectors. The new HV-CMOS technology allows implementing a sensor and read-out device in the same silicon substrate, combining the high-voltage performance of planar silicon sensors with the signal amplification and digitization of dedicated read-out chips, eliminating the need of the detector hybridization. HV-CMOS monolithic prototypes have been investigated for implementation in the ATLAS ITk detector, while HV-CMOS devices implemented as capacitively coupled pixel detectors (CCPD) were investigated for the CLIC vertex detector. Monolithic and CCPD prototypes were simulated and tested with particle beams. Detection efficiencies above 99%, before and after irradiation, were measured, endorsing the technology to be used in future detectors.

Reference

VICENTE BARRETO PINTO, Mateus. *New pixel-detector technologies for the ATLAS ITk upgrade and the CLIC vertex detector*. Thèse de doctorat : Univ. Genève, 2019, no. Sc. 5382

DOI : 10.13097/archive-ouverte/unige:140896

URN : urn:nbn:ch:unige-1408969

Available at:

<http://archive-ouverte.unige.ch/unige:140896>

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New pixel-detector technologies for the ATLAS ITk upgrade and the CLIC vertex detector

THÈSE

présentée à la Faculté des sciences de l'Université de Genève
pour obtenir le grade de Docteur ès sciences, mention physique

par

Mateus Vicente Barreto Pinto

Rio de Janeiro - Brésil

Thèse N° 5382

GENÈVE 2019



**UNIVERSITÉ
DE GENÈVE**

FACULTÉ DES SCIENCES

DOCTORAT ÈS SCIENCES, MENTION PHYSIQUE

Thèse de Monsieur Mateus VICENTE BARRETO PINTO

intitulée :

**«New Pixel-Detector Technologies for the ATLAS ITk Upgrade
and the CLIC Vertex Detector»**

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ABSTRACT

This thesis contains the Ph.D. work done on the characterization of novel silicon pixel detectors, based on the new HV-CMOS technology, for the ATLAS ITk upgrade and the future CLIC vertex detector. In order to provide the best precision and accuracies for the respective ATLAS and CLIC physics measurement plans, both ATLAS ITk and the CLIC vertex detectors are designed with high demanding requirements, pushing to the limits the standard technologies used for silicon pixel detectors.

Current silicon pixel detectors are built using a standard planar silicon sensor coupled to a read-out chip via bump-bonds, demanding the design of two different devices and the coupling process between them, called hybridization. The new HV-CMOS technology allows implementing a sensor and read-out device in the same silicon substrate, combining the high-voltage capabilities of planar silicon sensors with the signal amplification and digitization of dedicated read-out chips, eliminating the need of the detector hybridization.

The current ATLAS vertex and tracker detectors will be replaced by an all-silicon detector, covering a total area of a few hundred square meters, meaning the need of many detector modules to be designed, produced and assembled. In addition, with the higher irradiation levels to come with the High Luminosity LHC upgrade, the detector needs to have a higher radiation-hardness, while keeping the same performance of the current detector. The CLIC vertex detector, on the other hand, does not have a problem with radiation tolerance due to the nature of its electron-positron collisions. Nevertheless, to achieve the high precision physics measurements targeted, the detector module needs to be very thin ($< 100 \mu\text{m}$) and designed with small pixel sizes ($25 \mu\text{m}$), which current detector hybridization technologies are not fully capable to provide with the necessary production yield.

HV-CMOS monolithic prototypes have been investigated for implementation at the outer pixel layers of the ATLAS ITk detector, helping with the detector design and production time. For the CLIC vertex detector, HV-CMOS devices are investigated for implementation as capacitively coupled pixel detector (CCPD) modules, where the hybridization between the sensor and read-out devices is done via a thin layer of a dielectric glue, instead of the expensive and complex bump-bonds. In addition, the capacitive coupling of the sensor to the read-out allows having pixel sizes smaller than what currently bump-bonding techniques can provide, contributing to the miniaturization of the pixel size and, therefore, increasing the achievable detector pointing resolution.

The usage of the HV-CMOS technology is first analyzed with Finite Element simulations regarding the coupling between the sensor and read-out electronics (for CCPD prototypes), continuing with the process of detector assembly into modules and, finally, the detector module performance is tested using dedicated particle beams tests in different test-beam facilities. The UniGE FE-I4 particle telescope, necessary for the tracking of the particle beam as it goes through the prototypes, was used and improved regarding the automatization of performance measurement scans and support for different electrical and mechanical requirements of different prototypes.

The capacitive coupling process was optimized using a semi-automated flip-chip machine. A planarity in the order of a few hundred μrad was achieved, with an alignment accuracy $< 2 \mu\text{m}$ between the two devices. The cross-talk among multiple coupled pixel-pairs was simulated and found to be $< 4\%$ for the prototype investigated for the CLIC vertex, while an ATLAS CCPD prototype simulation, with a pixel pitch 2x larger than the CLIC prototype, resulted in a cross-coupling $< 0.5\%$.

The HV-CMOS prototypes investigated on test-been has shown good performance before and after irradiation. The fully monolithic HV-CMOS ATLAS prototype has shown a detection efficiency of 99.7% measured before irradiation, when tested with a high voltage reversed bias of 60 V and low signal threshold of about 750 electrons. After irradiation up to a dose of $10^{15} n_{eq}/\text{cm}^2$, the efficiency has decreased slightly to 99.2%, with 90 V high-voltage bias and a detection threshold equivalent to 1000 electrons.

The results from the different HV-CMOS detector prototypes, concerning production and performance, has indicated that the HV-CMOS technology is suitable for its application in future high-energy particle collision experiments, such as the outer layers of the ATLAS ITk upgrade as well as for the future CLIC vertex detector.

RÉSUMÉ

Ce travail de doctorat porte sur la caractérisation de nouveaux détecteurs silicium pixelisés, basés sur la technologie HV-CMOS, pour la mise-à-jour du trajectomètre du détecteur ATLAS (ITk) et le détecteur de vertex de CLIC. Afin de fournir la meilleure précision de détection pour le programme de physique de CLIC et ATLAS, ces deux détecteurs requièrent une précision accrue poussant à leurs limites les technologies existantes.

Les détecteurs silicium pixelisés actuels consistent de senseurs planaires en silicium, couplés à une électronique de lecture à l'aide de micro-soudures Sn-Ag ou Sn-Pb, nécessitant le design des deux composants ainsi que le développement d'une méthode d'hybridation. La

technologie HV-CMOS permet l'implémentation monolithique d'un senseur et son électronique de lecture sur le même substrat de silicium et combine les capacités de résistance à la haute-tension des senseurs planaires et l'amplification de faibles signaux normalement implémentés dans l'électronique de lecture, éliminant le besoin pour l'hybridation des deux composants. De plus, l'amplification des petits signaux dans le même substrat permet d'explorer l'hybridation par couplage capacitif, qui nécessitent de plus grands signaux que ceux produits par les senseurs planaires actuels.

Le trajectomètre du détecteur ATLAS actuel sera remplacé par une nouvelle mouture, le ATLAS ITk, complètement basé sur la technologie silicium et couvrira une surface de l'ordre de cent mètres carrés, nécessitant le design, la construction et l'assemblage d'un grand nombre de modules de détection. De plus, le niveau de radiation présent au point de collision après la mise-à-jour haute luminosité du LHC impliquant une exposition accrue du détecteur aux radiations, une plus grande tolérance à ceux-ci sera requise du nouveau détecteur afin de conserver les mêmes performances au cours de son opération. Dans le cas de CLIC, les niveaux attendus de radiation étant plus raisonnables, l'accent sera mis sur la précision des mesures effectuées avec le détecteur. Des détecteurs plus minces ayant de plus petits pixels seront donc requis, au-delà des capacités de la technologie actuelle.

De nouveaux prototypes monolithiques utilisant la technologie HV-CMOS ont été étudiés pour utilisation dans les couches externes du détecteur ATLAS ITk afin de simplifier l'assemblage de cette couche de large surface. La technologie fut aussi employée pour le design de nouveaux senseurs pour couplage capacitif à leur électronique de lecture. Le couplage entre le senseur et l'électronique étant établi grâce à une fine couche de matériel diélectrique (colle) entre les canaux au lieu des microsoudures normalement utilisées. Ce couplage ne nécessitant pas de procédés lithographiques, il permet ainsi de réaliser une hybridation avec un pas de pixel réduit par rapport aux techniques standards. Une meilleure résolution peut donc être atteinte.

Le couplage capacitif entre les canaux fut d'abord étudié grâce à la simulation par éléments-finis. L'information recueillie fut utilisée pour guider le processus de fabrication et la simulation Monte-Carlo des expériences en faisceaux réalisées avec les prototypes. Le télescope FEI4 fut utilisé et amélioré pour optimiser les mesures à effectuer avec les prototypes. De nouvelles structures thermomécaniques furent produites pour refroidir et opérer les prototypes après irradiation.

Le processus d'assemblage des prototypes par couplage capacitif fut optimisé à l'aide d'une machine de placement fin semi-automatique. Une co-planéité de l'ordre d'une centaine de microradians fut atteinte, avec une précision de placement de moins de $2\text{ }\mu\text{m}$. La diaphonie entre les pixels fut simulée et mesurée en dessous de 4% pour les pixels

fins dédiées à CLIC, et moins de 0.5% pour les pixels plus grossiers d'ATLAS ITk.

Les échantillons étudiés en tests faisceau ont démontré une bonne performance après irradiation, comme requis pour l'usage dans le détecteur ATLAS ITk. Le prototype monolithique dédié à ATLAS atteint une efficacité de détection de 99.7% avant irradiation, pour une tension appliquée de 60 V et un seuil de détection de 750 électrons équivalents. Après irradiation à une dose de $10^{15} n_{eq}/cm^2$, l'efficacité reste suffisante à 99.2% avec 90 V de tension appliquée pour un seuil de détection de 1000 électrons équivalents.

Les résultats obtenus avec les différents prototypes basés sur la technologie HV-CMOS, en termes de facilitation de la production et des performances attendues, démontrent que la technologie est viable pour l'utilisation dans de futures applications en physique des hautes énergies comme la mise-à-jour du trajectomètre d'ATLAS et le détecteur de vertex de CLIC.

*There is a theory which states that if ever anyone discovers exactly what the Universe is for and why it is here, it will instantly disappear and be replaced by something even more bizarre and inexplicable.
There is another theory which states that this has already happened.
The Hitchhiker's Guide to the Galaxy by Douglas Adams*

ACKNOWLEDGMENTS

This thesis is the successful and happy conclusion of my time as a Ph.D. student at Geneva University. Thank you, Prof. Giuseppe Iacobucci, for taking me as a student and for supporting me, providing all the great resources available from the university, so I could make the best of my Ph.D. It was a privilege to be able to learn and work with the high-quality research staff and laboratory from the Department of Nuclear and Corpuscular Physics. Thank you, Peppe. I am sure it has significantly boosted my career as a physicist. Many thanks to Dr. Mathieu Benoit, for bringing me the possibility of a Ph.D. at UNIGE and for helping me to be awarded with the Excellence Scholarship from the Swiss government. I will always be thankful to you, Mathieu, for always being around with the amazing expertise and friendship. Also, many thanks to the DPNC administrative and technical staff for helping me with all the support and knowledge.

My Ph.D. at UNIGE was also supported by the CERN Linear Collider Detector group. I want to thank Dr. Lucie Linssen for hosting me at CERN. It was a big differential in my career to be able to be a student at Geneva University while being fully based at CERN, meeting all world experts around the hallways, being able to learn from close to them, and also expose my ideas for debate. Thank you, Lucie, for all the support, and as well as for the fun times sailing around the lake. Big thanks also to Dr. Dominik Dannheim for always being available, guiding and helping me to improve the quality of my work.

I will not forget the many friends that I have made. Among all office mates, fellow master and doctoral students, post-docs gurus and so on, I want to give a special thanks to the UNIGE post-doc Dr. Moritz Kiehn, for all the help in the test-beam tracking and analysis, and thanks also to CERN fellow Dr. Simon Spannagel for the help programming my simulations into the Allpix Squared framework. I have always tried to hear and learn as much as I could from everyone, and I can say that I had the best luck with all the people around me.

I also want to thank my family. Being away from Brazil, where all family and friends are, was easier with the help of the love of my life, my wife Carolina. She was crucial for my Ph.D. to be the way it was. I could not be happier to conclude this phase by her side, at the same time as we start our own family with our first son, Gustavo. I love you both and everything is for you. Of course, many thanks for my parents and brother who always believed in me and my career, giving me unconditional support and love, even if it was to go further to the other side of the ocean, so I can be the best that I can. I love you all.

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Part I

INTRODUCTION TO HIGH ENERGY PHYSICS

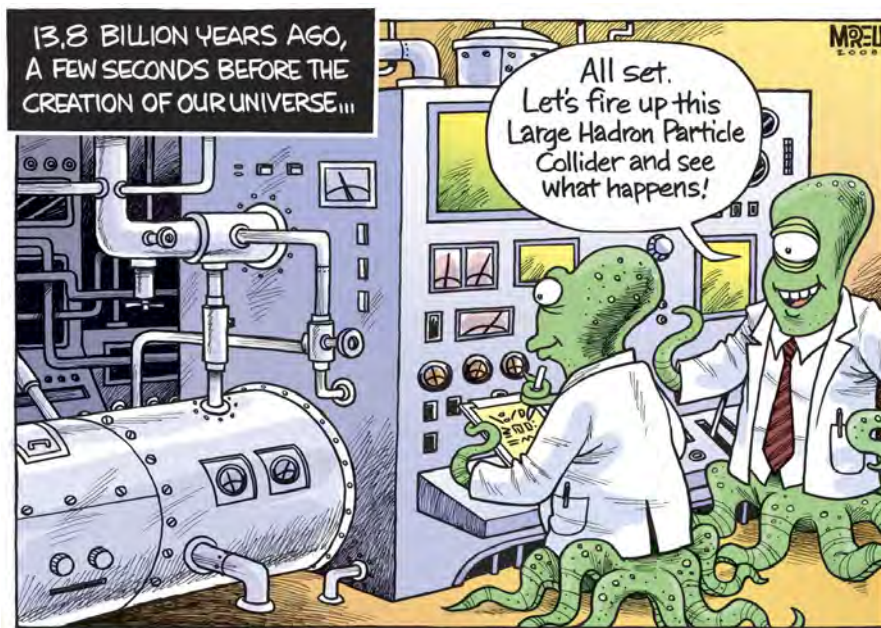


Image credit: Mike Moreu

This part of my thesis is to give a general introduction to High Energy Physics (HEP), and why we make experiments colliding particles. An introduction to the CERN particle accelerators and detectors provide the context in which this work was carried out.

INTRODUCTION

1.1 THE STANDARD MODEL OF PARTICLE PHYSICS

The Standard Model of particle physics (SM) [1] is the most accurate theory regarding the description of the universe as we know. The theory models how the most basic, elementary, building blocks of matter are created and interacts with each other through specific forces. The theory has passed all tests providing accurate predictions, such as the mass of the W and Z bosons, but yet there are open mysteries that the SM can't explain.

The SM describes how elementary particles (and their respective anti-particles), illustrated in Figure 1.1, interact with each other, modeling several phenomena from the big-bang to the evolution of galaxies. The particles can be organized into two groups, *Fermions* and *Bosons*, as described following.

Predicted vs measured W^\pm and Z^0 mass, in GeV [2].

Mass Boson	Measured	Predicted
W^\pm	80.387 ± 0.016	80.361 ± 0.006
Z^0	91.1876 ± 0.0021	91.1880 ± 0.0020

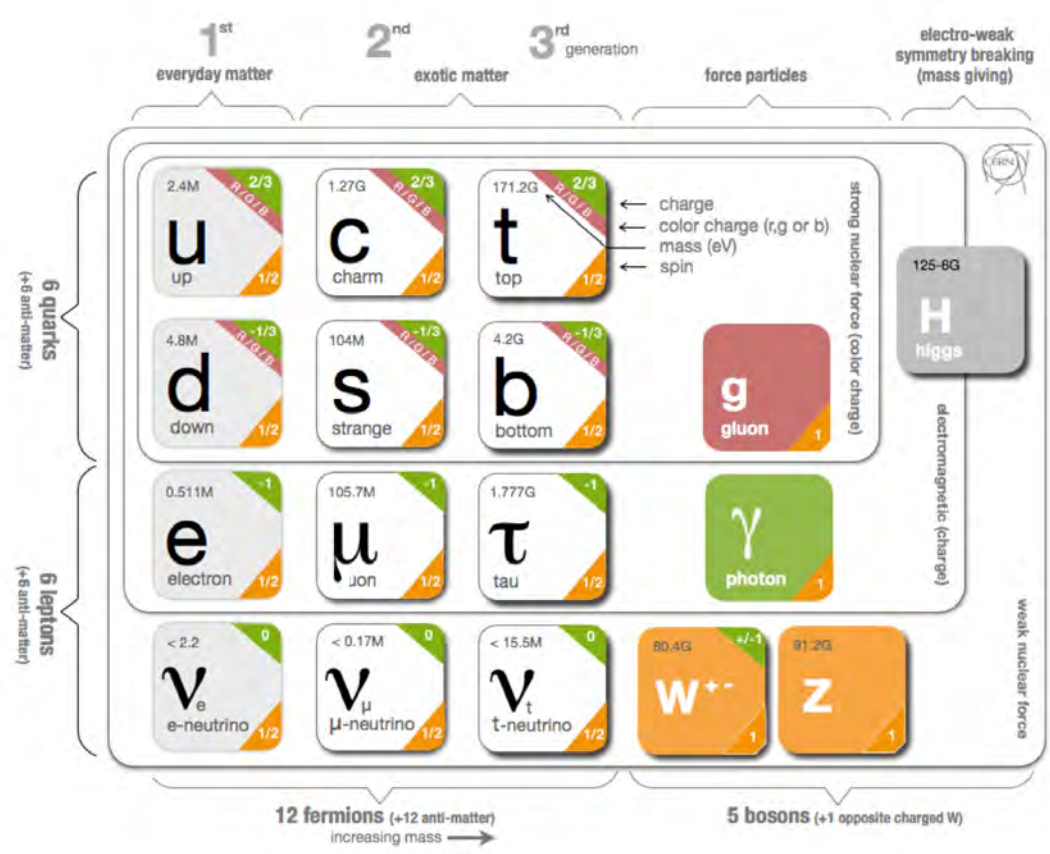


Figure 1.1: The elementary particles of the Standard Model [3].

Fermions

Fermions are particles with spin of $1/2$ and follow the Fermi–Dirac statistics. There are two types of elementary fermions, named *leptons* and *quarks*. Fermions are also divided into 3 generations, with newer generations being heavier than previous ones. Each fermion has its respective anti-particle, differing from its pair by having opposite physical charges, such as the electric charge in electromagnetism or the color charge in quantum chromodynamics, and inverted quantum numbers, such as baryon and lepton numbers.

Leptons The *leptons* are the stable *electron*, e^- , that surrounds the atom nucleus, and the *electron neutrino* ν_{e^-} (electrically neutral); the *muon*, μ^- , with the same properties as the electron but being heavier, and the *muon neutrino* ν_{μ} ; and the even heavier (3rd generation) *tau*, τ^- , and its respective *tau neutrino* ν_{τ} .

Quarks Due to the confinement phenomena [4], *quarks* are elementary particles that are found in nature always forming a *meson* (one quark combined with an anti-quark) or a *baryon* (combination of three quarks). In addition to its fractional electric charge ($2/3$ or $-1/3$ with respect to the electron charge), quarks also possess a *color* charge (red, green or blue), which is a property related to strong force in quantum chromodynamics (QCD). First generation quarks are the *quark up*, u , and *quark down* d , that combined can form *protons* (uud) and *neutrons* (udd), both baryons. The different combinations between first generation quarks and electrons form all the atoms that are present on the periodic table. Second generations quarks are the quark *strange* and *charm*, and third generation quarks are the *bottom* and the *top* quarks, the most massive elementary particle.

Bosons

The *bosons* have integer spin and follow the Bose–Einstein statistics. They include the spin 1 carriers of the electroweak and strong forces, as well as the spin 0 Higgs boson.

Photons *Photons*, γ , are responsible for carrying the electromagnetic force, being responsible for many macroscopic phenomena such as friction, diffraction or chemical bonding strengths. Photons couple, or interact, to all particles with electric charge and, as it is mass-less, it has an infinite range.

Z^0 and W^\pm The weak force, responsible for atomic radioactive decay, and therefore having an essential role in nuclear fission, is mediated by the electrically neutral Z^0 and the electrically charged W^\pm

bosons. The free neutron decay happens with an emission of a W^- boson from one of the *down* quarks within the neutron, while the *down* quark transforms into an (lighter) *up* quark, converting the neutron into a proton; the W^- subsequently decays into a (beta) electron and an anti-neutrino. The weak force acts upon all SM fermions and has a range of about $10^{-18} m$.

Gluons *Gluons*, g , are the mediators of the strong force and couple only with color charged particles (quarks), including them self as they also carry color charge. The strong force is responsible for binding quarks together, resulting in composed particles, such as baryons and mesons. The strong force, as the name indicates, is the strongest force in the nature, overcoming the electrostatic repulsion of protons within the atomic nucleus.

Higgs The *Higgs* boson [5], a visible manifestation of the Higgs field, was the last SM piece missing and an ultimate test for the theory. A priori the SM, as a gauge theory, predicts that all particles should be mass-less, which isn't true. A symmetry-breaking mechanism was then proposed in 1964 within three papers: one written by Peter Higgs, another by François Englert and Robert Brout, and a third by Gerald Guralnik, C. Richard Hagen, and Tom Kibble and. After the discovery of the Higgs boson by the ATLAS [6] and CMS [7] experiments in 2012, the mechanism was incorporated into the SM of particle physics.

The Higgs mechanism predicts that any particle that interacts with the Higgs field will acquire a specific mass, proportional to the particle-field interaction coupling. In the SM, photons don't couple with the Higgs field and, hence, are massless. Figure 1.2 shows a Feynman diagram of a possible production and decay channel of the Higgs boson, as predicted by the SM.

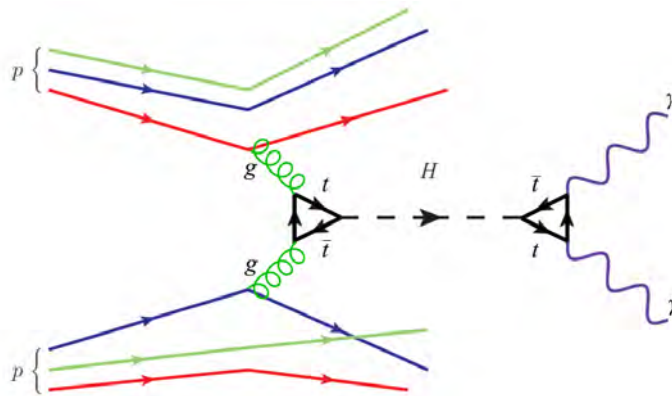


Figure 1.2: Protons collision producing a Higgs boson via a two-gluon fusion process. The decay process is via a loop of virtual top quarks, allowing the Higgs to decay into two photons.

1.2 PHYSICS BEYOND THE STANDARD MODEL

Even being one of the most successful and accurate theories ever created, the SM still fails to predict some physical phenomena observed. Figure 1.3 illustrates how phenomena of different nature are explained (or not yet) by different theories and how these theories are combined with each other, composing a bigger and more complete picture of the universe as we know.

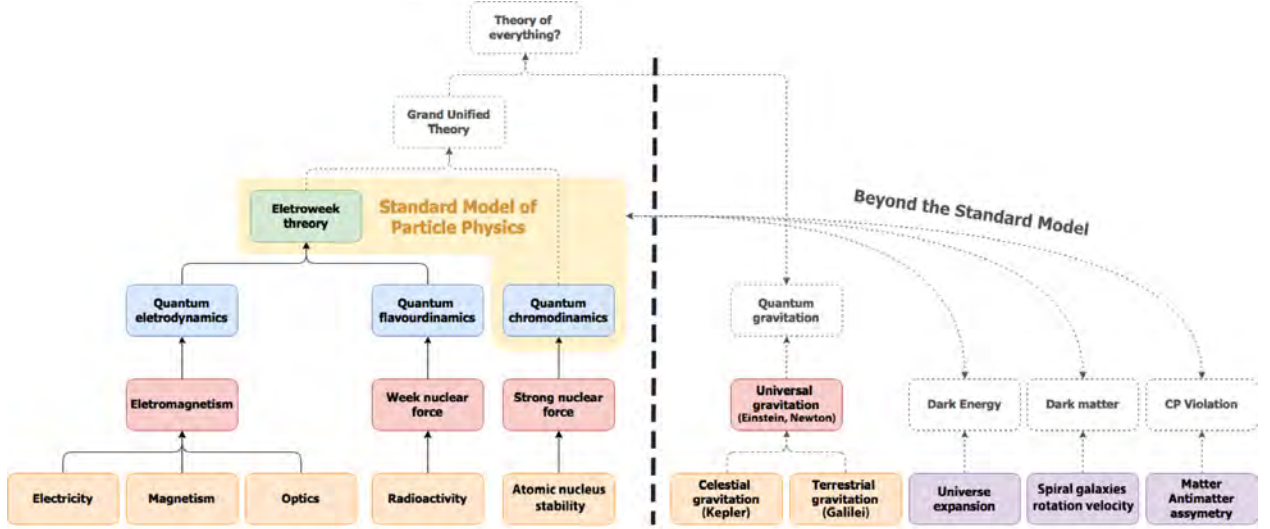


Figure 1.3: Panorama and evolution of different physics theories and evidences of physics beyond the standard model.

Even modeling the mechanism that makes particles massive, the gravitational interaction between massive particles is outside the SM. Different theories, beyond the the SM, predicts the *graviton* boson, a hypothetical elementary particle speculated to be the force carrier that mediates gravity. However, the graviton is not yet proven to exist, and no theory have successfully reconciled general relativity (modeling gravity) and the SM.

In addition, modern gravitational models predicts that the visible mass in the universe is not enough to explain the dynamics between celestial bodies and gravitational lensing effects. Observations suggests that 84% of the universe mass is composed by some particle that does not interact with the electromagnetic force, without absorbing or emitting any light [8] [9]. As it seems invisible for us, this unknown particle is named Dark Matter (DM) [10]. Although a few theories propose candidates for DM, such as Super Symmetry, measurements at LHC haven't confirmed any theory yet.

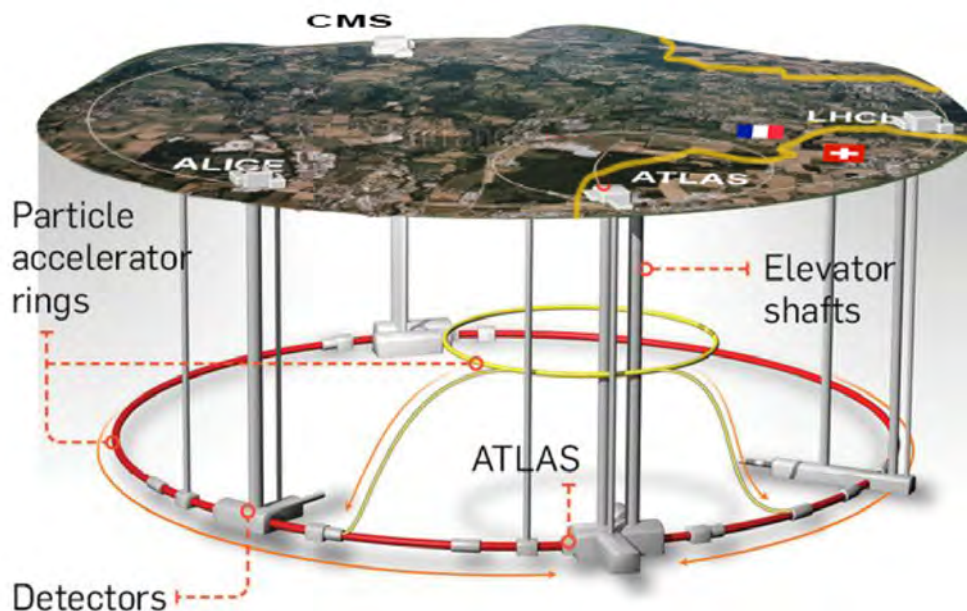
Another open question in the SM is the asymmetry between the matter and anti-matter quantity in the universe, which is not totally accounted by the SM of particle physics [11]. Some additional Charge-conjugation Parity symmetry (CP) violation mechanism, beyond the ones predicted by the SM, must still be incorporated in the SM, providing a more complete model of what is measured in the universe.



PARTICLE ACCELERATORS AND COLLIDERS

2.1 LHC AND HL-LHC

The Large Hadron Collider (LHC), illustrated in Figure 2.1, is the largest and most powerful particle accelerator in the world. It accelerates proton beams in opposite directions along a 27 km tunnel at about 80-100 m under the ground on the Franco-Swiss border, near Geneva. The LHC was constructed by the European Organization for Nuclear Research (CERN) between 1998 and 2008.



In the 27 km long circular tunnel, the two ends of the tunnel were excavated, between Lake Geneva and the mountain, the two ends up within 1 cm [12].

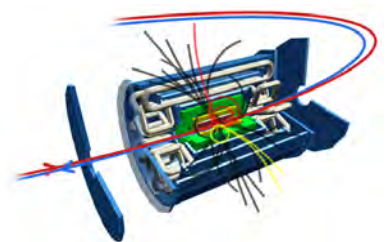
Figure 2.1: LHC tunnel illustration, with the 4 experimental caverns, each hosting one big experiment. Adapted from [13].

The LHC is the last accelerator of the large accelerator complex that is needed to gradually increase each proton beam energy up to the final beam-collision energy of 7 TeV.

2.1.1 The CERN accelerator complex

The protons accelerated in the LHC are stripped away from an hydrogen gas bottle and sent to a radio frequency quadrupole which will speed up the protons to 1.4% of the speed of light. During acceleration the beam is focused for injection into the linear accelerator LINAC2, the first accelerator in the chain of Figure 2.2.

Illustration of a particle collision in the ATLAS detector.



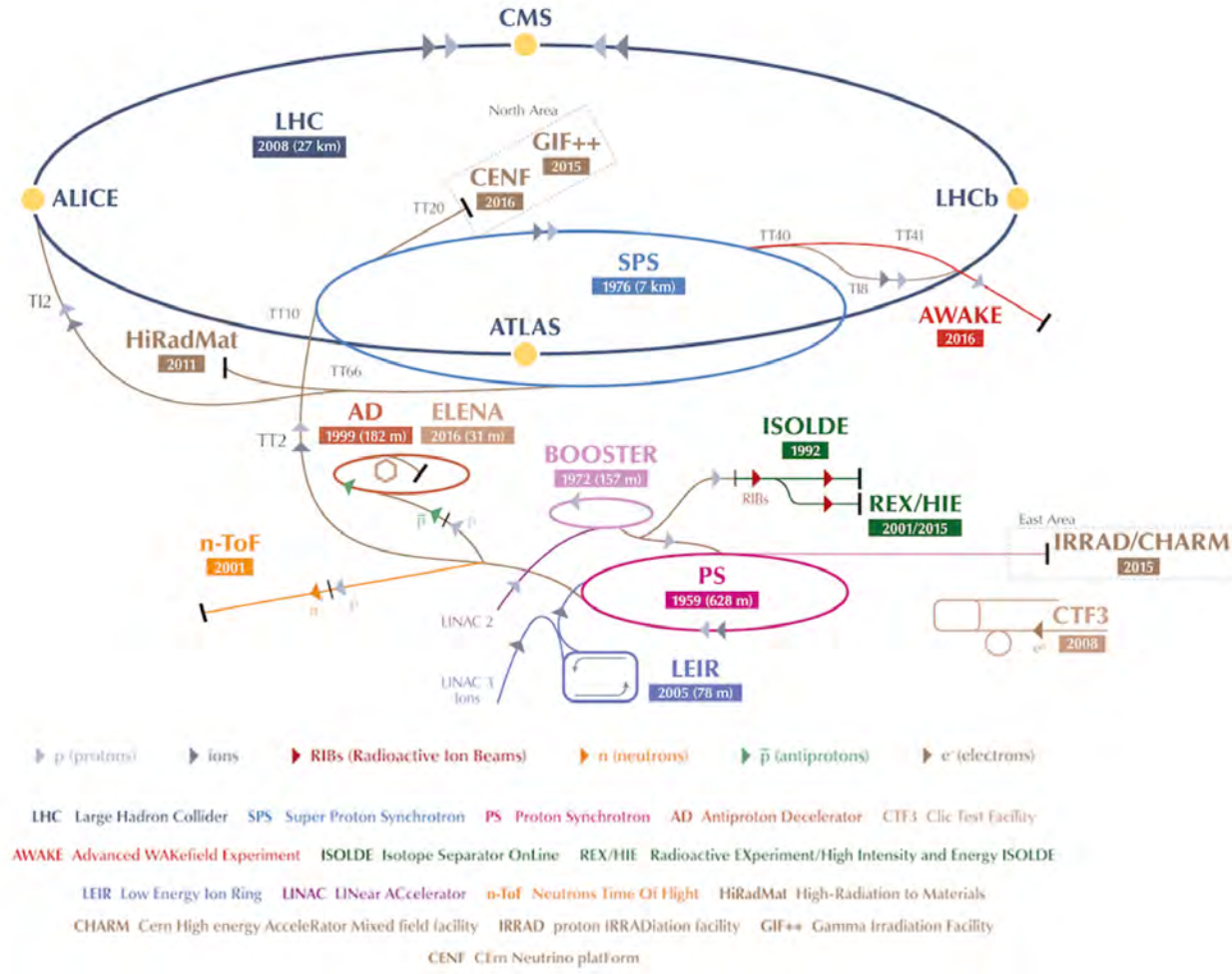


Figure 2.2: Accelerator complex at CERN [14].

The LINAC2 will provide more energy to the protons, accelerating them to 50 MeV. The LINAC2 is followed by the Proton Synchrotron Booster (PSB), which subsequently accelerates the beam to 1.4 GeV. Two last acceleration steps come before the injection of the beam into the LHC ring.

First, the proton beam is injected into the Proton Synchrotron (PS) and accelerated up to 25 GeV. Then, the beam is injected into the Super Proton Synchrotron (SPS), 7 km long and midway between the surface and the LHC underground tunnel, which will finally accelerate the beam at the LHC injection energy of 450 GeV.

2.1.1.1 The LHC beam

The SPS beam is split in two and injected into the LHC ring in two beam pipes. The protons are accelerated in opposite directions and cross in 4 different locations, shown in Figure 2.2, hosting the ATLAS [15], CMS [16], LHCb [17] and ALICE [18] detectors.

To accelerate the particle beams, 16 superconducting Radio Frequency (RF) cavities are placed along the 27 km LHC tunnel. The RF cavities store and resonate an electromagnetic wave on its interior, transferring energy to the particle beam each time it passes through the cavity. Each cavity uses a 5.3 MV/m electric field gradient to accelerate the proton beam, delivering 2 MV of RF power (16 MV in total on each lap around the LHC).

The frequency used in the cavity is 400 MHz, or 2.5 ns of length, providing a bunch of 7.5 cm length [19]. At this frequency and accelerator length (26.659 km), 35640 bunches can be accelerated simultaneously. Although, due to intrabeam effects during beam storage/acceleration [20], and technical limitations, such as the rise times of the various injection and dumper kickers [21], only one out of ten RF buckets is filled, providing a final proton collision rate of 40 MHz, or a *Bunch Crossing* (BC) interval of 25 ns.

2.1.1.2 Other beam lines

As it is possible to see in Figure 2.2, the same structure that feeds the LHC with protons also provides protons for other experiments, such as the AD [22] and ELENA [23], the East Areas irradiation facilities such as IRRAD [24] and CHARM [25], and Secondary Beam Areas (SBA) [26], such as the North Area H8 beam line, created by the collision of the SPS primary proton beam with fixed targets.

Many tests and results presented in this thesis were done using the H6 and H8 beam lines in the North Area. Also, some prototypes tested were irradiated by the IRRAD facility.

2.1.2 The LHC upgrade

Each LHC beam bunch typically consists of about 1.15×10^{11} protons, and together with the number of bunches being accelerated (n_b), the bunches revolution frequency f and the overlapping area of the colliding bunches A , the beam *instantaneous luminosity* \mathcal{L} can be defined as:

$$\mathcal{L} = \frac{n_b N_1 N_2 f}{A}, \quad (2.1)$$

where N_1 and N_2 are the number of protons on each beam bunch. The event rate for a specific collision process is proportional to the luminosity of the beam and can be written as:

$$\frac{dR}{dt} = \mathcal{L} \cdot \sigma_p, \quad (2.2)$$

where the instantaneous luminosity \mathcal{L} acts as a proportionality factor between the event rate, dR/dt , and the cross section, σ_p . \mathcal{L} has unit of $\text{cm}^{-2}\text{s}^{-1}$ and the LHC has a typical instantaneous luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ in 2016-2018.

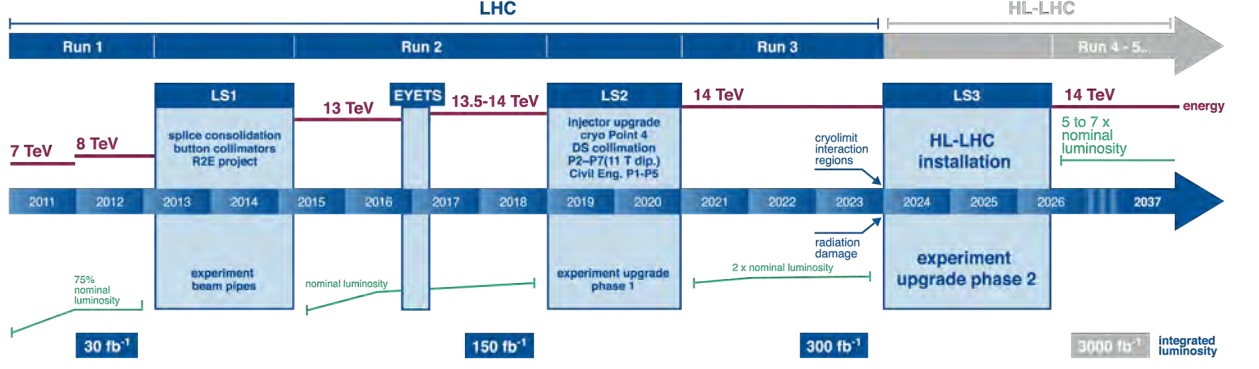


Figure 2.3: Evolution of the energy and luminosity on the LHC through the operation years and the projection to the future [27].

From the start of the LHC operation, providing collisions for the experiments in 2011, until the end of *Run 2*, at the end of 2018, the LHC delivered an integrated luminosity of approximately 150 fb^{-1} for the ATLAS experiment. During the Long Shutdown (LS) 2, a planned maintenance period of 2 years in 2019 and 2020, the LHC luminosity will be increased by replacing the LINAC2 with the LINAC4 [28], and by the upgrade of the collimation system, reducing the beam size and increasing the instantaneous luminosity by a factor of 2. It is expected that during Run 3 in 2021-2023, the integrated luminosity delivered to ATLAS and CMS will be equivalent to the integrated luminosity accumulated on the previous 8 year of operation, reaching a total value of 300 fb^{-1} .

Following the Run 3, another LS is expected to take place in between 2023 and 2026 for the last technology upgrade planned: the High-Luminosity-LHC (HL-LHC). During the LS 3 the acceleration structures will be updated, improving the beam optics, yielding a smaller overlapping area of the colliding bunches. This will allow the luminosity to increase from 5 to 7 times (w.r.t. the initial designed luminosity), reaching $> 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. From the expected start in 2026, following the 10 operational years predicted for the HL-LHC, the total integrated luminosity is expected to reach 3000 fb^{-1} , representing 10 times the data acquired during LHC operation [29]. Figure 2.3 illustrates the LHC schedule and parameters evolution.

The collisions at higher luminosity allow the experiments to observe more rare processes and improve measurements statistics. For example, the HL-LHC will produce up to 15 million Higgs bosons per year, compared to the 1.2 million produced in 2011 and 2012 by the LHC.

$$1 \text{ fb} = 10^{-43} \text{ m}^2 = 10^{-39} \text{ cm}^2$$

LHC produces 1 Higgs boson at each 10 billion collisions.

2.2 COMPACT LINEAR COLLIDER – CLIC

As the construction of an accelerator and detector is an endeavor that takes many years from project to first collision detection, future experiments are already under study and planning. In parallel to the LHC and HL-LHC program, physicists and engineers at CERN are already working on the next generation of accelerators and detectors in order to provide precise physics measurements at the high energy frontier, in the post-LHC era.

The proposed Compact Linear Collider (CLIC) implements a new linear accelerator [30] to collide electrons and positrons at maximum center-of-mass energies of 3 TeV, to be built near the LHC site, as shown in Figure 2.4a. Figure 2.4b shows the CLIC experiment detector to be build on the accelerator interaction point.

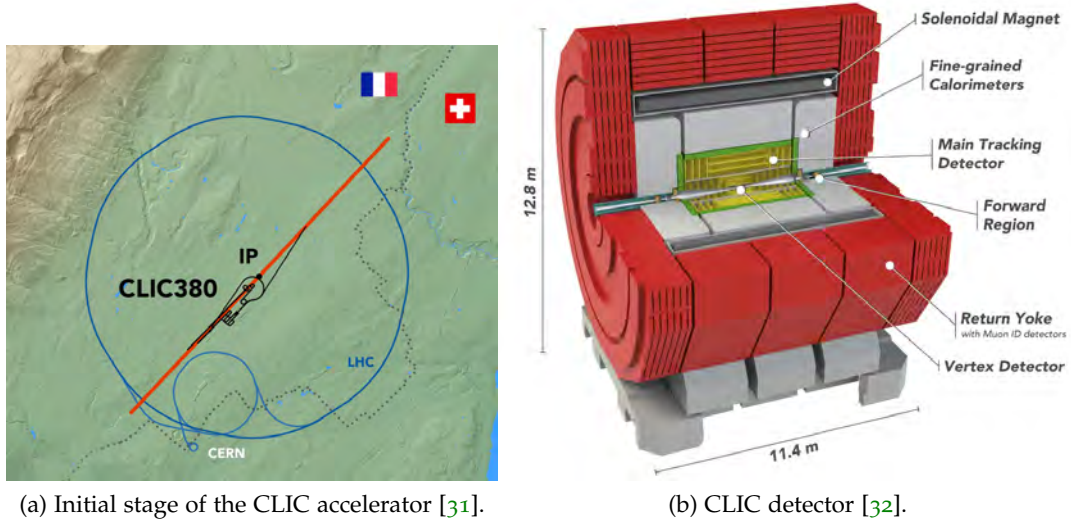


Figure 2.4: Illustration of proposed CLIC accelerator and detector.

2.2.1 e^+e^- vs hadron colliders

In hadron collisions, due to the partons energy distribution, only a fraction of the total beam energy is transferred to the particle collision. For this reason, the particles created in hadronic collisions will have only a small fraction of the acceleration energy. In addition, many partons still interacts with a small energy transfer inducing a large background in the experiment. Therefore, in order to cope with the large background and achieve a significant amount of statistics on rare physical events, hadronic colliders must operate with high collision rates, such the 40 MHz from the LHC.

An advantage in using e^+e^- is that, as an point-like particle, the full acceleration energy will be transferred to the particles on the beam, making the collision initial state to have an well defined initial state. With the full acceleration energy being transferred upon collision, new particle creations can take place almost up to the kinematic limit. In addition, e^+e^- collisions are almost free of background cre-

ated upon collisions as interaction will happen only among electrons and positrons, without remnants particle interactions as in hadron collisions. For this reason, CLIC can operate at a lower collision frequency (bunch train repetition rate of 50 Hz).

In addition, the well known initial states of the particles upon collision enhances the measurement precision, collision of fundamental particles provides unique opportunities to make precision measurement of the two heaviest particles in the SM: the Higgs boson (125 GeV) and the top quark (173 GeV). Deviations in the way that the Higgs or the top quark couples to other particles can be an indication of new physics and CLIC would offer such measurements as the first step of its physics programme.

Nevertheless, a disadvantage of accelerating e^+ and e^- , rather than protons, is the dissipation of acceleration energy in the form of synchrotron radiation. Having in mind the revolution time of $2\pi R/c$, the energy lost on each lap on a circular accelerator can be written as:

$$\Delta E_e = \frac{4\pi}{3} \frac{e^2}{R} \left(\frac{E}{mc^2} \right)^4 = C_\gamma \frac{E^4}{R} \quad (2.3)$$

where $C_\gamma = 0.8846 \cdot 10^{-4} m/GeV^e$ for electrons and $C_\gamma = 0.7783 \cdot 10^{-17} m/GeV^e$ for protons [33]. Equation 2.2.1 shows that the energy lost on each accelerator turn is inversely proportional to the particle mass at rest and the accelerator radius. Comparing C_γ values it is possible to see that electrons would lose $\approx 10^{13}$ times more energy than protons, due to synchrotron radiation emission, while being accelerated up to the same energy on a same accelerator. For this reason a linear accelerator was decided for CLIC.

2.2.2 CLIC accelerator programme

CLIC is foreseen to be built and operated in three stages with different CM collision energies [30]: 380 GeV, 1.5 TeV, and 3 TeV, illustrated in Figure 2.5. Each stage have been optimized to access different physics processes. With an instantaneous luminosity up to $6 \times 10^{34} cm^{-2}s^{-1}$, the expected integrated luminosity at each stage is $500 fb^{-1}$, $1.5 ab^{-1}$ and $2 ab^{-1}$, respectively.

In contrast with circular accelerators, where the same accelerating structures are used on each beam revolution, linear accelerators needs to accelerate the beam on a single passage through the accelerator. In order to reach the required high energy and luminosity levels in a realistic and cost efficient manner, the CLIC acceleration gradient has to be very high. To cope with this requirement a novel two-beam acceleration technique has been developed.

In the two-beam acceleration concept, shown in Figure 2.6, a *drive beam* with low energy (2.4 GeV) and high current (100 A) runs parallel to the e^+e^- *main beams*, running at a lower current (1.2 A). The drive beam is decelerated in power extraction structures and the generated RF power is transferred to the main beam by wave guides, accelerat-

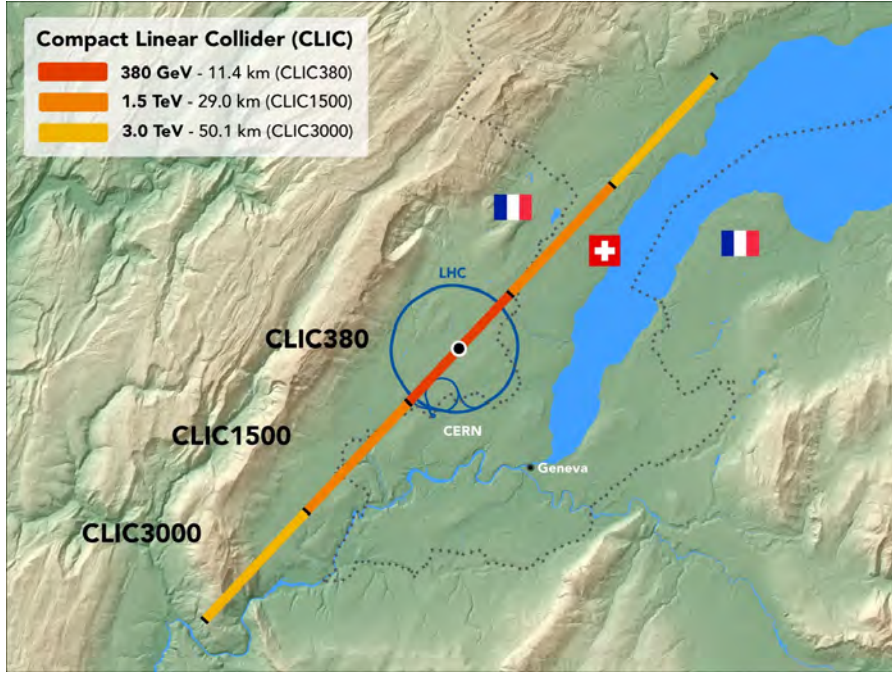


Figure 2.5: Illustration of the CLIC three energy accelerator stages [31].

ing it from 9 GeV to 1.5 TeV. The extracted RF power arrives the main beam copper cavities, running at room temperature, at 12 GHz and is capable of generate an acceleration gradient of 100MV/m, delivering a maximum of 9.2 TW of RF power. The main beam is structured in trains of $312 e^+e^-$ bunches, each spaced by 0.5 ns, and the trains crosses each other every 20 ms [30].

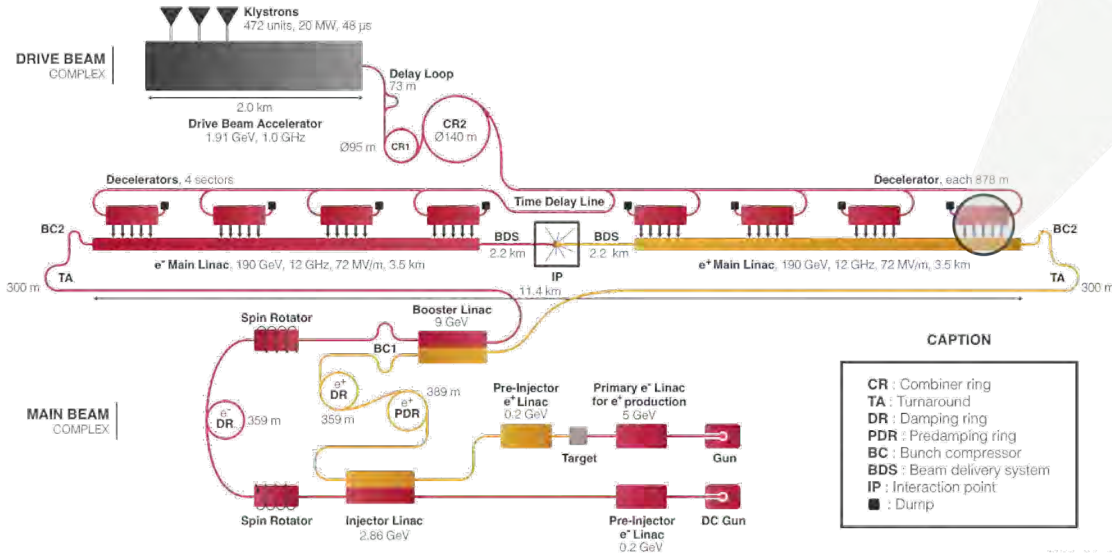


Figure 2.6: Layout of the CLIC first energy stage accelerator complex [30].

Employing this acceleration technique, the first energy stage proposed for CLIC requires an accelerator structure with 11 km, slightly larger than the LHC diameter, while for the final energy of 3 TeV the acceleration complex would be scaled up reaching about 50 km.

PARTICLE DETECTORS

In order to record the production of the beam collision, several particle detectors are used. Each experiment detector is composed by several sub-detector systems that are tailor-made to meet specific types of measurements that each experiment targets. Many experiments, such as ATLAS and CLIC, use detector geometries where its sub-detectors systems forms concentric cylindrical layers around the beam pipe, known as barrel type geometry, as illustrated in Figure 3.1. Each sub-detector system is responsible for performing one specific type of measurement and is placed in the experiment according to its properties. Figure 3.2 shows the different sub-detector of the ATLAS experiment.

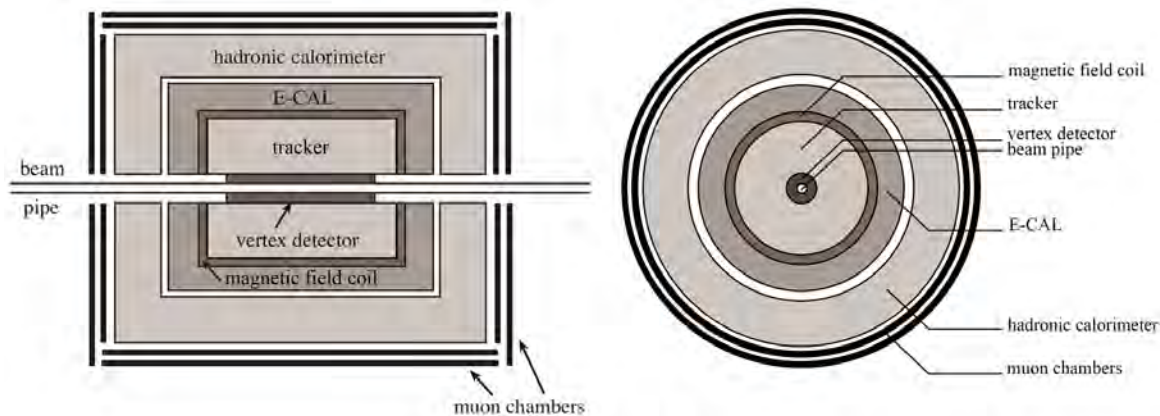


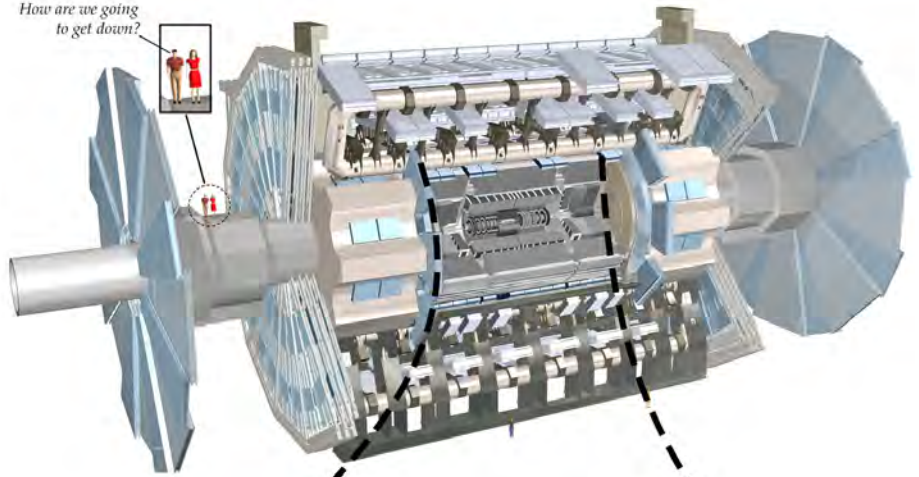
Figure 3.1: Illustration of detector layers on barrel type experiments.

Vertex and track detectors, for example, capture precisely the position of the particles as they move away from the collision point towards outside the detector. For this reason, detectors responsible for position measurements are placed as close as possible to the IP and, in order to have accurate measurements, these detectors are designed to interact with the particles with minimal disturbance to its original trajectory.

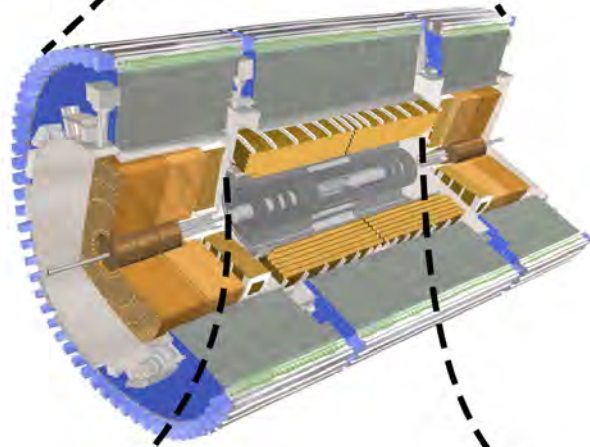
Calorimeters, on the other hand, are used to measure the energy of the particles, and for this it is necessary that the particle transfers completely, or almost, its energy into the detector. Doing so, particles will vanish inside the detector and its trajectory will be halted. Therefore, calorimeters are usually placed at the outer region of the experiment, surrounding the detectors responsible for position measurement. Calorimeters typically consist of layers of a high-density *absorber* material interleaved with layers of detectors. The absorber is used to generate as much momentum transfer interactions as possible and stop the particle inside the calorimeter detection volume.

The ATLAS experiment detector, with 44 m length and 25 m diameter. The central barrel region is enveloped by muon chambers, also presented in the extremity disks. It is also possible to see the prominent toroidal coils for the magnetic field generation.

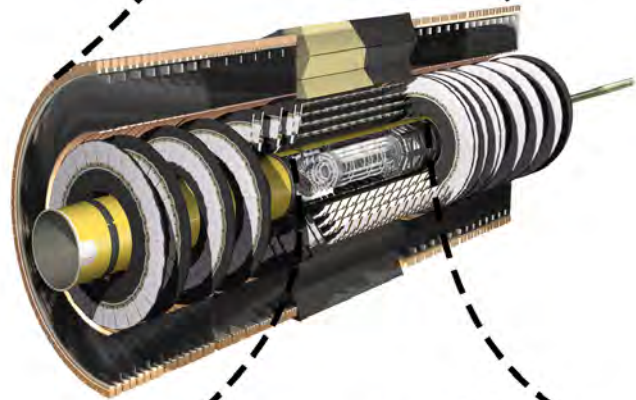
How are we going to get down?



ATLAS calorimeter sub-system. It is divided into the central barrel, with 5.56 m length, and its two end-caps with 2.91 m each. The hadronic Tile Calorimeter is placed in the outer part of the calorimeter, from a radius of 2.28 m to 3.86 m. The liquid argon (LAr) calorimeters are placed in the inner region due to radiation damage reasons. The LAr system is composed by: an electromagnetic calorimeter in the barrel region; the Forward Calorimeter, and the electromagnetic (EMEC) and hadronic (HEC) calorimeter, in the end-caps.



Inner tracking system of the ATLAS detector. It is 6.2 m long with 2.1 m diameter. It is also divided into the barrel and end-caps parts. The end-caps are composed by the disks-shaped Transition Radiation Tracker detector and the Semiconductor Tracker, composed by silicon microstrips. In the barrel region these two detectors are assembled in cocentral cylindrical layers and surrounds the ATLAS innermost (pixel) detector.



Pixel detectors, the ATLAS first detector that interacts with the particles produced by the beam collision. It has 80 million pixels covering an area of 1.8 m². It is composed by 3 disks, on each end-cap, and a central barrel with 4 pixel layers.

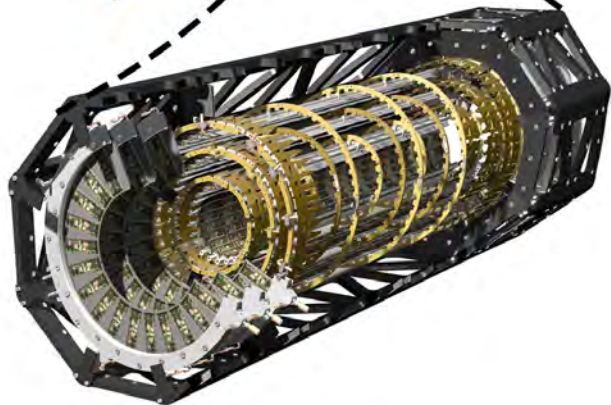


Figure 3.2: Inner view of different ATLAS detector layers.

3.1 DETECTOR SUB-SYSTEMS

3.1.1 Triggers

Triggers are an on-line decision-making system that uses a desired temporal and spatial correlation between the detector signals in order to select events to be stored for analysis. With a pile-up $\mu = 20$ in the LHC, considering a hadronic total cross-section in the order of 100 mb and a luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$, the final pp collision rate is about 1 GHz, generating enough data capable of fill 100 000 CDs per second, making data storage impractical.

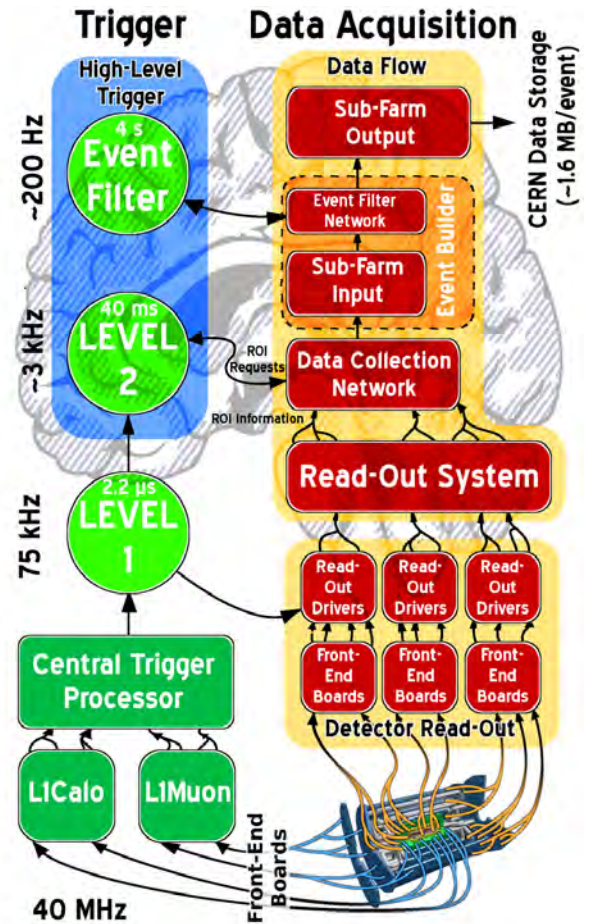
Nevertheless, as most of the hadron collisions will end up creating background events, most of the events doesn't need to be recorded at all. Therefore, the trigger electronic and software systems must operate in real-time, keeping as much of the interesting physics events while rejecting the maximal amount of background. Modern detectors adopts systems with multiple trigger levels.

Extracted from [34]

The ATLAS trigger system [35] performs the selection process in three stages. The Level-1 trigger works on a subset of information from the calorimeter and the muon detectors and the selection decision is made in about two microseconds after the event occurs. In addition, hits in the pixel detectors are also associated with the L1 trigger. This first stage reduces the event rate from 40 MHz to about 75 kHz.

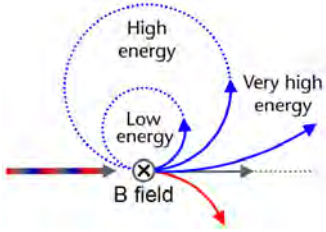
The second stage of the trigger system, Level-2, is a large array of custom processors running software based algorithms, utilizing information from all sub-detectors in fully granularity of the regions of interest around the objects that passed the Level-1 selection, reducing the event rate further to the order of 3 kHz.

The Level-3 trigger is a large farm of CPUs running a detailed analysis of the full event data. About 200 events per second are left after the Level-3 analysis, and these are permanently stored for off-line subsequent analysis.



Regarding CLIC, the low duty cycle of its accelerator leaves a gap of 20 ms between the crossing of the bunch trains. This low repetition rate, and a lower radiation background, allows the CLIC detectors to record all events detected by its systems and gives sufficient time for the read-out before the collision of the next bunch train. In this way, CLIC will operate its detectors in a trigger-less mode.

Trajectory deflection by a B field.
Blue, red and grey indicates positive, negative and neutral particles.



3.1.2 Magnetic fields

Magnetic fields help to distinguish the charge and momentum of the particles detected. Magnetic field can be generated by solenoids, with a magnetic field going along the beam axis, or by toroidal coils, which will bend charged particles toward/outward the beam.

The ATLAS magnet system [15], shown in Figure 3.3(left), is composed by: the Central Solenoid Magnet, providing 2 T and contained inside the calorimeter system, surrounding the ATLAS inner detector; the Barrel Toroid, composed by 8 separate 4 T coils with 25.3 m each and 100 km of superconducting wire; and the two End-cap Toroids, similar to the Barrel Toroid but with smaller dimensions. All the magnets sum up to 1315 tonnes, covering a volume of 12000 m^3 and storing a total of 1.618 GJ of energy (equivalent to the 385 tonnes TGV train at 330 km/hr).

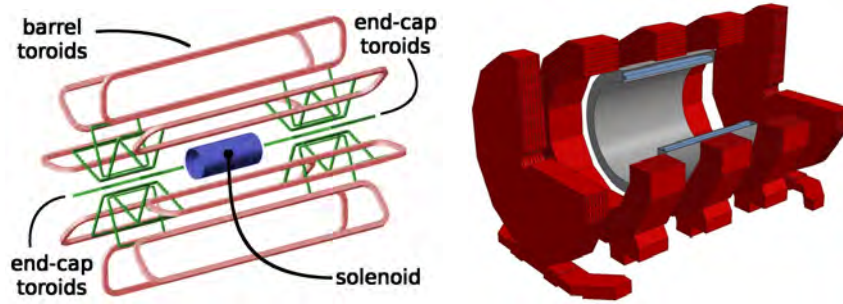


Figure 3.3: ATLAS and CLIC magnet system. Images from [34] and [36].

CLIC detector design implements a single superconducting solenoid magnet, Figure 3.3(right), providing an axial magnetic field of 4 T [30]. As the CLIC detector uses fine grained calorimeters to measure the particles position as the shower progress inside the calorimeters, the solenoid is placed surrounding the calorimeter detectors, minimizing multiple scattering due to the magnet material. The central solenoid coil fits tightly inside its iron *return yoke*, responsible for homogenizing the return magnetic flux generated outside the solenoid and increasing the magnetic field inside the detector, allowing its compact form with 11.4 m length and 12 m diameter.

3.1.3 Muon systems

Muons usually traverse the complete detector and the information coming from the muon detectors can be used to trigger the sub-detector systems. Due to its small cross-section for interactions, muons leave only small fractions of their energy through the different sub-detectors, without being contained in the calorimeter and, therefore, muon systems are usually the outermost detectors. In addition to trigger, when immersed in a magnetic field muon detectors can also be used to improve the momentum measurement of muons in a region free of confusion by other trajectories.

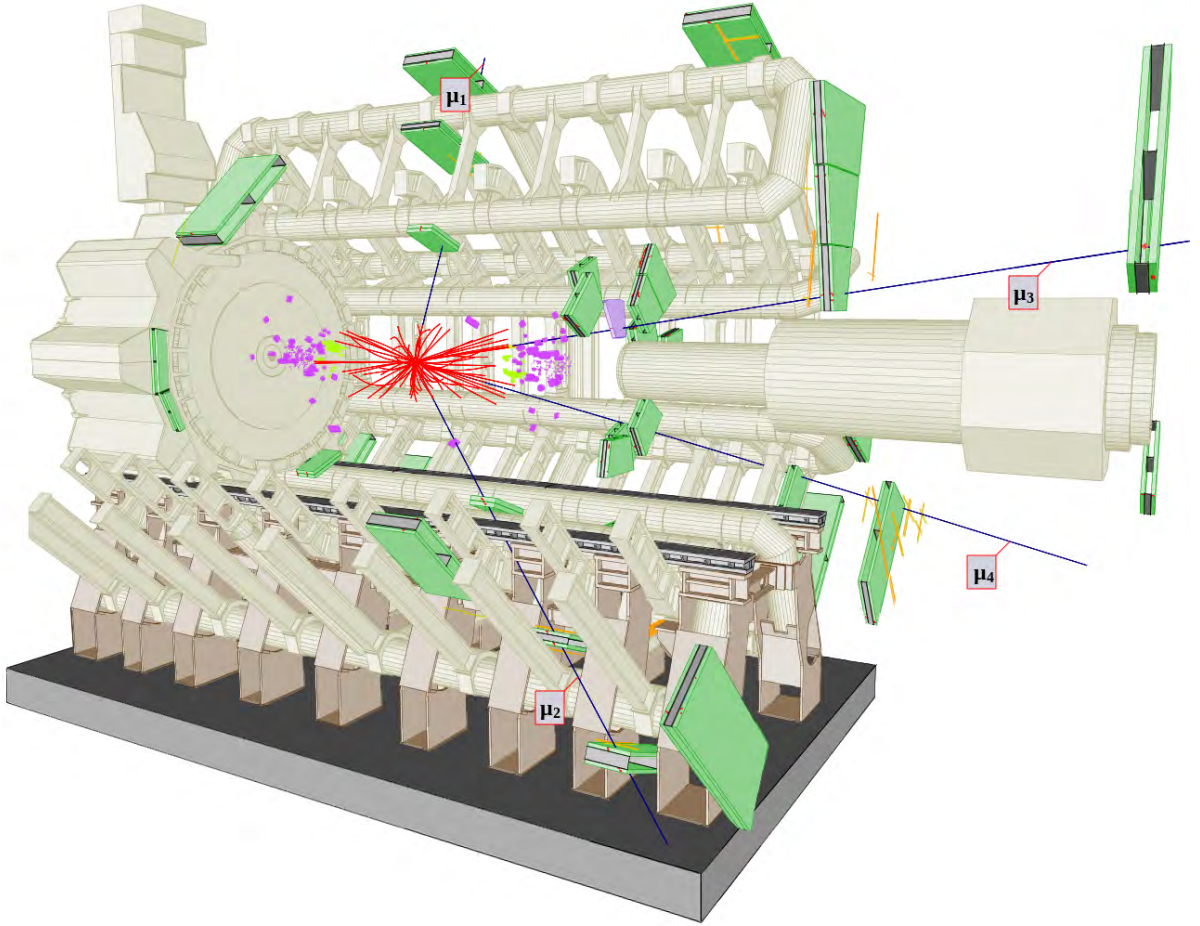


Figure 3.4: ATLAS event of a $ZZ \rightarrow 4\mu$ with muon chambers (in green) [37].

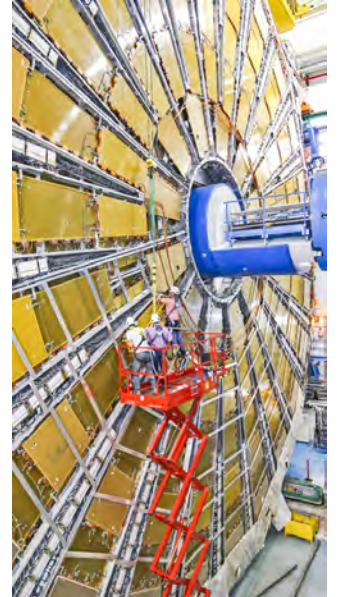
The ATLAS Muon Spectrometer [39] is composed by 4000 muon chambers, with 4 different flavors, designed for tracking and trigger: Thin Gap Chambers (TGC), Resistive Plate Chambers (RPC), Monitored Drift Tubes (MDT), and Cathode Strip Chambers (CSC). Figure 3.4 shows an event display where 4 muons traversing the detector, with the activated muon chambers highlighted in green.

The muon tracking uses information from the MDTs, 3 concentric cylindrical layers in the barrel region, and the CSCs, placed as perpendicular end-cap disks. The system is designed to measure muons with transverse momentum (p_T) > 3 GeV, providing standalone high precision p_T resolution of 3% for $p_T < 250$ GeV, increasing up to 10% @ 1 TeV [40]. The average spatial resolution of the ATLAS muon tracking system is about $70 \mu m$.

Three layers of RPCs in the barrel region and three layers of TGCs in the endcap regions provides the Level-1 trigger signal by measuring the spatial and temporal coincidence, with a timing resolution of about 3 ns, of hits pointing to the beam interaction region [41].

CLIC muon chambers are proposed to be built as resistive plate chambers with cells of $30 \times 30 \text{ mm}^2$ [30]. They will be placed intercalated with the iron layers of the return yoke, a region with an expected magnetic field saturation of 1.5 T.

ATLAS Muon spectrometer [38]



3.1.4 Calorimeters

Calorimeters are detectors dedicated to measure the energy that a particle loses as it traverses the detector volume. The detector, composed by layers of an “absorbing” high-density material, as lead, intercalated with layers of detectors, is designed to make the particles deposit all of their energy within the detector volume. Hence, calorimeters are thick detectors by construction, with ATLAS calorimeters ranging from 24 to 26 radiation lengths X_0 , while in contrast vertex detectors has about $0.5-1 X_0$.

Incoming particles will interact with the absorber material of the calorimeter initiating a shower of secondary particles. Particle showers can be divided into electromagnetic showers, produced by particles interacting via the electromagnetic force, and hadronic showers, produced by hadrons and proceed via the strong nuclear force. Therefore, calorimeters are designed in two different flavors, each dedicated for a specific shower type. Figure 3.5 shows what type of particles is detected at each sub-detector system.

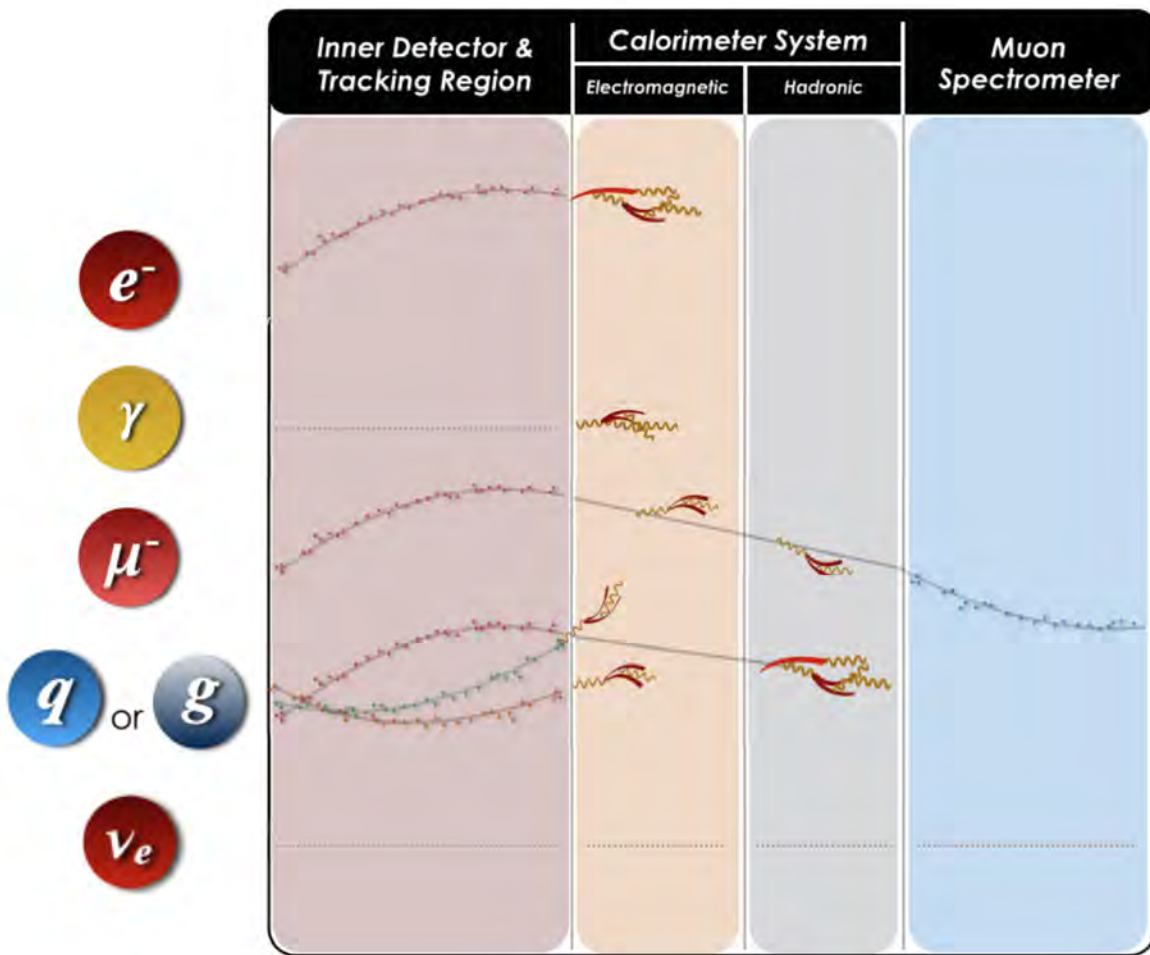


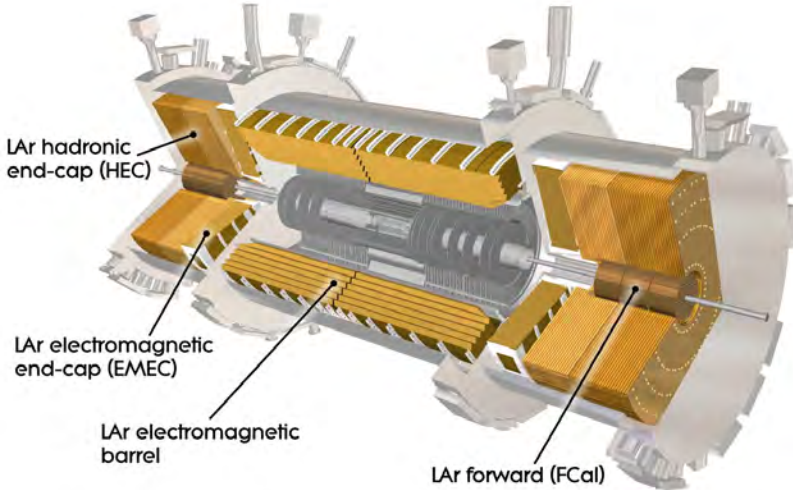
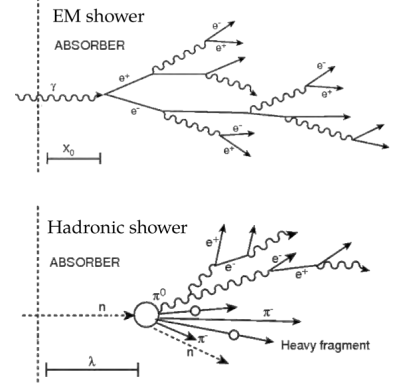
Figure 3.5: Illustration showing how different particles interact and deposit its energy in different detector systems. Adapted from [42].

Particles interacting electromagnetically are detected in the Electromagnetic calorimeters (EMC). Particles, such as photons and electrons, will interact with the EMC mainly via the *bremstrahlung* and pair-production processes, generating a shower of e^- and e^+ , that can subsequently create other showers, until the original particle energy is totally released, across the multiple absorption layers.

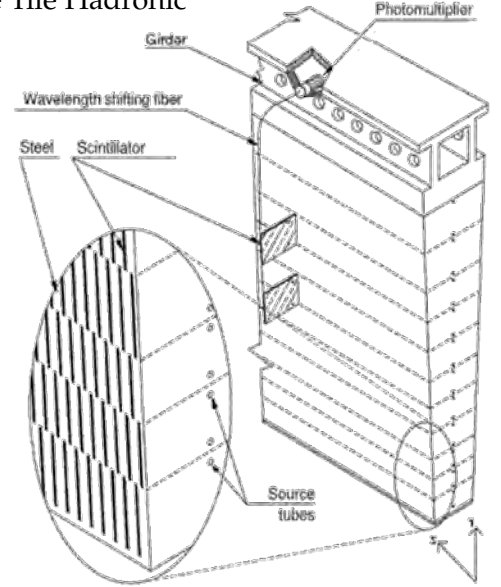
In the other hand, particles creating hadronic showers are detected by the Hadronic Calorimeters (HC). An hadronic shower is a series of inelastic hadronic interactions of a primary particle with the nuclei of the absorber material. Secondary particles will undergo further inelastic interactions and produce more particles. The evolution of a hadronic shower has the additional complexity that hadron showers can also generate electromagnetic showers. A distinguished characteristic of the hadronic shower is that it takes longer to develop. Hence, HCs need to be “thicker” than EMCs and, consequentially, HCs are always placed surrounding the EMCs in an experimental set-up.

The components of the ATLAS calorimetry system are the Liquid Argon (LAr) Calorimeter, in the central region, and the Tile Hadronic Calorimeter (TileCal), placed around the LAr.

Images from [43]



(a) ATLAS LAr calorimeter illustration [44].



(b) ϕ wedge of the Tile Cal. Illustration from [15]

Figure 3.6: Illustration of the ATLAS calorimeter sub-systems.

The ATLAS LAr calorimeter [45] is composed by a hadronic end-cap (HEC), an electromagnetic end-cap (EMEC) and an electromagnetic barrel layer, and the Forward calorimeter (FCal), segmented in one electromagnetic and two hadronic calorimeters). The combined energy resolution for electrons is $\sigma_E/E \approx 10\%/\sqrt{E} \oplus 170\text{MeV}/E \oplus 0.7\%$. Figure 3.6a shows an illustration of the LAr calorimeter.

As the TileCal [46] region has a less harsh environment in terms of radiation dose, it is composed by iron absorbers interleaved with plastic scintillator tiles, as shown in Figure 3.6b. Its energy resolution (tested for pions at test-beam) is $\sigma_E/E \approx 50\%/\sqrt{E} \oplus 6\%$ [47].

Figure 3.7 shows a picture of the complete TileCal detector during the ATLAS detector assembly. This TileCal system has 2.91 m in length and 8.6 m of diameter and is composed of 64 radial sections, with a total weight in the order of 1 tonne.



Figure 3.7: ATLAS Tile extended barrel, LAr HEC and FCal [48].

Regarding the CLIC calorimeters, in order to achieve the high measurements precision targeted for the CLIC detector physics performance, highly granular calorimeters are planned to be used in order to profit from a particle flow reconstruction.

Many of the interesting events at CLIC has final states containing multiple jets. Therefore, an accurate jet mass measurements is required for reconstruction and identification of physics events. The particle flow approach aims to improve jet energy measurements by reconstructing individually the four-vectors of all visible particles in an event, with the final jet energy being the sum of the energies of the individual particles in the jet. In this way, the energy and momentum for each particle can then be determined from the detector subsystem in which the measurements are the most accurate. Therefore, charged particle momenta are measured in the inner detector tracker, whilst photon energy measurements are extracted from the energy deposited in the ECAL, and the HCAL is used to measure only the 10% of jet energy carried by long-lived neutral hadrons [49].

The CLIC electromagnetic calorimeter (ECAL) detector [50] is a sampling calorimeter with 40 layers of silicon detector, with cells of $5 \times 5 \text{ mm}^2$ (with a silicon total area of approximately 2500 m^2), intercalated with 1.9 mm thick tungsten absorption layers. The total thickness of the ECAL corresponds to about $22 X_0$. It surrounds the inner tracker and vertex detectors and it has a inner radius of 1500 mm and outer radius of 1702 mm, with approx. 5m length.

The proposed hadronic calorimeter for the CLIC detector consists of 60 steel absorber plates, each of them 19 mm thick, interleaved with 3mm thick polystyrene scintillator tiles of $30 \times 30 \text{ mm}^2$, being readout with silicon photo-multipliers. The total scintillator area is in the order of 9000 m^2 [50].

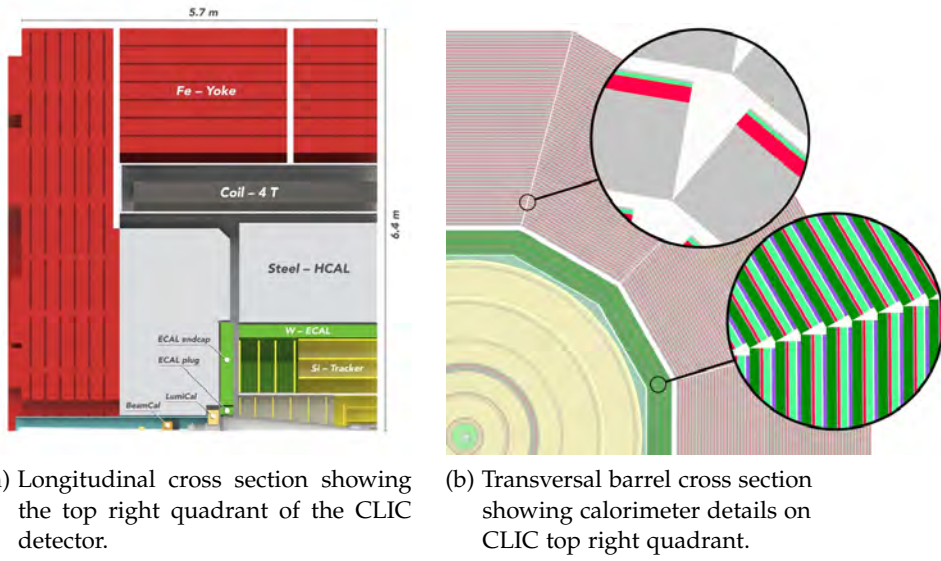
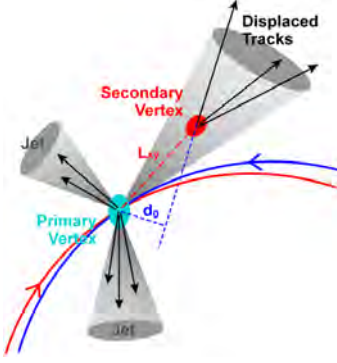


Figure 3.8: Illustration of the CLIC sub-detectors and calorimeters stack. Images from [50]

Figure 3.8 shows a cross section of the CLIC detector (fig. 3.8a) and a detailed view of the calorimeter stack (fig. 3.8b). In the ECAL stack illustration, the olive-green regions indicates the tungsten layers, while the red regions symbolize the silicon sensors. Purple layers are G10 (insulator material), green represents the PCBs and connectivity, and white is air. In the HCAL detail, light green regions indicate the steel layers (with thin steel sheets for the cassette), red stands for the scintillator, while green and white are PCB and air as in the ECAL.

In the CLIC detector two other smaller electromagnetic calorimeters, the LumiCal and BeamCal, are installed in the very forward region aligned with the beam axis. The LumiCal is responsible for precise measurements of electrons and positrons produced in Bhabha scattering, while the BeamCal is used for the tagging of forward electrons. Moreover, these two calorimeters extends the coverage of the detector down to 10 mrad.

Secondary vertex illustration [51]



3.1.5 Tracker and vertex detectors

Beside different names, both tracker and vertex detectors are responsible to measure the position of the particles along its trajectories, as accurate as possible and without disturbing the original track of the particle. Vertex detectors are distinguished by their position closer to the IP and the better position measurement resolution, making it able to find secondary decay vertices providing a measurement of the impact parameter, d_0 . In contrast, tracking detectors are placed further from the IP, creating a longer lever arm and, consequently, providing a better momentum resolution (when compared with vertex detectors).

A combination of technologies can be used in tracking detectors. Gaseous systems (projection chambers or transition-radiation detectors) can be combined with semiconductor detectors (such as silicon strips or pixels) depending on the requirements of the experiment. Nevertheless, modern detectors and experiments are converging towards tracking systems fully made of thin semiconductor detectors.

The tracker/vertex system will be covered in greater details, with emphasis on the pixel detectors, as the work developed in this thesis regards pixel detectors for future tracking and vertex detectors.

3.1.5.1 ATLAS Inner Detector (ID)

ATLAS ID is the innermost detector system, closest to the beam IP, responsible for measuring the direction, momentum, and charge of particles above a nominal p_T threshold of 0.5 GeV/c. It is composed by the Transition Radiation Tracker (TRT) surrounding the Semiconductor Tracker (SCT) and the Pixel Detector, extending over a length of 6.2 m and 2.1 m of diameter.

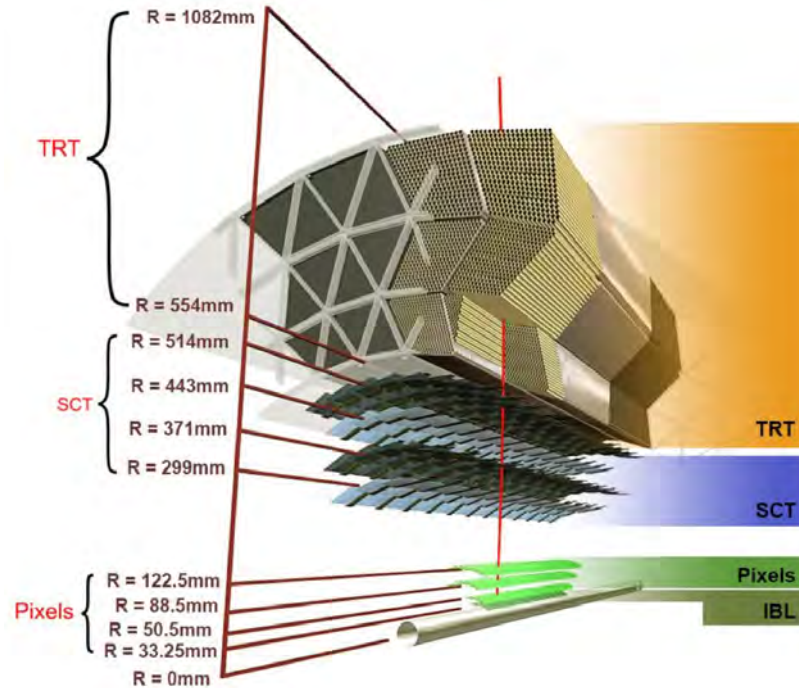


Figure 3.9: ATLAS ID illustrating positioning of detector barrel layers [52].

Figure 3.9 shows the detector layout in the barrel region, while Figure 3.10 shows the ID end-cap layout with the position of the multiple end-cap disks.

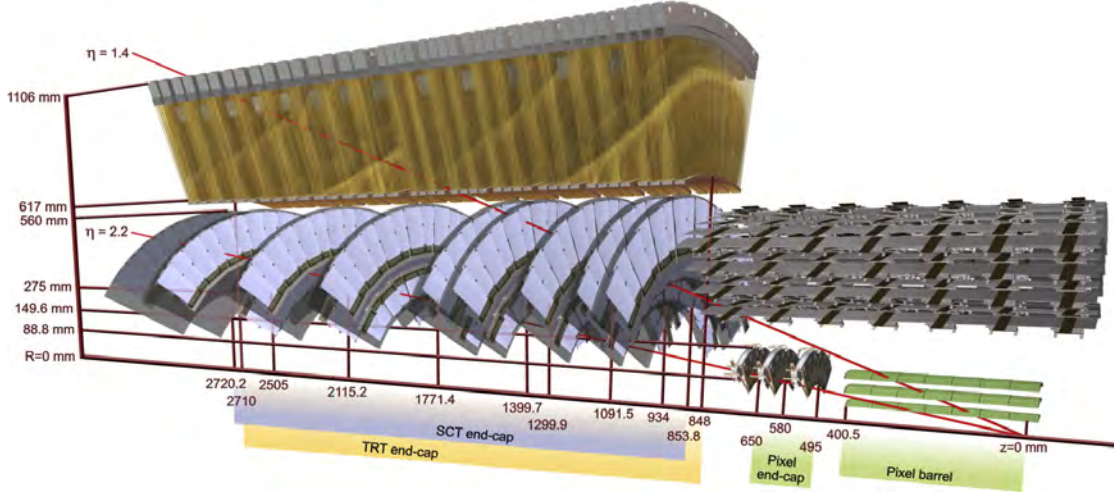


Figure 3.10: ATLAS ID with end-cap disks positioning. Image from [15].

TRT The TRT [53] is a gaseous detector occupying the outermost part of the ID. The choice for a gaseous system is practical as a semiconductor detector providing the same amount of hit signals per track would be of high cost. The TRT also provides electron identification capability by detecting transition radiation (TR) photons (soft X-rays). The detector provides an almost continuous tracking being composed by 420 000 readout channels made of gas filled straws with a coaxial electrode wire.

The TRT barrel region can be seen at the top of Figure 3.9 and the TRT end-cap disks can be seen in Figure 3.10. Figure 3.11a shows tracks recorded in the ATLAS ID, from a Higgs decay simulated event, and Figure 3.11b illustrates a particle traversing the TRT with channels from a track highlighted.

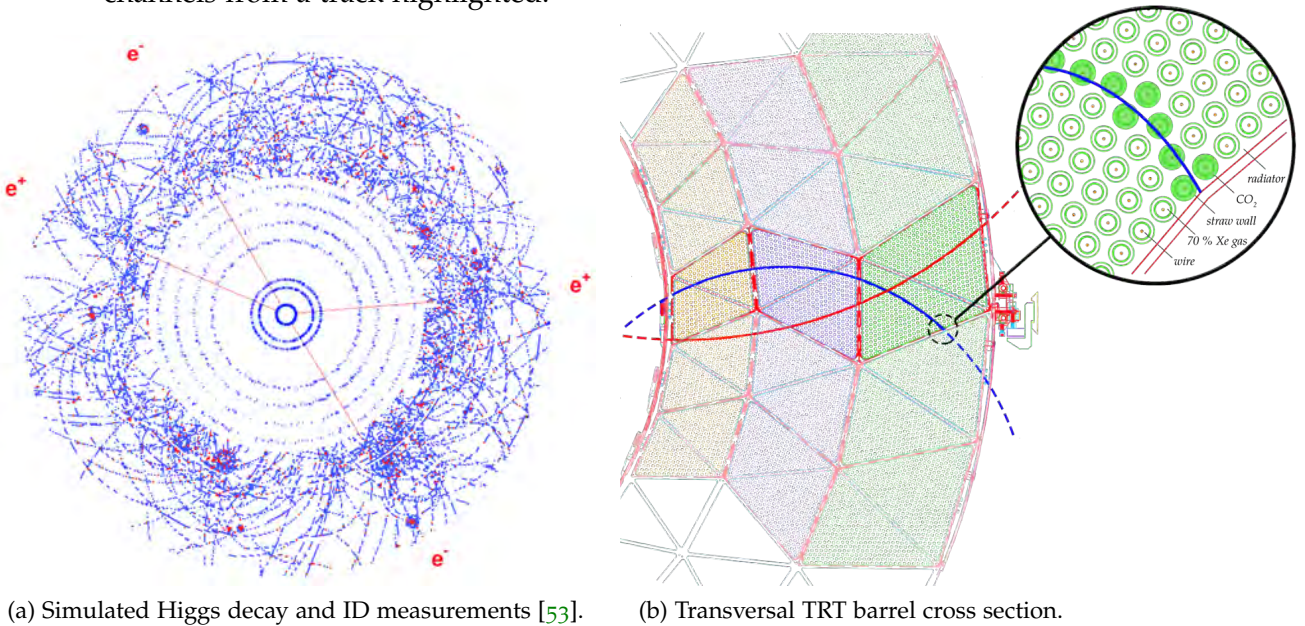


Figure 3.11: Illustration of the ATLAS TRT system.

End-cap disk straws [54].



Straw drift-tubes are used as tracker channels. The straws have a diameter of 4 mm and a length of 39 cm in the end-caps, and 144 cm in the barrel. The sensing is made with a $30\ \mu\text{m}$ diameter gold-plated tungsten wire electrode. The TR photons, emitted as charged particles traverses the detector, are absorbed in the active gas inside the straw tubes, serving as detecting elements for tracking and for particle identification. The straw wall is held at $-1530\ \text{V}$ w.r.t. the sense wire, generating an avalanche gain of 2.5×10^4 .

In the barrel region the straws are placed parallel to the beam-line covering a radii from 554 to 1082 mm and $|z| < 720\ \text{mm}$. In the end-caps the straws are arranged perpendicularly to the beam, covering $617 < R < 1106\ \text{mm}$ and $848 < |z| < 2710\ \text{mm}$. The total volume of the detector is $12\ \text{m}^3$ and a single-point resolution of $170\ \mu\text{m}$ in $R\phi$ direction is achieved. With a lower single-point resolution, the TRT complements the tracking from silicon trackers providing measurements with a large number of hits per track (typically > 30) and a long lever arm coping with better momentum resolution.

SCT The middle region of the ATLAS ID houses the SCT [55], illustrated in Figure 3.12. It is based in semiconductor detectors composed by silicon micro-strips and arranged in 4 concentric barrel layers and two end-caps with nine disks each. The detector has 5.6 m in length and 56 cm in radius and has a total active silicon area of $61\ \text{m}^2$.

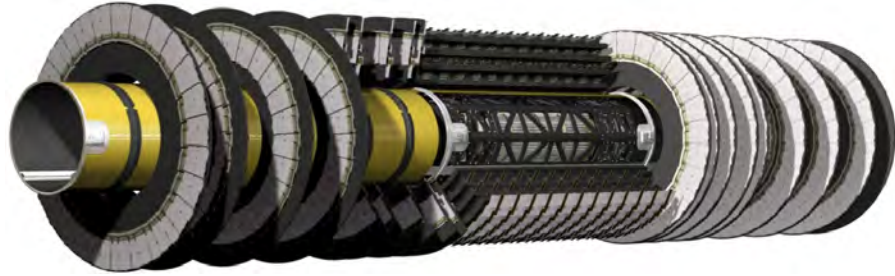


Figure 3.12: ATLAS SCT illustration. Image from [56].

The barrel detector module is made of two pairs of single-sided p-on-n strip sensors daisy-chained. The two sensor pairs are glued back-to-back at a $40\ \text{mrad}$ stereo angle in order to provide two-dimensional hit information. Each sensor thickness is $285\ \mu\text{m}$ with a strip pitch of $80\ \mu\text{m}$. Figure 3.13 shows the complete SCT barrel detector.

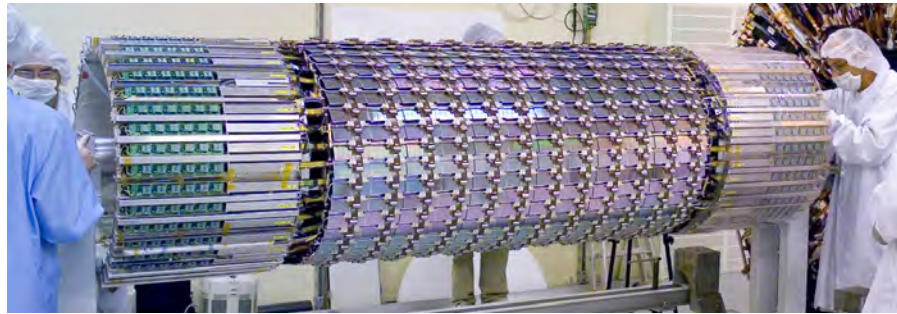


Figure 3.13: SCT barrel detector before insertion into TRT. Picture from [57]

In the end-cap region, the module have the two sides of strips running radially with the same stereo angle as the barrel module. Figure 3.14 shows the three different strip modules implemented in the SCT end-cap disk (right) and a complete SCT end-cap disk (left).

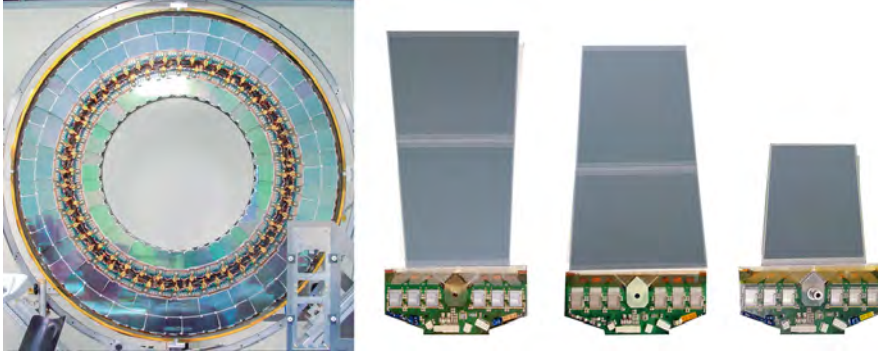


Figure 3.14: The three different SCT end-cap modules (right) and a completed SCT end-cap disk. Images from [58].

With a binary read-out, where the read-out from the strip doesn't allow charge weighted clustering, the spatial resolution achieved in the SCT is $16 \mu\text{m}$ in $R\phi$ and $580 \mu\text{m}$ in z direction.

Pixel detector The ATLAS Pixel Detector [59], illustrated in Figure 3.15 and depicted in Figure 3.16, provides high precision measurements with high granularity. With a high d_0 resolution, the pixel system is the responsible in the ATLAS ID for the identification of short lived particles via displaced vertices.

The original Pixel Detector system consists of three barrels of staves, each with 13 pixel modules, mounted on carbon-composite half-shells at average radii of approx. 5, 9, and 12 cm. There are three disks on each side, covering radii from 9 to 15 cm, each composed of eight sectors on which six pixel modules are loaded. The pixel detector covers an area of 1.7 m^2 with silicon pixel sensors.

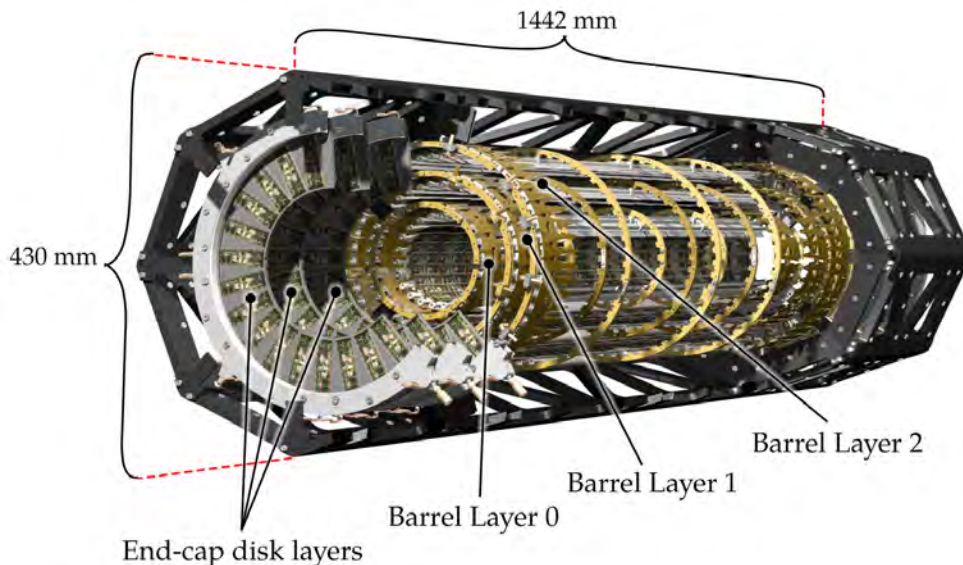


Figure 3.15: Details of the ATLAS Pixel detector [59].

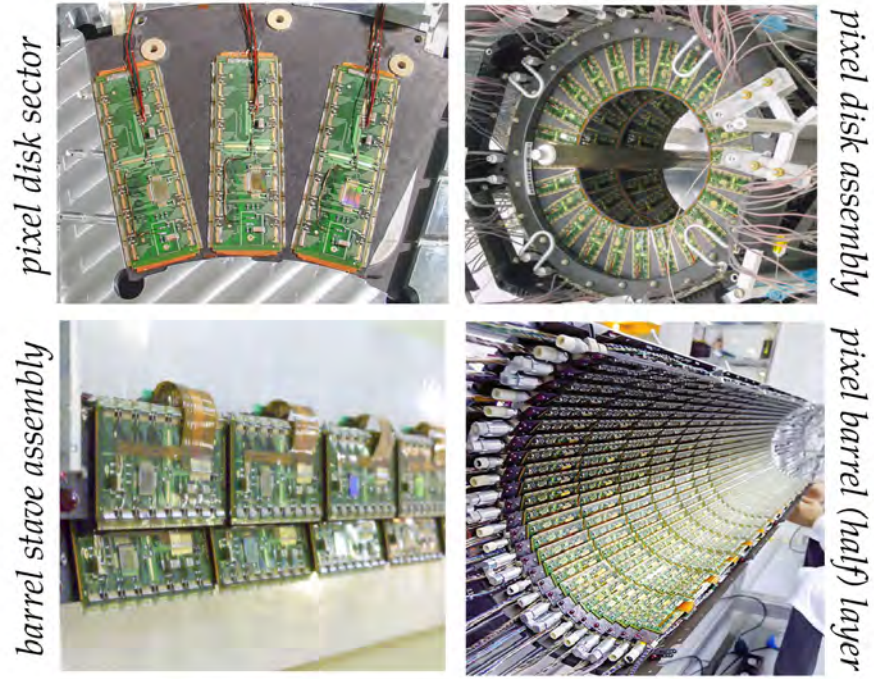
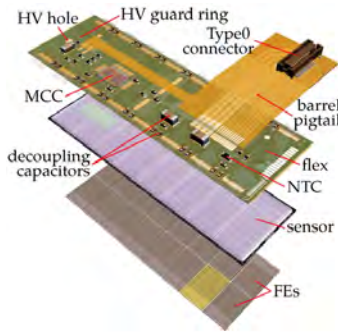


Figure 3.16: Details of the ATLAS Pixel detector

The detector requires a cutting edge technology to meet the space-point resolution of $12\ \mu\text{m}$ and $90\ \mu\text{m}$, in $R\phi$ and Z respectively. In addition, the detector must withstand 50 MRad and over 5×10^{14} neutrons per cm^2 over ten years of operation. The FE-I3 read-out chip (ROC) was designed to fulfil these requirements.

FE-I3 pixel module [60]



The FE-I3 [61], shown in Figure 3.17, developed in a 250 nm CMOS technology, contains an array of 18 by 160 pixels with a pitch of $50 \times 400\ \mu\text{m}^2$. A detector module is composed by 16, 200 μm thick, FE-I3 ROC bump-bonded to a 250 μm planar n-in-n silicon sensor. The assembly size is 62.4 mm long and 21.4 mm wide with $X_0 \sim 2.5\%$. All 16 FE-I3 communicate with the outer world, using optical links, through the Module-Control Chip (MCC), responsible for combining the individual events from the multiple ROCs and distributing the trigger and command signals.

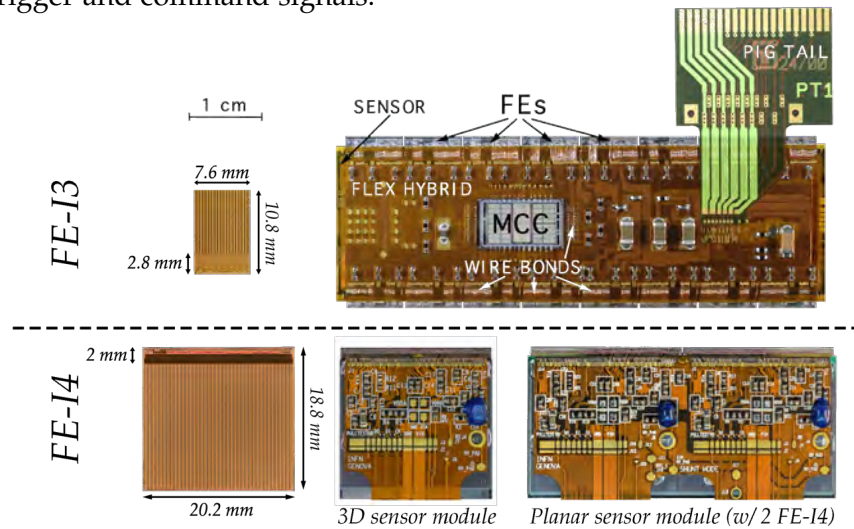


Figure 3.17: FE-I3 and FE-I4 pixel read-out chip and detector modules.

The FE-I3 contains data zero-suppression on chip and is readout with a 40 MHz clock. The analogue part consists of a double stage high-gain pre-amplifier and a differential discriminator (set to a nominal value of $3ke^-$), providing Time-over-Threshold (ToT) measurements that can later be calibrated into deposited energy in the sensor.

During the first long shutdown of the LHC in 2013/14, the pixel detector system was upgraded with the insertion of an additional innermost barrel layer, the Insertable B-Layer (IBL) [62]. The layer, located at 33.5 mm from the interaction point, was built to improve the impact parameter resolution and cope with better cluster separation in high track densities.

Due to the closer proximity to the interaction point a new ROC is needed in order to cope with the higher radiation doses and hit occupancy. The new detector will have to cope with radiation damage up to $5 \times 10^{15} (1\text{MeV}) n_{eq}cm^{-2}$ over the $300 fb^{-1}$ integrated luminosity expected at the end of Run 3.

The new FE-I4 ASIC [63], implemented in a 130 nm CMOS technology, contains a matrix of 80×336 pixels with $50 \times 250 \mu m$ pitch (aiming to improve the impact parameter resolution). It includes a local data buffering in the pixel region and a hit copy mechanism in order to correct for possible time-walk effects. The power consumption in the analogue and digital domain is, respectively, 16 and $6 \mu W/pixel$, significantly smaller when compared with the FE-I3 consumption, of 42 and $34 \mu W/pixel$.

Prior to bump-bonding, to a planar or 3D sensor, the FE-I4 is thinned down to $150 \mu m$. After the ROC-sensor coupling, the IBL module is completed by gluing a thin Cu-kapton flex circuit on the sensor backplane side, which is then wire-bonded to all chip and sensor connections. Figure 3.17 shows the FE-I4 chips and the 3D and planar pixel detector module assembly. The IBL layer is composed by 14 staves, each with 4 3D (single) pixel modules on each extremity and 12 planar (double) pixel modules in the middle. The average amount of material introduced by the IBL staves corresponds to approximately $N_{X_0} = 1.5$. Figure 3.18a shows the 3D modules placed on the stave and Figure 3.18b shows the IBL insertion into the Inner Detector.

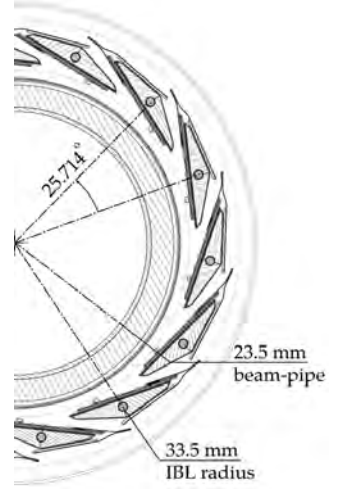
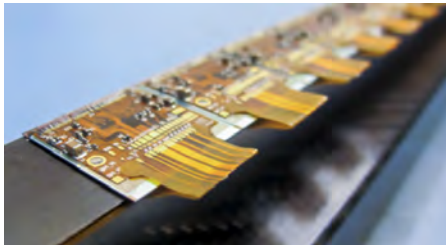
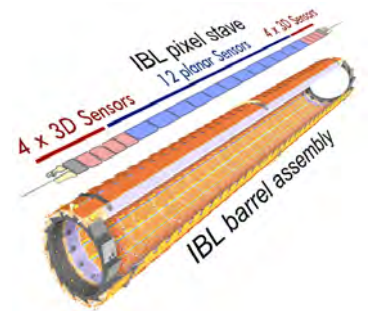


Image adapted from [64]



(a) Pixel modules in IBL stave.



(b) Insertion of new IBL layer.

Figure 3.18: Pictures of the ATLAS IBL stave and layer insertion [65].

The impact parameter resolution depends strongly on the track momentum. The resolution in the high p_T limit is largely determined by the intrinsic spatial resolution of detector sensors and the accuracy

of the alignment of each detector component. Figure 3.19 shows the alignment residuals for the complete IBL (3D and planar sensor).

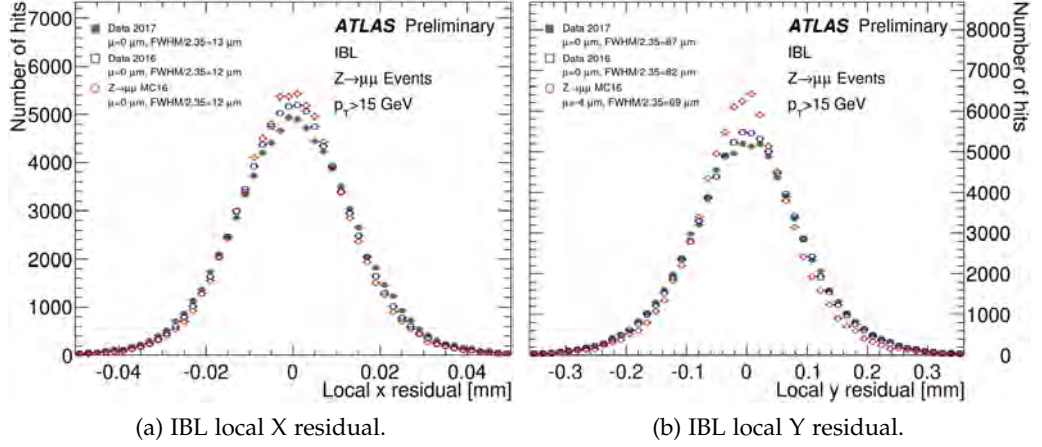


Figure 3.19: X and Y residuals of the ATLAS IBL for 2017 data compared to a run from 2016 and to a simulated $Z \rightarrow \mu^+ \mu^-$ event [66].

The difference in the width of the X and Y residuals of the IBL detector is due to the rectangular size of the pixels, with $50 \times 250 \mu\text{m}^2$. An adjusted Gaussian to the local X residual returns a sigma of $13 \mu\text{m}$ for the latest 2017 data, while the Y residual sigma is $87 \mu\text{m}$. These resolutions will be later compared with the residuals on the HV-CMOS devices under test (DUT) for performance comparison.

Nuclear interactions of primary particles with the detector material is the largest source of background events. Consequentially, the uncertainty in the track reconstruction is directly related with the knowledge of the detector material distribution. In addition, the knowledge of the material type and distribution is essential for the calorimeter energy calibration.

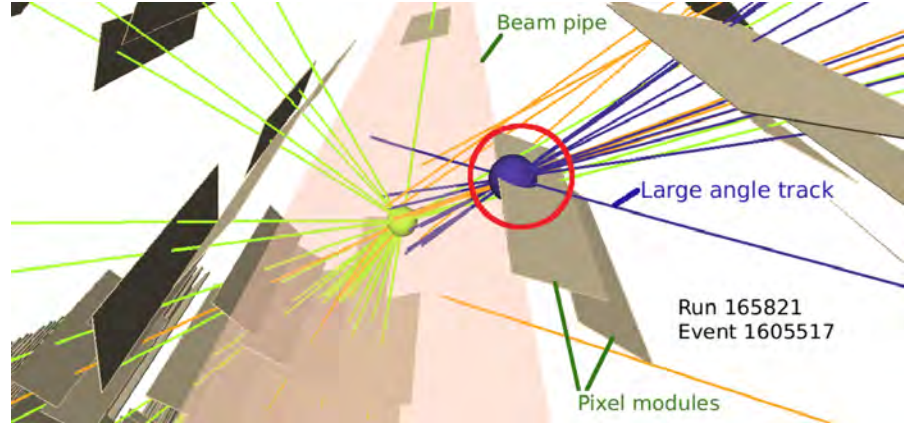


Figure 3.20: Nuclear interaction with detector material [67].

The location of particle interactions with the detector material can be identified by reconstructing secondary interaction vertices containing tracks with large d_0 , as shown in Figure 3.21. Obtaining an accurate description of this material is essential to understand the performance of the detector.

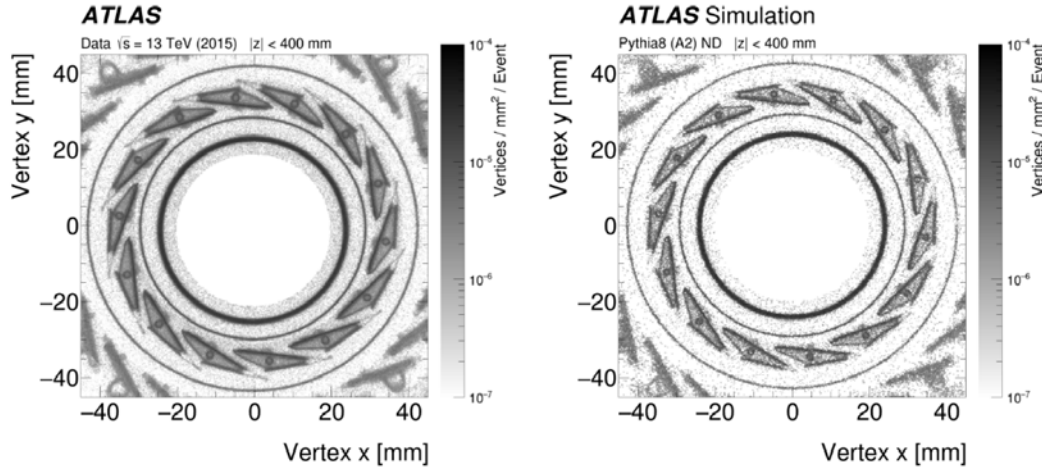


Figure 3.21: Comparison between secondary vertices reconstructed from 2015 data and simulation [68].

The reconstruction of hadronic interaction vertices enables a visual inspection of the material distribution due to its superb position resolution. Figure 3.21 shows a comparison, between real pp data and simulation, of the secondary vertices created by nuclear interactions with the material of the ATLAS IBL layer. The agreement between the position of the secondary vertices with the detector model indicates a good detector alignment and tracking reconstruction.

Figure 3.22 shows the transversal impact parameter resolution for the ATLAS ID as function of the particle p_T . The lower resolution for lower p_T is due to the higher susceptibility of multiple scattering by the detector material, while for high p_T the resolution converges to $\sim 15 \mu m$, mainly determined by the combination of the intrinsic resolution of the different systems in the ID.

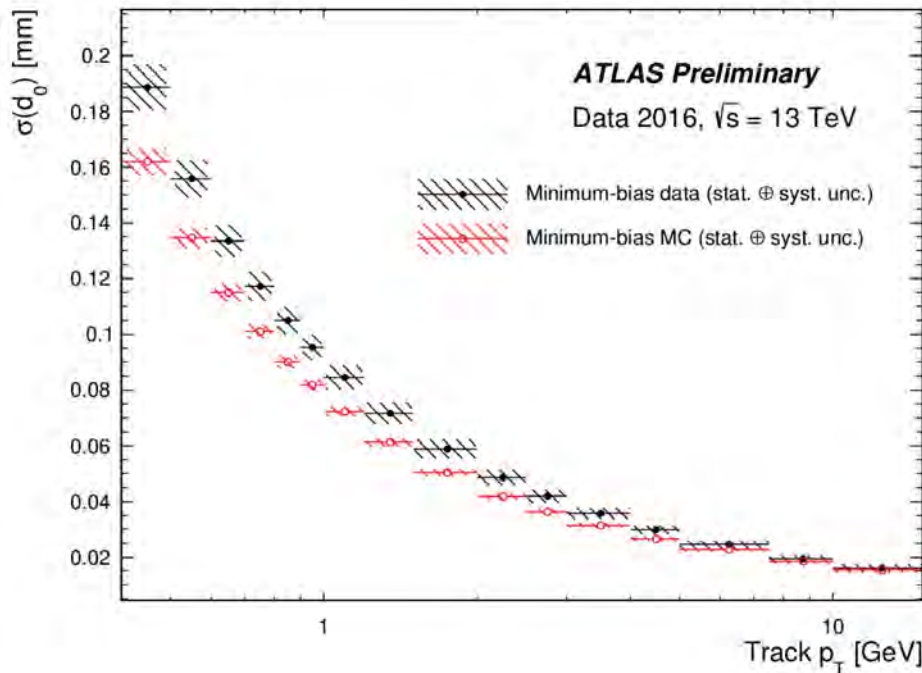


Figure 3.22: Impact parameter resolution as function of the particle transverse momenta [69].

3.1.5.2 ATLAS Inner Tracker upgrade

In order to continue the data acquisition during the HL-LHC operation, without loss of efficiency or reconstruction precision, ATLAS will undergo necessary updates to its sub-detectors systems to withstand the higher instantaneous luminosity. In contrast with the current LHC event pile-up $\langle\mu\rangle = 23$, the expected pile-up for the HL-LHC is $\langle\mu\rangle \sim 23$. The higher track density requires a new detector with higher radiation hardness and finer granularity in order to keep the detector performance at the same level as current ATLAS ID.

The update of the ATLAS tracking and vertex detector system, main focus of this thesis, will replacement of the current ATLAS ID by a new, all-silicon, detector named ATLAS Inner Tracker (ITk). The ITk will be composed of strip detectors [70], arranged in 4 barrel layers and 6 end-cap rings, and pixel detectors [71] placed in 5 barrel layers and several rings. The total active area covered by the strip sensors is 165 m^2 and 12.7 m^2 by the pixel detectors.

Figure 3.23 shows the radiation fluences in the region of the pixel detectors on the new ITk. Due to the higher amount of tracks traversing the detectors the inner layers of the new detector will have to survive higher fluences up to $2 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$, while the outermost layers will have fluences in the order of $10^{15} \text{ n}_{eq}/\text{cm}^2$.

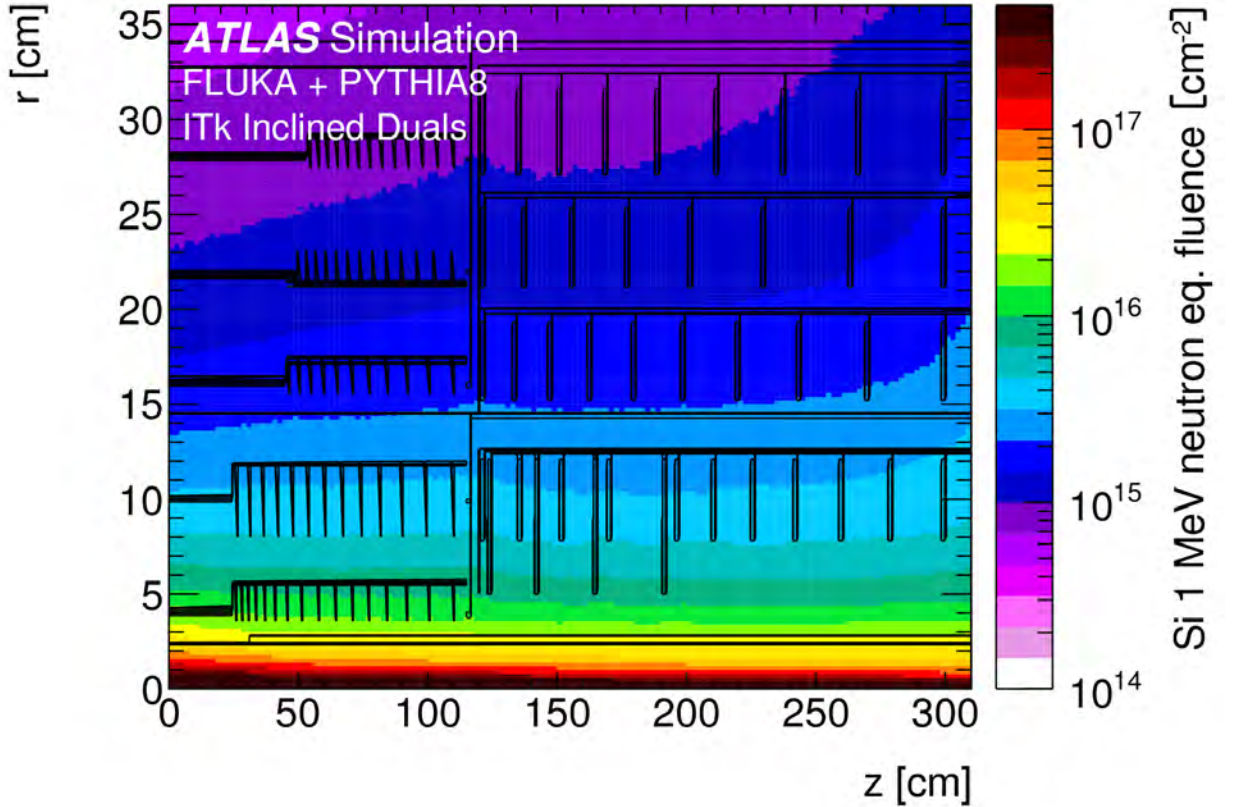


Figure 3.23: Radiation fluences in the ATLAS ITk on the HL-LHC [71].

The final layout of the ITk Pixel Detector is based on a inclined module layout where tracks originating from the interaction point cross the modules at an angle close to normal (reducing the mate-

rial traversed by the particles). The layout used reduces greatly the material budget, as shown in Figure 3.24, complying with the high precision measurement requirements.

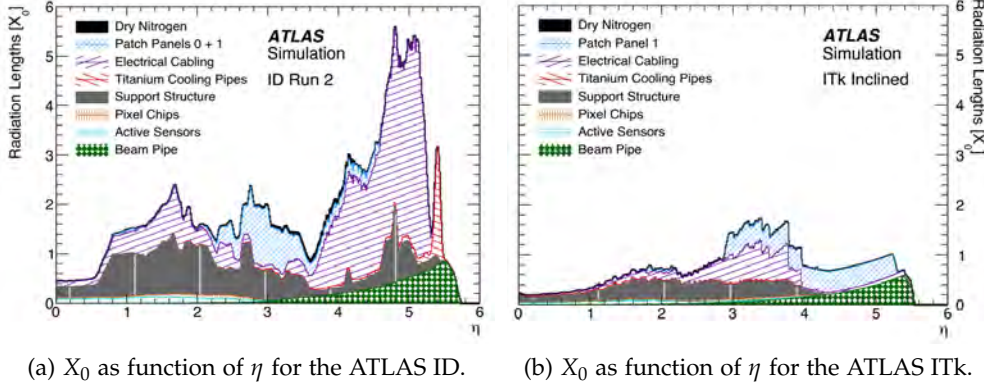


Figure 3.24: Radiation length X_0 versus the pseudo-rapidity η comparison between current ATLAS ID and future ATLAS ITk [71].

To cope with the new detector requirements with the higher occupancy, a new ROC is under development within ATLAS and the RD53 collaboration [72]. The new ROC is designed to be couple to planar and 3D sensor, composed by a pixel matrix with $50 \mu\text{m}$ pitch and binary read-out, limiting the resolution to digital clustering.

Nevertheless, the smaller pixel pitch results in larger charge sharing and better position resolution. For tracks with $p_T \approx 100 \text{ GeV}$ the detector intrinsic resolution dominates and a resolution below $10 \mu\text{m}$ is achieved, as shown in Figure 3.25. In addition, due to the decreased pixel pitch in the Z direction, the expected ITk Z_0 resolution is also better when comparing with ATLAS IBL.

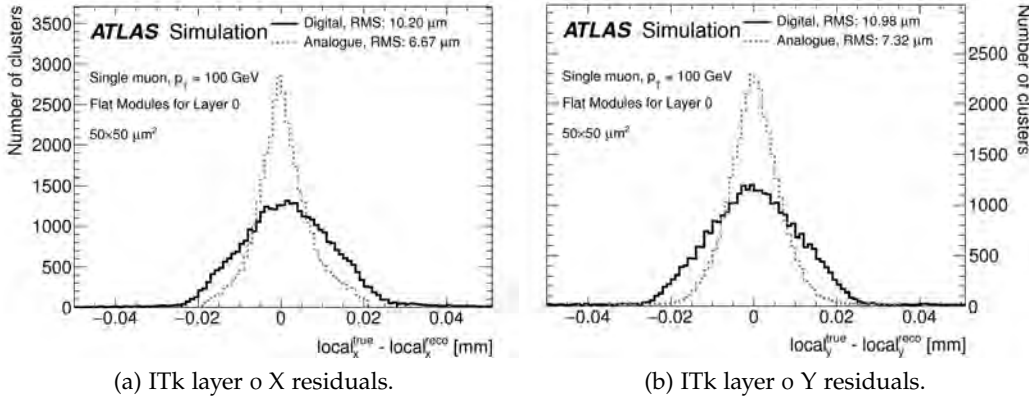


Figure 3.25: X and Y residuals for the ITk layer o barrel pixel detectors [71].

For the the ITk outer layers, which will cover a larger surface area, monolithic CMOS pixel detectors are being investigated to replace traditional bump-bonded hybrid pixel detectors. As CMOS modules already integrates sensor and read-out logic, bump-bonding hybridization (a very labor-, time-, cost-, and yield-loss-intensive production step) is avoided. For this reason, a number of new technologies are been characterized, such as the ams 180 nm HV-CMOS process, investigated on this thesis.

3.1.5.3 CLIC tracker and vertex detectors

CLIC physics program requires an excellent track-momentum resolution and efficient displaced vertices reconstruction. For this reason, a highly granular all-silicon tracking and vertex detectors is being designed. The detector will have in-chip data suppression in order to keep the readout occupancy at an acceptable level, allowing the full read-out of the detector in a trigger-less operation mode. In addition, a 10 ns hit time-slicing accuracy is targeted for the tracking and vertex detectors in order to separate background hits from physics events. Figure 3.26 shows an illustration of the CLIC tracker detector, in yellow, with the CLIC vertex detector on its center, in orange.

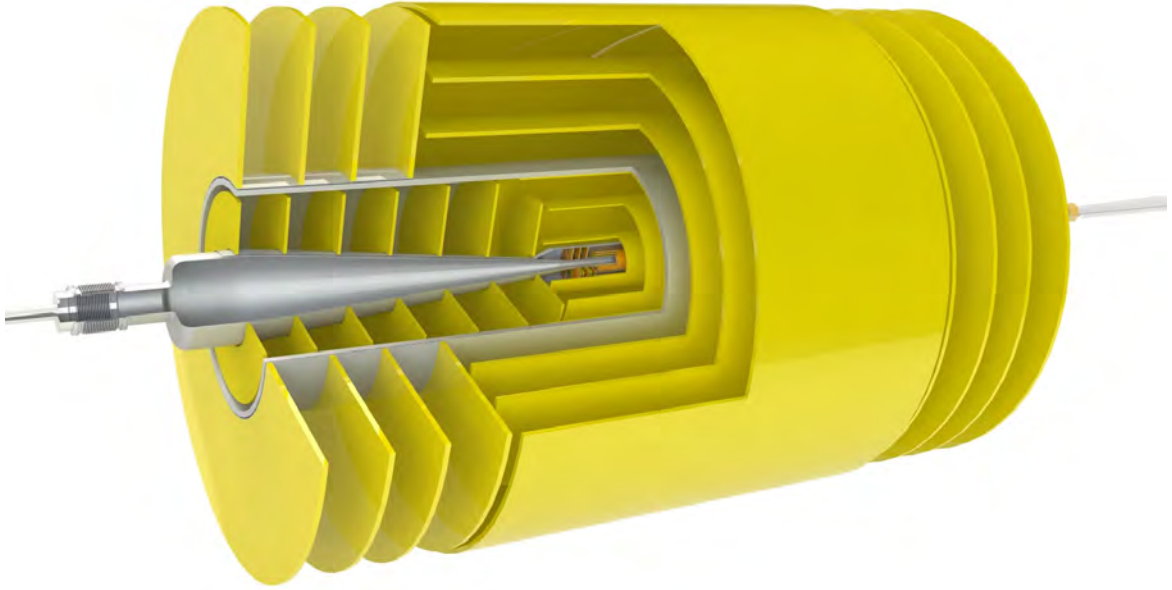


Figure 3.26: CLIC tracker (yellow) and vertex (orange) detectors [73].

In addition, in order to increase the impact parameter resolution a detector with low mass is required, reducing possible multiple scattering with detector material. The material budget available for the tracker and vertex detector is, respectively, $1\text{--}2\ X_0/\text{layer}$ and $0.2\ X_0/\text{layer}$, making the detector cooling more complex. Nevertheless, due to the low duty cycle of the CLIC accelerator (312 bunches in 156 ns long bunch trains every 20 ms) the pulsed powering operation is possible, turning off most high power consumption components on the readout chips during the gaps between bunch trains. The power pulsing of the pixel modules is expected to limit the maximum power dissipation of the readout electronics to about $50\ \text{mW}/\text{cm}^2$, enabling the pixel detector to be air-cooled.

In comparison to the current pixel detectors in the LHC experiments, the expected radiation level in the region of the CLIC vertex detector is moderate. For the inner-detector layers a total fluence of less than $10^{11}\ n_{eq}/\text{cm}^2/\text{year}$ and a total ionizing dose of less than 1 kGy/year are expected. Therefore, radiation hardness on CLIC detectors is not a limiting factor.

The silicon tracker consists of 6 barrel layers, 7 inner discs and 4 outer flat discs, corresponding to an active silicon detection area of $\sim 140 \text{ m}^2$. The tracker must provide a single point resolution of $7 \text{ } \mu\text{m}$ and comply with the required hit time-slicing of 10 ns. In order to cover such large detection area while attending the high demanding resolution requirements, the CLIC tracking detector is envisioned to be constructed with a monolithic detector using short silicon strips, from 1 to 10 mm long.

The vertex detector, illustrated in Figure 3.27, consists of three double layers in the barrel region, ranging from 31 mm to 70 mm in radius, and 3 discs on each side of the detector. The overall length of the barrel vertex detector, built from staves, is 260 mm. The total area of the sensors in the three barrel double layers is 0.487 m^2 . As the detector will be cooled with forced air-flow, the pixel discs are arranged in a spiral geometry, allowing better air-flow inside the vertex detector.

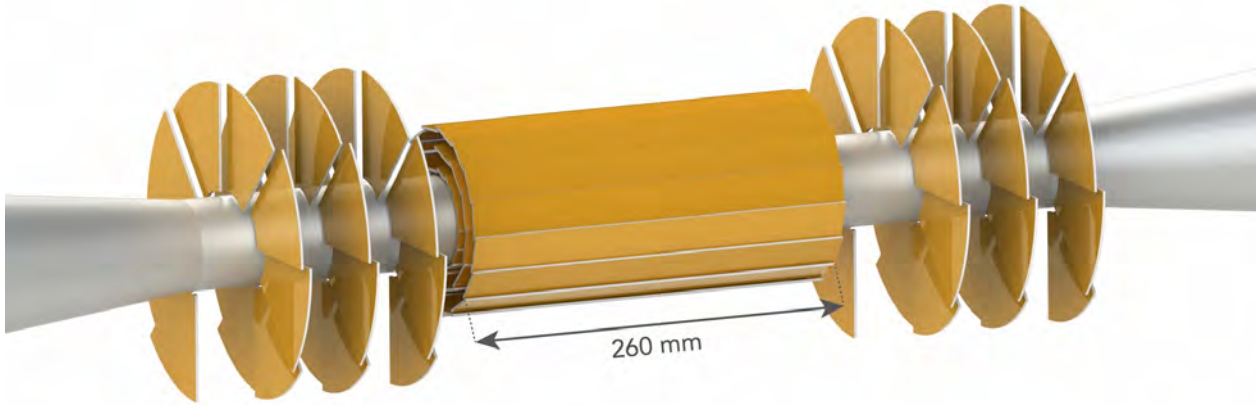


Figure 3.27: Concept of the CLIC vertex detector [73].

To meet the required impact parameter resolution and flavour tagging efficiency, $3 \text{ } \mu\text{m}$ single point resolution has to be achieved throughout the vertex detector. In order to achieve the low mass required with such high single-point resolution, each vertex detector module will be built from $50 \text{ } \mu\text{m}$ thick sensors attached to $50 \text{ } \mu\text{m}$ thick ASICs with $25 \times 25 \text{ } \mu\text{m}^2$ pixels. The read-out pixels are designed with electronics capable of ToT measurement, allowing analogue clustering and coping to achieve the single point resolution required.

Currently, hybrid detector modules with planar sensors (with active edge [74]) or with capacitively coupled sensors [75] are under consideration for the vertex system. As read-out ASIC the CLICpix chip was designed and it will be described in detail in Chapter 5, section 5.3.

Part II

SILICON PIXEL DETECTORS

In this second part, the particle detection mechanism in silicon pixel detectors will be described, from the signal generation to its digital read-out. The HV-CMOS technology will be introduced and the different detector prototypes will be detailed. Finally, the detector tests and module assembly will be briefly discussed. My work is shown on Chapter 6, including: the commissioning of the probe-station, testing the first H35DEMO wafers and developing the programs for the different tests to be performed automatically on the wafer dies; the development of the capacitive coupling flip-chip process of the different HV-CMOS sensors to its respective read-out chips, together with the quality check of the assembly using dedicated test-structure and performing cross-section measurements on the detector prototypes; and on the testing and integration of different detectors to the CaRIBOu DAQ system.

SEMICONDUCTOR DETECTORS

4.1 WHY SILICON?

Silicon is one of the most abundant elements that exists on Earth. During the semiconductor electronics revolution, many industries, developed different technologies with large commercial impact, covering applications from hand-held calculators to satellites.

Silicon is largely used in particle detectors, since the 1960s, as it is the most researched semiconductor in many technological areas, making the electrical properties of silicon very well understood and characterized. When compared with other particle detectors technologies, such as gaseous detectors with ionization energy of about 30 eV, silicon offers a better energy resolution and a larger signal-to-noise ratio (SNR) due to a smaller ionization energy, of ~ 3.6 eV for the e^-h^+ pair generation. With the low ionization energy and good SNR, allowing the construction of sensors as thin as $50\text{ }\mu m$, minimizing multiple scattering, silicon detectors are largely used to measure the particle tracks, as close as possible to the beam interaction point.

4.2 PARTICLE DETECTION WITH SEMICONDUCTORS

A particle detector is composed by several components: a detection medium is needed, where particles will interact and leave a signal; the signal needs to be conditioned, with the use of amplifiers and shapers, before being processed; analog-to-digital converters are used for further signal processing and a digital logic is needed for the detector read-out. Different detector architectures can be used to implement these components according to the experiment requirements. Detectors can be classified as:

hybrid detectors Detectors where the sensitive material of the detection system is designed and produced decoupled from the detector read-out electronics, on a separate physical device. This approach provides a few advantages, such as the possibility of optimize the sensor design in parallel to the read-out architecture (possibly using a different semiconductor technology than the sensor). Nevertheless, a drawback, for example, is the necessity of a sensor/read-out integration which adds a further step on the detector construction, meaning more time/money spent.

monolithic detectors Are detectors with the particle sensitive material developed and integrated on the same device as the read-out

circuit (ROC). By skipping the interconnection between sensor and ROC, the detector production can be simplified significantly. A possible disadvantage is that the choice of technology is more restricted and one can offer advantages for the particle sensing, while not allowing a high performance read-out architecture design.

A few semiconductor detector technologies are listed: hybrid silicon micro-strips and pixel, planar or 3D sensors; High-Voltage CMOS (Complementary Metal-Oxide-Semiconductor) devices as capacitively coupled or monolithic detector; MAPS (Monolithic Active Pixel Sensors) using High-Resistivity HR-CMOS technology; Silicon on Insulator (SOI) detectors. Details about these and more detector technologies can be found in [76][77].

Independent of the semiconductor technology, the charge detection mechanism on the semiconductor sensitive bulk is the same, described over the next sections.

4.2.1 Semiconductor theory

4.2.1.1 Silicon intrinsic charge carrier

When single atoms are grouped forming a crystal lattice, such as silicon atoms forming a diamond structure, the atom's electronic orbitals begins to overlap. As the Pauli exclusion principle dictates that electrons can not have the same quantum numbers, atomic orbitals split into N molecular orbitals, each with a slightly shifted energy, where N is the number of atoms in the crystal. Since N is a large number ($\approx 10^{22}$), each orbital energy level suffers a small shift, making adjacent orbitals to have extremely close energy levels, apart from each other by about 10^{-22} eV, allowing the orbitals to be considered as a continuous energy band. This mechanism is illustrated in Figure 4.1, showing the discrete s and p electron orbital levels when atoms are too far from each other, not forming a crystal lattice, and how the orbital levels get degenerated as the atoms get close together. The silicon lattice structure has a lattice distance of 5.431 \AA .

Si face-centered cubic lattice [79]

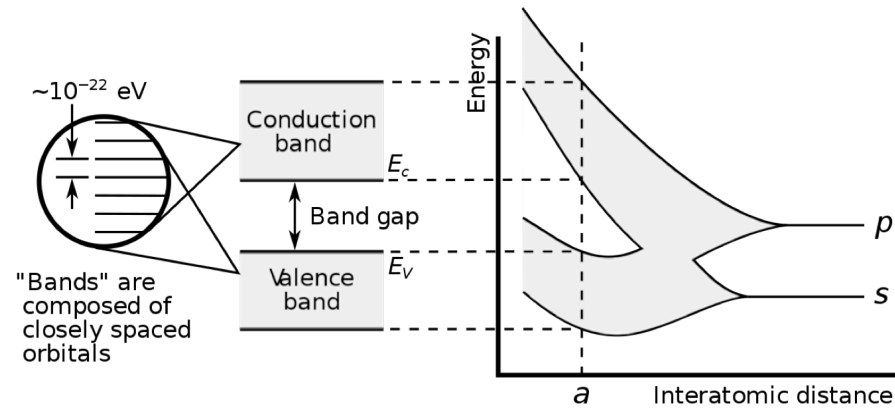
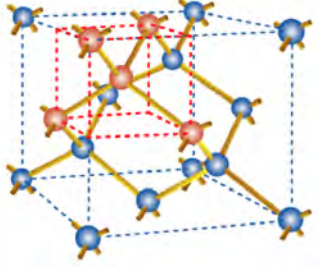


Figure 4.1: Illustration of degenerate energy levels in the lattice split into closely spaced bands, as function of the inter-atomic distances [78].

As the name states, the electrical conduction of semiconductors lie in between insulators and conductors. The distinction between the material classification comes from the size of the *energy-band gap* - an energy region between the valence and conduction band that charge carriers can not occupy. The conductivity of a material arises from the capability of the promotion of electrons from the valence band into the conduction band.

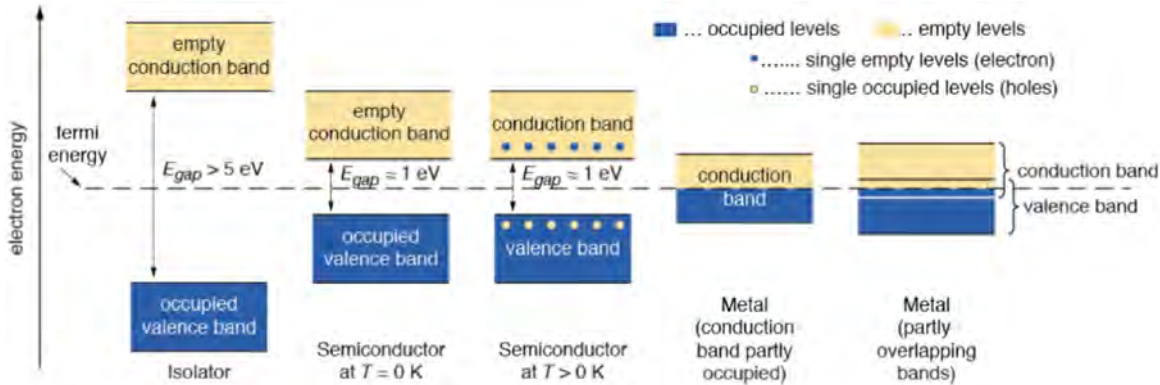


Figure 4.2: Relative valence and conduction band spacing for insulators, conductors, and semiconductors [80].

The valence band is occupied by the highest binding energy electrons in the atom, located at the last electronic orbitals, therefore taking part in chemical bonds. Silicon forms its crystal lattice by sharing its four valence electrons in four covalent bonds, as illustrated in Figure 4.3. The conduction band is occupied by charge carriers that have enough energy to not get associated with atoms in the lattice, being able to move freely across the array. In conductors, the valence band overlaps with the conduction band. Hence, conductors, such as metals, contain only weakly bound electrons and its charge carriers are free to move and conduct electricity with the presence of the weakest electric field. In non-conductors, the valence and conduction bands have a separation energy, named *band gap*, that corresponds to the energy needed to disassociate an electron from a lattice bond. Semiconductors are specific materials where it is possible to control the band-gap structure, changing the material electrical properties.

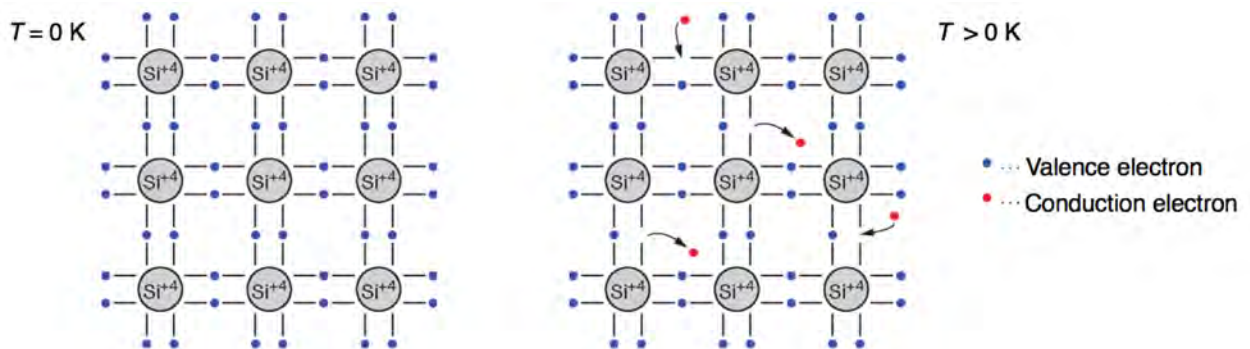


Figure 4.3: Illustration of the silicon crystal lattice and an electron being promoted to the conduction band by the thermal energy [80].

At $T = 0$, in a silicon bulk free of impurities (intrinsic silicon), the valence band is complete and the conduction band is empty. At $T \neq 0$, the electron concentration, n , at the conduction band, and holes¹, p , at the valence band, is equal to the, so called, intrinsic concentration n_i , $n_i = n = p$.

Regarding intrinsic silicon, it is possible to calculate n and p by multiplying the Fermi-Dirac distribution with the possible states density $N(E)$, which depends on the energy of the charge carriers [77]. The probability of a state with energy E being occupied is:

$$P(E) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \approx e^{-\left(\frac{E-E_F}{kT}\right)} \quad (\text{for } E - E_F \ll kT) \quad (4.1)$$

where E_F is the Fermi energy, k is the Boltzmann constant, and T is the temperature (kT is ~ 0.03 eV at room temperature).

The state density is given by:

$$N(E) = 4\pi \left(\frac{2m_{n(p)}}{h^2} \right)^{\frac{3}{2}} \sqrt{E} \quad (4.2)$$

where h is the Planck constant and $m_{n(p)}$ is the electron (hole) effective mass. Therefore, n or p can be calculated as

$$n(p) = \int_{E_c}^{E_{max}} P(E)N(E)dE = 2 \underbrace{\left(\frac{2\pi m_{n(p)}kT}{h^2} \right)^{\frac{3}{2}}}_{N_{C(V)}} e^{-(E_{C(F)} - E_{F(V)})/kT} \quad (4.3)$$

where E_V , E_F , and E_C are the energy at the last level of the valence band, the Fermi energy, and the first level of the conduction band, respectively. It is interesting to note that the product between the electron and hole concentrations is independent of the Fermi energy level or the purity of the bulk. For a given temperature and band-gap,

$$np = n_i^2 = N_C N_V e^{-E_g/kT} \quad (4.4)$$

with E_g being the band-gap energy. Therefore, the charge carriers concentration for a silicon bulk at 300 K is

$$n_i = \sqrt{np} = \sqrt{N_C N_V} e^{-E_g/2kT} = 1.45 \times 10^{10} \text{ cm}^{-3} \quad (4.5)$$

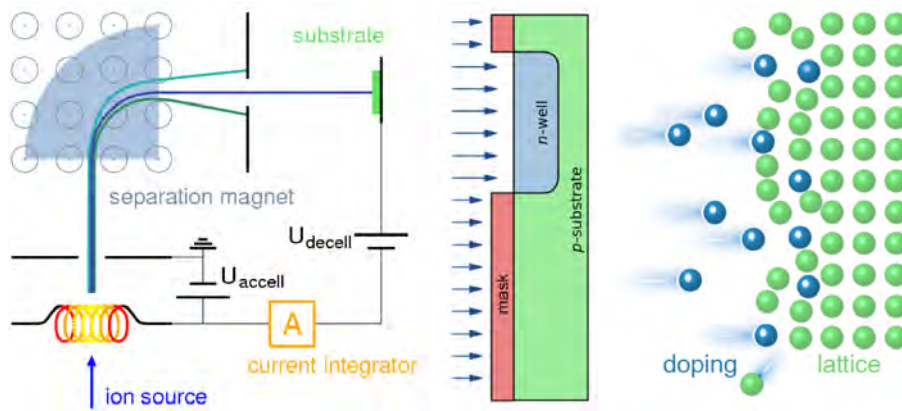
With a minimum ionizing particle (MIP) generating about 24 k electrons in a 300 μm silicon sensor (see Section 4.2.2.1), any electric signal generated by a particle interaction would be lost inside the noise generated by the electron-hole pairs thermally created in the sensor bulk. In order to make silicon viable as a sensitive material for particle detection, silicon doping is needed to change its electrical properties.

¹ If an electron is promoted to the conduction band, its vacancy in the valence band, or hole, has a positive net charge and can also be treated as a particle.

4.2.1.2 Silicon doping

The mechanism used to control the silicon electrical properties is called *doping*. It consists of inserting specific atomic impurities, creating additional energy levels for the charge carriers in the band-gap region.

An ion implantation system, illustrated in Figure 4.4, consists of an ion source, an accelerator, and a target chamber where the material to be implanted is located. The total amount of ions implanted in the target, or dose, is the integral over time of the ion current. The ion energy ranges from keV, with ions implantation mainly over the material surface (with depth in the order of nanometers), up to MeV, depositing the ions deeper in the bulk, $\sim 6 \mu\text{m}$ from the surface (according to the Bragg peak).



(a) Ion accelerator scheme [81]. (b) Doping mask [82]. (c) Ion implantation [83].

Figure 4.4: Illustration of silicon doping.

Distinct ions are used to add different energy levels in the band gap region, tuning the material conductivity with energy levels closer or further from the conduction and valence bands. The additional energy levels increase the probability for an electron/hole excitation. Figure 4.5 shows the additional energy levels, inserted in the band gap, for each specific doping. Blue lines and the letter *D* indicate charge donor doping, while red lines and the letter *A* represent charge

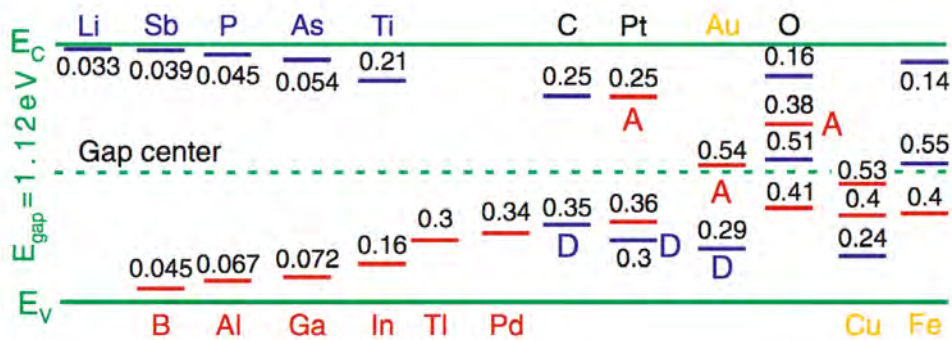


Figure 4.5: New energy levels allowed in the band gap region, added by the impurities. Phosphorus, for example, introduces a new level only of 0.045 eV from the conduction band. Image from [76].

acceptor-like doping. The distance to the valence or conduction band is also indicated (in eV).

By introducing elements from group V of the periodic table, such as phosphorus as illustrated in Figure 4.6, with 5 electrons in its valence band, an excess of weakly-bound electrons will be created. When silicon is doped with donor type elements, the silicon is called *n-type* silicon.

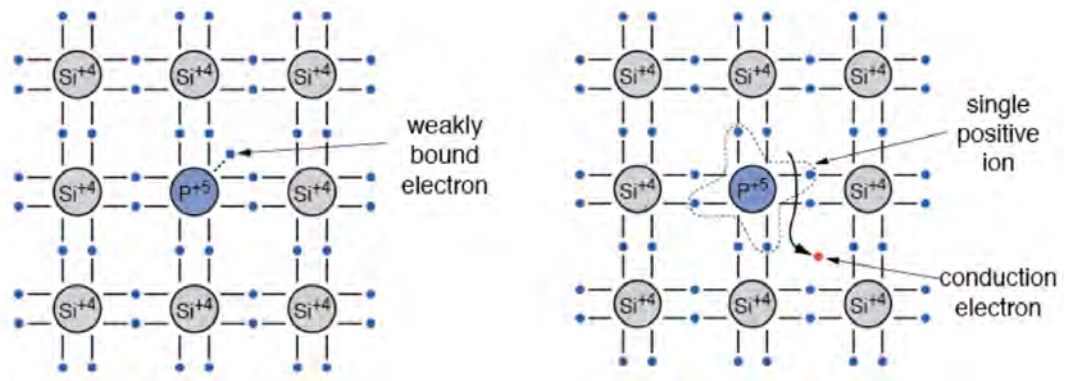


Figure 4.6: Phosphorus doping in a silicon crystal lattice, inserting an weakly bounded electron, increasing the lattice conductivity [80].

Such doping is classified as *donor type* as it introduces (almost) unbounded electrons in the crystal lattice, "donating them" to the lattice, increasing its conductivity. Figure 4.7 indicates the proximity of the additional energy level created by a donor, n-type, doping to the conduction band. Typically, the thermal energy available can be enough to excite the doping electrons and promote them to the conduction band.

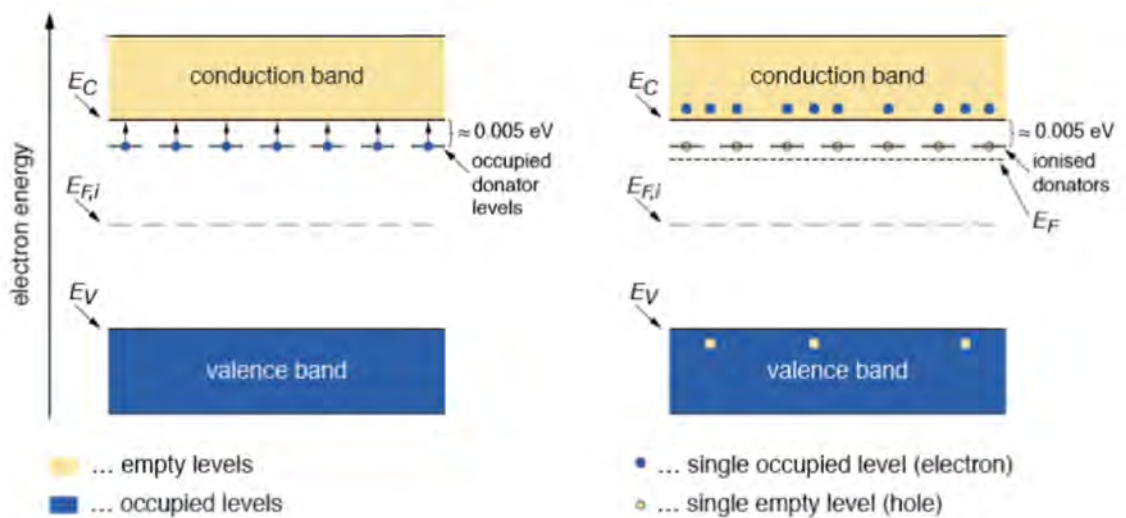


Figure 4.7: Donor type energy level illustration [80].

The other type of doping is done with elements from the periodic table group III, such as boron, as illustrated in Figure 4.8, with only 3 electrons in the valence band. When these elements are inserted in between the silicon lattice, the lack of one electron (in comparison

with the silicon atom) creates an electron vacancy in the crystal lattice. Other electrons from the lattice can migrate and occupy this vacancy, effectively moving it to another position in the lattice. Therefore it acts as a particle with a positive net charge - a hole. This type of doping is called an *acceptor* and creates *p-type* silicon.

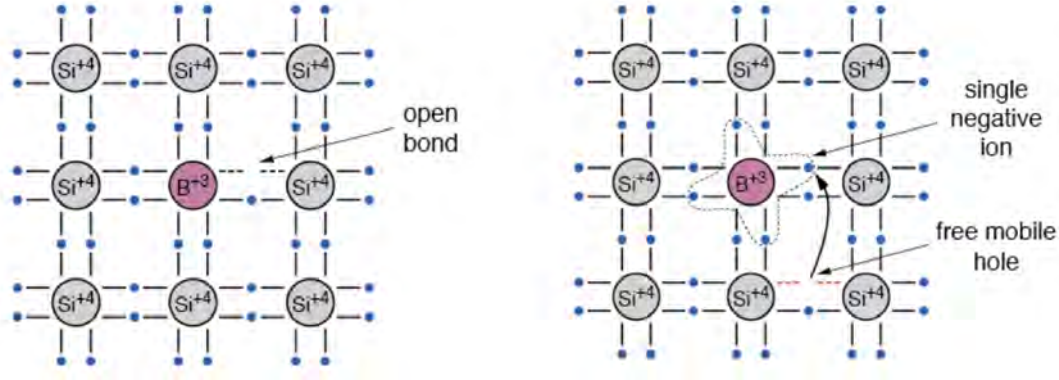


Figure 4.8: Boron implantation in the silicon crystal lattice [80].

Figure 4.9 illustrates the additional energy level created by the p-type doping. As it is close to the valence band, the thermal energy available can promote electrons to occupy the vacancy/hole introduced by the doping. This will propagate the hole to new positions, conducting a positive net charge over the lattice.

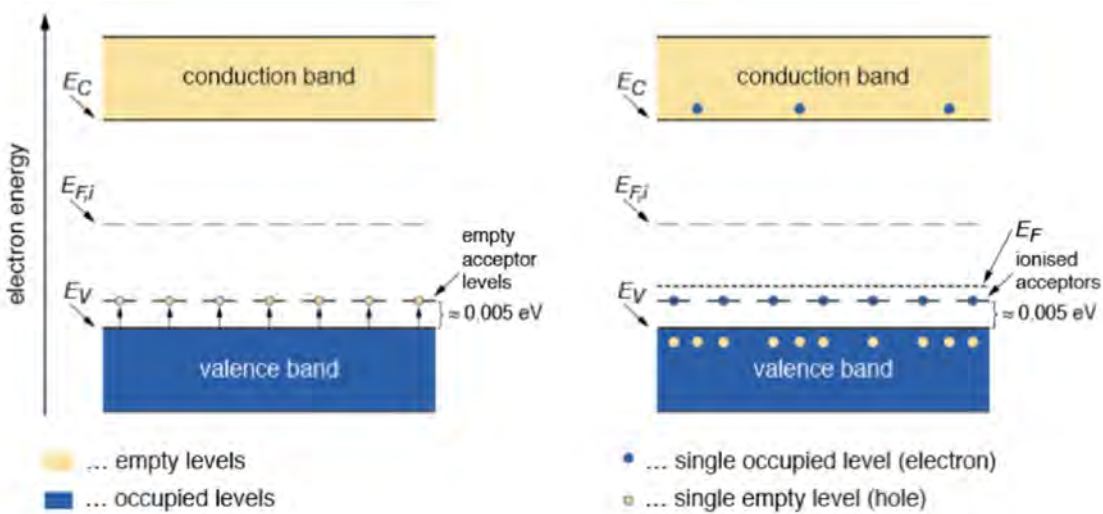


Figure 4.9: Acceptor type energy level illustration [80].

The concentration of new charge carriers is approximately the same as the doping concentration, making the new (doped) silicon resistivity, ρ , to be a function of the doping concentration, N , and of the mobility, μ , of the charge carrier added by the doping. It can be written as:

$$\rho = 1/eN\mu \quad (4.6)$$

where e is the electron/hole charge.

4.2.1.3 The PN junction

It might seem contradictory that the end of the previous section states that doping would help to make the signal generated by a particle interaction more distinguishable w.r.t. the thermal electric noise in the crystal lattice. Until now, doping only introduced more charge carriers, that will increase the electric noise even further. In order to cope with this, it is needed to lower the charge carrier concentration by several orders of magnitude. This can be done by using cryogenic temperatures, or by depleting the silicon bulk of charge carriers, by combining n-type and p-type silicon, forming a PN junction. As the cryogenic cooling is not practical for the detectors, the properties of PN junctions is explored.

Doping is essential to build the basic building-block for semiconductor detectors, and all modern electronics devices: the PN junction. Illustrated in Figure 4.10, the PN junction is the interface region between n-type and p-type silicon. It is depleted, free of charge carriers, as the charge carrier of each silicon type will recombine through drift and diffusion along the junction.

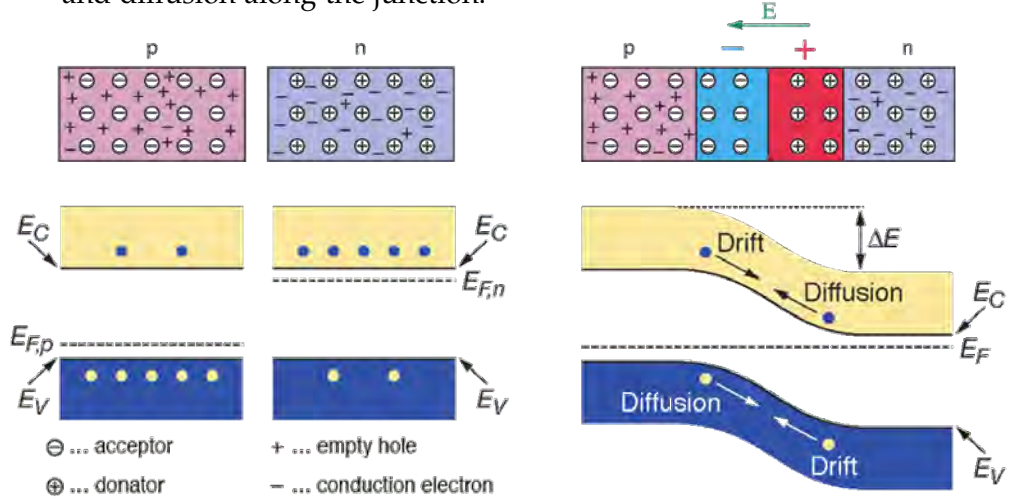


Figure 4.10: Energy bands and levels in a PN junction [80].

In the depleted region there will be an excess of charge from the doping ions fixed in the crystal lattice. This excess will generate an electric field that will balance out the drift/diffusion of the charge carriers, leading the system to equilibrium and generating an intrinsic potential barrier, V_{bi} (built-in voltage), usually in the order of 0.5V.

The equilibrium region, characterized by the lack of free charge carriers, extends to a width, W , around the PN junction and is called *depletion zone/region*. The extension of the depletion zone depends on the doping concentration N and on the voltage V_{bias} across the junction and is written as:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V_{bi} - V_{bias})}, \text{ where } V_{bi} \approx \frac{kT}{e} \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad (4.7)$$

where ϵ_0 and ϵ_{Si} are the vacuum and silicon permittivity, respectively, N_A is the p-type (acceptor) doping and N_D is n-type (donor) doping concentration [77].

In silicon sensors, the PN junction is usually done using different concentrations of p-type and n-type doping. The construction of silicon pixel sensors is done by starting with an already doped bulk, with concentration in the order of 10^{12} cm^{-3} , and depositing an array, forming the pixel matrix, of (the opposite type) doping, usually with concentration $> 10^{18} \text{ cm}^{-3}$. In this way, the depleted zone extends deeper inside the silicon bulk than into the pixel implants.

Therefore, Equation 4.7 can be re-written as:

$$W = \sqrt{\frac{2\epsilon_0\epsilon_{Si}(V_{bi} - V_{bias})}{eN}} \approx \sqrt{2\epsilon_0\epsilon_{Si}(V_{bias}\mu\rho)} \quad (4.8)$$

where μ , ρ and N were already defined in Equation 4.6, and having in mind that usually, V_{bias} is much larger than V_{bi} .

4.2.1.4 PN junction polarization

As Equations 4.7 and 4.8 show, an external voltage V_{bias} can be applied through the junction. This voltage can help to increase, or decrease, the extension of the depletion zone, depending on the polarization of the applied voltage.

With a direct polarization, illustrated by the left image in Figure 4.11, the potential difference between the extremities of the junction will create an electric field in the opposite direction w.r.t. the field created by the intrinsic potential, making the effective potential barrier, that maintains the PN junction in equilibrium, lower. Therefore, electrons in the conduction band, in the n-side of the junction, can migrate to the conduction band in the p-side if $V_{bias} > V_{bi}$. In silicon, V_{bi} is typically $\sim 0.7\text{V}$.

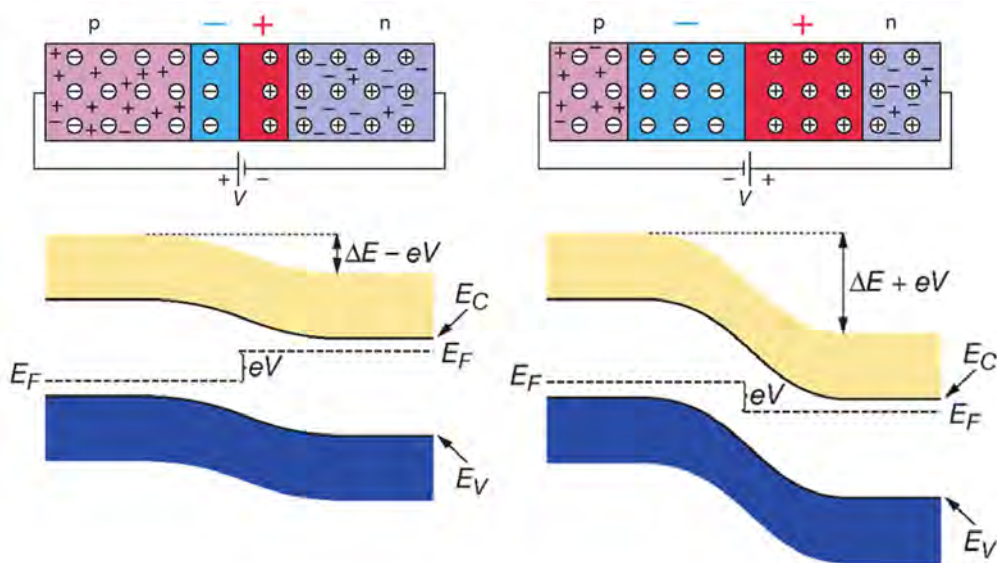


Figure 4.11: Energy bands and level on a polarized PN junction [80].

In the reverse polarization, illustrated on the right side of Figure 4.11, the voltage applied generates an electric field on the same direction as the intrinsic field generated by the junction built-in potential. With the reverse polarization, the holes are attracted to the negative side of the potential, while the electrons go towards the positive terminal node, extending further the depletion region W .

Equation 4.8 can be re-written to return the needed bias/polarization voltage needed to fully deplete the junction, extending the depletion zone through the silicon bulk thickness d :

$$V_{dep} = d^2 / 2\epsilon_0\epsilon_{Si}\mu\rho \quad (4.9)$$

Equation 4.9 is a model for ideal diodes. Nevertheless, it is a good approximation for the depletion voltage for real pixel sensors with the same thickness d .

The sensor depleted zone is the region effectively sensitive for the detection of particle interactions. As it is free of charge carriers, any electron-hole pair created by an ionizing radiation will be separated before recombining, by the electric field generated by V_{bias} , with each charge carrier drifting towards the electrodes. Therefore, sensors with the depletion region extending completely through the sensor bulk will yield the best SNR. Normally, $V_{bias} > V_{dep}$ in order to create a strong electric field inside the sensor, making electron-hole pair recombination less probable to happen and charge drift faster. The limit for V_{bias} is the voltage where the silicon has its dielectric breakdown (in the order of $30 \text{ V}/\mu\text{m}$).

As the sensor is reversely polarized, the major charge carrier is halted from movement through the increased barrier potential across the PN junction, while there is a constant removal of the minority charge carriers from the ions implanted in the crystal lattice. This generates a dark current, also called *leakage current* J_{leak} . Typical values for silicon pixel sensors are in the order of $1 \text{ nA}/\text{cm}^2$, and it is highly dependent on the temperature, as thermal energy can excite charge carriers. The leakage current can be expressed as:

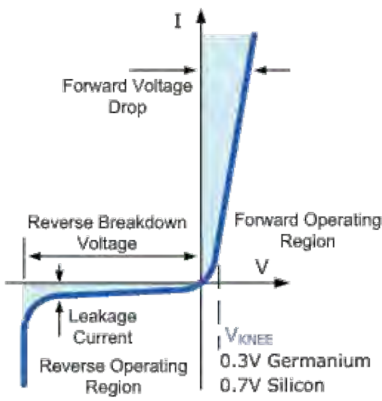
$$j_{leak} = -e \frac{n_i}{\tau_g} W = -e \frac{n_i}{\tau_g} \sqrt{2\epsilon_0\epsilon_{Si}(V_{bias}\mu\rho)} \quad (4.10)$$

where τ_g is the carrier generation life-time [77]. Using n_i from Equation 4.3, Equation 4.10 can be re-written as:

$$j_{leak} = \frac{-e}{\tau_g} \sqrt{2\epsilon_0\epsilon_{Si}(V_{bias}\mu\rho)} 2 \left(\frac{2\pi m_{n(p)} kT}{h^2} \right)^{\frac{3}{2}} e^{-(E_{C(F)} - E_{F(V)})/kT} \quad (4.11)$$

In this formula it is possible to see the dependence of the leakage current on the temperature, as previously mentioned. As the bias voltage increases and the full volume is depleted, the leakage current saturates until the dielectric breakdown voltage, as shown in the image on the left margin.

Characteristic current vs voltage curve for a PN junction diode [84]



As a summary of the different semiconductors properties discussed so far, Figure 4.12 is a nomogram² correlating most of the semiconductor sensor parameters. Any straight line traversing the diagram will cross the axis correlating an approximation of values encountered in real devices.

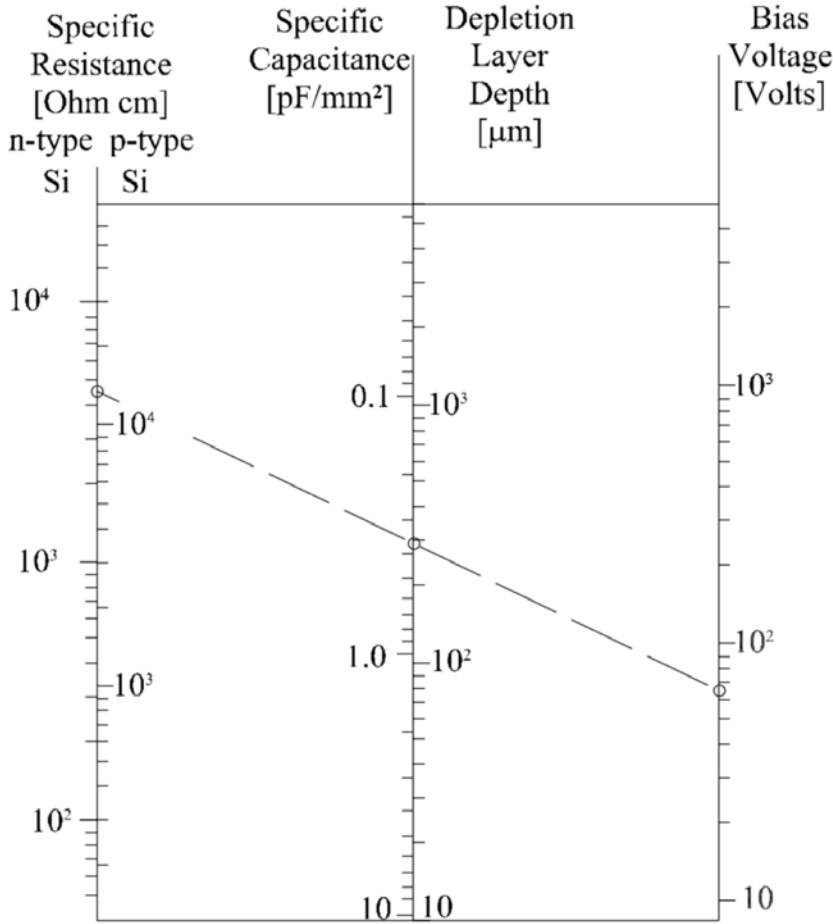


Figure 4.12: Nomogram correlating the principal properties of a semiconductor sensor. Any straight line provides, to first order, the characteristics of a certain sensor. Extracted from [77]

4.2.2 Particle interaction with matter

Silicon detectors operate by measuring the ionization of the sensor silicon bulk upon radiation incidence. The following sections will describe the type of interactions that different type of particles can have with matter.

² A nomogram, or nomograph, is a two-dimensional diagram designed to allow the approximate graphical computation of a mathematical function, invented in 1884 by the French engineer Philbert Maurice d'Ocagne (1862-1938). It provides a fast graphical way to calculate complicated formulas to a practical precision.

4.2.2.1 Charged particles

Electrically charged particles will interact with the sensor material via the electromagnetic force. The radiation interaction can happen with the atomic orbital electrons or with the atomic nucleus, depending on the radiation energy. In addition, if the radiation is composed by particles with color charge, such as the proton or other hadrons, it can also interact with the atomic nucleus via the strong force.

The electromagnetic interaction happens continuously as charged particles traverse the material media, due to the extension of the electric field of the electronic orbitals. It can be seen as a series of collisions where the incident particle loses gradually its energy. The interaction goes until the material is completely traversed or until the incident particle loses all its energy. The average energy lost by a particle traversing matter and is described by the Bethe-Bloch Equation 4.12.

$$\left\langle \frac{dE}{dx} \right\rangle = -Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \quad (4.12)$$

where z is the material atomic number, A is the atomic mass, K is a constant equal to $0.307 \text{ MeV mol}^{-1} \text{ cm}^2$. I is the average excitation energy of the media, $\delta(\beta\gamma)$ is a relativistic factor describing the transversal electric field of the incident particle, $\beta = v/c$ and $\gamma = 1/\sqrt{1-\beta^2}$, with v being the velocity in the observer frame of reference. T_{max} is the maximum kinetic energy transmitted to a free electron [85].

The average energy lost $\left\langle \frac{dE}{dx} \right\rangle$ is also called *stopping-power* and it is shown in Figure 4.13 for a muon traversing copper is, as function of $\beta\gamma$.

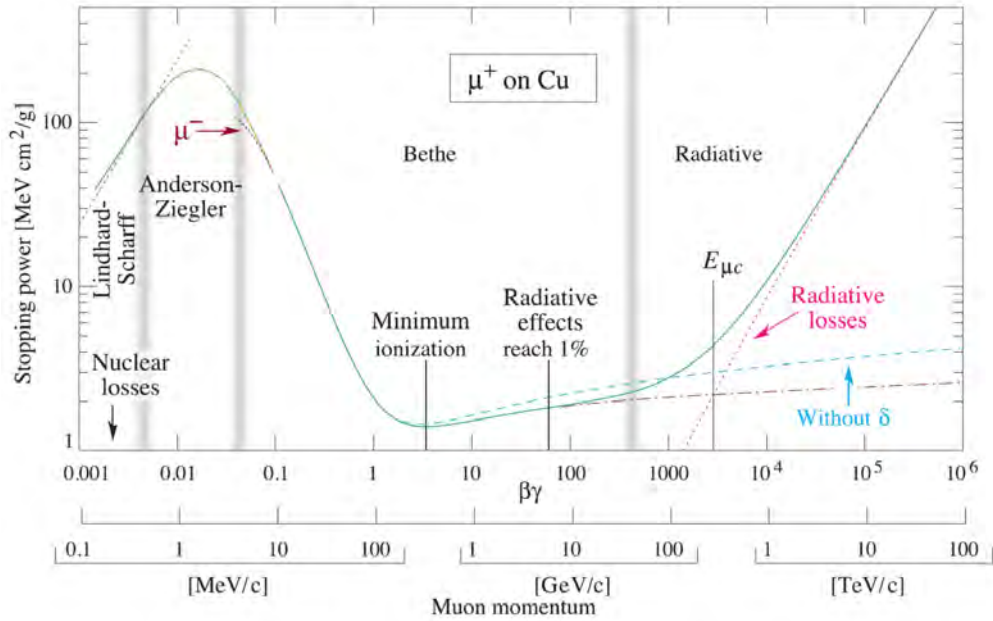


Figure 4.13: Average muon energy loss traversing copper as a function of muon momentum [85].

The $\beta\gamma$ region between 0.1 and 10^4 , well described by the Bethe-Bloch equation, is of big interest to semiconductor detectors. Figure 4.14 shows the average stopping-power for different particles and media, for the mentioned $\beta\gamma$ range.

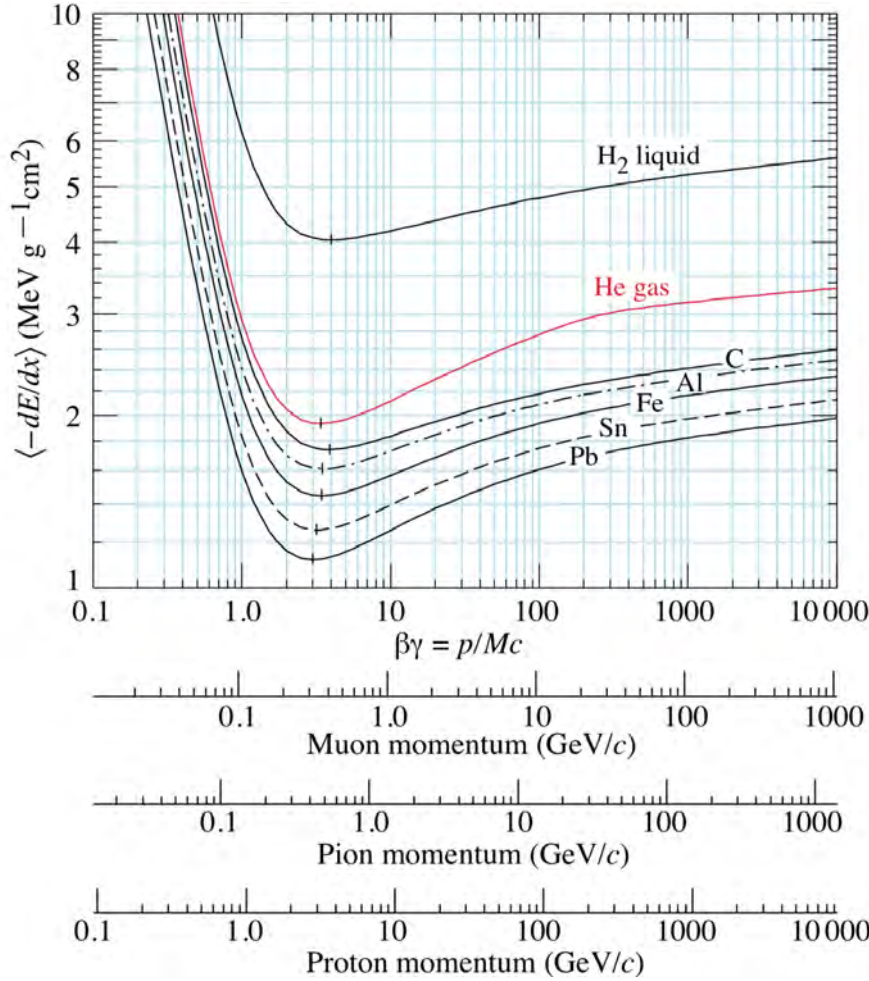


Figure 4.14: Average energy loss described by the Bethe-Bloch equation for different particles in function of its energy and the interaction medium [85].

Figure 4.14 shows that the minimum energy deposited per unit of traversed length is approximately independent of the absorption material or the incident particle. A particle with $\beta\gamma \sim 3$ is called a Minimum Ionizing Particle (MIP) and, in silicon, it deposits its energy generating about 80 electron-hole pairs per micron traversed.

4.2.2.2 Neutral particles

Neutrons will interact via the strong force with the atomic nuclei. The interaction is capable of knock out atoms from its original lattice position, possibly causing what is known as radiation damage of the detector (see Section 4.3). Photons, on the other hand, will interact mostly with the atomic electron cloud.

Albert Einstein was awarded the Nobel Prize in Physics "for his services to Theoretical Physics, and especially for his discovery of the law of the photoelectric effect" in 1921.

The main interactions of photons with matter are three: the photoelectric effect; Compton scattering; and (electron-hole) pair production. Differently from electrically charged particles, that interact along their paths with gradual energy transfer, the photoelectric and pair production interactions have the characteristic of transferring completely the photon energy in a single interaction. In the Compton scattering the photon ejects an electron from the atomic orbitals and is deviated from its original path. The scattered photon energy is proportional to the deviation angle.

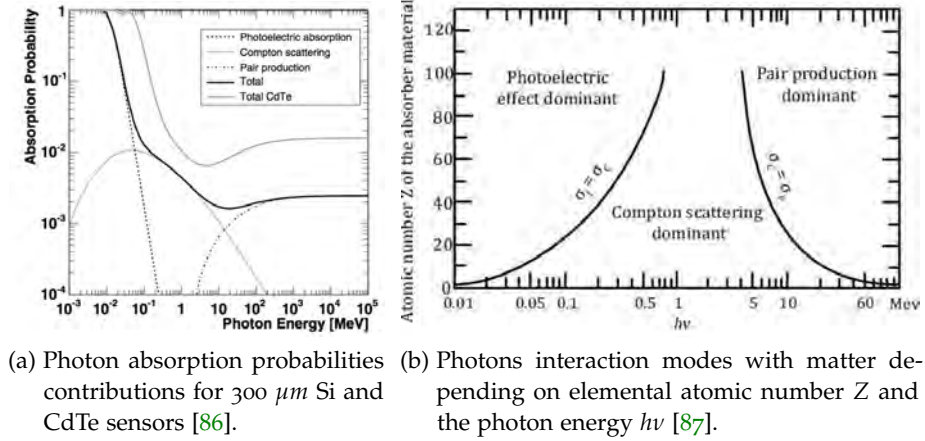


Figure 4.15: Probabilities of photon absorption.

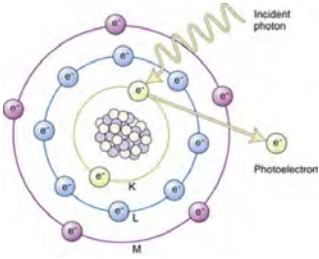
Figure 4.15a shows the probability of each interaction, as function of the incident energy, for a silicon substrate 300 μm thick. To illustrate the dependency of the mass of the material, the absorption probability is also shown for a CdTe bulk, with the same thickness. Figure 4.15b shows the photon interaction modes as function of the photon energy and of the media atomic number.

In the photoelectric effect the incident photon ejects an electron with energy $E_{\text{electron}} = E_{\text{photon}} - w$, where w is the so called, work function (the necessary energy for ionization) of the material. In silicon, w is approximately 3.6 eV, about 3 times higher than the silicon band-gap, of about 1.12 eV. This is due to the fact that the lowest level of the conduction band has a different vector moment than the highest level of the valence band, making necessary an energy higher than the band-gap, in order to maintain momentum conservation in the crystal lattice. The energy excess is used for phonon creation, that will be later dissipated over the crystal lattice as thermal energy.

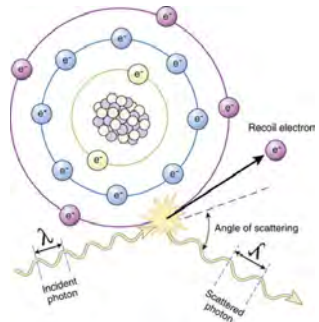
As shown in Figure 4.15b, the Compton effect becomes more relevant than the photoelectric effect as the incident energy increases. Compton scattering happens when the incident photon has a much larger energy than the electron bonding energy. This makes the electron and the photon to be scattered, with the photon final energy [89]

$$E_{\gamma}^f = \frac{E_{\gamma}^i}{1 + \frac{E_{\gamma}^i}{m_e c^2} (1 - \cos \theta)} \quad (4.13)$$

Photoelectric effect illustration [88]

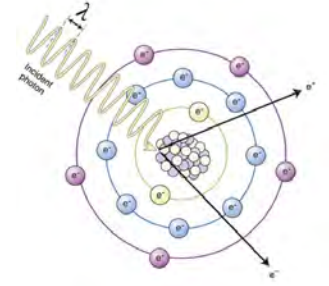


Compton scattering illustration [88]



Pair production happens when the incident photon has an energy higher than the (electron-positron) pair production energy threshold. The energy threshold is 1.02 MeV and corresponds to the combined electron and positron mass at a rest frame of reference. Therefore, if the incident photon has exactly 1.02 MeV, the electron-hole pair will be created at rest. Any "excess" energy will be translated into kinetic energy for the electron and positron. As an e^-e^+ pair produced in free space can not satisfy energy and momentum conservation, an atomic nucleus is needed to be present to receive the respective recoil momentum from the incident photon.

Pair production illustration [88]



4.2.3 Signal generation from particle interactions

As an incident radiation traverses a semiconductor sensor, energy will be released in the crystal lattice through the different mechanisms described in the previous section, and 1 electron (e) and hole (h) pair will be created for each (approximately) 3.6 eV deposited (silicon ionization energy). Due to the present electric field, extending through the sensor, the electrons and holes will drift apart each other, towards the sensor electrodes. The speed of electrons and holes is directly proportional to the electric field [77]:

$$v_{e,h} = \mu_{e,h} E = \frac{-e\tau_c}{m_{e,h}} E \quad (4.14)$$

where $\mu_{e,h}$ is the electron/hole mobility in the semiconductor, m_e and m_h are the effective electron and hole mass, respectively, and τ_c is the charge carrier mean free time, defined as the average time between collisions while moving in the crystal structure. The drift of the electrons through the sensor can be defined as a current, per unit area, as shown on Equation 4.15.

$$J_{e(h),drift} = -eq\mu_{e,h}E \quad (4.15)$$

where q is the electrons, or holes, concentration. During the drift movement, the electrons and holes are also subject to a diffusion movement, migrating from a high-concentration region towards a low-concentration region. An additional diffusion current, per unit area, can be defined as:

$$J_{e(h),diff} = -D_{e,h}\nabla_{e,h} = -\frac{kT}{e}\mu_{e,h}\nabla_{e,h} \quad (4.16)$$

where $\nabla_{e,h}$ is the electron/hole concentration gradient and $D_{e,h}$ is the so called diffusion constant, related to the charge mobilities via the Einstein relation $D_{e,h} = \mu_{e,h}kT/e$. The spread of the charge distribution can be described by a Gaussian distribution with the standard deviation defined as:

$$\sigma_{e,h} = \sqrt{6D_{e,h}t_{e,h}} \quad (4.17)$$

where $t_{e,h}$ is the lifetime for electrons and holes.

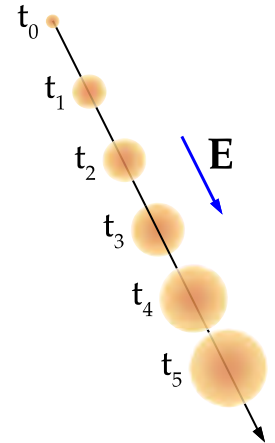
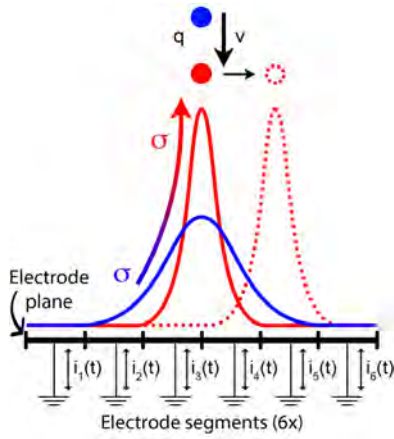
Illustration of a moving charge concentration, due to an electric field E , at different times t .

Illustration of induced current due to a moving charge cloud



Following the illustration on the left, as a charge q drifts and diffuses, following the electric field lines inside the sensor, its movement will induce a current signal at the sensor electrodes. The signal generated is induced by the local change in the induced charge density (σ) in the electrode, generated by the real charge drift. Although the total induced charge density over the electrode plane doesn't change, the local charge density on each electrode segment will depend on the real charge position. Therefore, charge will flow to change the charge density on each segment, as long as charge carriers move, originating a current signal.

In this way, every charge moving in the vicinity of the electrodes will induce a signal, with the amplitude of the signal being proportional to the proximity of the charge to the electrode. Given the opposite electric charge of electrons and holes, the induced signal will have the same polarity as the charges go towards opposite direction. The signal starts with the movement of the first charge created and ceases when the last charge reaches the sensor electrode, taking typically about 10 ns, or gets recombined with an hole or gets trapped by a lattice defect.

The instantaneous electric current induced on electrodes can be calculated with the Shockley–Ramo theorem [90]. The theorem is developed on the instantaneous change of electrostatic flux lines ending on the electrode and states that

$$i = E_w q v \quad (4.18)$$

where i is the instantaneous current on the given electrode, q is the particle charge, v is its velocity and E_w is the so called weighting field. The weighting field depends only on the electrode's topology and is calculated for a static case where the charge is not present, the given electrode is raised to unit potential and all other conductors are grounded. Therefore, according to the theorem, the induced signal will depend only on the electrodes geometry and charge carriers position and velocity.

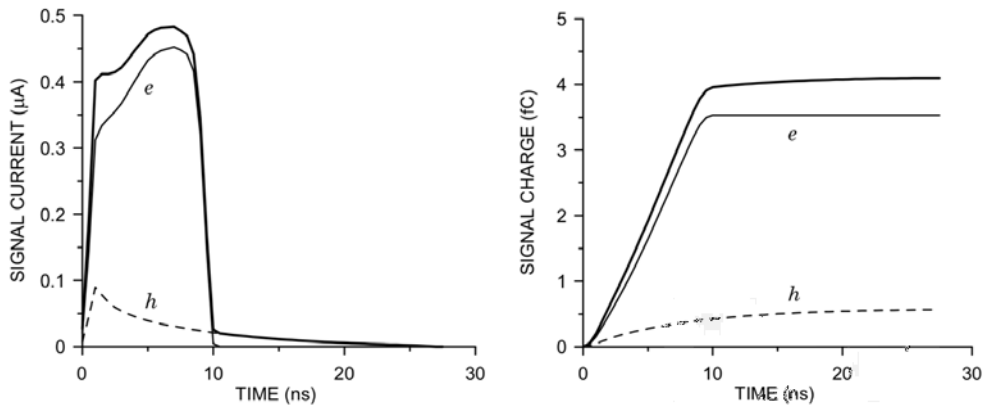


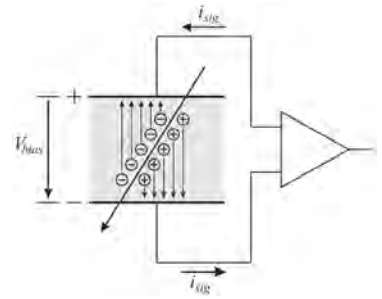
Figure 4.16: Instantaneous current (left) and integrated current (right) on a n-type electrode. The electrons (e) and holes (h) components are shown together with the total signal (in bold line) [91].

Figure 4.16 shows (on the left) the current pulse induced by the movement of the electrons and holes through the sensor bulk, and the total integrated current (on the right). The difference in the charge signal generated by the electrons and holes rises from the difference in their respective mobility. Standard drift velocities for silicon (with electric field below 10^4 V/cm) are $1500 \text{ cm}^2/\text{Vs}$ and $480 \text{ cm}^2/\text{Vs}$ for the electron and hole, respectively [77].

In addition, as the signal generated is proportional to the velocity of the charge carriers, charge carriers moving only by diffusion will add a long tail in the current signal as thermal diffusion lasts longer than drift. Therefore, the operation of the sensors is typically done with an over-depletion voltage to assure that the full sensor volume is depleted and has a strong electric field, inducing fast charge drift and, subsequently, fast current signal. This aspect of the signal is of extreme importance in experiments with high detector occupancy as slow signals will be more prone to signal pile-up.

Typically, the charge signal in a $300 \mu\text{m}$ thick silicon sensor, fully depleted, has about 24 k electrons, or about 4 fC. The sensor electrodes are coupled to preamplifier inputs in order to start the subsequent signal read-out and processing, described in the following section.

Illustration of the charge signal, on a planar diode, connected to amplifier [91]



4.2.4 Read-out of sensor information

Once the particle signal is generated in the sensor, it needs to be processed, stored and sent to the "outside world" for further analysis. In semiconductors, the signal is a charge current. The time integral of the charge current yields the total charge of the signal, which is proportional to the energy deposited by the incident particle. In order to record the interaction event, while exploring the signal characteristics, the read-out system must be composed by multiple steps, such as signal acquisition, pulse shaping, digitization and readout, as illustrated in Figure 4.17.

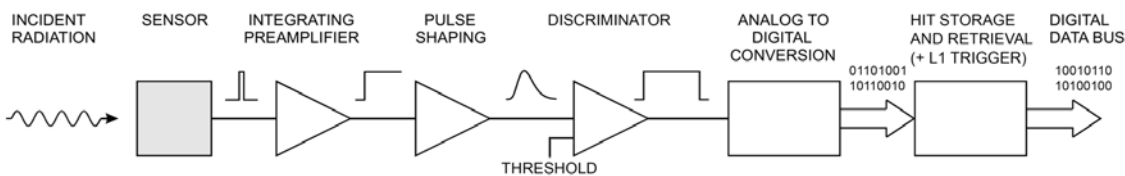


Figure 4.17: Basic detector functions: Radiation signal generation in the sensor; signal integration in a preamplifier; signal pulse shaping; and digitization for subsequent storage and analysis [91].

The preamplifier, receiving the sensor signal, is configured as an integrator, which converts the narrow current pulse from the sensor into a step pulse with a long decay time. In the process, noise can be also amplified and, as noise is proportional to the capacitance, to keep the input capacitances small is important.

The preamplifier stage is followed by a further signal amplification and shaping, helping to improve the SNR and further process the signal. As the electronic noise has a different frequency spectrum w.r.t the signal, it is possible to improve the SNR by applying a series of filters. As changing the frequency spectrum of the signal also changes its time response, improving the signal-to-noise ratio commonly implies reducing the bandwidth, increasing the duration of the pulse. Figure 4.18 illustrates the shaping steps.

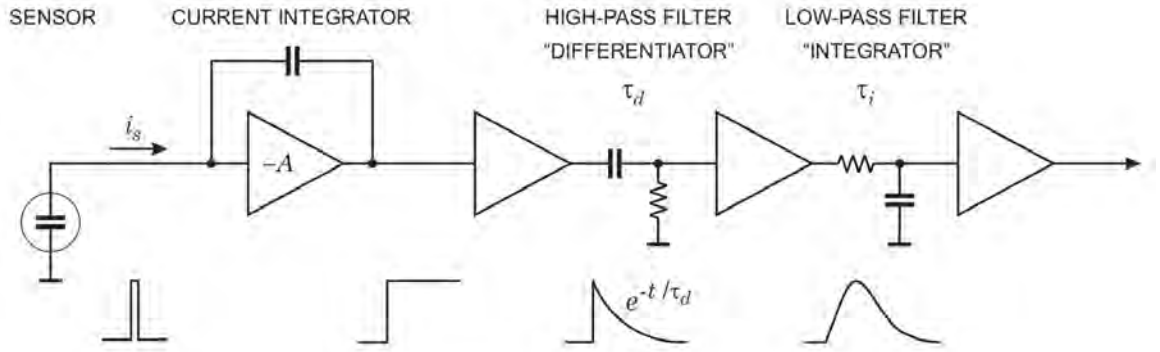


Figure 4.18: Components of a pulse shaping system. The signal current from the sensor is integrated to form a step impulse with a long decay. A subsequent high-pass filter ("differentiator") limits the pulse width and the low-pass filter ("integrator") increases the rise-time to form a pulse with a smooth cusp [91].

A CR high-pass filter introduces the desired decay time and, sequentially, a RC low-pass filter limits the bandwidth and sets the rise time. With the high particle occupancy in collider detectors, large pulse widths can lead to pile-up of successive pulses, what will lead to wrong pulse amplitude or timing measurements.

The signal shapers are designed in order to shape the pulses in the same way, independent of the pulse signal magnitude. As the total integrated charge is proportional to the pulse signal, the amplitude of the shaped pulse will be proportional to the deposited energy in the sensor. With a controlled feedback system in the shaper filters, it is possible to have the amplitude proportional to the width of the pulse, making possible to perform energy measurements by measuring the time length of the pulse above a threshold, so called Time-over-Threshold (ToT) measurement. The pulse ToT is illustrated in Figure 4.19.

Once the particle signal is shaped it is needed to translate it to the digital domain in order to be processed and stored. This is done by digitizing the signal using Analogue-to-Digital Converters (ADCs).

The first stage amplification capacitor integrates the charge until its voltage is equal to the amplitude of the input pulse from the sensor. When this condition is reached the capacitor is discharged linearly. After, the shaping of the pulse goes through a comparator and, while above a predefined threshold, it initiates a gate pulse. As already men-

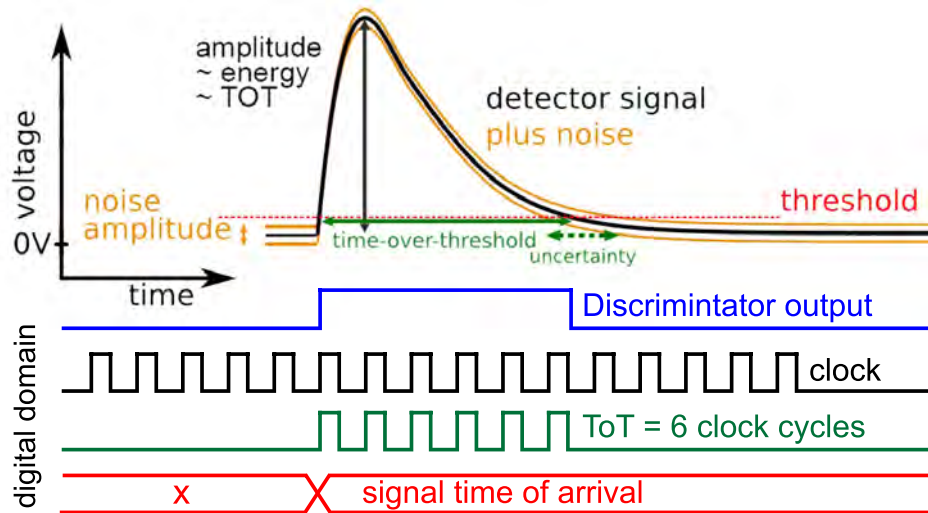


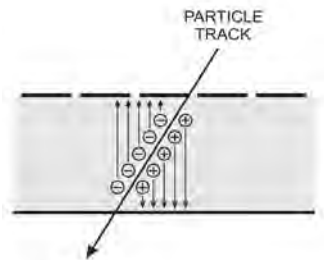
Figure 4.19: Illustration of the pulse digitization. Adapted from [92].

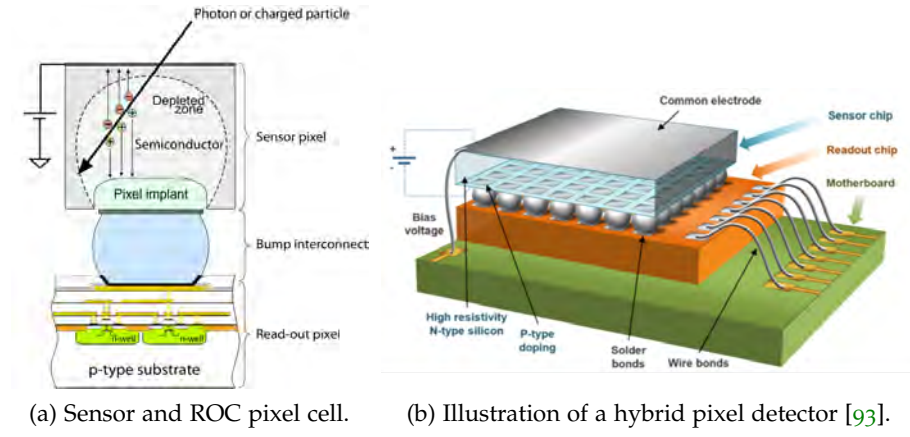
tioned, the duration of the gate pulse (ToT) is directly proportional to the amplitude of the input pulse from the sensor. This gate pulse operates a linear gate that receives pulses from a high-frequency oscillator clock (in the order of hundreds of MHz). While the gate is open, a discrete number of clock pulses passes through the linear gate and are counted by an address register. Further, a digital counter records how many clock cycles passed the gate digitizing the ToT information, and also allowing to infer other possible informations such as the signal Time-of-Arrival (ToA).

The first semiconductor detectors in the 60-70s, such as surface barrier detectors, used discrete components on each step of the data read-out. This has the advantage of the detector system being modular and adaptable. In modern experiments, highly granular and fast detectors are required, together with large volume coverage and minimum additional mass to the detector. This requires sensors with high segmentation and miniaturized integrated read-out components, commonly developed as a CMOS Application Specific Integrated Circuit (ASIC), giving origin to the Read-Out Chips (ROCs). A disadvantage of using ROCs instead of modular discrete elements is that the design of the ROC must comply with many, sometimes conflicting, requirements. As, generally, processing speed and resolution are opposing parameters, as are speed and power, many trade-offs must be taken into account.

In hybrid pixel detectors, as illustrated in Figure 4.20, the sensor is segmented in an array of pixels, each with its own collection implant and electrode. The ROC must be segmented in the same way so each pixel on the sensor can be connected, commonly via solder bump-bonds, to a pixel cell in the read-out ASIC. Each pixel cell operates independent of the other pixels on the matrix, acting as a single detector channel.

Sensor electrode segmentation [91].





(a) Sensor and ROC pixel cell. (b) Illustration of a hybrid pixel detector [93].

Figure 4.20: Hybrid pixel detector cell (a) and assembly (b) illustrations.

Figure 4.21 shows the Timepix3 [94] read-out chip bump-bonded to a planar sensor. The hybrid detector is segmented in a matrix of 256×256 pixels, each with $55 \times 55 \mu m^2$, covering a total area of about $14 \times 14 mm^2$. The ROC is capable to record the position of the particle interaction, while measuring the signal's ToA with 1.56 ns precision, simultaneously with the signal's ToT.



Figure 4.21: Picture of a silicon planar sensor bump-bonded to the Timepix3 ROC below, wire-bonded to the chip-carrier board [95].

Following the digitization of the signal, it is needed to store and send it to the outside world, where the information of multiple detectors will be combined, reconstructing the underlying event. As each detector module is tailored to meet the specifications of each experiment, different detectors will have different architectures to store and read-out the processed signal data. Systems can store the hit information in a local buffer until a trigger command is issued, retrieving the information from the ROC, or send the hit information outside as signals are processed on chip, in a trigger-less, or data-driven, mode.

Independent of the read-out scheme used, or of the sensor design, all detectors will need to be able to survive long periods of exposure to radiation, what can ultimately degrade the detector performance. Therefore, the detector design must take radiation damage into consideration in order to prolong the life span of the detectors.

4.3 RADIATION DAMAGE

Semiconductor detectors can have their crystal lattice damaged by incident radiation, inducing defects in the detector performance. Defects in the lattice that can be electrically active can be categorized into surface and bulk effects. Surface effects regard defects caused by the accumulation of electric charges in the dielectric layers, being more relevant for the electronics of the signal processing in the ROC. Bulk effects influence the charge generation and propagation in the sensor bulk, altering the charge signal generated and read-out by the ROC.

The radiation damage depends on the radiation fluence, defined as the number of particles dN per da area unit.

4.3.1 NIEL normalization and hardness factor

For non-ionizing radiation, the damage is proportional to the energy loss in the material displacing atoms from its original position in the crystal lattice. The NIEL (Non Ionising Energy Loss) hypothesis defines a standard fluence, equivalent to $1 \text{ MeV neutron/cm}^2$, with which the damage caused by other particles can be scaled [96]. In this way, it is possible to compare the damage from different radiation fluences, with the damage caused by $1 \text{ MeV } n_{eq}/\text{cm}^2$ used as "unity".

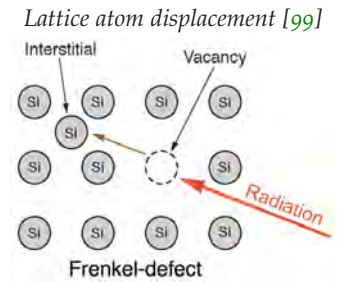
An effective $1 \text{ MeV } n_{eq}/\text{cm}^2$ fluence, ϕ_{eq} , can be defined from the actual radiation fluence ϕ_{phys} and by the hardness factor, κ , dependent of the particle type and energy:

$$\phi_{eq} = \kappa \phi = \kappa \int \phi(E) dE; \quad [\phi_{eq}] = n_{1\text{MeV}}/\text{cm}^2 \quad (4.19)$$

The proportionality constant, κ , can be calculated theoretically [97] or by experimental measurements, such as of the temperature normalized leakage current [98]. The value for a 24 GeV proton beam, such as the CERN PS beam, is $\kappa = 0.62$. In contrast, the pion beam at the Paul Scherrer Institute cyclotron, with 193 MeV, has $\kappa = 1.14$.

4.3.2 Bulk damage

The bulk damage is created when the radiation interacts with the nucleus of the atoms in the sensor crystal lattice, knocking out lattice atoms from their original position, and it is primarily produced by neutrons, protons and pions. A minimum recoil energy of approximately 25 eV is needed to displace a lattice atom [100]. The maximum energy transferred during the nuclear interaction depends on the mass of the incident particle. Electrons need to be accelerated to 260 keV in order to knock out an silicon atom, while the heavier protons and neutrons need approximately 190 eV.



This displacement of atoms generates defects in the lattice, adding new energy levels between the valence and conduction bands. Therefore, these defects will act as generation-recombination centers, depending on the position of the new energy levels in the band gap, modifying the effective doping and charge concentration.

4.3.2.1 Macroscopic observables

With the addition of new levels in the silicon lattice band gap, the bulk electrical properties will be altered. Main macroscopic observables of the radiation damage in particle detectors are the increase of the leakage current; the increase of the voltage required for full depletion; and the reduced total charge collected.

Leakage current Energy levels added in the middle of the band gap acts mainly as generation and recombination centers for charge carriers, increasing the conductivity of the bulk and, consequently, increasing the leakage current. The increase of the current can be parametrized as:

$$I_{vol} = I_{vol,\phi=0} + \alpha \cdot \phi \quad (4.20)$$

where I_{vol} is the leakage current per volume unit, ϕ is the radiation fluency and α is a universal constant parametrizing the current related damage. For silicon sensors at 20°C α is about $8 \cdot 10^{-14} \text{ A/cm}$ [96]. The validity of Equation 4.3.2.1 has been demonstrated for sensors with different resistivities and up to high fluences and is illustrated in Figure 4.22.

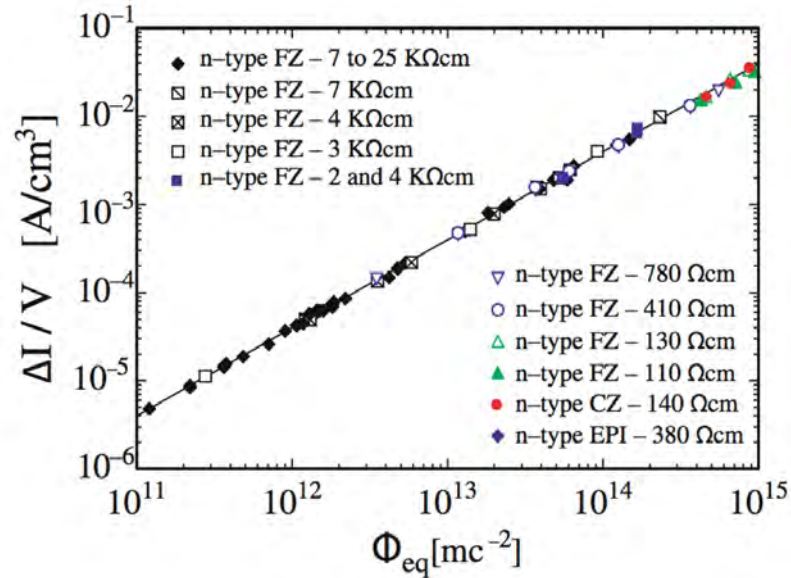


Figure 4.22: Leakage current versus radiation fluency [96].

Charge trapping Traps are defects located in the depletion region, where the particle interaction signal will be generated by drift. The traps will be unoccupied due to the lack of free charge carriers,

being able to hold the electrons or holes created by the particle interactions, limiting the charges drift towards the electrodes, consequently reducing the induced current signal height. The degradation of the charge collection efficiency can then be defined as:

$$Q_{e,h}(t) = Q_{0,e,h} \exp\left(-\frac{1}{\tau_{eff,e,h}} \cdot t\right), \text{ where } \frac{1}{\tau_{eff,e,h}} \propto N_{defects} \quad (4.21)$$

$Q_{e,h}(t)$ represents the amount of charge drifting through the sensor after a certain time t ($Q_{0,e,h}$ represents the total amount of charge initially created). Having in mind that τ_{eff} represents the charge carrier mean free time, typical values for fluences of 10^{15} and $10^{16} \text{ n}_{eq}/\text{cm}^2$ are 2 and 0.2 ns, respectively [76]. At these fluences levels, trapping becomes the limiting factor of silicon usage as a particle detector. To mitigate this problem, higher voltages are desirable in order to create a stronger electric field that will drift faster the charges, decreasing the necessary time t to collect all charges, avoiding them to get trapped and increasing the signal induced.

Depletion voltage If the number of electrically active defects is in the same order as the original doping concentration, a new effective doping, N_{eff} , must be defined. The effective doping is defined by $N_{eff} = N_D - N_A$, the difference of all donor-like states and all acceptor-like states. As the voltage required for the full depletion of the sensor is correlated to its doping concentration, Equation 4.8, V_{dep} will change according to the fluency dose.

Figure 4.23 shows the dependency of the full depletion voltage (on the figure indicated as U_{dep}) with the fluency ϕ_{eq} , measured for an originally n-type 300 μm silicon sensor with high resistivity ($> 1\text{k}\Omega\text{cm}$). As the effective doping concentration can be calculated from the measured U_{dep} , N_{eff} is also shown on the right vertical axis in Figure 4.23.

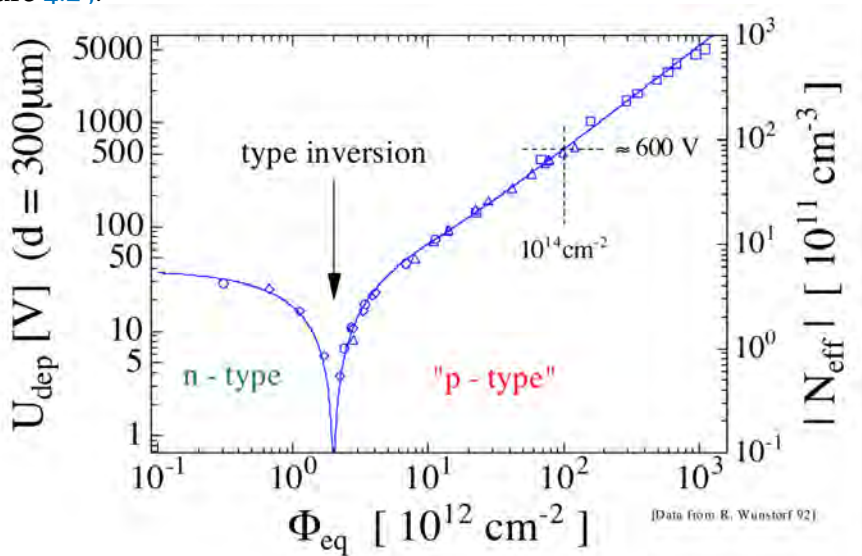


Figure 4.23: Effective doping concentration (and subsequently the voltage for full depletion) as function of the irradiation fluency [96].

From the results shown in Figure 4.23 it is possible to see that the defects introduced in the substrate bulk act like an acceptor, or p-type doping, making an n-type bulk to be gradually transformed into an effectively doped p-type bulk, a process known as *space-charge sign inversion*. Phenomenological models, such as the Hamburg Model [96], were developed using results from high resistivity silicon sensors. The Hamburg model successfully helped the construction of the planar silicon sensors, to be used in the LHC experiments, providing accurate predictions regarding their properties after irradiation.

In the last years, with the advance of new silicon sensor technologies, such as Low-Gain Avalanche Diodes and HV-CMOS (to be described in Chapter 5), new radiation damage phenomena have started to be seen, requiring a revision on the Hamburg model [101][102]. Measurements on new devices with low resistivity p-type substrate have shown a decrease of U_{dep} for low fluency levels, which is not expected according the Hamburg model. Figure 4.24 shows the effective doping concentration, calculated by measuring U_{dep} , as function of the fluency for three devices with different initial resistivities.

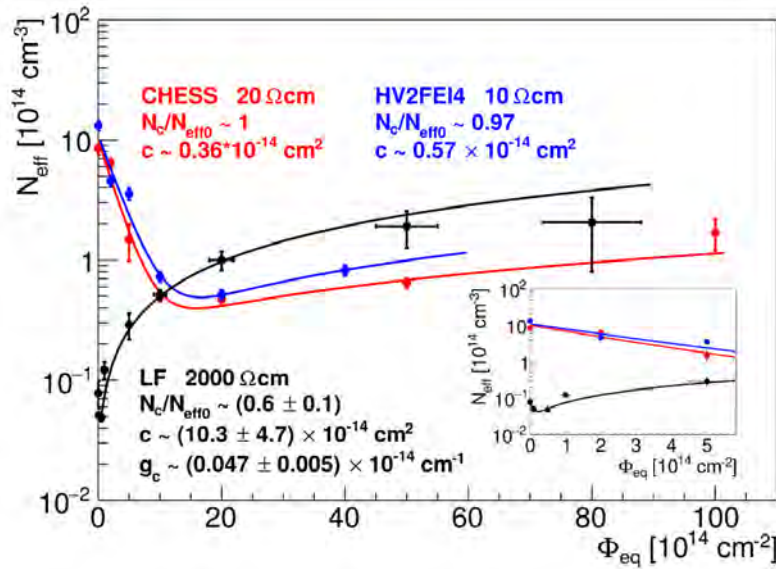


Figure 4.24: Effective doping concentration *vs* radiation fluency for three devices with different initial resistivity [101].

As it is possible to see in Figure 4.24, up to $\phi_{eq} \sim 1.5 \cdot 10^{15} \text{cm}^{-2}$, the low resistivity devices have their effective doping concentration decreasing, while for the high resistivity device it increases as a function of ϕ_{eq} . Analyzing the high resistivity device at lower fluences ($< 0.5 \cdot 10^{14}$) the same behavior of decreasing N_{eff} as the fluency increases was also observed, although in a smaller scale, as shown on the insert plot in Figure 4.24.

The lower values of N_{eff} lead to an increase of the depleted volume of the sensors, for a given voltage, helping to increase the signal generation with rising fluency. With higher charge signals, this effect can help to increase the detection efficiency of detectors up to certain levels of irradiation.

A possible explanation for this effect is that the defects in the silicon lattice can interact with the initial boron (acceptor) doping on a p-type substrate, changing the properties of the initial acceptor levels making them to not contribute any more to the space charge concentration. Although, at the same time, other defects in the lattice can generate new acceptor levels which will contribute to the space charge. This competing mechanism can effectively decrease N_{eff} as function of the fluency if the number of removed acceptors is larger than the number of introduced defects. Effective initial acceptor removal has been observed in different detectors with high boron concentration [103][104][105].

This effect is known as “acceptor removal” and, depending on the initial acceptor concentration (linked to the substrate resistivity), the complete acceptor removal can take place at different fluency levels. The mechanism behind the dependence of acceptor removal rate on initial resistivity is yet to be understood. Once all acceptors are removed, the increase of N_{eff} with the fluency is similar in all materials regardless of initial bulk resistivity or type.

4.3.2.2 Defects annealing

The defects presented in the bulk are free to move around the lattice and their diffusion is highly temperature dependent. Defects can interact with each other, giving place to defect clusters or vanishing completely. Therefore, given some time and temperature, some of the induced defects can be repaired, and the whole defect dynamic process is called *annealing*.

The complex evolution of the defects and their effect on the doping concentration can be parametrised, as shown on Equation 4.22, containing three components contributing for the effective doping concentration [77]: a term representing the (constant) damage that cannot be repaired, called stable damage N_C ; a short term annealing N_A ; and a long term annealing N_Y .

$$\Delta N_{eff}(\phi_{eq}, t, T) = N_C(\phi_{eq}) + N_A(\phi_{eq}, t, T) + N_Y(\phi_{eq}, t, T) \quad (4.22)$$

ϕ_{eq} stands for the 1 MeV neutron equivalent fluency, t represents the time elapsed and T the temperature. N_C , representing the stable damage, is independent of the annealing time or temperature. The short-term annealing N_A helps to increase the effective doping concentration, making the annealing to be beneficial on its early stages, reducing the damage effects. The last term, N_Y is the term used to describe the increase of the full depletion voltage after some weeks at room temperature, as more acceptors are created making N_{eff} decrease, being known as reverse annealing.

The radiation damages on the detectors and some of their effects, e.g. depletion voltage evolution, can be controlled with temperatures below 0°C. Hence, the thermal history of irradiated detectors must be recorded in order to avoid the reverse annealing stage. Nevertheless,

due to the different time scales between the beneficial and reverse annealing, short periods (e.g. during maintenance) where the detectors is heated up can be used to enhance the beneficial annealing.

4.3.3 Surface damage

Surface damage regards defects taking place in the interface between the sensor bulk and the dielectric layers of the device, and is primarily produced by photons and charged particles. As the structure of silicon oxide is highly irregular, atoms displacements due to irradiation do not lead to macroscopic changes in the detector operation.

Nevertheless, particles can still be create e-h pairs by ionization in the oxide layers. Due to the non-uniform crystal lattice the charge carriers have a much lower mobility, w.r.t. silicon, being more susceptible to be trapped in these layers. As the mobility of electrons is several orders of magnitude higher in the oxide than that of holes ($\mu_{e, SiO_2} \approx 20 \frac{cm^2}{Vs}$ vs $\mu_{h, SiO_2} \approx 2 \cdot 10^{-5} \frac{cm^2}{Vs}$), the electrons will drift towards the metal electrodes leaving only the holes to get trapped in the oxide layers.

Due to the low mobility of defects in the oxide layers, the charge accumulation may be not fully reversible, causing steady changes of the interface properties. This can be observable in the detector operation as an increase of the digital noise, or as an increase in the power consumption, needed to compensate the change in the voltage threshold of the transistors.

As CMOS transistors are constructed with a combination of metal, oxide and semiconductor layers, the charge built-up in the oxide layer will shift the transistor threshold voltage, the potential required to open or close the transistor gate. In addition, the charge accumulation in the oxide will attract parasitic charges to the vicinity of the transistor channels, possibly decreasing the signal-to-noise ratio or even shorting electrically the transistor. This type of effect is dependent on the Total Ionizing Dose (TID) on the detector, which is a cumulative effect of the total deposited energy measured in Gray (where 1 Gy = 1 J/kg). A commonly used unit for TID measurement is *rad* (Radiation Absorbed Dose) and 1 Gy = 100 rad. The detectors at HL-LHC needs to stand a high level of TID. The ATLAS ITk outer layer pixel detectors will have to sustain about 80 MRad.

4.3.4 Single event effects

Radiation damage can also induce effects other than a degradation in the performances of a detector due to NIEL or TID. Transient effects can occur if a high energy ionizing particle traverses a depleted gate region of a given transistor, which can cause the value stored in the transistor to be “flipped”.

These transient effects, known as *single event effects* (SEE), can have a variety of outcomes on the circuit and can be classified as: a Single Event Transient (SET) and a Single Event Upset (SEU).

A SET happens when a transient signal is created on a signal path. The consequence of this type of event depends on the signal function. For example, if a SET happens on a clock line, synchronization between different circuit elements can be lost. A SEU is caused when a stored bit has its value changed, and it can lead to wrong information stored in or transmitted by the chip. These errors are random, non-recurring and not permanent, but it can have a very large impact on the operation of digital circuits, as it can lead to invalid data or complete system failure due to upsets in the state bits of state machines.

SEE robustness is strongly dependent on the technology used. Technologies with smaller feature sizes, and thus smaller circuit components (as memory cells), will have a smaller cross-section for a SEE as it is less probably for an incident radiation to hit a sensitive node with smaller area. On the other hand, smaller nodes will require less energy/charge to cause a bit upset. A technique used to correct for this effect is the redundancy of the memory cells combined with a majority vote logic.

For the ATLAS ITk upgrade, silicon detectors in the fifth pixel layer must comply with a SEU rate on a full chip < 0.01 per hour per chip (and on a single pixel < 100 per hour per chip) for a particle flux of 0.3 GHz/cm^2 .

4.3.5 *Radiation damage summary*

As seen in the previous sections, the radiation defects generated on the sensor will have impact on the macroscopic properties of the detector, such as the increase of the leakage current and the reduction on the total charge collected.

Due to the additional energy levels (in the band gap) generated by the damage in the sensor lattice, the leakage current will increase and it can become a non negligible source of noise, being capable of clogging the pixel matrix read-out if the leakage current gets drained by the pixel electronics, creating noisy pixels that are always generating hits for the read-out. In addition, due to the change in the effective doping, a higher voltage will be required to fully deplete the sensor.

The increase of the operational voltages and of the leakage current will subsequently increase in power consumption and induce significant heat load on the detector. As the leakage current depends exponentially on the temperature, the temperature of the sensor must be controlled in order to avoid the detector thermal runaway. Therefore, in order to be able to sustain higher voltages, and also to prevent the degrading reverse annealing, the detectors are usually operated cooled down to temperatures $< 10^\circ\text{C}$.

HV-CMOS PIXEL DETECTORS

Silicon pixel detectors are a common choice for the vertex and tracker detector in collider experiments. Each experiment collaboration investigates specific technologies in order to design the best detector possible, and a few technologies were already mentioned in Section 4.2. As the work done in this thesis is on the investigation of the use of the HV-CMOS technology, this technology will be explained in greater detail.

5.1 THE HIGH-VOLTAGE CMOS TECHNOLOGY

CMOS technology uses NPN and PNP MOSFET (or NMOS and PMOS) type transistors¹ in order to generate logical gates and implement electronic circuits, to be used in the signal processing for example. A cross-section of a CMOS device, implemented on a p-type substrate, is shown in Figure 5.1, and a cross-section of a real device is shown on the right. In order to have an PNP transistor, on a p-type substrate, it is needed to create an n-well to isolate the p implants of the transistor from the p-doped substrate.

SEM image of a CMOS device with 6 metal layers [106].

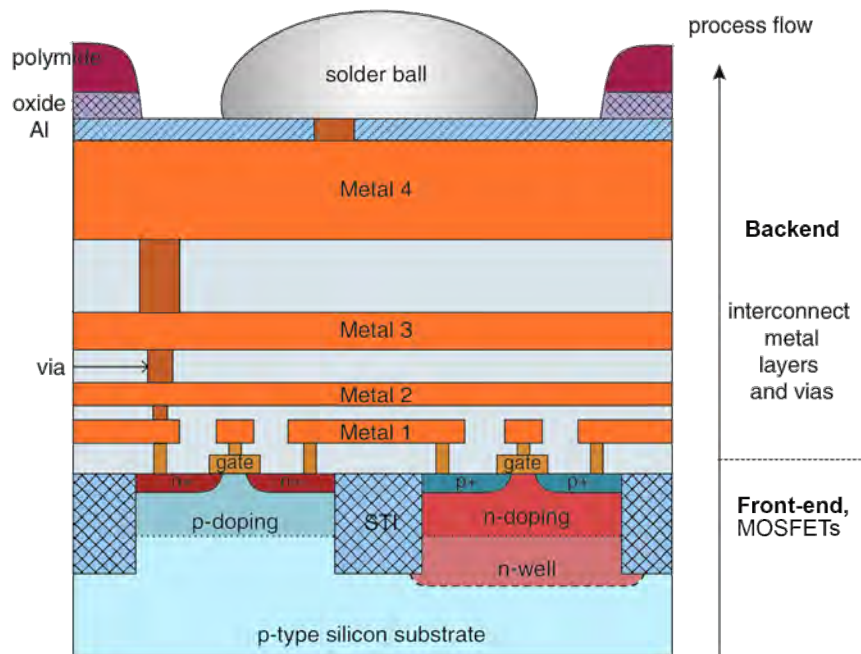
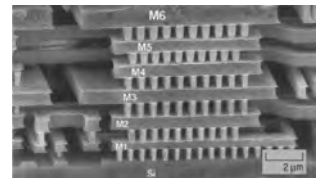
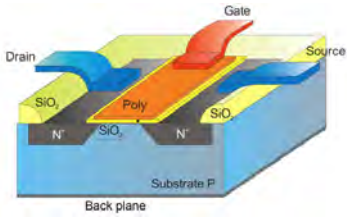


Figure 5.1: CMOS device cross section illustration. Adapted from [107].

¹ MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) is a transistor type, and it can be either a NPN or PNP transistor. A NPN transistor, for example, has a N-type silicon connected to the transistor source and drain, implemented on a P-type bulk. PMOS circuits are composed by only PNP MOSFET transistors, while CMOS are composed by PMOS and NMOS transistors, separated by a Shallow Trench Isolator (STI) oxide region.

NPN MOS transistor [108]



Once the transistor N and P type doping is implanted in the silicon surface, layers of metals and dielectric materials are deposited on the silicon surface, creating metal lines that will connect the transistors together, distributing power and routing the signal across the device. In addition, the metal lines are also used to create circuit components like capacitors, inductors and resistors.

The voltage applied on the transistor gate, responsible for controlling the current channel between the transistor terminals, is measured relative to the substrate potential. Therefore, there is a maximum voltage that can be applied on the substrate without compromising the operation of the transistors, known as body effect. In conventional CMOS technology the maximum voltage to be applied on the chip substrate is in the order of 5V.

The High-Voltage (HV) CMOS technology introduces the deep N-wells: deep n-type doping that extends further into the substrate bulk. These deep implants are set to a fixed voltage, in the order of 1.75 V, while the substrate can reach above 100 V. These large implants can host PMOS and NMOS transistors, shielding them from the HV applied on the substrate. Figure 5.2 illustrates a cross section of a HV-CMOS device. The capability of applying HV to the chip substrate, where CMOS transistors are implanted, is of big interest for pixel detector designers as it allows to combine silicon sensor features with signal processing capabilities from CMOS circuits.

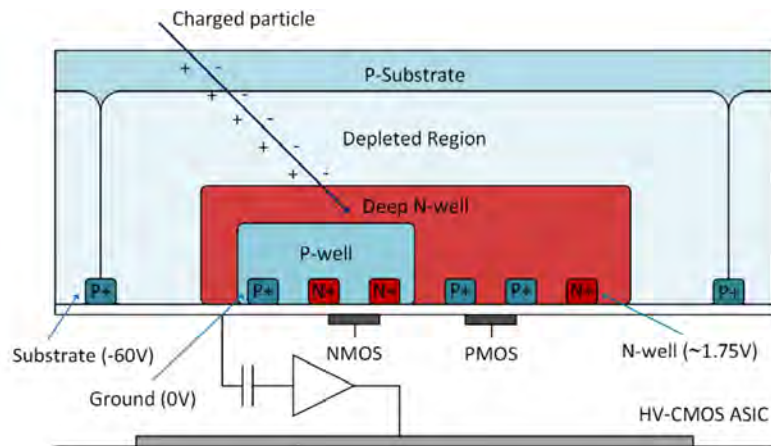


Figure 5.2: HV-CMOS cross section illustration.

While shielding the CMOS transistors from the HV in the substrate bulk, the deep N-well can also be connected into the input of a pulse shaping and read-out chain, composed by the transistors contained inside the deep N-well itself. In this way, the deep N-well will act also as the charge collection implant, like in the regular planar silicon pixel sensors. This brings advantages such as the possibility of having the charge signal generated in the sensor already processed in the same device, avoiding possible problems that can arise from the sensor-to-ROC interconnection. With the possibility of having electronic cir-

circuits integrated on the sensor, HV-CMOS devices can be used as fully monolithic detectors or as sensors for hybrid detectors.

Hybrid pixel detectors commonly consists of a planar silicon sensor, where only simple collection implants are present in the device, coupled (via bump-bonds) to a read-out ASIC. Bump-bonds are micro-solder balls (about $20\ \mu\text{m}$ diameter) composing a high-density interconnection. This type of coupling requires device post-processing and increases the production time and cost of the detector, representing about half of production cost. In addition, current bump-bonding technology imposes a minimum size for the pixel pitch as there is a technical limitation for the minimum size of the bumps.

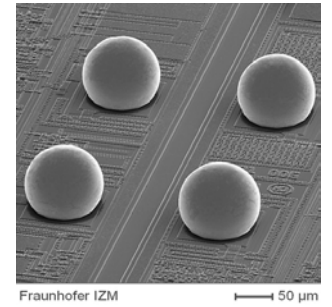
HV-CMOS allows the construction of hybrid detectors where the signal processing can start already in the sensor, before the signal transmission to the read-out electronics. To have part of the signal processing happening in the sensor allows to allocate a larger area for other functionalities in the read-out pixel. This is an advantage as analogue circuits occupy a large area in CMOS devices, making a pixel area be composed of about 50% of analogue circuit (such as amplifiers and shapers) and 50% digital circuit (such as ADCs and buffering). HV-CMOS hybrid pixel detectors allows detector architectures where the sensor device is responsible for the signal acquisition and shaping, while the ROC pixel can be 100% digital, containing the high resolution and fast ADCs and buffers.

Another advantage of the HV-CMOS technology is that, as it allows the signal amplification, the sensor can be capacitively (AC) coupled to the ROC, avoiding the expensive, and design restricting, bump-bonds [110]. The signal output from the sensor can be amplified sufficiently to be strong enough to be transferred via a capacitive injection to the input pad of the ROC.

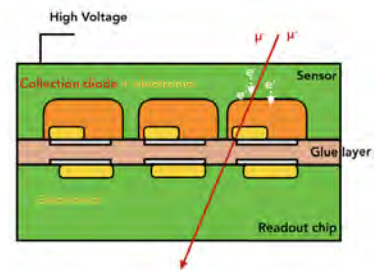
The capability of an AC coupling allows to perform the coupling, or the hybridization, of the detector module by depositing a layer of a dielectric glue onto the sensor and ROC surfaces, aligning the pixel pads and applying a calibrated force to bond the devices together [111]. This process is called flip-chip and will be described in the following chapter. AC coupled detectors are called Capacitively Coupled Pixel Detectors (CCPDs). The CCPD flip-chip doesn't require device post-processing, representing a reduction ($\sim 50\%$) on the detector production cost, when comparing with bump-bonded hybrid detectors. In addition, it allows to have smaller pixel pitches, or even to create detectors with sub-pixel encoding by connecting, capacitively, more than one pixel from the sensor to the read-out chip. As the method of charge transfer is done via a capacitive injection, the effect of neighbor pixel cross-talk, during the charge transfer through the glue layer will be investigated in a later chapter.

In addition, as a HV-CMOS device can have a charge sensitive bulk implemented together with analog and digital circuits, the HV-CMOS technology also allows fully monolithic detector architectures, so-called HV-MAPS.

Bump-bonds deposited on chip [109]



CCPD illustration



5.2 HV-CMOS USE CASES

ATLAS As already described in Section 3.2.5.2, the ATLAS ITk upgrade is designed as a large area all-silicon tracking detector. The detector design is optimized for construction time and cost. The upgrade aims to implement the mature and well established hybrid pixel detectors with planar sensors in the innermost layers and a new monolithic technology in the 4th layer, located at a radius of 271 mm and with a half-length of 780 mm, covering a surface of 2.7 m^2 (with about 7000 chips). Considering the large area to be covered, lower production cost and time, the most attractive solution for layer 4 is the use of monolithic CMOS sensors.

The new monolithic detector must have the same, or better, performance than the current hybrid pixel detector, a planar silicon sensor bump-bonded to the FE-I4 ROC. This means that the new detector must sustain $1.5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ NIEL and 80 MRad TID, delivering a detection efficiency $> 99\%$ before irradiation, and $> 97\%$ at the end of life of the detector layer with accumulated 4000 fb^{-1} .

CLIC The future vertex detector for CLIC covers a surface area of about 0.84 m^2 . Its timing and spatial resolution requirement of 5 ns and $3 \text{ }\mu\text{m}$, respectively, is expected to be fulfilled with hybrid detectors, with $50 \text{ }\mu\text{m}$ thick sensor and ROC, with $25 \text{ }\mu\text{m}$ pixel pitch. As such small bump-bonding pitch is still to be achieved with good yield, HV-CMOS CCPDs modules are being investigated as an alternative to bump-bonded planar sensors for the CLIC vertex detector.

5.2.1 Other investigated technologies

In parallel to the research on HV-CMOS CCPDs and monolithic detectors, other interesting and promising technologies are also under investigation. Each technology has its up and down points and the different detectors will have their main features described next.

5.2.1.1 Small fill factor

From Equation 4.8 it is known that the depletion zone thickness is proportional to $\sqrt{V\rho}$. Therefore, instead of depleting the sensor by reverse polarization of the PN junction, the CMOS technology [112] takes advantage of a substrate with a high resistivity in order to deplete the sensor. An illustration of the CMOS technology is shown in Figure 5.3.

An advantage of the CMOS detectors is that the collection implant can be much smaller when compared with HV-CMOS technology, making the collection diode capacitance smaller, coping with smaller noise at the amplifier input and lower power consumption.

Figure 5.3a shows the depletion zone grows from the collection implant towards the sensor bulk. TCAD simulations and test-beam

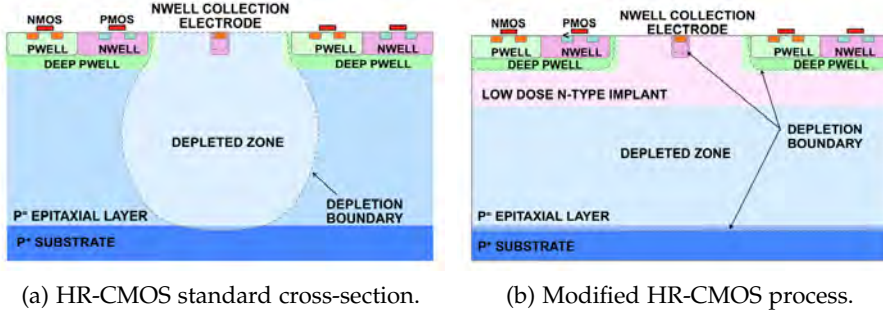


Figure 5.3: HR-CMOS device cross-section illustration [113].

results have shown that the depletion region was confined in the region between pixel implants, which can lead to detection inefficiency. Therefore, a modification for the HR-CMOS process was proposed, including a new low-concentration n-type layer implanted (Figure 5.3b) that helps to extend and homogenize the depletion region over the sensor volume [113].

A drawback of the technology is the lack of the HV in the sensor bulk. Without the HV generating a strong electric field in the sensor the signal generated in the pixel electrode will be mainly from the diffusion of the charges through the bulk, instead of their fast drift. This compromise makes the detector signal slow and in environments with high detector occupancy this might make the detector pile-up signal higher than what the read-out logic can handle. In addition, the small collection implant with charge collection via diffusion is more prone to degradation due to radiation damage as the charges are more prone to trapping, inducing a smaller charge signal.

5.2.1.2 Silicon-on-Insulator

Another technology under investigation is the Silicon-on-Insulator (SOI) CMOS [115]. Illustrated in Figure 6.1, the SOI process implements a 200 nm insulator layer (buried oxide, or BOX) between a thick high-resistivity substrate and a thin low-resistivity epitaxial silicon layer. The BOX layer acts as a shield for the low-resistivity silicon layer, containing the read-out CMOS transistors, blocking the HV applied in the high-resistivity substrate back-gate, fully depleting its volume. Such a structure provides the possibility to fabricate a monolithic pixel-detector.

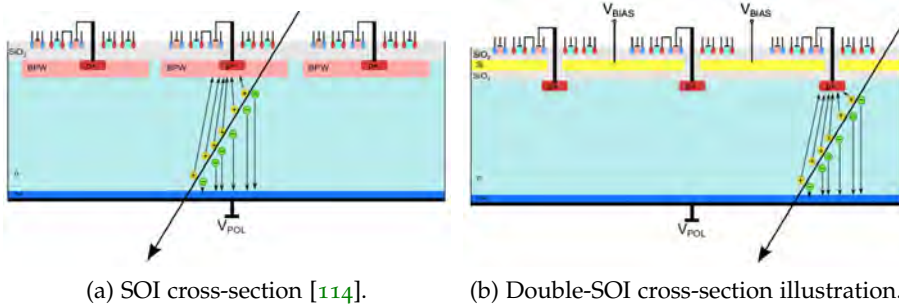


Figure 5.4: (Double-)Silicon-on-Insulator device cross-section illustration.

As it was already discussed in the previous Section 4.3, charge carriers have much smaller mobility in oxide materials, getting trapped inside it indefinitely. Due to the proximity to the epitaxial layer, trapped charge in the BOX layer will prejudice the read-out electronic circuits, inducing a threshold shift in the transistors. In order to extend the radiation-hardness of the technology, an additional BOX layer can be included, with a silicon layer in between both BOX layers. The mid-silicon layer is designed in order to compensate the electric field generated by the holes trapped in the BOX layers. Figure 6.1b shows the SOI structure with double BOX layers, or double-SOI (DSOI) as its called. Further tests and performance results of SOI and DSOI devices can be found in [116].

5.3 HV-CMOS PROTOTYPES AND DEDICATED READ-OUT ASICS

This section will describe the HV-CMOS prototypes, and their hybrid ROC, developed for the ATLAS and CLIC detectors, that were tested in the work developed for this thesis.

5.3.1 CCPDv3 and the CLICpix ROC

The CCPDv3 sensor The Capacitively Coupled Pixel Detector version 3 is a HV-CMOS sensor fabricated in the AMS 180 nm technology, designed to be used as a sensor coupled to the CLICpix ASIC, as shown in Figure 5.5.

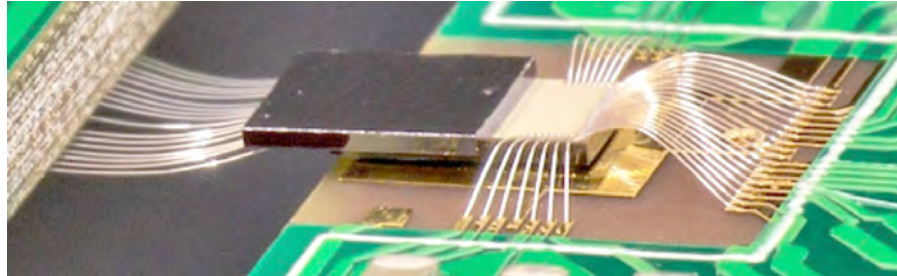


Figure 5.5: Picture of CCPDv3 (top) coupled to CLICpix (bottom).

The CCPDv3 pixel matrix matches the CLICpix pixel footprint, ie. 64×64 pixel matrix with $25 \times 25 \mu m$ pitch. A CCPDv3 pixel is illustrated in Figure 5.6a. The CCPDv3 was produced in a low resistivity ($10\text{-}20 \Omega cm$) substrate and, therefore, the active depth is not expected to exceed $30 \mu m$ as shown in Figure 5.6b, found from TCAD simulation performed to investigate the performance of the device [117].

Due to the small pixel size and the limitations from the technology node size (180 nm) and design rules, the pixel area is composed by only an analogue circuitry embedded in the deep N-well implants, without digital functionality (such as discrimination) being present. The charge signal is amplified by an integrating amplifier with a sec-

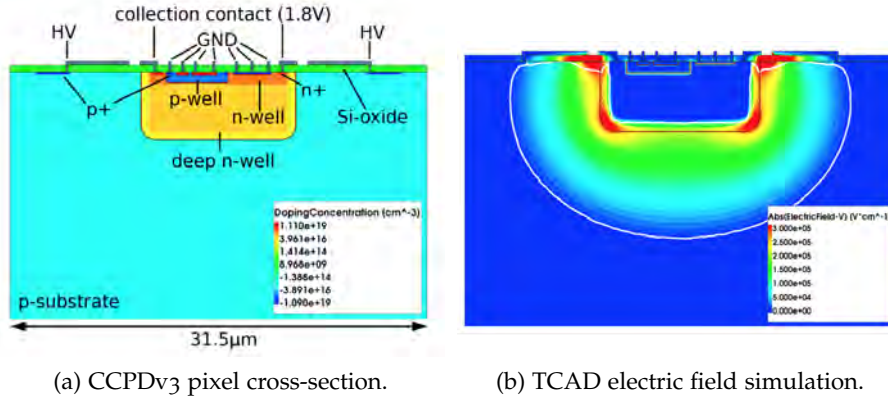


Figure 5.6: Illustration of the CCPDv3 pixel cross-section (a) and TCAD electric field simulation (b) [117].

ond stage voltage amplifier, and the resulting voltage is directed towards an output pad AC coupled to the ROC pixel pad, via a layer of a dielectric glue, as shown in Figure 5.7.

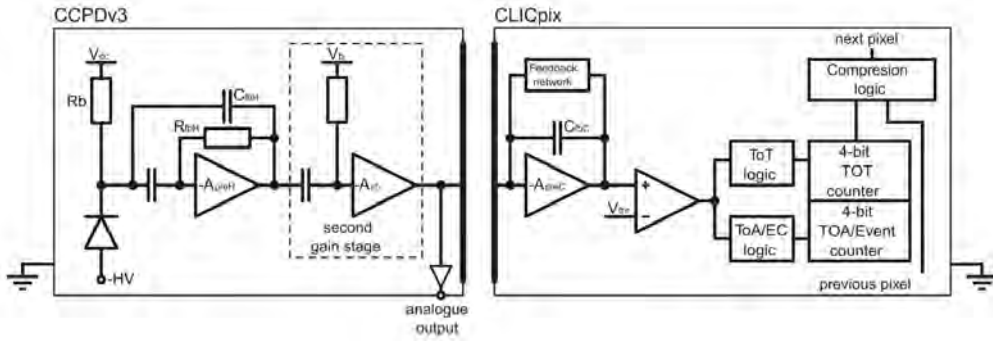


Figure 5.7: CCPDv3 schematic pixel coupled to CLICpix pixel [75].

CLICpix ROC CLICpix is the hybrid read-out ASIC prototype developed for the CLIC experiment. As the requirement of 3 μm position resolution is expected to be achieved with 25x25 μm² pixels, a 65 nm low-power CMOS technology is used [118].

The first CLICpix prototype has a pixel matrix of 64x64 pixels. Each pixel can perform, simultaneously, a ToT and ToA measurement with an 100 MHz clock and two 4-bit counters (4-bit ToT and 4-bit ToA with 10 ns binning). The energy measurement is designed with a dynamic range of up to 45 ke⁻. A block diagram of the CLICpix analogue front-end and digital electronics is shown in Figure 5.7.

As described in the previous sections, the current pulse coming from the sensor will be shaped and discriminated by the analogue front-end. The comparator can be locally adjusted, in order to compensate mismatches between different pixels, with a 4-bit DAC. The processed signal is then digitized by counting clocks, finally providing the pulse ToT and ToA. In addition, the ToT counting clock frequency can be divided to adjust the dynamic range to the measurement. The content of the 4-bit ToA and 4-bit ToT counters forms the 8-bit data acquired by each pixel.

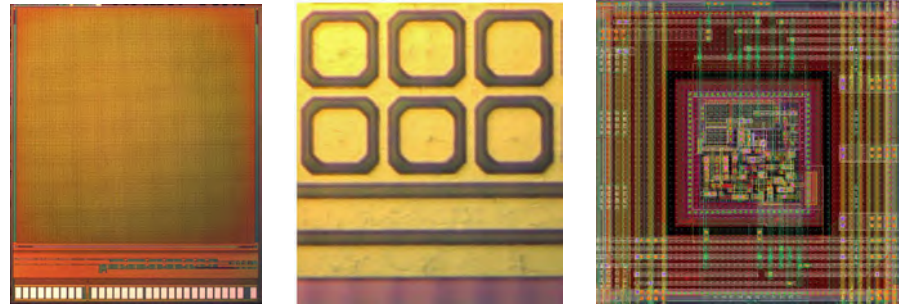
Due to the collision time-structure of the CLIC accelerator, having bunch train periods of 156 ns at a repetition frequency of 50 Hz, a power pulsing scheme is implemented, in order to save power and reduce heat dissipation, by turning off the analog part of the pixel during the 20 ms gaps between bunch trains. In addition, with the expected occupancy of less than 3%, the readout architecture is optimized with a “zero suppression” scheme in a trigger-less read-out.

5.3.2 C₃PD and CLICpix2

The C₃PD sensor The CLIC Capacitively Coupled Pixel Detector (C₃PD) [119] is the next next generation of HV-CMOS sensor, designed as a successor of the CCPDv3. The C₃PD implements an interface based on the I²C bus interface for configuration and control of the chip features.

As the CCPDv3, the C₃PD is implemented in a 180 nm HV-CMOS process and contains pixels of $25 \times 25 \mu\text{m}^2$. The C₃PD has a pixel matrix with 128×128 pixels, making an active area of $3.2 \times 3.2 \text{ mm}^2$. As the H35DEMO, the C₃PD was produced with substrate resistivities ranging from 20 up to $1000 \Omega\text{cm}$. From TCAD simulations a depletion region extending about $10 \mu\text{m}$ from the deep N-well is expected with a HV bias of -60V and a substrate resistivity of $20 \Omega\text{cm}$ [117].

Figure 5.8a shows a picture of the C₃PD chip. A new feature in the C₃PD is the guard-ring surrounding the pixel pads, to be coupled to the ROC pixel pads. Figure 5.8b shows a picture of 6 pixel pads and the guard-ring in-between. The guard-ring function is to shield the sensor pixel pad from the ROC pixel pads surrounding the respective pixel pad pair.



(a) C₃PD chip picture. (b) Pixels and guard-ring. (c) Pixel layout and bias lines.

Figure 5.8: C₃PD chip pictures. Photos (a) and (b) by Jerome Alozi.

A draw back of the HV-CMOS technology is that any P+ type implant (from the PMOS transistors for example) will couple capacitively to the deep N-well. This parasitic coupling can induce a signal in the sensor during the circuit operation. With more complex electronic circuits, w.r.t. CCPDv3, and in order to minimize possible noise sources, the use of PMOS transistors was minimized in the C₃PD design. As such design is sensitive to parasitic capacitances and different ways of routing and placing the circuit components can result

in significant performance variations, the pixel layout was optimized with systematic simulations. The layout design, shown in Figure 5.8c, converged to pixels organized in a double column structure with adjacent pixels sharing common biasing lines.

The CLICpix2 ROC The C3PD was designed to be capacitively coupled to the successor chip of the CLICpix ASIC, the CLICpix2 [120]. The new CLICpix2 is designed on the same 65 nm technology and implements new features to improve the ROC performance and fix previous design issues. It also contains pixels of $25 \times 25 \mu m^2$ and a matrix of 128×128 pixels. The design of the front-end blocks was improved in order to have better noise immunity and make their footprint smaller.

The CLICpix2 is still organized in 2×8 super-pixels, where pixels share part of their digital logic. In addition to the larger pixel matrix, the length of the ToT and ToA registers was also extended. The CLICpix2 records 5-bit ToT and 8-bit ToA. A new feature on the CLICpix2 ASIC is the possibility of combine the ToT and ToA registers into one single ToA register with 13-bit, providing a timing depth of $82 \mu s$ at 100 MHz clock. Figure 5.9a and 5.9b shows the CLICpix2 chip and the CLICpix2/C3PD assembly, respectively.

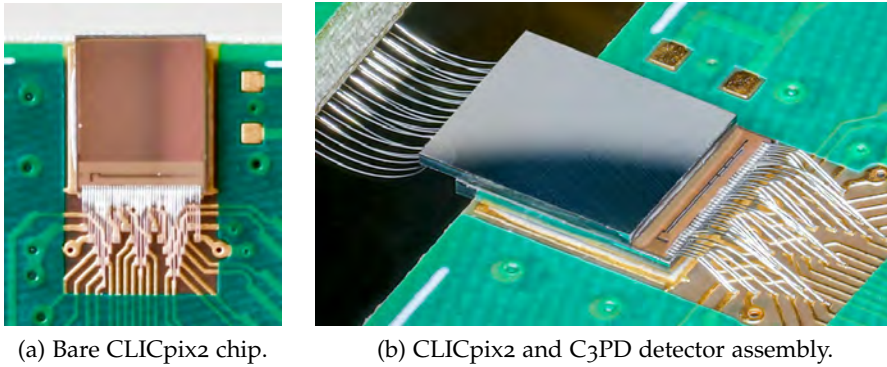


Figure 5.9: CLICpix and C3PD pictures.

5.3.3 CCPDv4 and FE-I4

The CCPDv4 sensor The next version of investigated HV-CMOS devices is the CCPDv4, also designed in the AMS 180 nm technology (as the CCPDv3 and C3PD prototypes) for the ATLAS ITk R&D. Even if ATLAS target monolithic devices, hybrid detectors allow the investigation of the sensor aspects of the technology decoupled from the technology read-out capabilities. Therefore, the CCPDv4 was designed to be read-out by the FE-I4 ROC (the same used in the ATLAS IBL) through an AC coupling. As the sensor will be capacitively coupled to the ROC, the CCPDv4 can have pixels with different size than the FE-I4 chip. The CCPDv4 pixel has $33 \times 125 \mu m^2$ and was manufactured in a $20 \Omega cm$ substrate, with a total size of $\approx 2.4 \times 2.9 mm^2$ and a thickness of $250 \mu m$.

The CCPDv4, shown in Figure 5.10a, was designed with its pixel matrix divided into 4 different flavors, each containing pixels with different electronics. With a larger pixel area (w.r.t. CCPDv3) an in-pixel digital circuit is possible and, therefore, the discrimination of the signal was also implemented in order to investigate the performance of digital (simple) architectures in this new technology. The *STime* pixel flavor implements a two-stage amplifier followed by a discriminator with tunable output amplitude, with a 4-bit DAC (TDAC) to correct per-pixel threshold dispersion.

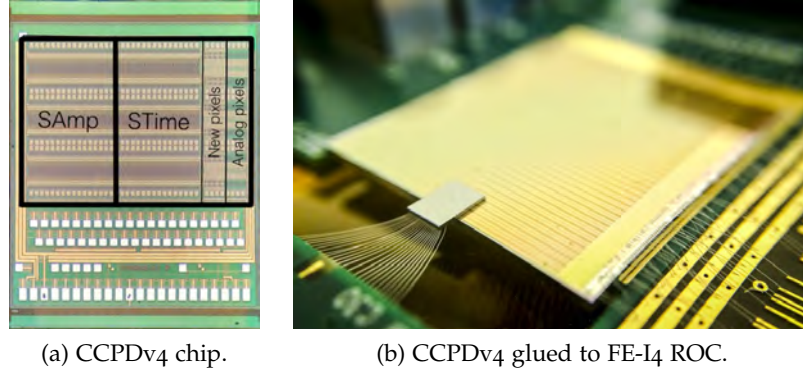
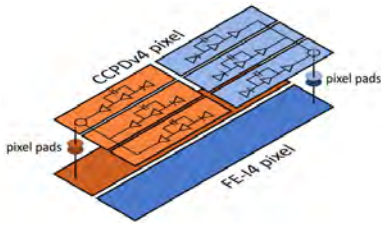
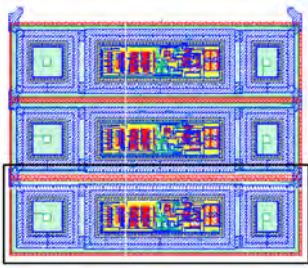


Figure 5.10: CCPDv4 and FE-I4 coupling.

Illustration of CCPDv4 and FE-I4 pixels coupling.



CCPDv4 pixel layout.



Similar to the super-pixel in the CLICpix, 6 pixels in the CCPDv4 are grouped (3x2) forming a single pixel cell. The total dimension of the pixel cell is $100 \times 250 \mu\text{m}$ and 3 pixels of the cell are merged and connected capacitively into a single pixel in the FE-I4 ROC, as illustrated on the figure on the left. The sensor and ROC were coupled together with the same flip-chip method used for the CLICpix + CCPDv3 assembly. Figure 5.10b shows a picture of the CCPDv4 HV-CMOS sensor coupled to the FE-I4 read-out ASIC.

Each pixel in the CCPDv4 has 3 deep N-wells acting as collection diodes. The middle N-well is the larger one, housing the pixel electronics. In order to distinguish which pixel is sending signal to the ROC, the sub-pixel address can be encoded into amplitude of the signal transferred, as illustrated in Figure 5.11a. Figure 5.11b shows the ToT spectrum, measured by the FE-I4, of the signal transferred from the HV-CMOS sensor.

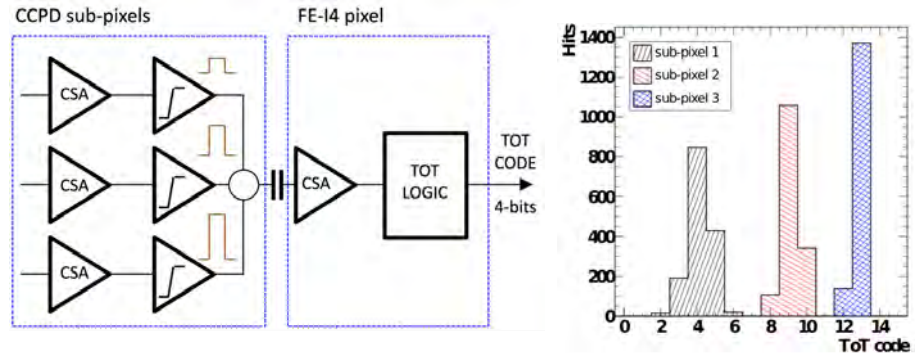


Figure 5.11: CCPDv4 sub-pixel encoding.

The FE-I4 ASIC The FE-I4 read-out ASIC, designed for the ATLAS IBL, was decided to be used to characterize the CCPDv4 as the ASIC was already extensively characterized during the IBL commissioning. In this way, with a well known read-out front-end, it is possible to investigate the performance of the HV-CMOS technology, regarding its sensitive properties, decoupled from read-out features. Figure 5.12 shows the electronics schematic of a FE-I4 pixel. Its electronics is similar to the CLICpix pixel, but as the FE-I4 pixel is 20 times larger more electronics fits inside the pixel.

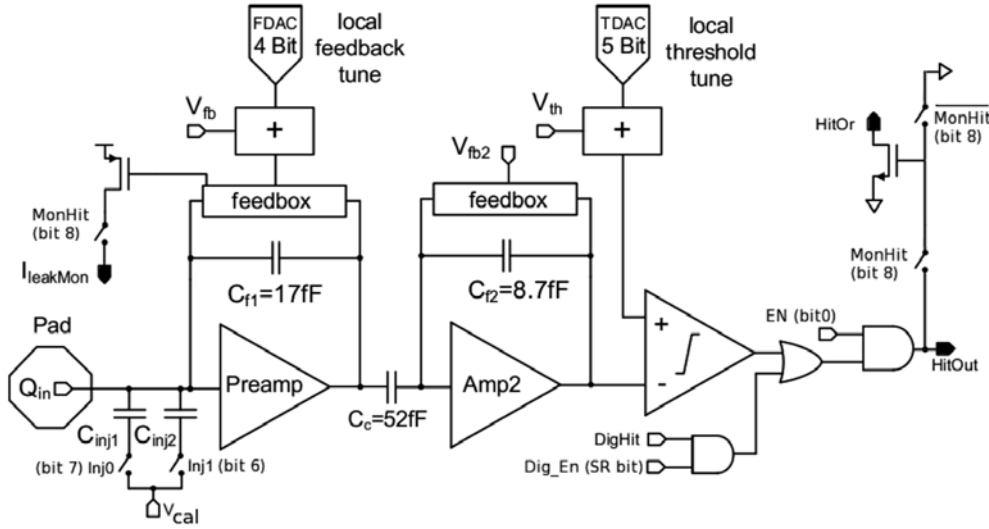


Figure 5.12: FE-I4 pixel electronics schematic [63].

The FE-I4 pixel has a pre-amplifier with a tunable feedback circuit that is responsible for equalize the fall-time of the amplified signal through the pixel matrix. It also has a tunable discriminator with 5-bits adjustment. It is possible to inject analogue and digital signals into the pixel in order to verify the pixel state and the discriminator of all pixels is ORed together and sent to a single line called *HitOr*, to be used later as trigger mechanism for the particle telescope used in the characterization tests.

A top level diagram of FE-I4 is shown in Figure 5.13. The FE-I4 pixel array is organized in double-columns, like the CLICpix ROC, and each double-column is further divided into 2x2 pixel regions. Each region connects the 4 pixel discriminators into one shared memory and logic block called Pixel Digital Region (PDR), as illustrated in Figure 5.13. The PDR stores locally the hit information until triggering (or until the maximum latency configured), to reduce the data transfer and power consumption when reading out the matrix. Each pixel has an hit processing unit and buffer memory, where up to 5 ToT hits information can be stored. The PDR is the responsible for the time-stamping of trigger and hits processed and also for storing the local pixel configuration, such as pre-amp feedback and discriminator tuning configuration (or TDAC map).

As many front-end read-out functionalities are already implemented on the pixel matrix, only global functionalities are needed to be implemented on the device periphery (such as communication and powering). In addition, as all voltages needed for the chip operation are generated internally, powered by a single external low-voltage (LV) line, the FE-I4 can be operated with the mentioned LV line and 3 LVDS (low-voltage differential signal) lines running at 40 MHz, each line responsible for clock, command input and data output.

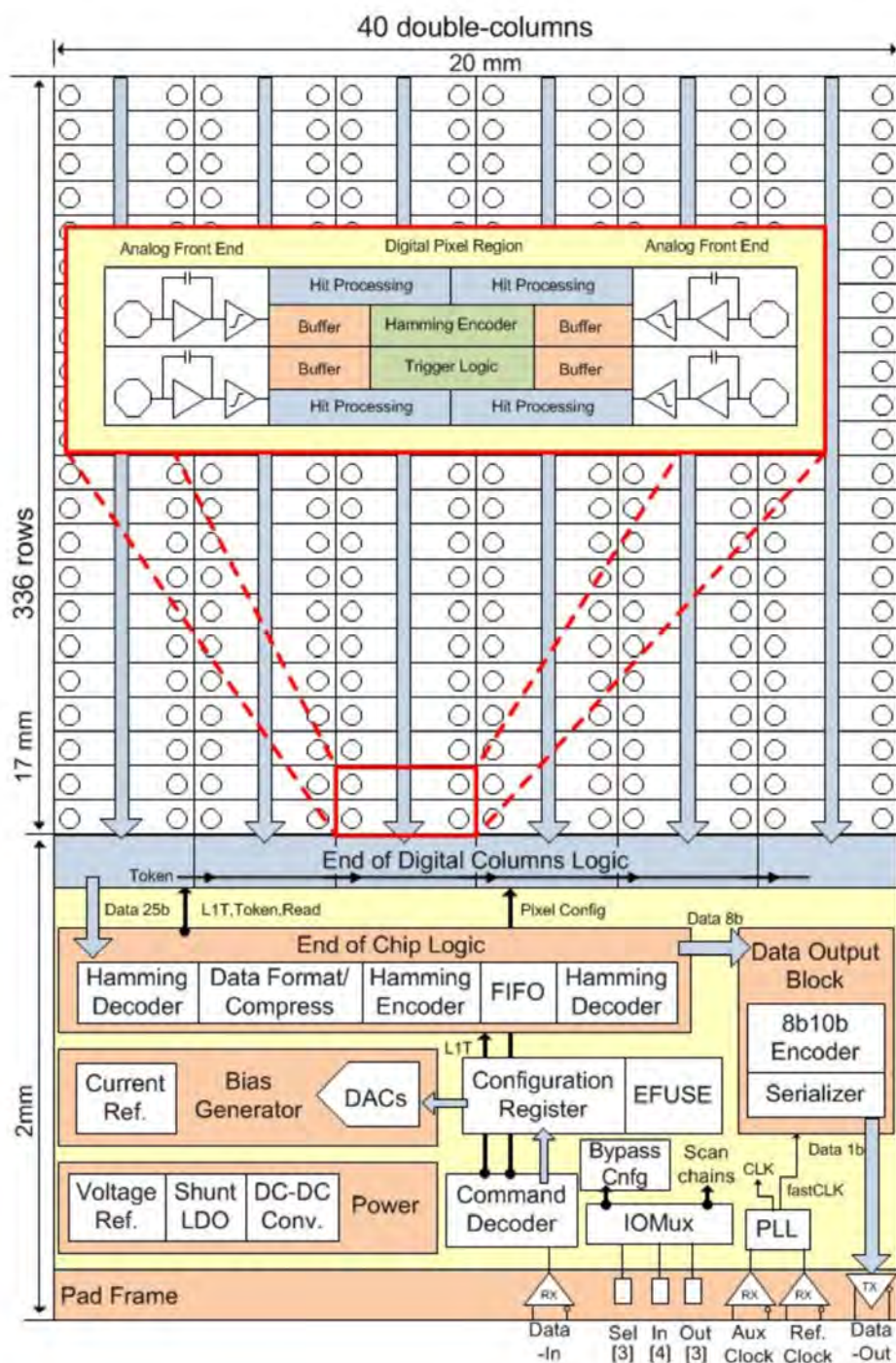
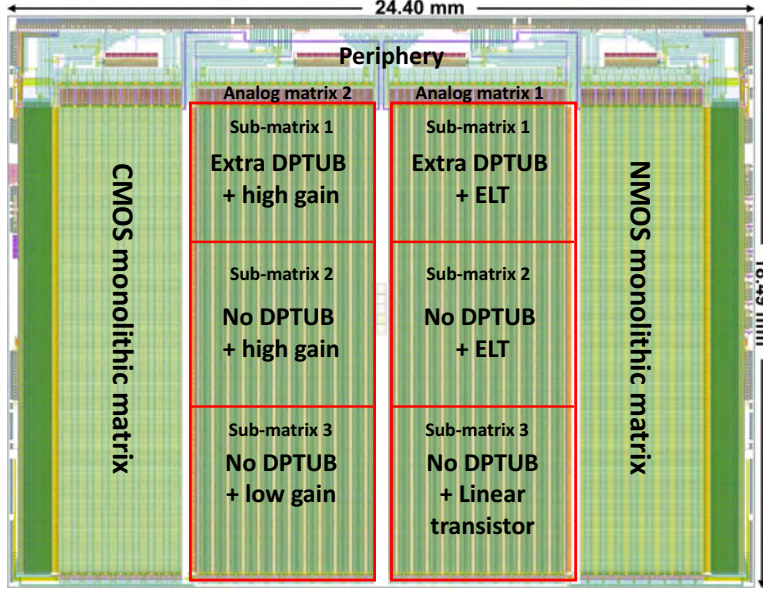


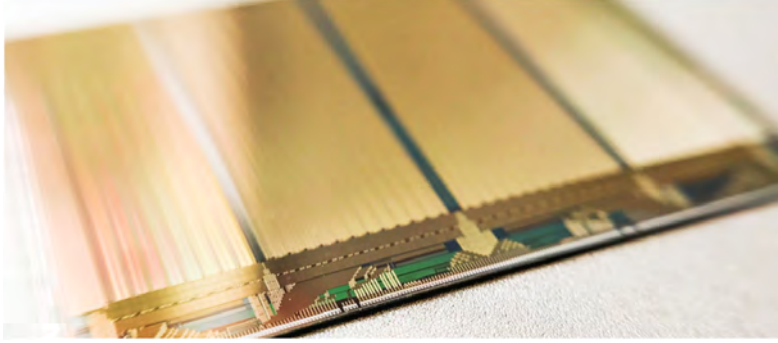
Figure 5.13: Top level block diagram of FE-I4 ROC [63].

5.3.4 H35DEMO and FEI4 hybrid

The H35DEMO [122][123], shown in Figure 5.14, is the first HV-CMOS designed as a full scale ("FE-I4 size" with a total area of 18.49 mm \times 24.40 mm) prototype in order to prove the feasibility of large area ($\mathcal{O}(cm^2)$) HV-CMOS sensors, as required for ATLAS ITk project, while investigating the effect of higher sensor resistivities. It was produced in the ams h35 (350 nm node size) HV-CMOS technology using three types of high-resistivity substrates: 80 Ωcm ; 200 Ωcm ; and 1000 Ωcm .



(a) H35DEMO device floor-plan with sub-matrices description [123].



(b) 100 μm tick H35DEMO picture.

Figure 5.14: H35DEMO HV-CMOS sensor.

As the CCPDv4, the H35DEMO includes four independent sub-matrices: the NMOS and CMOS monolithic matrices, integrating sensor and readout electronics into the same die, composing a monolithic detector; and two analogue matrices (ANA 1 and 2) designed for capacitive-coupling to the FE-I4 readout ASIC, decoupling readout electronics aspects from sensor diode properties. The ANA 1 and 2 pixel matrix has the same pitch as the FE-I4 (50x250 μm^2), creating an 1-to-1 pixel mapping from the H35DEMO sensor and FE-I4 ROC. Figure 5.15 shows the H35DEMO layout.

ANA 1 and 2 matrices are divided into 3 sub-matrices of 23×100 pixels, each with a different in-pixel amplification circuits. ANA 1 matrix consists of pixels containing different flavors of transistors (linear or with enclosed layout) and containing (or not) deep P-wells, to cope with NMOS transistors isolation and higher voltage biasing. ANA 2 matrix contains pixels with different gain in the second stage of amplification and different P-wells for high-voltage biasing.

Figure 5.15 shows the electronic design of the ANA1 H35DEMO pixel. As the CCPDv4, ANA 1 and 2 pixels also contain 3 deep N-wells acting as collection diodes, being connected to the input of the amplifier stages, with the middle N-well hosting and shielding the CMOS electronics. Finally the signal is transferred to the FE-I4 through the pixel pad, represented by the dark blue square shown on the bottom-left part of Figure 5.15.

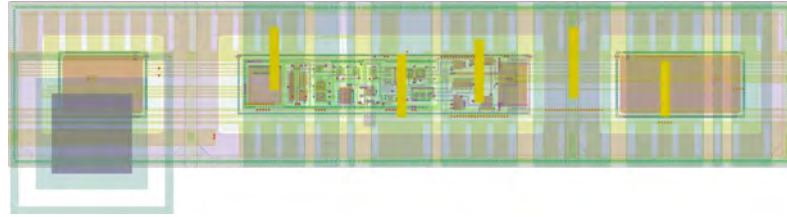


Figure 5.15: H35DEMO ANA 1 pixel circuit [123].

The expected output amplitude of the pixel is, in average, 300 mV for a detected charge of 4500 electrons. From simulations (see Chapter 7) the H35DEMO-FE-I4 pixel pad coupling is ~ 3.5 fF, resulting in a charge pulse in the FE-I4 pad equivalent to 6500 electrons. The H35DEMO ANA1 and ANA2 pixel electronics contains a two stage amplifier (similarly to the circuit shown in Figure 5.7 (CCPDv3), coupled to a FE-I4 ROC pixel).

TCAD simulations investigating the effect of different substrate resistivities has shown that higher resistivities yield larger depletion zones in the sensor bulk [124]. Figure 5.16 shows the comparison of the TCAD simulated electric field, at -120 V bias, for a $20 \Omega\text{cm}$ (on the left) and $1 \text{ k}\Omega\text{cm}$ (right) substrate. The white line in the figure shows the depletion region. It is possible to see that the depletion zone extends about $60 \mu\text{m}$ deeper into the bulk for the $1 \text{ k}\Omega\text{cm}$ substrate, while the region with high intensity electric field gets smaller, getting confined to the region between the collection implants.

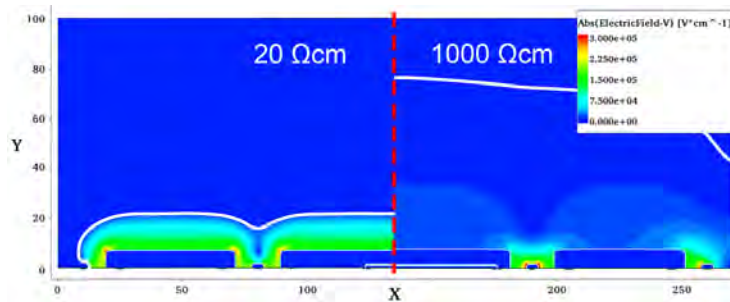


Figure 5.16: Comparison between $20 \Omega\text{cm}$ (left) and $1000 \Omega\text{cm}$ (right) electric field and depletion region, delimited by the white line [124].

5.3.5 ATLASpix

The ATLASpix [125][126] is the latest monolithic HV-CMOS pixel detector prototype under study by the time this thesis is being written. The ATLASpix, shown in Figure 5.17, was designed in a commercial 180 nm HV-CMOS process. In a similar way to the previous prototypes, the ATLASpix was designed in 3 different flavors, to be operated independently, named ATLASpix M2, Simple and IsoSimple.

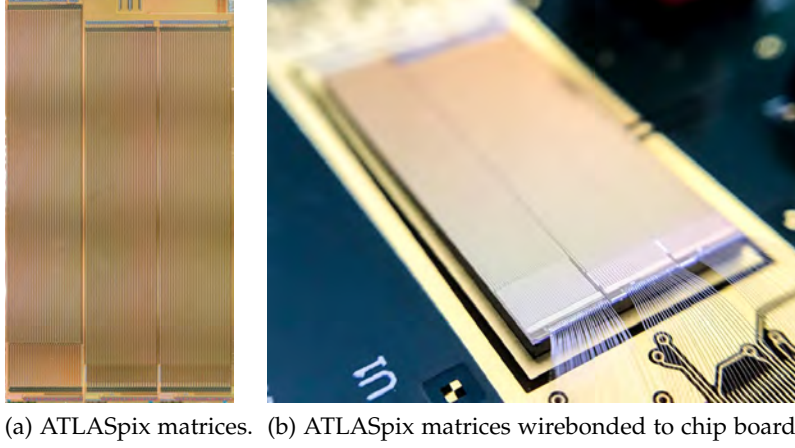


Figure 5.17: ATLASpix chip pictures.

The ATLASpix M2 implements the so called parallel-pixel-to-buffer (PPTB) readout. The hit information is transferred from pixels to the trigger-buffer blocks with a parallel bus. The pixel cells in the matrix contain an amplifier stage and a comparator (with a threshold tune DAC). The chip periphery contains the trigger-buffer block, which receives the comparator output of each pixel, digitizes the hit information (assigning a pixel address, a 10-bit time-stamp and 6-bit ToT) and stores the information for the duration of the trigger delay (up to 25 μ s), or until a trigger is received, similarly to the FE-I4 read-out. The matrix contains 56x320 pixels with 60x50 μ m² pitch, and each group of 16 pixels in the matrix shares 4 buffers.

The ATLASpix (Iso)Simple design implements the so called column drain readout and it is the flavour investigated in this thesis work. The address and time-stamp information is generated still in the matrix, in the digital part of the pixel, while the whole column shares a common data bus. In the case of multiple hits, the data are read out in a serial way, row-wise. Figure 5.18 illustrates the ATLASpix (Iso)Simple pixel block diagram.

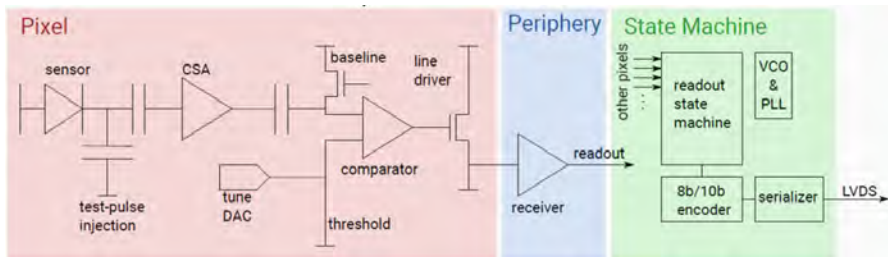


Figure 5.18: ATLASpix pixel and matrix read-out top level block diagram.

The Simple matrix contains 25×400 pixels with $130 \times 40 \mu\text{m}^2$. The pixel analogue and digital circuit is physically separated, with the analogue part being placed inside the collection electrode and the digital part being placed at the periphery. The read-out mode is data-driven, meaning that the data processed by the pixel is readout without trigger, continuously.

The ATLASpex Simple was implemented in two variants: the nominal ATLASpex Simple and the variant that uses deep P-well implants to isolate the PMOS transistors from the deep N-well, named ATLASpex IsoSimple.

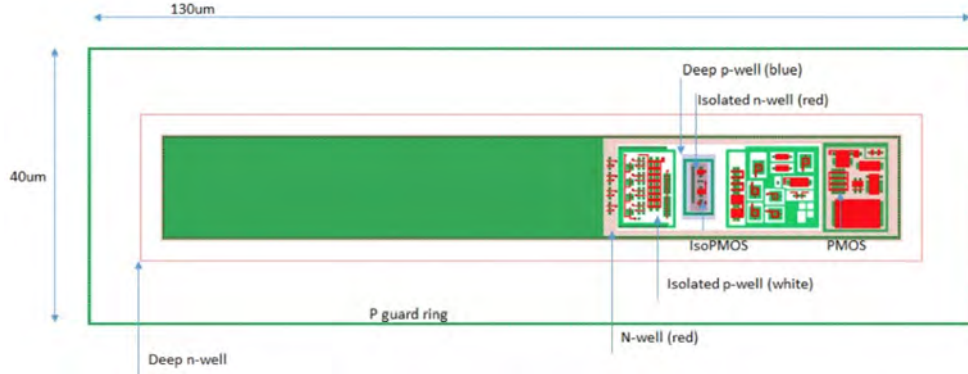


Figure 5.19: ATLASpex Simple pixel layout.

Shown in Figure 5.19, the pixel in the Simple pixel type electronics is contained in a deep n-well (outer red line) that also acts as the charge collection electrode. The pixel is composed of a charge sensitive amplifier and discriminator (also with a 3-bit tuning DAC). As PMOS transistors can be a source of noise, the comparator (which consumes large current and generates large signals) was designed only with NMOS transistors to avoid large crosstalk.

In contrast, the IsoSimple pixel type is composed of two types of PMOS transistors: the normal PMOS transistors, placed inside the shallow N-well, and the isolated PMOS transistors, where the respective N-well is surrounded by a new deep P-well implant, isolating the N-type substrate of the transistors from the deep N-well, as illustrated in Figure 5.20. The use of IsoPMOS transistors allows the implementation of CMOS comparators (composed of NMOS and (Iso)PMOS transistors), with lower power consumption and higher radiation tolerance.

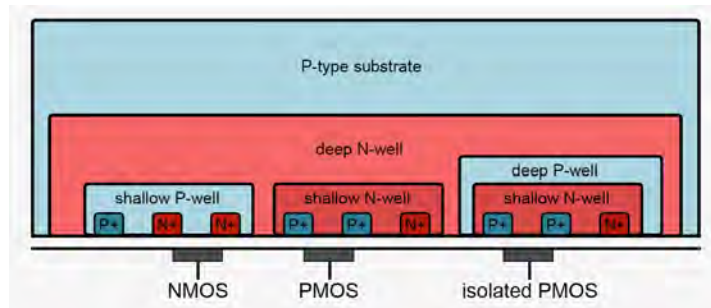
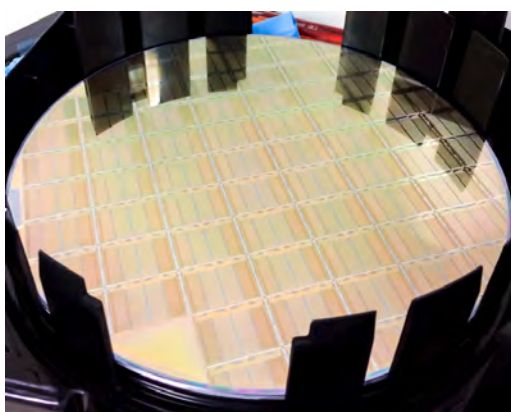


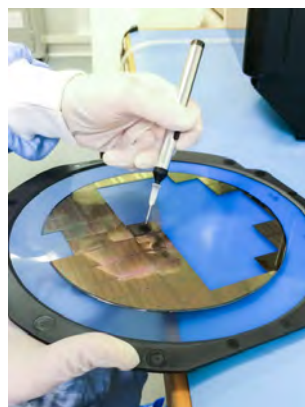
Figure 5.20: Illustration of NMOS, PMOS and isolated PMOS transistors.

WAFER TESTS, FLIP-CHIP AND THE CARIBOU READ-OUT SYSTEM

This chapter will introduce the detector assembly process, from its reception - still in the wafer format - to its integration in a test system. After the detector design is completed and submitted to the chip foundries, it arrives from production in wafer format. Many tests can be performed on the devices while still in the wafer and once the good devices are mapped in the wafer, classified according to test results, the wafer is sent for dicing, where the dies (detector chips) will be separated by a mechanical saw or by laser cut.



(a) H35DEMO 8-inch wafer.



(b) H35DEMO diced wafer.

Figure 6.1: Steps of the detector production.

If the detector is hybrid-type, it is needed to perform the coupling between the sensor and ROC. This is done in the flip-chip step, to be described in the following sections.

Once the detector module is produced, it needs to be wire-bonded to its respective carrier board, that will power and route its control and data signals. The part responsible for controlling the detector is called data acquisition (DAQ) system.

6.1 WAFER-PROBING AND HV-CMOS RESISTIVITY INVESTIGATION

The detector wafer can be tested and characterized using a wafer-probing system. The main components of such systems are: the wafer chuck, which should be flat and contain a vacuum system in order to hold the wafer in place; the needle probes with high-precision positioning stages; a microscope, to be used for the wafer-probe alignment; and a chiller in order to maintain a constant temperature on the wafer. Depending on the test to be performed on the wafer, the probes can be connected to equipments dedicated for semiconductor tests, or directly connected to the detector DAQ system.

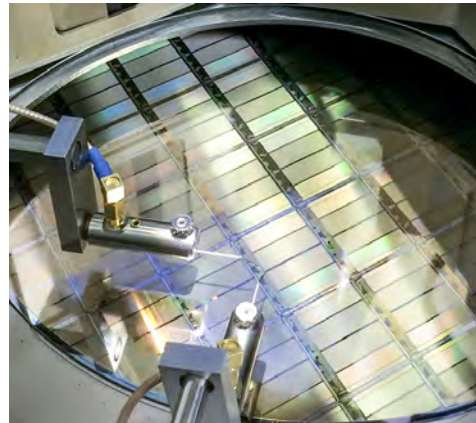


Figure 6.2: Semi-automatic probe station.

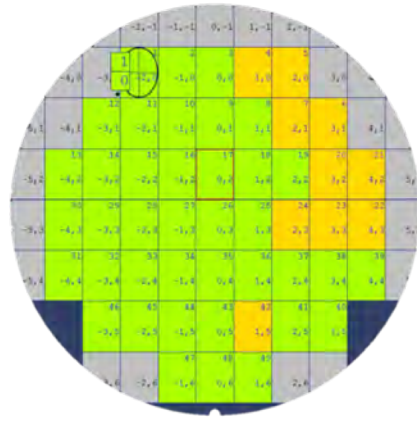
Figure 6.2 shows a picture of the CascadeMicrotech CM300 probe-station system used at Geneva University for the tests performed on the prototypes under study. The left part of the picture shows the vortex-based chiller with the semiconductor Source Measure Unit (SMU) on the top. Figure 6.2 also shows the wafer load port on the bottom-right, two probes positioned in the center and the microscope and screens on the top.

The vortex-based chiller provides fast and accurate temperature control, with cooling capability from -60°C to $+300^{\circ}\text{C}$, consuming up to 600 l/min of dry air. The chiller is directly integrated to the wafer chuck and can be controlled by the SMU. The probe-station microscope is integrated with the probe-station software and automatic wafer alignment and die mapping is possible, allowing automatic positioning and thermal contraction corrections.

The SMU can perform several types of tests, such as capacitance *vs* voltage (CV) or current *vs* voltage (IV), to determine properties such as depletion and breakdown voltages. The tests can run automatically over all dies on the wafer, for a set of temperatures and the results are used to select the fully functional (Class A) devices.



(a) Probes on H35DEMO wafer.



(b) H35DEMO wafer map.

Figure 6.3: Picture of HV probes on wafer and wafer map with die class in color.

Figure 6.3a shows a picture of the two probes connected to a single die on the H35DEMO wafer and Figure 6.3b shows an H35DEMO wafer quality map, determined by the breakdown voltage V_{bd} , with Class A devices, defined as $V_{bd} > 150$ V, in green and Class B (150 V $> V_{bd} > 120$ V) devices in yellow.

The H35DEMO was produced in three resistivities (80, 200 and $1000 \Omega\text{cm}$) in order to investigate the effect of the substrate resistivity on the charge collection efficiency and the timing performance. Although the higher resistivity will help to increase the depletion zone on the substrate bulk, the capability of sustaining high voltages (above 100 V) has to be confirmed. As the transistors in the HV-CMOS devices are shielded by the collection implant, their size (350 nm for the H35DEMO) will not change significantly the leakage current, making the breakdown voltage dependent on the geometry of the deep N-well implants and the HV distribution.

The IVs were performed between -25 and 25°C in steps of 5°C . The IV performance of the 80 and $200 \Omega\text{cm}$ samples are very similar, showing an HV breakdown at 178 and 180 V, respectively. Figure 6.4a contains the IV curves for the $200 \Omega\text{cm}$ sample and it shows that the leakage current is kept below $1 \mu\text{A cm}^{-2}$ for all temperatures.

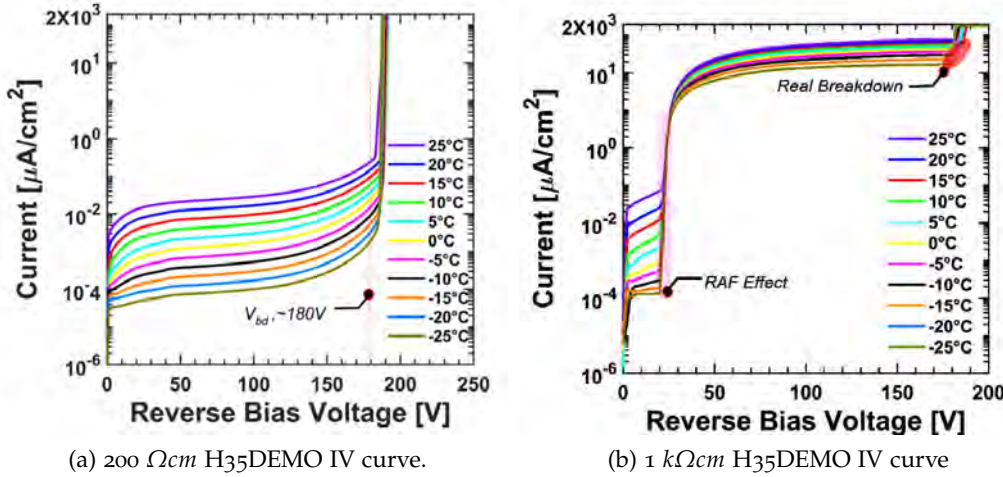


Figure 6.4: H35DEMO single die IV measurement [127].

The IV scan performed on the $1 \text{ k}\Omega\text{cm}$ sample shows an early rise on the leakage current for low voltages (< 30 V). Initially this effect was mistaken as an early breakdown of the sensor, limiting the HV data set produced with test-beam for the $1 \text{ k}\Omega\text{cm}$ sample. Later measurements, as the one shown in Figure 6.4b, revealed that a current plateau is reached before a second current upset at 180 V, corresponding to the real breakdown. The additional leakage current was found to be due to a surface current generated by parasitic metal structures at the edge of the sample when high-resistivity substrate are used, an effect known as the Rise-And-Flatten effect [128].

In principle the depletion voltage could also be obtained from IV measurements, as the leakage current generated in the sensor volume would saturate once full depletion is reached. However, the transition

from where the current is proportional to \sqrt{V} (as shown in Equation 4.11) to its saturation is not precisely measurable. For this reason, capacitance measurements are more suitable. The sensor capacitance can be approximated to two parallel conductive plates separated by the depletion width $W(V)$:

$$C(V) = \frac{\epsilon_0 \epsilon_{Si}}{W(V)} \propto \begin{cases} \sqrt{\frac{\epsilon_0 \epsilon_{Si} e N_D}{2V}}, & \text{for } V < V_{depl}. \\ \frac{\epsilon_0 \epsilon_{Si}}{d}, & \text{for } V > V_{depl}. \end{cases} \quad (6.1)$$

The upper part in Equation 6.1 shows that the sensor capacitance is proportional to \sqrt{V} while the bias voltage V is lower than the full depletion voltage V_{depl} , while the bottom expression shows that the capacitance is constant for the fully depleted sensor, with thickness d . The full depletion voltage can be determined by plotting $1/C^2$ vs V and finding the transition between the two regimes, when V gets higher than V_{depl} . The CV measurements were done on the H35DEMO Analogue matrix 1 using a frequency of 100 kHz, with an AC signal of ± 100 mV, while the wafer was cooled down to 0°C .

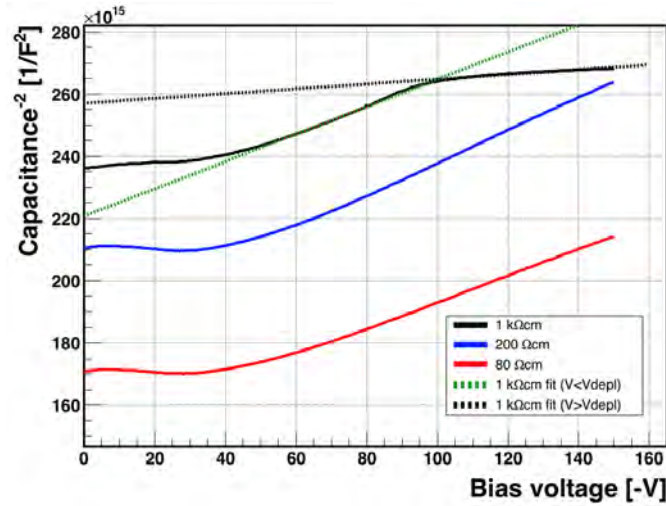


Figure 6.5: H35DEMO ANA1 capacitance vs HV bias curve.

The measured capacitances, for the three different resistivities available, are shown in Figure 6.5. The (approximately) constant capacitance between 0 V and 30-40 V indicates that the depletion region also expands laterally, counterbalancing the increasing depletion depth¹. The three resistivities have shown a similar lateral depletion, which depends on the distance between the last pixels and the device edge. After 40 V the depletion region expands more towards the sensor bulk and the 1 kΩcm sample reaches maximum depletion at around 100 V, while the 80 and 200 Ωcm sensors don't reach full depletion, with an expected depletion depth (from TCT measurements) in the order of 50 μm at 100 V [129].

¹ An effect analogous as if the area A of a parallel plate capacitor, with capacitance $C = \epsilon A/d$, increases in the same proportion as d .

6.2 FLIP-CHIP SETUP, TESTS AND ASSEMBLY

In order to capacitively couple the HV-CMOS sensors with their respective ROC, a method was developed using the semi-automatic *Accura 100* flip-chip bonder [130]. The flip-chip machine, shown in Figure 6.6, is composed of a thermal chuck and Z-arm, each with a vacuum channel to hold a device (the sensor or the ROC). The chuck is supported by stages and it can move in the X and Y directions, with a nominal accuracy of $0.5 \mu\text{m}$, and rotate in theta with $1 \mu\text{rad}$ resolution. A microscope with two cameras is placed in between the chuck and Z-arm and can move in the X, Y and Z directions. One microscope camera points down to the chuck while the other points up to the Z-arm, and both images overlaid are used to align the chuck under the Z-arm, aligning the devices to be bonded. In addition, the flip-chip machine has an automatic glue dispenser in order to deposit a fixed amount of glue on the assembly.

The flip-chip machine is calibrated to correct for a possible offset between the position of the cameras and to ensure an optimal parallelism between the surface of the chuck and of the Z-arm. To guarantee good assembly yield, the flip-chip machine is installed in a temperature controlled clean-room in order to maintain the calibration.

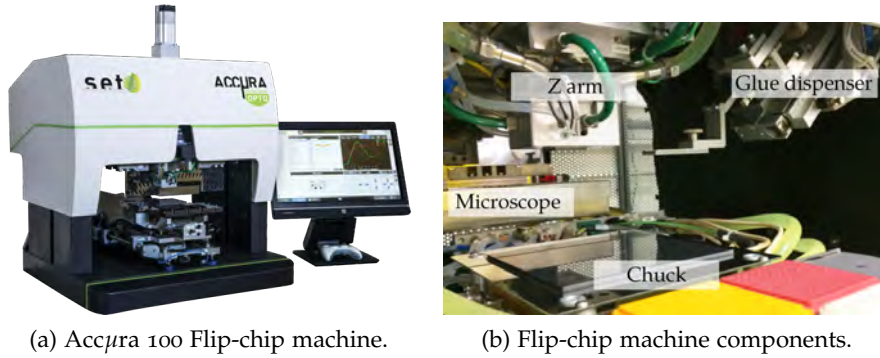
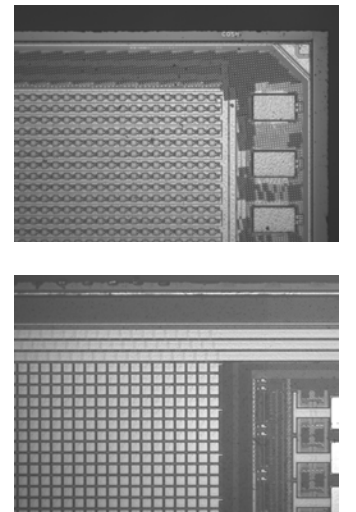


Figure 6.6: Accura 100 Flip-chip machine pictures [131].

Once the ROC and HV-CMOS sensor are loaded on the Z-arm and on the chuck, respectively, both devices are aligned using the pixel pads at the top surface (last metal layer of the CMOS stack) of each chip. This is done semi-automatically by the flip-chip program by overlaying the two images from the microscope cameras, shown in Figure 6.6, and manually moving the chuck, under the fixed Z-arm, until the pixels are on the desired position. By running this alignment in two distinct parts of the assembly (preferably at the detector edges) the flip-chip software calculates the relative offset and angle between the devices and corrects the misalignment.

As the accuracy of the final alignment depends mainly on a visual inspection using the flip-chip camera, a software tool was developed in order to find the pixel pads position in the images from the microscope and calculate the remaining offset from the alignment prior to the bonding.

CLICpix (top) and CCPDv3 (bottom) microscope pictures



6.2.1 *PixelShop alignment tool*

The PixelShop [132] software was developed, using the OpenCV (Open source Computer Vision) library [133], in order to quantify the alignment between the chips being coupled. It works by finding the contours of the pads from the flip-chip pictures and calculating their relative offset.

OpenCV finds contours on the flip-chip pictures by grouping adjacent image pixels, containing the same color or intensity, in continuous curves. A single image pixel can be part of multiple contours and, for this reason, a hierarchy between the different contours is internally defined by the library.

Among the many contours found in an image, the contours corresponding to the pixel pads must be filtered. This is done by checking the following contours properties: the total area of the contour found; the aspect ratio of an upright rectangle enclosing the contour; and the solidity of the contour, defined by the ratio between the contour area and the area of the contour convex hull. Specific parameter values must be used for each pixel pad geometry and the values for the CLICpix and CCPDv3 pixel pads can be seen in [134].

In order to facilitate the search of the pixel pad contours, the image must have some key qualities enhanced. Qualities adjusted by the PixelShop software are brightness, contrast, clarity and threshold. Figure 6.7 shows the effect on the picture after changing the mentioned qualities, making the edge of the pixel pads more pronounced.

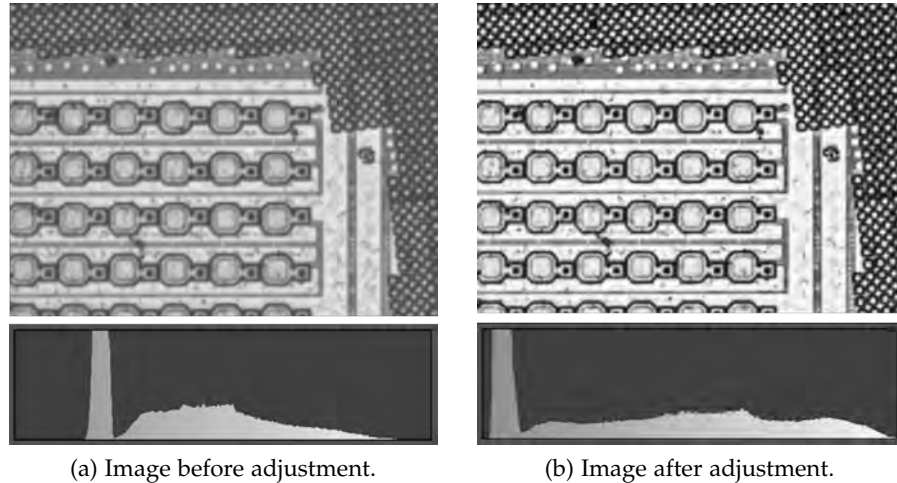
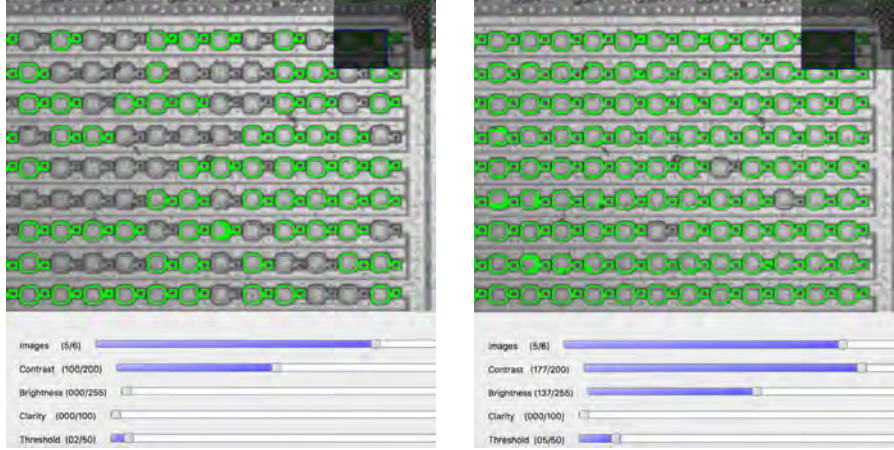


Figure 6.7: Flip-chip image enhancement of CLICpix pads with PixelShop.

The histogram on the bottom of Figure 6.7 represents the amount of pixels as function of their color (in a grey scale), with total black and white in the left and right sides of the spectrum. The change in brightness shifts the histogram distribution homogeneously to darker or brighter tones. The contrast stretches the distribution around its mid tones. Clarity is a contrast applied only for the mid tone range, having a smaller effect at the margins of the distribution (keeping the

dynamic range of the image). Lastly, a threshold cuts out pixels above or below a specified tone.

Figure 6.8 shows the pixel pads contours found before and after the image adjustment. The change in parameters can be seen in the software controllers shown on the screen-shot.

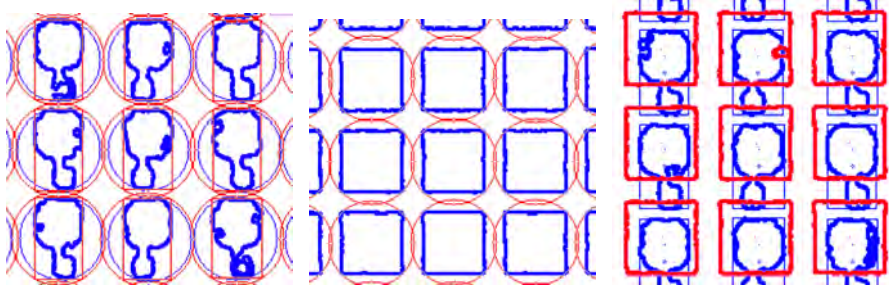


(a) Found contours before adjustment.

(b) Found contours after adjustment.

Figure 6.8: Comparison of the CLICpix pad contours found before (a) and after (b) image treatment.

The position of each pad is found by adjusting circles and/or rectangles enclosing the found pad contours, as shown in Figure 6.9, and extracting the position of the center of each fitted shape. By having the X and Y position of each pixel pad on the pictures, and assuming that the microscope cameras are aligned, it is possible to calculate the difference in the position of the sensor-ROC pad pairs.



(a) CLICpix pixel contours.

(b) CCPDv3 pixel contours.

(c) Overlaid pads contours.

Figure 6.9: Pixel pads found by the PxlShop software.

Figure 6.10 shows the measured offset in the XY plane between the pad positions, as well as for the separated X and Y components, for each pixel with a contour found within the field of view of the cameras of $900 \times 700 \mu m$. It is possible to see that the distance between the pads depends on the position of the pads in the flip-chip images, assuming that the pixel pitch doesn't change within the chip surface.

As during the flip-chip alignment possible rotation angles between the chips are compensated, with a resolution of $1 \mu rad$, the gradient visible in Figure 6.10 is expected to be an effect from the flip-chip

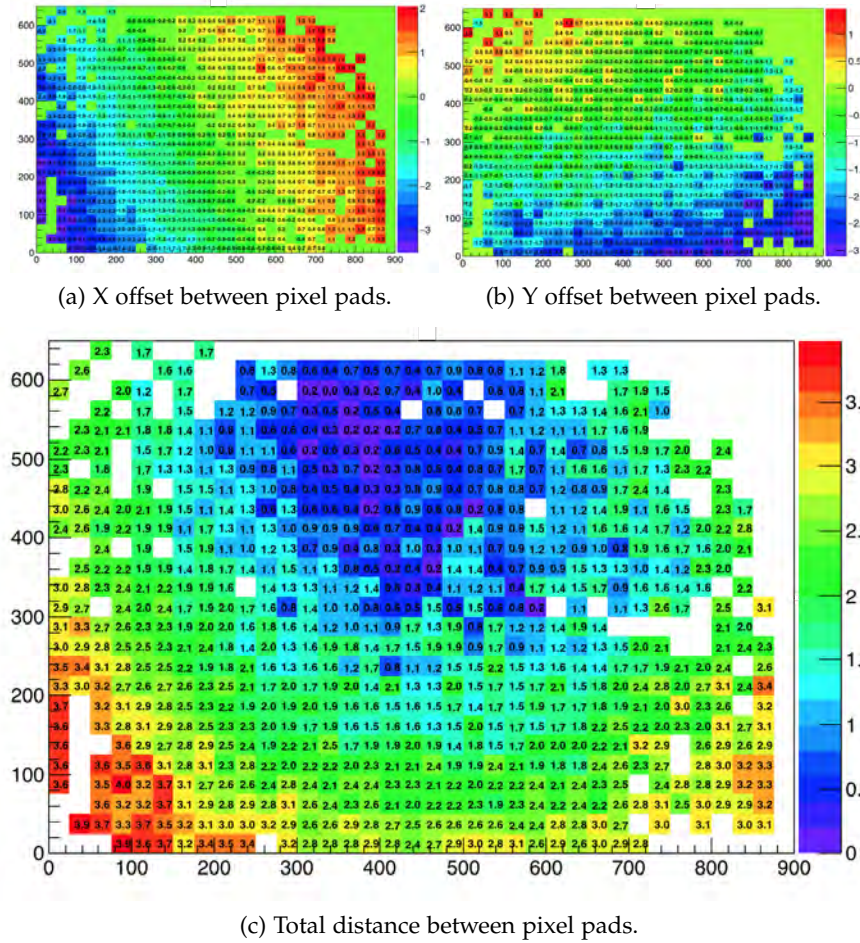


Figure 6.10: X (a), Y (b) and combined (c) offset between the CLICpix and CCPDv3 pixel pads.

camera lenses distorting the images. Therefore, the image of each camera was analyzed individually.

Assuming that the bottom-left pixel in the image from the flip-chip camera has coordinate $(0,0) \mu m$, the position of all pixels in the image can be compared with the nominal pixel position, calculated by multiplying the pixel index (within the image) by the pixel pitch. Figure 6.11 shows the difference between the nominal and measured position of the pixel pads of both flip-chip cameras. Empty bins are pixels without a contour found.

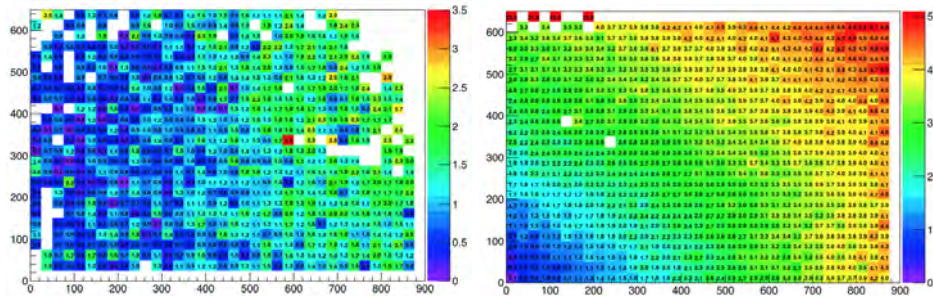


Figure 6.11: Distortion seen in the top camera (left) and bottom (right).

As expected from a lens correction effect, it is possible to see that the distance difference changes for different positions within the camera field of view and this effect was notified to the manufacturer of the flip-chip machine. In order to minimize the image distortion effect on the flip-chip assemblies, the alignment during the coupling was done always ensuring that the alignment points were located at the center of the field of view of the cameras.

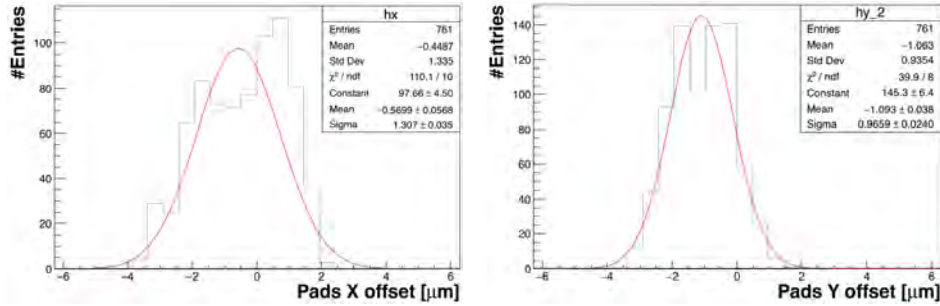


Figure 6.12: Horizontal (left) and vertical (right) offsets between pixel pads.

Figure 6.12 shows the 1D distributions of the distances measured and shown in Figures 6.10a and 6.10b. Having in mind that the width of the distribution comes from the lens distortion effect, it is possible to see that the distributions are centred around 0, with a mean (from a Gaussian fit) at $\sim 0.6 \mu\text{m}$ and $\sim 1 \mu\text{m}$, in X and Y respectively, indicating a good absolute alignment precision in the order of $1.1 \mu\text{m}$. Assembly cross-section measurements, such as the one shown in Figure 6.20, have confirmed that the practical alignment precision after bonding is in the order of $1 \mu\text{m}$. Simulations, described in Chapter 7, have shown that small misalignment effects won't affect significantly the signal transfer in CCPDs.

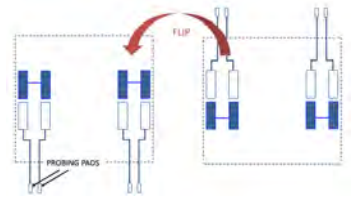
6.2.2 Assembly planarity investigation

Capacitive test-structures (developed by INFN Genova) were used to evaluate and optimize the flip-chip glueing process. The capacitive tiles consist of quartz glass chips with a single aluminum layer, $1.2 \mu\text{m}$ thick. The metal layer is designed with pads of $0.5 \times 1.5 \text{ mm}^2$ to form multiple capacitors when two chips are bonded together, as shown in Figure 6.13.



Figure 6.13: Capacitive test chip design (left), glue deposition (center) and final assembly (right).

Tile capacitors assembly



The bonding recipe used for the test chip is the same as used for the H35DEMO/FE-I4 bonding (described on the next session) and the capacitance was measured, using the probe-station described earlier, at 1V with a 50 mV 1 MHz AC signal (the maximum frequency available from the probe-station equipment is 5 MHz). The test chip has 48 capacitors that can be measured independently, providing a measurement of the planarity of the assembly. The first two test structures assembled resulted in the capacitance distribution shown in Figure 6.14. A clear gradient is present on both test chips from top left to bottom right, with the capacitance ranging from 1 up to 16 pF (indicating a gap ranging from ~ 0.5 up to $10 \mu\text{m}$, assuming a glue dielectric constant of 3.2).

1,11	1,09	1,07	1,12	1,19	1,34	1,62	2,1	1,15	1,12	1,11	1,13	1,19	1,33	1,6	2,05
1,23	1,22	1,23	1,24	1,31	1,46	1,76	2,25	1,92	1,25	1,24	1,27	1,53	1,88	2,54	
1,45	1,41	1,39	1,42	1,51	1,69	1,99	2,49	1,47	1,41	1,39	1,45	1,59	1,84	2,3	3,21
1,86	1,77	1,75	1,83	2,06	2,4	2,83	3,3	2,06	1,88	1,84	1,98	2,31	2,8	3,56	
2,58	2,4	2,37	2,56	2,97	3,73	4,70	5,5	3,05	2,63	2,49	2,62	3,13	4,23	5,29	7,09
4,64	4,07	3,96	4,32	5,18	7,28	10,7	16,7	6,75	4,87	4,25	4,2	5,11	7,76	10,4	12

Figure 6.14: Test-structure capacitances, in pF.

The gradient was explained to be due to a bad planarity on the flip-chip machine. A measurement on the machine confirmed an angle between the chuck and the Z-arm of $1000\text{--}2000 \mu\text{rad}$, which after calibration was reduced to the order of $5 \mu\text{rad}$.

Two capacitive tiles were assembled after the new machine calibration and both still show a gradient (6.15). The measured mean capacitance of the first sample, from a Gaussian fit, is 7.1 pF with a deviation of 1.1 pF, while the second sample shows a mean capacitance of 6.5 pF with a deviation of 0.8 pF. To quantify the effect of the capacitance gradient in terms of the gap distance, the average gap was calculated for the top, left and bottom capacitors (indicated by

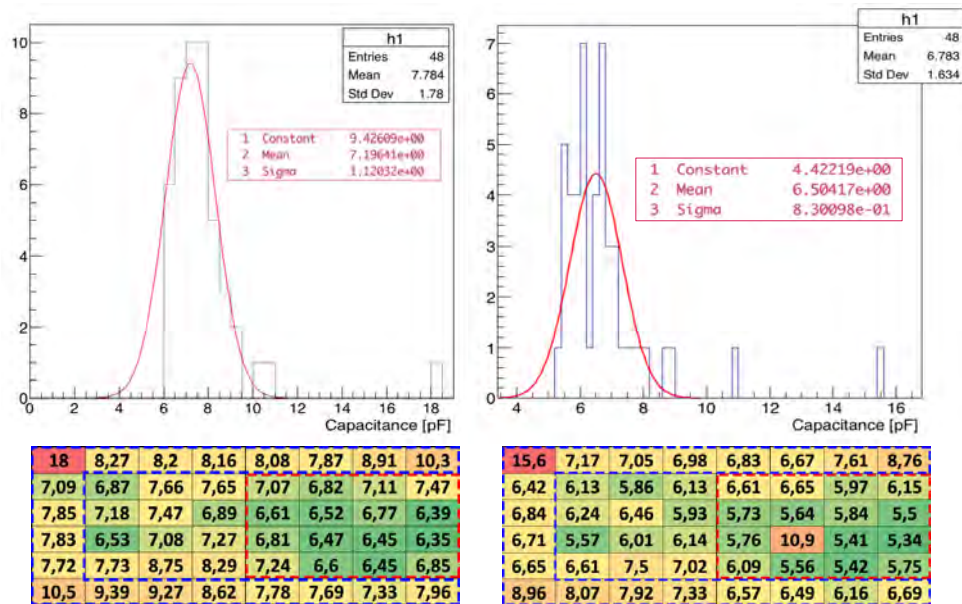


Figure 6.15: 1D and 2D capacitance distribution. Values are in pF.

the blue line in the capacitance map) and for the 4x4 capacitor group, indicated by the red line. The estimated gap difference is $0.38 \pm 0.24 \mu\text{m}$ and $0.37 \pm 0.39 \mu\text{m}$ for the first and second sample, respectively.

The 0.6 pF difference in the mean values measured from the two samples is expected to come from small differences in the alignment and from the quantity of glue used for the coupling. As the same glue mixture was used for both samples, with a curing time of 1 hour (at room temperature) and with about 20 minutes needed for each assembly coupling (time being non-optimized), the amount of glue being dispensed onto each chip can be different when the same dispensing pressure and time is used. To evaluate the planarity of the sample the relative standard deviation (RSD), defined by the ratio of the standard deviation σ to the mean μ and expressed as a percentage, will be used. In this metric, the first and second samples yield a RSD of 15.5 % and 12.7 %, respectively.

6.2.2.1 Capacitive tiles with pillars

In order to improve the parallelism of the flip-chip process, pillars used to constrain the gap between bonding devices were investigated. The pillars were deposited on the chip wafer by spinning KPMR photoresist over the respective pillar mask. The rotation speed was set to create a $5 \mu\text{m}$ KPMR layer (and consequently pillars) and the height of the pillars was measured at INFN-Genova, using a mechanical profilometer, resulting in a mean height of $5.12 \pm 0.025 \mu\text{m}$. Two more samples were assembled using the chips with $5 \mu\text{m}$ pillars and the capacitance measurement distributions are shown in Figure 6.16.

$250 \mu\text{m}^2$ pillars deposited between the capacitors

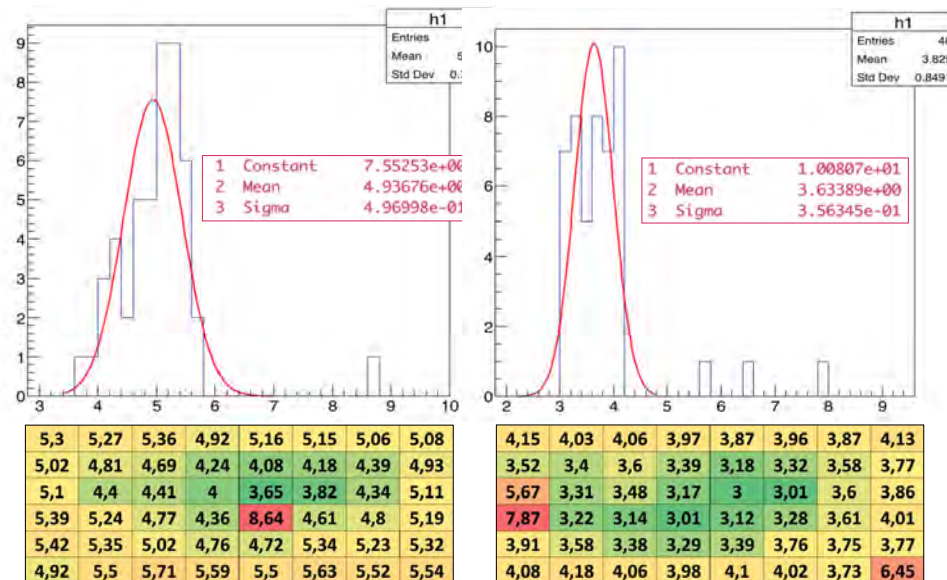
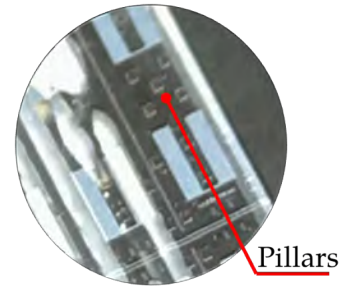


Figure 6.16: Capacitance distribution of two samples assembled with pillars. Values are in pF.

The bottom plots shows that the pillars help to centralize the capacitance gradient over the capacitor array. It is possible to see on the

capacitance histogram for the two samples that the capacitance deviation σ is about two times smaller than without pillars. The calculated RSD is 9.8% for the first sample and 10% for the second, showing an improvement with respect to the samples without pillar.

Even with a smoother gradient (smaller sigma), the center of the test chip still shows a smaller capacitance, indicating a gap $\sim 1 \mu m$ larger between the pads in the center. This bowing effect is expected to come from the large area of the chip ($\approx 2 cm^2$) and a non-optimized gluing recipe.

6.2.2.2 Pillars cross-section measurement

In order to verify the pillars after assembly, a cross-section was done on the bottom row of the first sample (Figure 6.16 right plot) and the gap between the chips was measured using the SEM setup available at CERN. Figure 6.17 shows a SEM picture with a pillar and the capacitor pads in the camera field of view (a) and a detailed zoom at the edge of the capacitor pads (b).

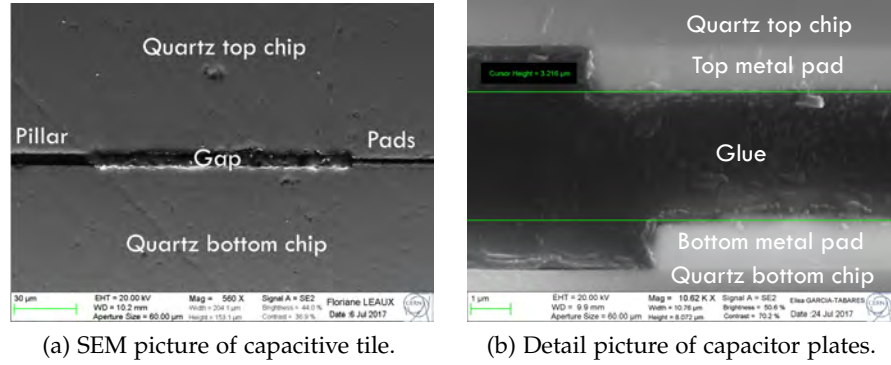


Figure 6.17: SEM pictures of the capacitive tile cross-section.

The gap between the chips was measured along the bottom capacitor row (approximately 2 cm long) and the result is shown in Figure 6.18a. The mean gap measured, $5.11 \mu m$, shows a very good agreement with the height of the pillars measured. Having in mind that with $5.11 \mu m$ between the chips the final distance between the pad surfaces is $2.7 \mu m$, accounting the nominal thickness of $1.2 \mu m$ of

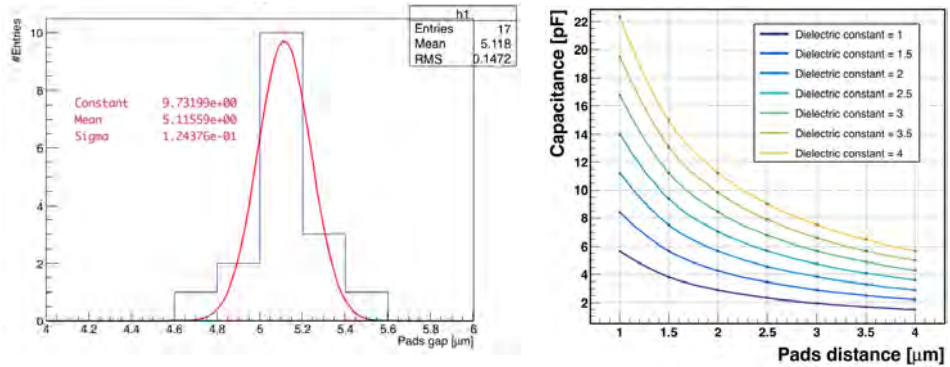


Figure 6.18: Gap measurement and simulation of the capacitance vs gap .

each pad. From finite element simulations of the system (accounting for electric field fringe effects), for such gap of $2.7 \mu\text{m}$ and a nominal glue dielectric constant $\epsilon_{\text{Araldite2011}} = 3.2$, a higher capacitance (~ 7 pF) is expected. Figure 6.18b shows the simulated capacitance *vs* pad distance for different dielectric values.

The pillars have shown to be effective to constrain the gap between the devices to be bonded. Although the test chip has shown to be useful as a simple tool to check the bonding planarity of the flip-chip machine, more work is needed in order to show the coupling homogeneity using this test chip, possibly being achieved with higher bonding force. In addition, with a relative permittivity higher than the glue, one can design the pillars to be used as the dielectric medium between the (pixel) pads, with the glue used as bonding agent.

6.2.3 Glue dielectric constant measurement

Given a dielectric constant of 3.2, the expected capacitance for a gap of $2.7 \mu\text{m}$ is in the order of 7 pF, approximately $2\times$ higher than what was measured. Therefore, the dielectric constant of the glue could be overestimated (what can affect significantly the signal transmission strength in CCPDs).

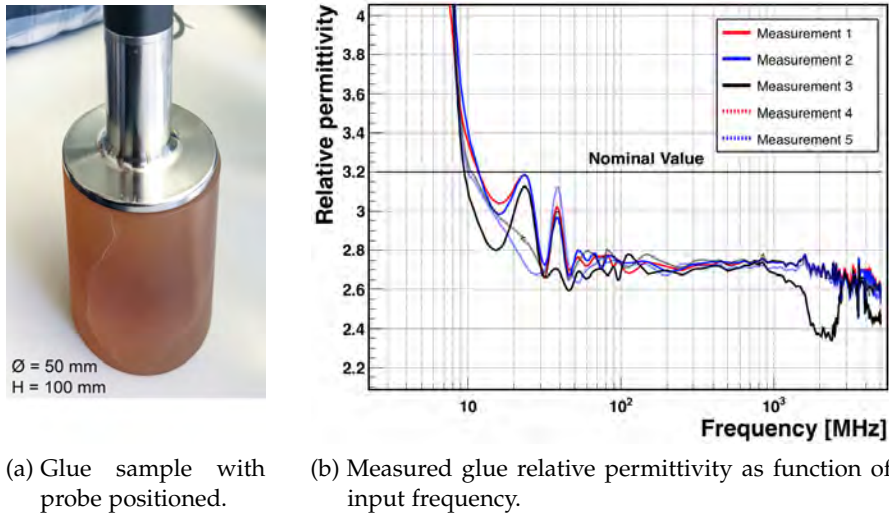


Figure 6.19: Glue dielectric constant measurement.

A preliminary measurement of the relative permittivity of the glue was performed at Speag [135] using a system composed by a vector network analyser and an open-ended co-axial probe [136], with a measurement capability ranging from 10 MHz up to 3 GHz. The probe was manually (by hand) attached to the surface of a cylindrical glue sample (5 cm diameter, 10 cm height and N5 grade surface finish), as shown in Figure 6.19a. The EM fields at the end of the probe penetrate into the material and the reflected signal (S_{11}) can be measured, as function of the signal frequency, allowing the computation of the complex permittivity of the media.

Figure 6.19b shows the resulting dielectric constant measured. The different measurement curves are from different positions of the probe on the sample. The differences between the curves are due to the fact that the probe was not mechanically fixed and, hence, the interface between the probe and the sample was not constant. It is possible to see that the measured value is lower than the one quoted for the Araldite 2011, being in the order of 2.7 at 100 MHz. According to the simulation shown on the previous section, a dielectric constant of 2.7 would yield a coupling in the order of 5.8 pF.

The differences between the results shown here are expected to come from the different frequencies used on each measurement performed and possible glue non-uniformities, such as air bubbles trapped at the chip assembly. In addition, in order to provide a more accurate glue dielectric constant value, a mechanical support for a stable interface between the measurement probe and sample is needed.

6.2.4 Glue dispensing and bonding

The machine operates the dispensing automatically. The three main parameters driving the glue dispensing are the diameter of the dispensing tip, the air pressure applied on the syringe, and the time during which the pressure is applied.

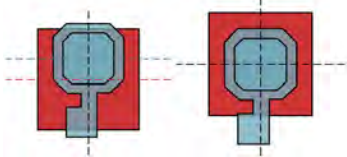
Depending on the desired glue pattern to be applied, these parameters must be adjusted as function of the dispensing movement. In addition, other parameters are available for better dispensing process control, such as: the delay between the start of the dispensing and the start of the pattern movement, and the same for the end; and the time delay before returning the dispensing needle to the idle position after releasing the pressure.

Typical values used for the CCPD production are: 3cc syringe with 600 μm tip; 4 bar of pressure; 2000 $\mu\text{m}/\text{s}$ travel speed while dispensing, or a stationary dispense for 500 ms; and 2000 ms for idle position return. The glue used for the coupling is the Araldite 2011 Epoxy Resin [137]. Once it is placed on the syringe it is centrifuged for about 3 minutes at 5000 RPM to remove possible trapped air bubbles.

The CLICpix and CCPDv3 were coupled together by depositing a single glue dot on top of one of the chips and bringing the other into contact with a force equivalent to 500g and a temperature of 100°C applied for 6 minutes.

Regarding the alignment between the CLICpix and CCPDv3 chips, two possible alignment types are possible, designed in order to investigate the signal transmission. The figure in the left margin illustrates the CLICpix (blue) and the CCPDv3 (red) pads aligned in the so-called *pad+via alignment* (left) and on the *pad alignment* (right), where the center of the passivation opening in the CLICpix pad, is centred with the CCPDv3 pad.

CLICpix and CCPDv3 in the Pad+via alignment (left) and in the Pad alignment (right)



Cross-section measurements of the detector assembly were done, by the CERN EN-MME-MM group, using a scanning electron micro-

scope (SEM). The measurements revealed a glue layer thickness of about $0.2\ \mu\text{m}$. The total distance between the CCPDv3 and CLICpix pads includes also the passivation layers of the respective devices. Figure 6.20 shows a cross section picture of one of the assemblies.

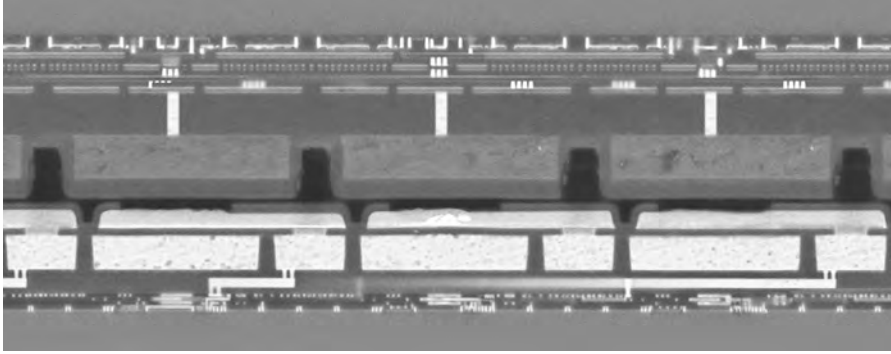
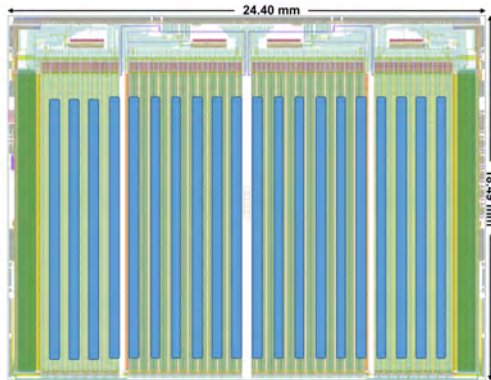


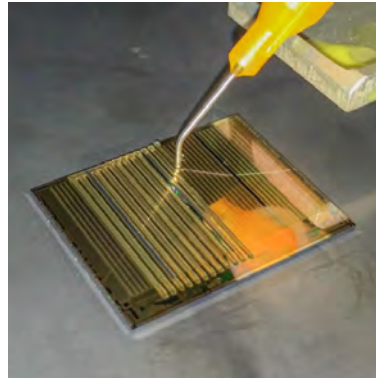
Figure 6.20: SEM picture of a CCPDv3 and CLICpix cross-section.

The top chip in the picture is the CCPDv3, and the bottom is the CLICpix. The chips were arranged in the pad alignment way and the SEM picture shows a shift of about $1\text{--}2\ \mu\text{m}$ from the target position. Simulations using finite element method (FEM) were performed in order to quantify the effect of the flip-chip precision in the pixel coupling and results will be shown in Chapter 7.

For the H35DEMO/FE-I4 coupling a pattern with 40 continuous lines of glue is used, one line for each pixel double column as shown in Figure 6.21a. Figure 6.21b shows the glue being automatically deposited on the H35DEMO. Figure 6.22a shows the glue line deposited along the H35DEMO double pixel column (for the picture, part of the column was left without glue for better visualization).



(a) Designed pattern on H35DEMO.



(b) Glue deposition on chip.

Figure 6.21: Glue pattern on H35DEMO.

For the C3PD/CLICpix2 assembly 5 dots of glue were placed on the C3PD, one on each chip quadrant and one in the center. Using 4 bar and 500 ms dispensing a glue dot between 600 and $700\ \mu\text{m}$ diameter, shown in Figure 6.22b, was consistently achieved (having

in mind that as the glue goes through curing at room temperature higher pressures are needed to achieve the same glue dot diameter).

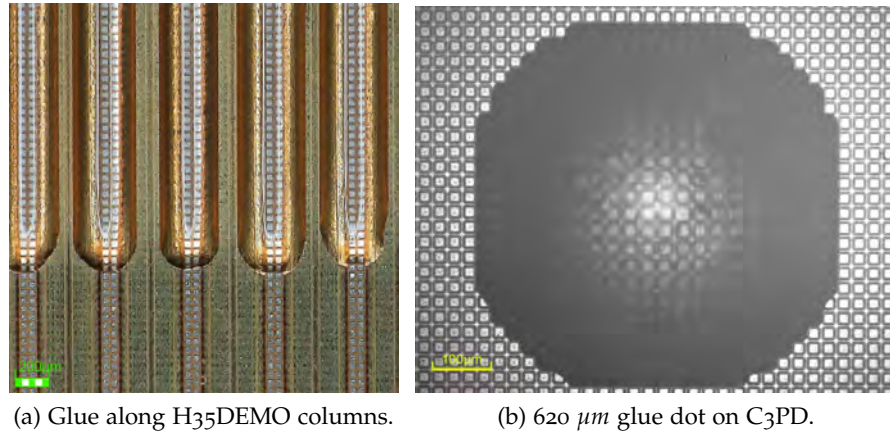


Figure 6.22: Pictures of glue deposited on chip.

The properties of the Araldite 2011 play an important role for the dispensing and the coupling. The higher viscosity of $30\text{--}45\text{ kgm}^{-1}\text{s}^{-1}$ at 25°C , when compared to the Araldite 2020 with viscosity of $0.15\text{ kgm}^{-1}\text{s}^{-1}$, makes the glue spread over the pixel matrix to be contained within the topology of the chip surface, avoiding the glue to overflow at the chip edges and gluing it to the machine chuck.

After checking that the alignment is kept after the glue deposition, both device chips are brought into contact by the controlled movement of the Z-arm. The flip-chip machine has a feedback system to measure the contact force on the Z-arm, upon contact with the chuck, and control its position with a resolution of $0.01\text{ }\mu\text{m}$, accurately maintaining the bonding force set for the process.

Different forces are applied depending on the size of the device to be bonded. The C3PD/CLICpix2 bonding was done with a force of 0.5 kgf , while 2 kgf was used for the larger H35DEMO/FE-I4 CCPD. In addition, different temperatures can be used depending on the desired curing of the glue. The quoted Araldite 2011 curing time is 6 min at 100°C (yielding a lap shear strength $> 1\text{ N/mm}^2$). After gluing trials the process converged to a first fast curing (2-3 minutes at 100°C) while the bonding pressure is applied on the chips, followed by a final curing (2-3 minutes at 150°C) with the pressure released. This recipe allows the recovery of the assembly if it gets glued to the machine during process, while assuring a good initial bonding.

Cross-section pictures, such as the one shown in Figure 6.20 and 6.23, show that the coupling distance between the pixel pads ranges from $0.2\text{ }\mu\text{m}$ up to $5\text{ }\mu\text{m}$, depending on the bonding pressure applied. Figure 6.23 shows the cross-section pictures of a mechanical dummy produced by gluing 2 H35DEMO devices together in order to test the sample planarity over large regions. The assembly regions shown on the left and right pictures are about 2 cm away and the gap measurement along the cross-section shows a good assembly parallelism, with less than 100 nm difference between the extremities, correspond-

ing to an angle of $\sim 5 \mu\text{rad}$. Finally, the strength of the coupling will depend on the alignment and distance between the pixel pads and the dielectric constant of the glue.

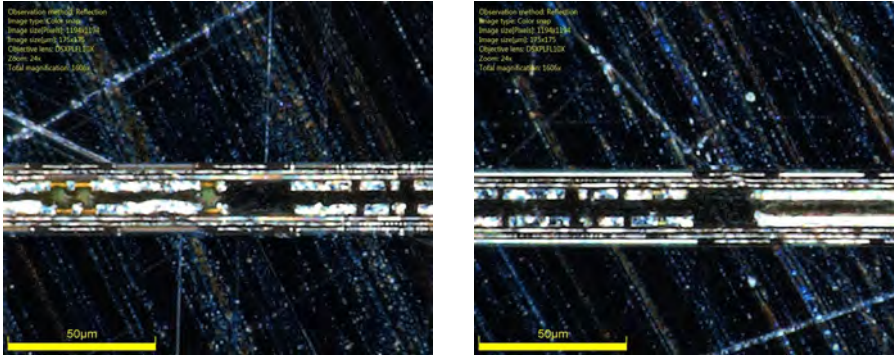


Figure 6.23: Two cross-section measurements of two H35DEMO coupled together, 2 cm apart, with a gap difference smaller than 100 nm.

6.3 CARIBOU READ-OUT SYSTEM SETUP

Once the detector prototype to be tested is selected from the wafer, and after the flip-chip is done if it is a hybrid, the last step before testing the detector is to wire-bond it to its respective carrier board and integrate it to a DAQ system.

As several prototypes are to be tested, an effort was made in order to design a modular system that can supply all resources needed for the operation of different DUTs (device under tests), minimizing the work on design revision for different sensors. The system, named CaRIBOu (Control and Read-out for ITk Board) [138][139], was developed in a collaboration between Brookhaven National Laboratory, Geneva University and CERN. It is an open-source DAQ system, comprehending software, firmware, and hardware, shared through a Gitlab repository [140]. The target applications include the read-out of test assemblies for the ATLAS ITk upgrade and for the CLIC pixel detector R&D.

The hardware configuration used in the CaRIBOu system is composed of: the commercial Xilinx System-on-Chip (SoC) ZC706 Evaluation Kit [141], which contains the Zynq-7000 FPGA and a dual core ARM Cortex-A9 core processor accessible via a Gigabit Ethernet interface; the Control and Read-out (CaR) board, responsible for driving the power and signals to/from the DUT; and the respective DUT chip board, hosting the detector itself.

The non-hardware part of CaRIBOu consists of 3 components: a DAQ software framework (Peary), which runs on a customized full Linux distribution (Meta-caribou) hosted on the ARM processor, and the FPGA image (Peary-firmware). The main advantage of Peary is its user-friendly hardware abstraction layer, which translates the software requests to various Linux device driver calls, enabling the control of the CaR board and the prototype chips. The Peary framework

Xilinx ZC706 SoC



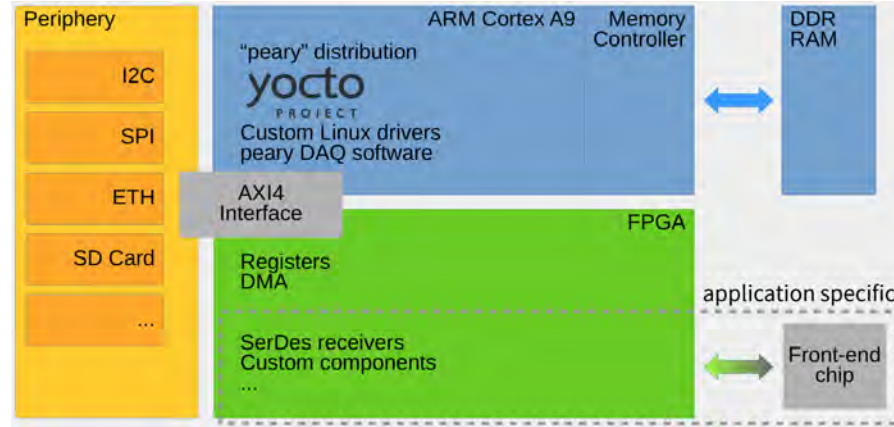


Figure 6.24: CaRIBOu framework system layout.

provides a command line interface enabling sequential step-by-step control of the chip, which is useful at the commissioning stage of new devices.

The CaRIBOu Figure 6.24 shows a block layout of the different system components. In orange the high level functionalities of the ZC706 are listed, such as support for I²C and SPI protocols or SD card interface. The Meta-caribou operational system, hosting the Peary DAQ software, runs on the ARM processor (in blue). The FPGA, in green, runs the firmware responsible for driving the control signals to the CaR board and receives the data from the detector, decodes and sends it to the processor for analysis and storage.

The CaR board, designed to be compatible with different detector requirements, possess a long list of resources for detector operation, supporting different voltage levels, communication standards, and local measurement capabilities. The resources include: 8 general purpose power supplies (0.8 - 3.6 V, 3 A max) with voltage/current monitoring; 8 SERDES (serializer-deserializer) links; 16 channel ADC (65 MSPS/14-bit); 4 charge injection channels; clock generator; general CMOS signals (10x outputs, 14x inputs) and 17x LVDS pairs.

While the first CaR board v0 was designed to test the CCPDv4 prototype, testing up to two devices simultaneously, the later prototypes (H35DEMO, ATLASpix and CLICpix2/C3PD) have been tested with the CaR board v1.x. Both CaR boards are shown in Figure 6.25.

The chip board is specific for each DUT, containing the wire-bonding pads to send/receive the signals to/from the detector chip, and power the device. Having in mind the resources available from the CaR board, the chip carrier board is designed to contain minimum functionalities. Figure 6.26 shows two CCPDv4 chip boards (connected to the CaR board v0), on the left picture, and an H35DEMO chip board connected to the CaR board v1.0 (on the right).

The CCPDv4 and H35DEMO prototypes were read-out by the FE-I4 ROC and, therefore, the read-out of these two detectors was not done by the CaRIBOu system but by the same system used to read-out the planes of the particle telescope used to test these DUTs, con-

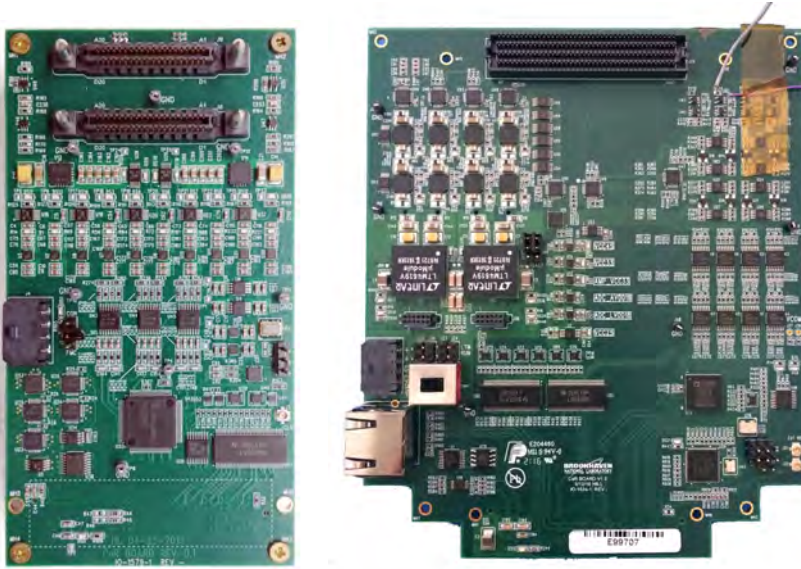


Figure 6.25: CaR board version 0 (left) and 1.x (right).

veniently having the DUT data already integrated with the raw track data. The CaRIBOu system was only used to configure these two HV-CMOS prototypes, although it also offered the possibility to configure and read-out the FE-I4 ROC. Therefore, in addition to the routing of the signals between the chip and the CaR board (with a few test points on the way), these boards contained an Ethernet connection for the 3 LVDS signals for the FE-I4 operation.

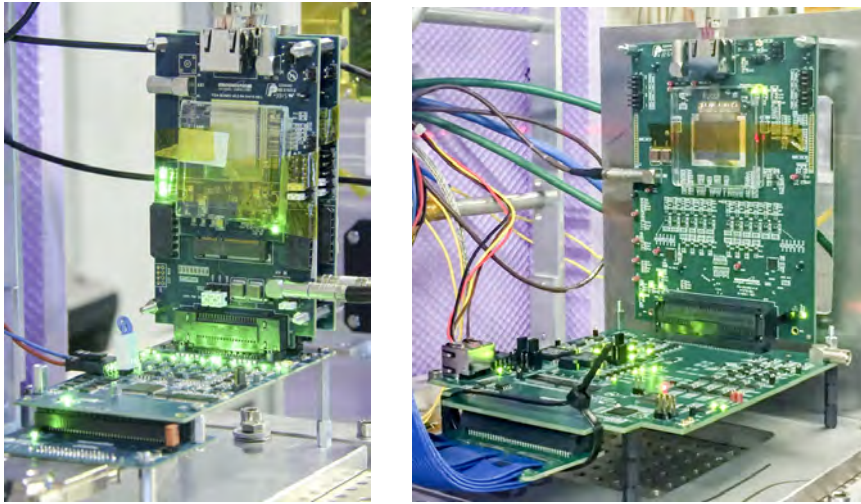


Figure 6.26: CCPDv4 (left) and H35DEMO (right) DUTs on chip board during test beam.

6.3.1 Detector read-out and slow control implementation.

The latest two prototypes are the hybrid CLICpix2-C3PD and the monolithic ATLASpix detector. These two detectors are fully controlled by the CaRIBOu system and, therefore, their implementation with the system will be described in more detail.

CLICpix2 uses CML (current-mode logic) signals for configuration and read-out. The interface of these signals with the DAQ system is done via CML-LVDS converters present on the chip board. For the slow-control of CLICpix2 a Serial Peripheral Interface (SPI) bus is used, running at 100 MHz, where the FPGA acts as the master device, generating the frame for writing/reading, while the CLICpix2 acts as the slave device. The registers written by the SPI commands are used by the periphery DACs to control the various biasing voltages and currents.

The CLICpix2 read-out uses an 8b10b encoded output based on the Ethernet protocol, running on a 640 Mbps SERDES link. This choice allows clock recovery from the data, besides achieving data DC balance and bounded disparity. When no data is output from the chip, a sequence of the Ethernet idle packets is sent to allow the Phase-Locked Loop (PLL) of the DAQ to lock on the data, keeping the DAQ system in phase with the chip clock.

The C3PD configuration interface is based on an I²C bus interface, which provides 2-way communication with only 2 digital signals (a serial data line and a serial clock line). Therefore, only power supply voltages and the two digital lines have to be provided, allowing to control and configure all features of the chip.

The ATLASpix simple prototype uses CMOS and LVDS signals for communication. The configuration of the DAC values is done via shift registers. The ATLASpix read-out is controlled by the Digital-Control-Unit (DCU), responsible for generating and formatting the hit information from the pixels, and finally sending it out of the chip for read-out.

The data formatting block receives the hit data from the in-chip state machine, performs an 8-bit to 10-bit encoding (as the CLICpix2), and transmits the data serially. The chip contains a PLL with an input clock of 160 MHz, generating an output clock of 800 MHz. The serializer transmits a bit on the rising and the falling output clock edge, which leads to a maximal data rate of 1.6 Gbps. The readout block generates the signals for the readout of hit information, transmitting the hit data on a single 1.6 Gbps serial link using the Aurora 8b10b protocol, supported natively by the DAQ FPGA.

Part III

RESULTS AND CONCLUSIONS

In this final part the results of simulations and measurements are shown.

In Chapter 7, the coupling capacitance between the pixels in CCPDs, as function of the gap between the chips or as function of possible horizontal misalignments, is shown and the effect of pixel pads guard-ring is also investigated. The simulation of CCPDs, using the results from the pixel coupling simulation, was implemented via the addition of a new module to the AllPix² framework and is discussed in Section 7.4. The simulation is further compared with data from test-beam measurements. Concluding the Chapter 7, a new tool used to implement results from TCAD simulations into the AllPix² framework is shown.

Chapter 8 shows an introduction to the beam-lines used for the test-beam measurements, together with a description of the used UniGE FE-I4 beam telescope and the Proteus track reconstruction software.

Finally, Chapter 9 contains results obtained for the tested HV-CMOS prototypes during the test-beam campaigns, before and after irradiation.

My direct contributions for this part of the thesis are on the simulations and tools developed and described in Chapter 7; on the improvements to the FE-I4 telescope and support for the telescope users mentioned in Chapter 8, as well as testing and contributing to the development of the Proteus framework; and the preparation (such as tuning and calibrations) of the prototypes tested in Chapter 9, together with the reconstruction of the tracks and analysis of the detector performance.

7.1 PIXEL COUPLING SIMULATION

The extraction of parasitic circuit models is important for various aspects of design verification such as signal timing and integrity and substrate coupling. Being able to predict the cross talk between different circuit components is an important step in evaluating how well a design will meet the performance specification. As electromagnetic behaviour is governed by Maxwell's equations, parasitic extraction can be done by solving the Maxwell equations.

COMSOL Multiphysics [142] is used in this work to solve the differential form of Maxwell's equations, together with a set of initial and boundary conditions, using the Finite Element Method (FEM), and post-process the results to calculate derived quantities, such as capacitances. COMSOL here is used as an electromagnetic field solver software. Field solvers provides a solution from first principles with high accuracy results.

A field solver is a tool that solves the Maxwell Equations for a specific geometry and a set of boundary conditions of the respective conductors and dielectric materials. The equation that is solved for the calculation of the electric fields at every point in space is the LaPlace Equation. In its simplest differential form, it is written as

$$\nabla^2 \varphi = 0 \quad (7.1)$$

The uniqueness theorem assures that, giving a set of boundary conditions provided for the LaPlace equation, the solution calculated is the only one possible to exist.

If the geometry of the object is complex, without any symmetry and edges for example, solving the entire object without dividing it into smaller pieces can be impossible, as holes, corners and angles can make it extremely difficult for solvers to obtain a solution. Therefore, the discretization (meshing) of the domain, in which the electromagnetic fields reside, is required. Small cells, called finite elements, are comparably easy to solve and therefore the preferred strategy. Each cell of the mesh represents an individual solution of the equation, which, when combined for the whole object domain, results in a solution for the entire mesh.

The FEM generates a linear algebraic system (matrix) that must be solved. The resulting matrix is usually large and sparse (contains very few non-zero entries) and sparse linear solution methods, such as sparse factorization, conjugate-gradient, or multigrid methods can be used to solve these systems, the best of which require CPU time and memory of $\mathcal{O}(N)$, where N is the number of elements in the

discretization. FEM then uses variational methods to approximate a solution by minimizing an associated error function.

In this section the objective is to calculate the cross-coupling between different pixel pads. In order to describe the multiple capacitances present during the sensor and ROC coupling, the Maxwell Capacitance Matrix will be used.

7.1.1 Maxwell's Capacitance Matrix

The Maxwell Capacitance Matrix [143] provides the relation between voltages and charge on a set of conductors. The value of each element in the matrix is a direct measure of the amount of capacitive coupling between two conductors. This will directly determine the capacitively coupled current that would flow between each pair of conductors for a given dV/dt . The larger the matrix element, the larger the coupling, indicating a stronger electric field, and more fringe fields, between the conductors.

The construction of the Maxwell capacitance matrix can be derived by a simple example using 5 conductors, as shown in Figure 7.1. The equivalent capacitance model is drawn in the image on the side.

Equivalent circuit with capacitively coupled conductors. Image from [144]

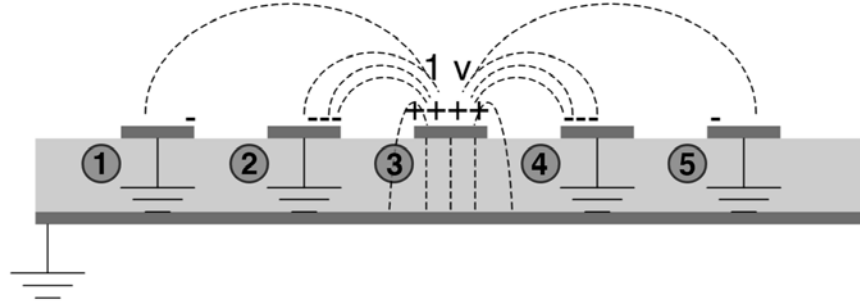
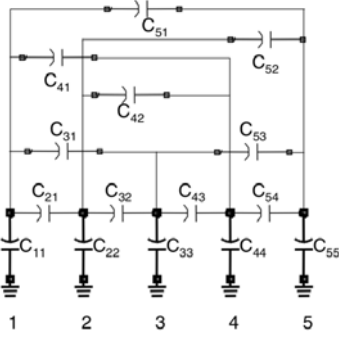


Figure 7.1: Illustration of conductors near each other capacitively coupled. Image from [144].

Having in mind that the charge on a conductor is $Q = C \cdot V$, where C is the capacitance and V is the voltage, the charge Q_i on the conductor i , with the given voltages V_1, V_2, V_3, V_4 and V_5 on the five conductors, can be written as:

$$Q_i = \sum_{j=1}^N C_{ij} V_j \quad (7.2)$$

Choosing the first conductor as an example, it is possible to write:

$$Q_1 = C_{11} \cdot V_1 + C_{12} \cdot (V_1 - V_2) + C_{13} \cdot (V_1 - V_3) + C_{14} \cdot (V_1 - V_4) + C_{15} \cdot (V_1 - V_5) \quad (7.3)$$

which can be arranged as

$$Q_1 = (C_{11} + C_{12} + C_{13} + C_{14} + C_{15}) \cdot V_1 - C_{12} \cdot V_2 - C_{13} \cdot V_3 - C_{14} \cdot V_4 - C_{15} \cdot V_5 \quad (7.4)$$

Therefore, the first element of the capacitance matrix in equation 7.2 can be written as:

$$|C_{11} + C_{12} + C_{13} + C_{14} + C_{15} \quad -C_{12} \quad -C_{13} \quad -C_{14} \quad -C_{15}| \quad (7.5)$$

Completing the same steps for the other conductor indices and further extending the notation for the general case with N conductors, the Maxwell capacitance matrix has the form shown in 7.2.

$$\begin{vmatrix} C_{11} + C_{12} + \dots + C_{1N} & -C_{12} & \dots & -C_{1N} \\ -C_{21} & C_{21} + C_{22} + \dots + C_{2N} & \dots & -C_{2N} \\ \dots & \dots & \dots & \dots \\ -C_{N1} & -C_{N2} & \dots & C_{N1} + C_{N2} + \dots + C_{NN} \end{vmatrix} \quad (7.6)$$

The diagonal elements of the Maxwell capacitance matrix are the loaded capacitances of each conductor, comprising the capacitance to the return path (ground) and to all the other conductors that are also tied to ground. The off-diagonal elements are a direct measure of the coupling between the conductors indicating how much excess charge will be on one conductor when the other is at a fixed potential and all other conductors are grounded. The capacitance between two conductors can be calculated in 6 steps:

1. A fixed potential is set on conductor #*i* and the potential of every other conductor is set to 0 V;
2. Given this boundary condition, LaPlace's Equation is solved to find the potential everywhere in space;
3. The electric field is calculated via the solved potential by $E = -\nabla V$ at the surface of each conductor;
4. The total charge is calculated on each conductor via the Gauss law $Q = \epsilon_0 \oint E dA$;
5. From the charge on each conductor, the capacitance is calculated from the definition of the Maxwell Capacitance matrix, $C_{jk} = Q_j / V_k$;
6. This process is repeated with a fixed potential sequentially placed on each of the conductors;

Suppose a fixed potential is set on conductor 3, by placing extra positive charge on the conductor to raise its potential, while all the other conductors are at ground potential (0 V). This extra positive charge will attract negative charges (coming from the ground) to all the conductors in the vicinity. The amount of charge that is attracted to each conductors is a measure of how much capacitive coupling

there is to the first conductor placed at 1 V. Since the charge induced on the neighbouring conductors is negative, every off-diagonal capacitor-matrix element is also negative.

The greater the spacing between the conductors, the less charge will be induced as the density of the fringe-field lines between the conductors will get lower and, consequently, the coupling capacitance will be smaller. In addition, the physical presence of any conductor between two pads will affect the field lines between them. This will reduce the coupling capacitance and this effect is the basis to the use of guard-rings, discussed in detail later in this chapter.

7.1.1.1 The energy method for the capacitance calculation

COMSOL makes use of the 6 steps mentioned previously in order to calculate the Maxwell capacitance matrix, with a slight modification for step #4. Instead of using the integral of the calculated electric field to extract the charge surface distribution on the capacitor terminals, a method based on evaluation of total electric energy stored in dielectric space around the capacitor, named Stored Energy Method [145], is used by COMSOL.

The equation for the electrostatic potential energy U of a continuous charge distribution, induced from a field E in a volume v is (in the approximation of a parallel plate capacitor):

$$U = \frac{1}{2}\epsilon \int_v |E|^2 dv = \frac{\epsilon}{2}|E|^2 A \cdot d \quad (7.7)$$

where dv is the differential volume element, ϵ is the permittivity of the material in which the electric field extends, A and d are the area and distance between the capacitor terminals. Using equation 7.7 and the relation $C = Q/V = \epsilon A/d$, it is possible to rewrite equation 7.7 as

$$U = \frac{QV}{2} = \frac{CV^2}{2} \quad (7.8)$$

Finally, the capacitance can be derived from the calculated stored energy as

$$C = \frac{2U}{V^2} \quad (7.9)$$

7.2 CAPACITANCE SIMULATION WITH COMSOL

7.2.1 Simulation workflow

For the COMSOL simulation, the workflow is as follows. First the geometry of the chips are defined; materials are assigned to the domains of the model; a *Physical Interface* is chosen with the model's respective boundary and initial conditions; the model mesh is created; a solver is selected and subsequently the results are computed. In COMSOL, all these steps are accessible from the same graphical user interface.

The Physical Interface provides the set of partial differential equations, such as Maxwell's equations and material laws, with the corresponding initial and boundary conditions, to be solved. A mesh is defined to divide the volume of the model into discrete parts where the equations will be computed. After the calculation for the mesh elements, the results are interpolated over the volume.

7.2.2 Geometry and material definition

A 3D model of the detector assembly was created using SolidWorks [146]. A matrix of 3x3 pixels was created for each chip, based on their GDSII¹ design files. Each matrix was created as a SolidWorks Part. Figure 7.2 shows the SolidWorks model of the CLICpix ROC.

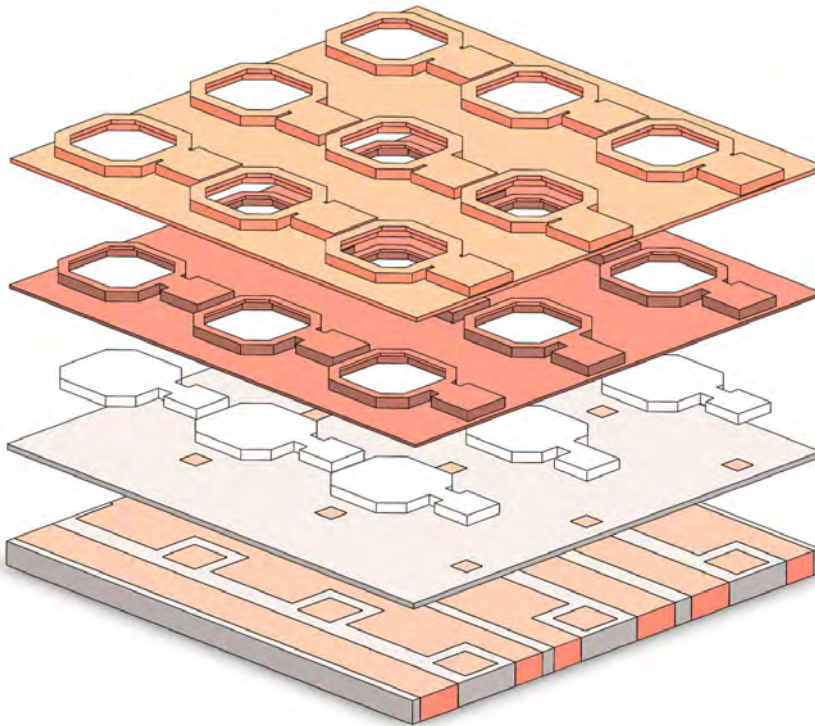


Figure 7.2: CLICpix geometry from SolidWorks. The exploded view shows the 2 passivation layers on the top, the pixel pads, the oxide layer with the pad vias, and the layer with the signal routing metal lines.

The thickness of the different chip layers was extracted from the technology process manual used for each chip. Both ROC and sensor chip use two passivation layers after the pixel pads (last metal layer) and, on the ROC, the passivation has an opening so it can also be bump-bonded to sensors. In the ROC, the metal layers containing the signal routing were also included in the model, in order to extract possible parasitic capacitances/loads for the sensor pixel output cir-

¹ Graphical Design Station II. Industry standard format file for data exchange of integrated circuit layouts.

cuitry. The oxide layers, responsible for isolating the metal layers, are also included in the model. Figure 7.3 shows the assembly model of the CLICpix together with the CCPDv3.

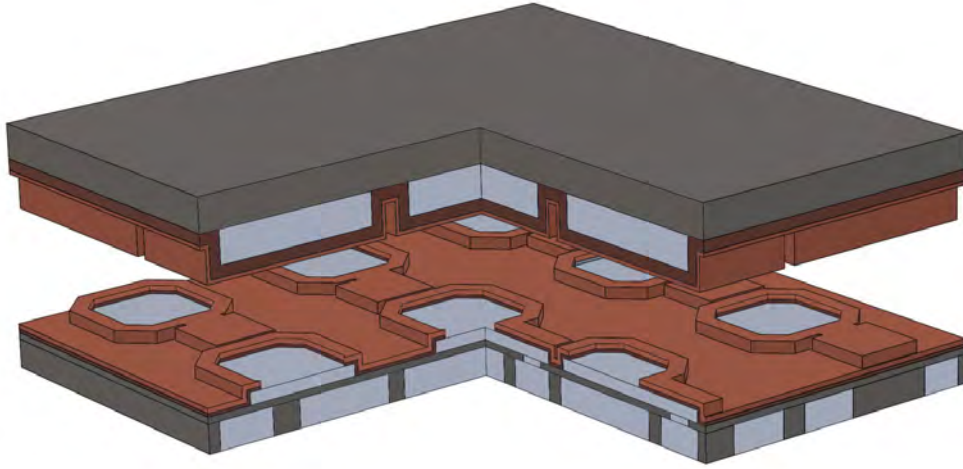


Figure 7.3: CLICpix (bottom) and CCPDv3 (top) assembly.

It is possible to import 3D CAD² files into COMSOL. Therefore, the last remaining step is to create the missing epoxy glue layer that will fill the gap between the two chips. It is easier to model the glue layer with COMSOL, as it offers some basic CAD tools such as boolean operations (difference or intersection for example) between different parts of the geometry. Therefore, the glue layer is defined by the volume surrounding both chips minus the volume of the chips.

After the geometry is created, a material is assigned to each volume of the model, so that the corresponding material properties, such as the dielectric constant, are taken into account (in the electric field calculation, for example). The materials used in the model are Aluminium for the pixel pads and metal lines + vias; silica glass for the material between the metal lines and between the metal layers; epoxy resin for the glue layer and SiO₂ and Si₃N₄ for the passivation layers.

In reality only the pixel pads are made of Aluminium, with the other metal lines and vias being made of copper. As the pixel pads and metal lines have no electric field in their interior, the different dielectric properties of Aluminium and Copper have no impact on the capacitance calculated. The volume inside metal domains does not even need to be modelled or meshed, as it can be defined only by its boundaries conditions on its surface, saving computational power. Hence, Aluminium was chosen to represent all metals to simplify the model. Table 7.1 shows the dielectric constant for the materials listed above.

The dielectric constant of the Araldite 2011 epoxy glue was already discussed in the previous chapter. As the measurement of the relative permittivity of the glue was done after the simulations here described, the ϵ_{glue} value used was extracted from the glue data sheet, which

² Computer Aided Design.

Table 7.1: Dielectric constants used.

Material ID	Dielectric constant	Domains
Aluminium	1.7	Metal pads and lines
Silica Glass	2.09	Insulation layers
Epoxy resin	3.2 (at 10 kHz)[137]	Coupling glue
SiO ₂	4.2	ROC 1 st passivation
Si ₃ N ₄	8.1	ROC 2 nd passivation
SiO ₂	3.9	Sensor 1 st passivation
Si ₃ N ₄	7.5	Sensor 2 nd passivation

quotes $\epsilon = 3.2$ for frequencies higher than 10 kHz. The values for the dielectric constant of the passivation layers were extracted from the process technology manual from each corresponding foundry.

7.2.3 Boundary conditions

For the simulations in this work, the *Electrostatic interface* was used in a *Stationary Study* (time independent) for the capacitance calculation. The interface connects the geometry modelled with the equations of electrostatic physics by assigning the respective Boundary Conditions (BC), such as a specific potential distribution, on the elements of the geometry (points, edges, surfaces or domains).

COMSOL, by default, implements a set of boundary conditions necessary for the integrity of the model, which can be overwritten at any point. These are: *Charge Conservation* over all domains, assuring the continuity of $\mathbf{E} = -\nabla V$ over the full geometry; *Zero Charge*, $\mathbf{n} \cdot \mathbf{D} = 0$, over all boundaries, fixing that no displacement field can penetrate the boundary and that no electric potential is discontinuous across the boundary (this BC is overwritten by any other boundary conditions fixing the potential in a given domain); and, lastly, *Initial Values* setting $V = 0$ over all domains (also being overwritten as the *Zero Charge* BC).

In COMSOL the capacitances are calculated for and between the electrodes defined in the model. Therefore, all pixel pad surfaces are defined with the *Terminal* BC, which sets the electric potential as constant on the respective electrodes, each one being identified by a unique number. Figure 7.4a shows the surfaces of the CLICpix pixel pad (in blue) and the CCPDv3 pixel pad (red), where the *Terminal* BC is applied. In addition, a *Terminal Sweep* is activated in order to loop the excitation (application of a potential or current) over the terminals and, hence, calculate the capacitance matrix elements. Figure 7.4b shows the CCPDv3 pixel pad, for which the coupling capacitances will be calculated, with the respective (neighbouring) pixels in the CLICpix ROC. The *Terminal* BC is also used to model the signal routing metal lines and vias (not visible on the figures), allowing to

compute the additional load that these lines place on the amplification circuit, connected to the output pad of the sensor circuitry.

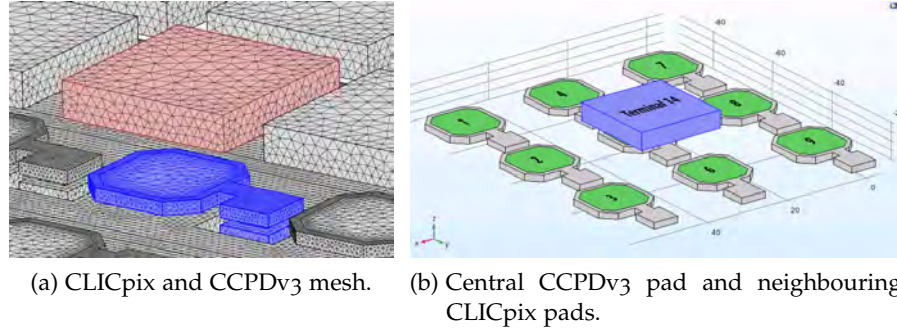


Figure 7.4: CLICpix and CCPDv3 mesh and geometry.

7.2.4 Meshing and solver selection

After the model boundary condition assignment, a mesh of the modelled volume is created, in order to generate smaller domains (or sets of element equations) where the Maxwell equations will be solved. After the calculations for each element, the results are combined into a global system of equations for the final calculation. COMSOL contains advanced automatic meshing algorithms, making it possible to mesh the complex geometric volume with a small set of parameters. The volume was meshed with tetrahedrals with minimum element size of $0.1 \mu\text{m}$, maximum element size of $2.6 \mu\text{m}$ and maximum element growth rate of 1.35 (determining how fast a mesh element can grow from the minimum to the maximum size). An example of a resulting mesh is shown in Figures 7.4a and 7.5. The CLICpix+glue+CCPDv3 ($75 \times 75 \times 20 \mu\text{m}^3$) mesh was created in the order of 1 min.

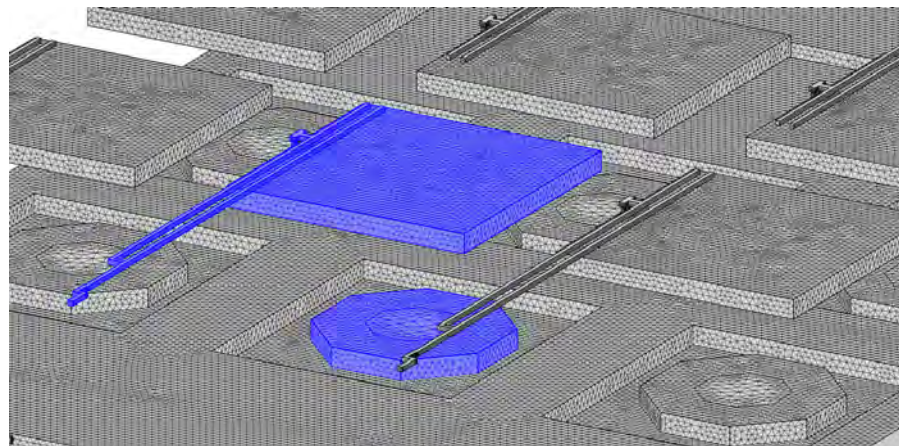


Figure 7.5: Simulation mesh used for H35DEMO (top square pads) coupling to FE-I4 (bottom octagonal pads).

COMSOL chooses automatically a solver sequence based on the physical interface and BCs created, although it is possible to manu-

ally choose the solver to be used. For this simulation, the conjugate gradient method was set automatically, as an iterative algorithm.

7.3 SIMULATION RESULTS

7.3.1 Results for CLICpix+CCPDv3 nominal geometry

The electric field and the energy density are computed over the model and are used to derive the capacitance matrix of the system as described above. The electric field is calculated for each node element of the mesh and interpolated between the nodes such that it is known continuously inside the volume. The norm (or amplitude) of the electric field between the CCPDv3 and CLICpix pixel pad is shown in Figure 7.6. Regions of high electric field are visible in the pad corners. This is a feature of the simulation, as the simulated geometry has sharp edges, while the physical implants have rounded edges.

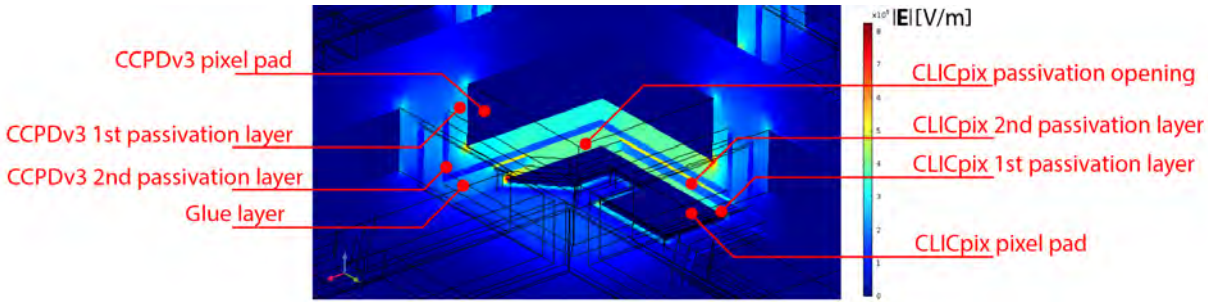


Figure 7.6: Norm of the electric field (in V/m) between pixel pads represented in the color scale.

The calculated capacitance matrix, for a nominal geometry with a $0.2 \mu\text{m}$ gap between the chips, or $3 \mu\text{m}$ between the surface of the pads, is shown in Table 7.2. The terminals 1-9 are the pixels pads in the 3×3 matrix of the CLICpix ROC (first column and row pixel is terminal 1), see Figure 7.4b. The terminals from 10 to 18 are the pixels in the CCPDv3 (enumerated in the same order as the corresponding CLICpix pads). In the following, it will be analysed how the central pixel in the CCPDv3 sensor couples to the directly opposite pixel in the ROC and its surrounding 8 first neighbours. This corresponds to

Table 7.2: CLICpix and CCPDv3 Maxwell's capacitance matrix (values in fF).

	Terminal 10	Terminal 11	Terminal 12	Terminal 13	Terminal 14	Terminal 15	Terminal 16	Terminal 17	Terminal 18
Terminal 1	-3,799489	-0,141598	-0,088012	-0,022053	-0,003152	-4,92E-04	-0,024017	-0,002943	-0,001187
Terminal 2	-0,088664	-3,800048	-0,141603	-4,92E-04	-0,02207	-0,003154	-0,001632	-0,024473	-0,002944
Terminal 3	-0,140576	-0,088654	-3,799223	-0,003152	-4,92E-04	-0,022066	-0,002128	-0,001633	-0,023665
Terminal 4	-0,022141	-0,003153	-4,96E-04	-3,799337	-0,141108	-0,088061	-0,024102	-0,002897	-0,001568
Terminal 5	-4,96E-04	-0,022145	-0,003155	-0,088286	-3,799738	-0,141164	-0,001571	-0,024108	-0,002903
Terminal 6	-0,003155	-4,96E-04	-0,022148	-0,140856	-0,088271	-3,799606	-0,002899	-0,001569	-0,024105
Terminal 7	-0,021495	-0,003069	-3,51E-04	-0,024237	-0,002892	-0,001617	-3,799323	-0,141554	-0,088335
Terminal 8	-4,83E-04	-0,021626	-0,003068	-0,001619	-0,024244	-0,002895	-0,088647	-3,799454	-0,141528
Terminal 9	-0,002226	-4,83E-04	-0,020801	-0,002894	-0,001617	-0,024255	-0,140525	-0,088636	-3,798824

the first 9 rows (9 CLICpix pixels) at the "Terminal 14" column (central CCPDv3 pixel) in the capacitance matrix, as illustrated in Figure 7.4b.

Figure 7.7 gives the coupling capacitance values of the central pixel on the CCPDv3 matrix with the 9 pixels in the ROC. The biggest coupling capacitance is, as expected from the geometry, with the central pixel in the ROC matrix, with a capacitance of 3.80 fF.

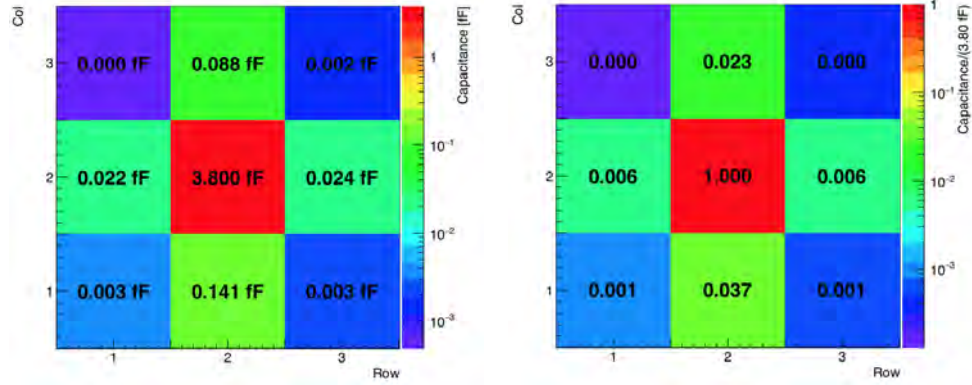


Figure 7.7: CCPDv3 central pixel capacitance with 9 ROC pixels. The right plot is normalized to the closest pair coupling capacitance.

The cross coupling capacitance (coupling with the first neighbour pixel pads) is a value that is interesting to be analysed with respect to the "main" coupling capacitance, as it is important to know the parasitic charge fraction that would be created on the neighbours from a voltage pulse in the sensor pixel pad. Figure 7.7 shows the capacitance values normalized to the main capacitance on the right plot. Only two pixels of the first neighbours obtain a significant fraction of the charge induced in the central pixel. These two neighbouring pixels can see a "parasitic" hit if the charge from the CCPDv3 pixel is high enough.

The coupling with the metal lines is 1.68 fF, or 44%. This high coupling capacitance is due to its area being much larger than the one of the pixel pads, causing a bigger overlap volume with the sensor pixel pad. This capacitance represents an additional load on the amplifiers inside the CCPDv3 pixels that must be taken into account during circuit design.

The geometry of the pixel pads leads to an asymmetric cross coupling with the neighbouring pixels. The CLICpix pixel pad has a rectangular aspect ratio. Therefore, the lateral pixels (1, 2, 3, 7, 8 and 9) have a much smaller capacitance than pixels 4 and 6. The asymmetry in the vertical axis causes pixel 6 to have a capacitance 1.6 times larger than pixel 4. This asymmetry in the cross coupling was observed in testbeam data [75].

7.3.2 Results for FE-I4+H35DEMO

The same simulation was also performed to evaluate the coupling between the pixels in the H35DEMO HV-CMOS sensor to the FE-I4 ROC. The geometry used is shown in Figure 7.8.

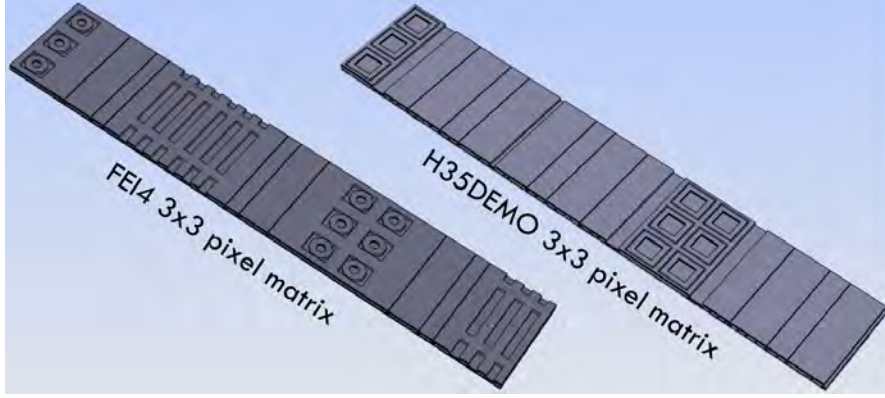


Figure 7.8: FE-I4 (left) and H35DEMO (right) 3D geometry model.

The size of the H35DEMO coupling pad is $36 \times 36 = 1296 \mu m^2$, while the FE-I4 has an octagonal pad with $528 \mu m^2$. As the H35DEMO and FE-I4 pixels are organized in double columns, there will be a column of pixels that will be away approximately 2x the pixel pitch, reducing significantly the coupling. Figure 7.9 shows the electric field norm and the field lines between one pixel on the H35DEMO and the closest pixels on the FE-I4.

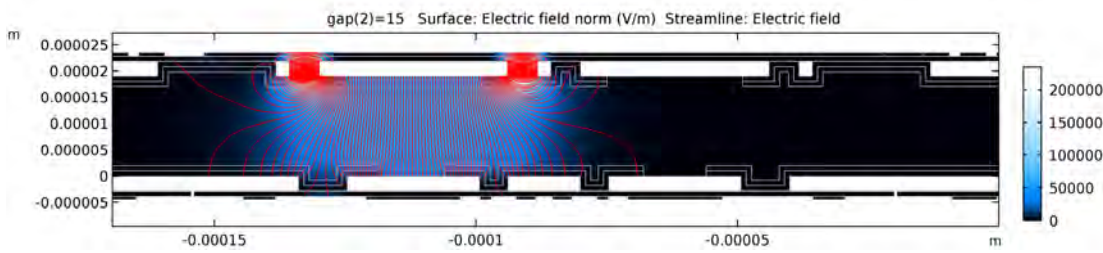


Figure 7.9: Electric field norm and field lines between H35DEMO (top) and FE-I4 (bottom) pixel pads for a gap of $15 \mu m$ between the chips.

The calculated capacitances are shown in Figure 7.10 for a gap of $1 \mu m$ between the chips. Accounting the thickness of the passivation layers of both chips, the surfaces of the pixel pads are $5 \mu m$ apart. The capacitance between the closest pixel pair is 3.93 fF . As the H35DEMO and FE-I4 pixel pads are larger, when comparing with the CLICpix and CCPDv3 pads, even with the larger gap between the chips, the coupling capacitance is comparable to the coupling between the CLICpix and the CCPDv3 pads. Due to the larger pixel pitch, the largest cross coupling is only 0.004% .

7.3.3 Dependence on the glue layer thickness

7.3.3.1 CLICpix+CCPDv3 results

The thickness of the glue layer, and consequently the distance between the pads, depends on the parameters of the flip-chip bonding process. Hence, it is important to know how the coupling capacitance changes with the distance between the pixel pads. The same simu-

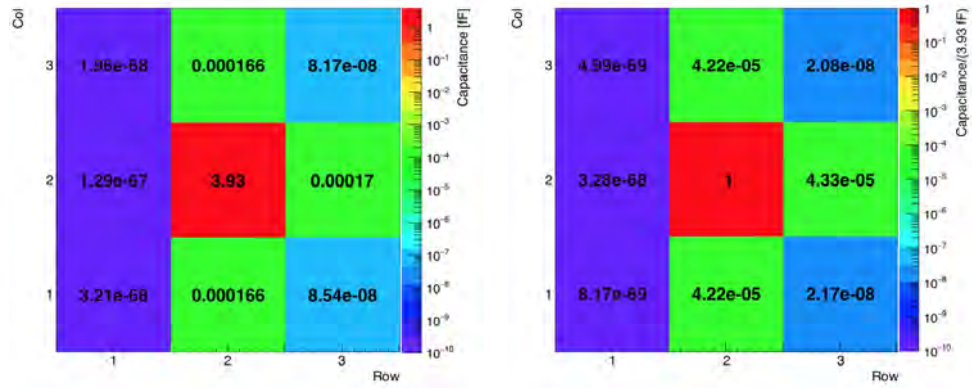


Figure 7.10: H35DEMO central pixel capacitance with 9 ROC pixels. The right plot is normalized to the closest pair coupling capacitance.

lation, as described above, was repeated while changing gradually the distance between the chips, using the *Parametric Sweep* feature of COMSOL. The distance between the pixel pads was changed from 3 up to $100 \mu\text{m}$, in steps of $1 \mu\text{m}$. The resulting pixel capacitances are shown in Figure 7.11 as function of the distance.

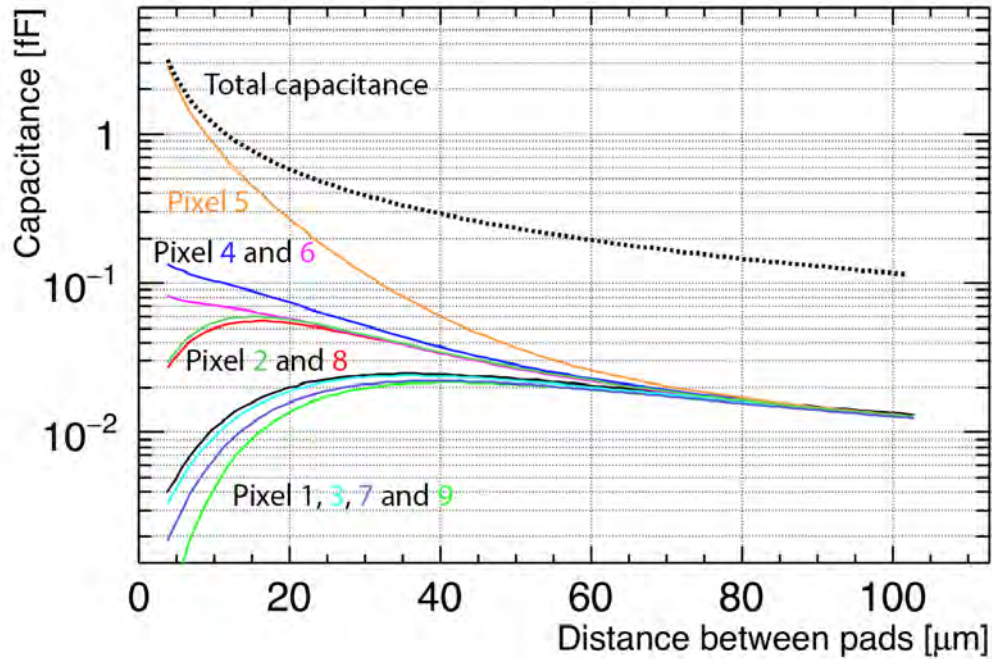


Figure 7.11: CLICpix+CCPDv3 coupling capacitances as function of the pads distance.

As the distance increases, it is expected that the capacitance between the CCPDv3 pixel to the pixels on the CLICpix will decrease in absolute value, as its seen in Figure 7.11. The relative difference between the capacitance to the closet pixel on CLICpix and its neighbours get smaller, as the capacitance to the closest pixel is proportional to the gap between the pixel pads (called Z) and the capacitance to the neighbouring pixels are proportional to $Z/\sin\theta$, where $\lim_{Z \rightarrow \infty} \sin\theta = 1$ and when all capacitances are comparable.

In Figure 7.11 it is possible to see that with a $40\text{ }\mu\text{m}$ gap, the main coupling decreased by about two orders of magnitude, being about two times higher than the coupling to neighbouring pixels, instead of 25-50 times when compared with at nominal gap of $3\text{ }\mu\text{m}$. It is also possible to see that for a typical gap between sensor and ROC in bump-bonded hybrid detectors ($\sim 20\text{ }\mu\text{m}$), the capacitance to the closest pixel drops by about one order of magnitude while for 6 neighbouring pixels the absolute value of the capacitance increases.

This effect is due to the complex 3D geometry of the pixel pads. When the pixel pads are close to each other, part of the neighbouring pixel pads in the CCPDv3 chip and the adjacent CLICpix pixel pads act as a shield for the electric field, reducing the cross-coupling to the peripheral pixels in the CLICpix. For small distances and as the chips move apart, the surface overlap between the pixel pads increases and, consequently, the shielding part of the pads gets smaller. This allows more field lines to reach the peripheral pixels, as shown in Figure 7.12, increasing the capacitance up to the point where the contribution of the larger overlap is counterbalanced by the larger distance, when the capacitance starts to decrease.

This hypothesis was confirmed by a 2D simulation where the neighbouring pixels in the CCPDv3 chip were removed. More details can be found in [147].

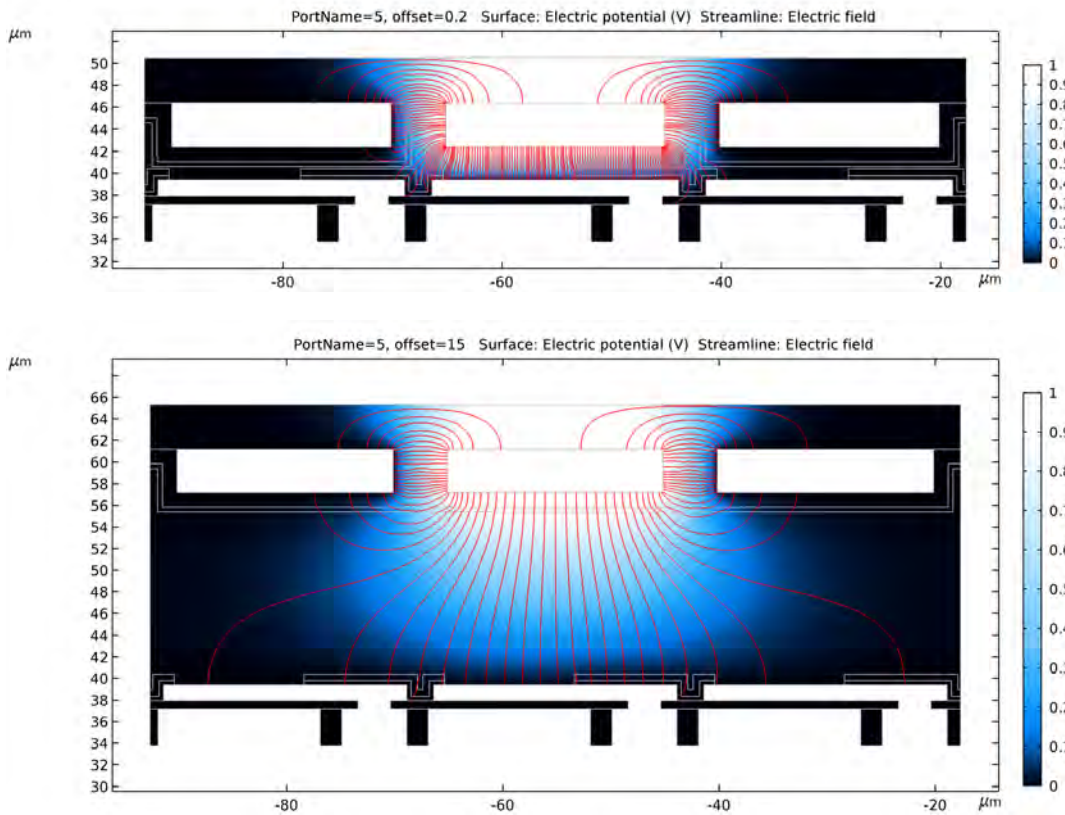


Figure 7.12: Electric field lines for different gaps between the chips. As the distance increases from $0.2\text{ }\mu\text{m}$ (top image) to $15\text{ }\mu\text{m}$ (bottom), more fields lines reach the neighbouring pixels, increasing their coupling capacitances.

7.3.3.2 H35DEMO+FE-I4 results

The dependence of the coupling between the H35DEMO and FE-I4 on the thickness of the glue layer was also simulated and the result is shown in Figure 7.13. It shows the same behaviour where the coupling to neighbouring pixels increases as the gap between the pads gets larger. Due to the larger pixel pads and pitch, in contrast to CLICpix/CCPDv3, where the cross coupling increases up to the gap $\sim 20 \mu\text{m}$, the cross coupling between H35DEMO and FE-I4 increases up to about $40 \mu\text{m}$.

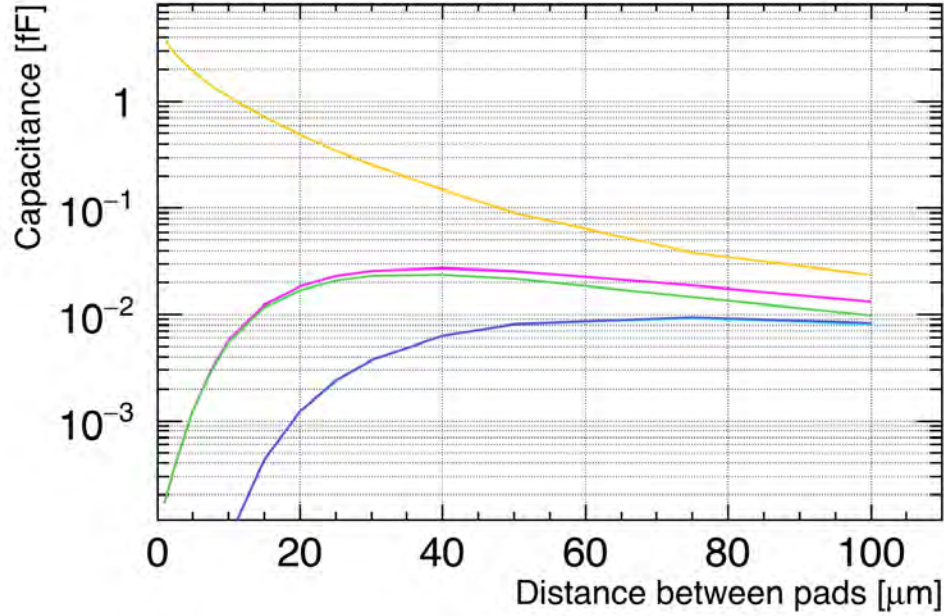


Figure 7.13: Coupling capacitances on the H35DEMO+FE-I4 for different gap distances between the pixel pads.

7.3.4 Effect of the flip-chip precision on pixel coupling for CCPDv3-CLICpix

In order to visualize the effect of the two-dimensional position uncertainty that comes from the flip-chip precision, the simulations described above were repeated in a 2-dimensional scan going from -2 up to $2 \mu\text{m}$, in the row and column directions, creating a measurement plane with respect to the nominal "pad+via alignment" ($X=Y=0$ position). The gap used between the chips was 200 nm . Figure 7.14a illustrates the CCPDv3 pixel pad in the "pad+via alignment" and with the CCPDv3 pixel pad shifted $-2 \mu\text{m}$ in the X direction and $-1 \mu\text{m}$ in the Y direction. The inner segmented square represents the points where the CCPDv3 pixel pad was simulated with respect to the CLICpix pixel pad. Each point represents one bin in the 2D histogram in Figure 7.14b.

Figure 7.16b shows the simulated capacitance for each position of the 2D scan. The simulation shows that in the worst simulated alignment case ($+2 \mu\text{m}$ in X and Y), the coupling capacitance decreases by

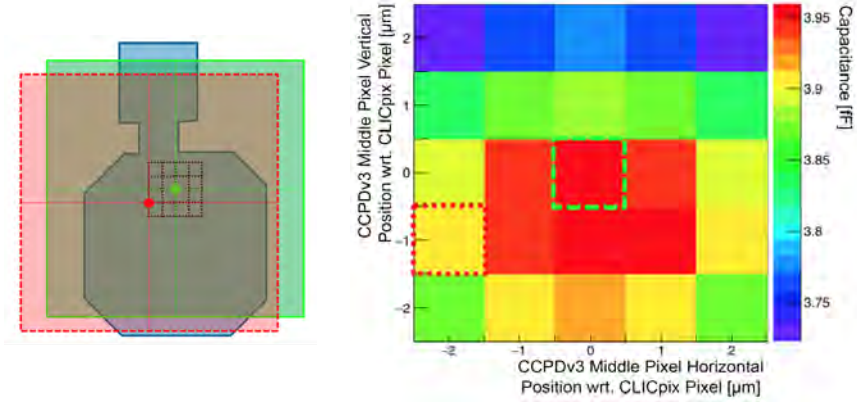


Figure 7.14: CCPDv3 central pixel capacitance with 9 ROC pixels. The right plot is normalized to the closest pair coupling capacitance.

about 200 aF, or $\sim 5\%$. The asymmetry in the vertical direction is due to the shape of the CLICpix pixel pad.

The effect of the uncertainty on the position of the CCPDv3 pixel can also be calculated for the neighbouring pixels in the CLICpix chip, as in the previous simulations, in order to understand the global effect of the alignment precision on the cross-couplings. Figure 7.15 shows the coupling capacitance of the 9 CLICpix pixels with the central CCPDv3 pixel in the 3×3 pixel matrix. As before, each bin rep-

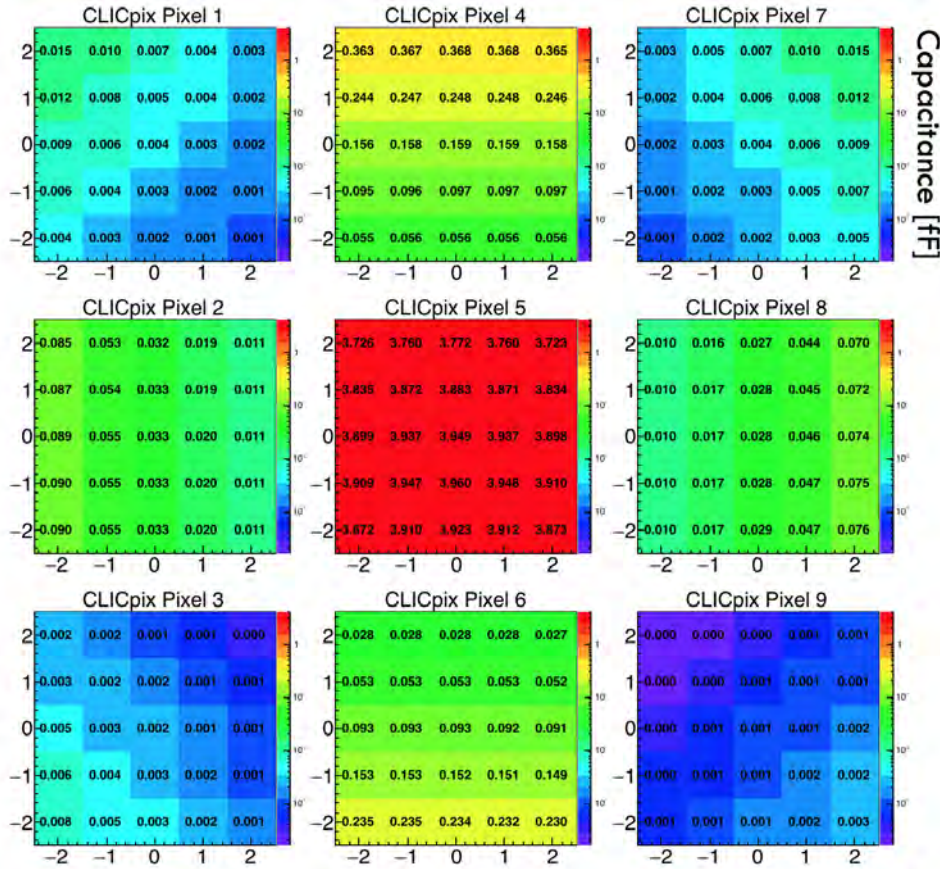


Figure 7.15: Capacitances for the 9 pixels in the CLICpix matrix for different positions of the CCPDv3 pixel matrix.

resents one position in the 2-dimensional scan. Each 2D-histogram, in Figure 7.15, represents one pixel on the CLICpix. The color scale range is the same for all histograms and the values are in fF.

The cross coupling capacitances are more affected by misalignment than the capacitance to the closest CLICpix pixel (pixel number 5). Within the $\pm 2 \mu\text{m}$ misalignment range, changes of cross coupling capacitances by about one order of magnitude are observed. In a simulation that can be found in the Reference [147], the chips were shifted, from their nominal position, $\pm 12.5 \mu\text{m}$, in the column or row direction (while keeping the alignment column or row-wise). For the assemblies done with the pad alignment ($-4.25 \mu\text{m}$ misalignment shifted in the column direction), one can expect relative capacitances of 0.4% and 12% for pixels 4 and 6, respectively.

This possible misalignment effect, from the flip-chip process, was not simulated with the H35DEMO/FE-I4 geometry. Nevertheless, due to the larger pads, it is expected that the worst case misalignment ($2 \mu\text{m}$ along the columns and rows) should have an effect smaller than 5% on the coupling capacitance between the closest pixel pair.

7.3.5 Guard ring effect

The C3PD is a new design with features based on the CCPDv3 chip. The new main feature, relevant regarding the cross coupling, is a guard ring (GR) structure, surrounding the pixel pads, in order to decrease the cross coupling between the pixels. A picture of the pixel pads surrounded by the GR is shown in Figure 5.8(b) and the 3D model of the new chips is shown in Figure 7.16.

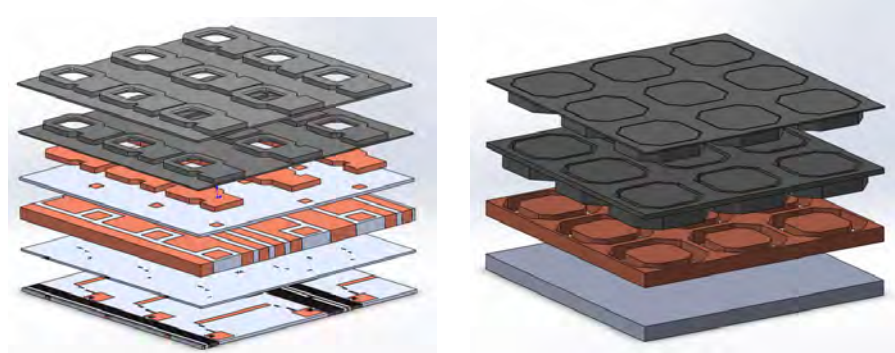


Figure 7.16: CLICpix2 (left) and C3PD (right) exploded geometry.

They were assembled with the same gap of $0.2 \mu\text{m}$ as before. As the chips were created with the same process technology, the materials used in this model are the same. The *Electrostatics* physics interface was used here as well, with the addition of a new BC for the GRs. The GRs are connect to ground and, therefore, their boundaries were defined with the *Terminal* BC in order to extract the additional load to the pad circuitry from the new GR. In order to compare the effect of the GR on the cross coupling, the C3PD was also modelled without the GR, maintaining the rest of the geometry identical.

The CLICpix2 was modelled with an additional metal layer, containing layers M5 and M6, in comparison with the CLICpix, which contains only M6. The effect of the additional metal layer was analysed in [147] and it was shown that it does not contribute significantly to the coupling, as the M5 layer has a thickness that is four times smaller than the M6 layer and is further away from the C3PD pixel pad, making the model containing just M5 accurate enough.

The guard ring shields the C3PD pixel pads from the neighbouring pixels in the ROC by adding a conductor in between the pads, making the overlap surface between the pads smaller. The effect can be seen looking at the electric field distribution and the field lines between the pixel pads shown in Figure 7.17. The cross section shows the middle C3PD pixel pad on the top and the CLICpix2 pixels 6, 5 and 4 (from left to right) on the bottom.

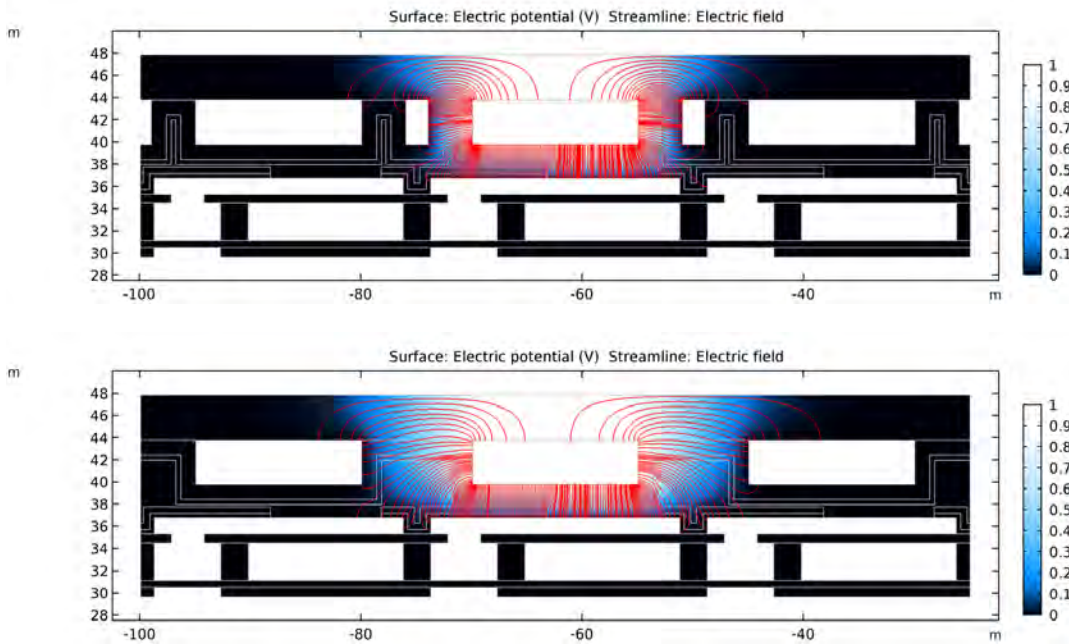


Figure 7.17: Comparison between electric field and field lines on the C3PD-CLICpix2 geometry with (top) and without (bottom) GRs. CLICpix2 pixels 4,5 and 6 are shown from left to right.

Table 2 summarises the coupling capacitances found for pixels 4, 5 and 6 with and without GR. The GR blocks the potential and electric field from reaching the neighbouring pixels, decreasing the cross coupling by almost a factor of 10, while increasing the capacitance to the closest, or main, pixel by ~ 100 attofarads ($\sim 4\%$).

Table 7.3: Pixel 14 coupling capacitances, in fF, with and without guard ring.

	Pixel 4	Pixel 5	Pixel 6	Metal lines	GR
Without GR	96E-3	3.360	96E-3	854E-3	-x-
Grounded GR	12E-3	3.484	12E-3	398E-3	3.14

The GR also helps to shield the metal lines from the sensor pixel, decreasing its coupling capacitance by almost half. On the other hand, it adds a parasitic capacitance, as the sensor pixel will also induce a charge on the GR. The result shows that the coupling capacitance is 3.14 fF, comparable with the capacitance to the ROC pixel. This capacitance is relevant for the design of the pixel electronics, as it adds a non negligible load to the pixel output amplifiers.

7.4 CAPACITIVE TRANSFER MONTE CARLO SIMULATION

In order to quantify the effect of the capacitive coupling between the sensor and the ROC, the results from the COMSOL finite element simulation were implemented into the AllPix² simulation framework [148], with the creation of a new module.

7.4.1 Introduction to AllPix²

Allpix² is an open-source software framework for the simulation of silicon detectors. It is designed as a lightweight framework with independent configuration and simulation modules, communicating through common objects passed between them using a message broker. Each module is easily configurable in order to have a complete control of the simulation. Modules responsible for the physics simulation are executed sequentially for every simulated event.

The modular approach of Allpix² allows a wide variety of possible simulations to be carried out. A typical simulation is composed of the following modules: a geometry manager; an electric field generator; a module for the stochastic particle interaction and energy deposition on the sensor; charge propagation inside the sensor; transfer of the

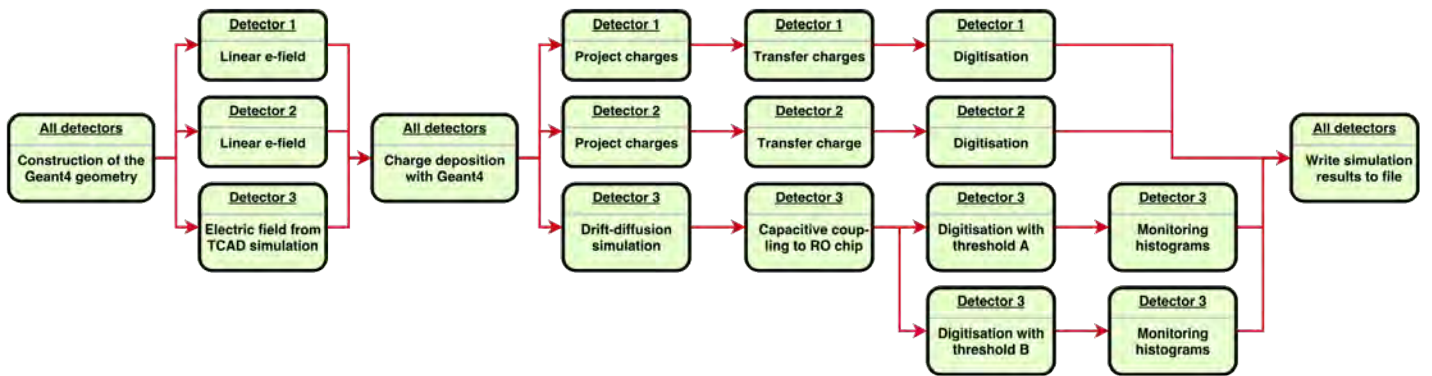


Figure 7.18: Layout of an Allpix² simulation with three detectors. Detectors 1 and 2 are treated as reference devices with a relatively simple simulation flow. Detector 3 is a DUT with a more complex simulation, being configured with a TCAD electric field, drift-diffusion propagation and capacitively coupled to its front-end electronics. The digitisation is performed with two different thresholds for comparison.

charge signal from sensor to ROC; and, finally, digitization of the signal. With this modular approach, complex simulation setups, such as the sketch shown in Figure 7.18, can be produced.

The geometry is built by the *GeometryBuilderGeant4* module, which creates a geometry description using native Geant4 objects, from the pre-defined AllPix² detector models.

The module responsible for the particle interaction and energy deposition is called *DepositionGeant4*, acting as an interface to Geant4, which converts all energy deposition, produced within the sensitive volume of the sensor, to charge carrier deposits.

The *ElectricFieldReader* module describes the electric field which will drift the charges created upon particle interactions inside the sensor. Two types of electric field profiles can be applied: a simple linear electric field, where the depletion voltage or depletion depth of the sensor can be specified along with the applied bias voltage, defining an electric field that varies linearly inside the depleted region of the sensor. The second approach involves the import of an electrostatic field simulation from packages such as TCAD, providing a more accurate electric field description. A converter tool was developed to convert the electric field simulated in a non-structured mesh produced by the TCAD software to a uniformly-spaced grid mesh, reducing the time needed for the propagation of the charge carriers across the sensor volume. This conversion will be discussed in a later section of this chapter.

Currently, two different modules are implemented in Allpix² for the propagation of the charge carriers along the sensor electric field. The most simple - and thus fastest - is the *Projection-Propagation* module, where the total drift time for each group of charge carriers, with user-defined size, is calculated in a linear electric field. A randomised lateral diffusion is calculated from a two-dimensional Gaussian distribution according to the Einstein Diffusion-Mobility relationship, and the group of charges is projected into the direction of the collection implants. A more detailed algorithm is implemented in the so-called *Generic-Propagation* module, which parametrizes the charge carrier mobility to calculate the charge group trajectory throughout the sensor. The charge carriers are stepped through the sensor, taking into account the electric field and the calculation of the mobility (function of the electric field) at each position. Random diffusion is also added to every step of the drift motion.

A dedicated module is used to simulate the transfer of the propagated charges from the sensor to the read-out chip. In monolithic or in hybrid DC-coupled detectors, the signal is formed by the *SimpleTransfer* module, which groups together all charge carriers located within the pixel boundary to be digitised. For capacitively coupled hybrid pixel detectors stray capacitances to the neighbouring pixel pads may induce additional pixel hits, while variations on the glue thickness can cause detection inefficiencies. For this scenario, the *CapacitiveTransfer* module was developed.

Using the charge transferred to a given pixel, a generic digitization module is used to simulate the response of the front-end pixel electronics. The module contains configurable parameters which allows a variety of chip architectures to be simulated. The input charge can be combined with electronic noise before comparing with a threshold, also with an optional pixel-to-pixel dispersion. A conversion factor from electrons to ADC units can be used to simulate pre-amplifier gain and to map the charge onto a counter, with customisable precision, allowing to simulate the response of a typical Time-over-Threshold (ToT) digitization.

Figure 7.19 shows an AllPix² simulation used to simulate the UniGE FE-I4 telescope (3 first planes and 3 last planes), with a H35DEMO/FE-I4 sample as DUT in the middle, being illuminated by a 120 GeV π^+ particle beam.

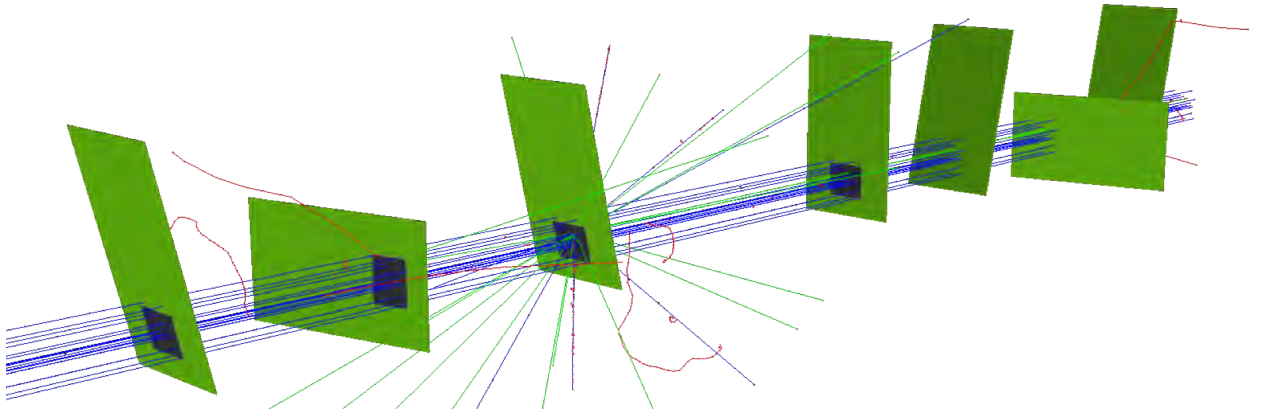


Figure 7.19: UniGE FE-I4 telescope simulation (3 first and 3 last planes), with an H35DEMO/FE-I4 DUT in the middle, illuminated by a particle beam.

7.4.2 Capacitive transfer module

An AllPix² module was developed in order to simulate the effect of the capacitive coupling between the sensor and the ROC. The *CapacitiveTransfer* module groups the propagated charge carriers that arrive at a predefined distance to the pixel collection implant (as the *SimpleTransfer* module) and applies a *charge-to-voltage* transfer function, emulating the charge signal integration, shaping and the output as a voltage signal that will be transferred capacitively from the sensor to the ROC. Such transfer function is imported to the AllPix² framework via ROOT TF1 mathematical objects, stored in ROOT files read-out during simulation initialization.

The capacitive transfer is simulated using the results from the FEM capacitance simulation described in the previous section. The COMSOL results are also imported into the simulation via a ROOT file containing the capacitance-*vs*-gap curves for different pixel pairs (stored as TGraph objects), as shown in Figures 7.11 and 7.13. Therefore, the capacitance for the signal transfer is calculated according to the gap

distribution over the detector, for each sensor/ROC pixel pair, defined by two angles (along the row and column axes, in radians or degrees), a minimum gap and its location in the matrix (using the pixel coordinates). If no angle is given the simulation will assume a perfectly parallel sensor and ROC, with an uniform gap and coupling.

Due to the nature of the capacitive coupling, a voltage signal from the sensor will capacitively induce a charge signal in the ROC according to $Q = CV$. Hence, the total charge induced in the ROC pixel is defined by the sensor output voltage, calculated via the *charge-to-voltage* transfer function, multiplied by the coupling capacitance, retrieved at the hit position.

The pixels cross-coupling effect, mentioned in sections 7.3.1 7.3.3.2 and 7.3.5, can also be included in the simulation, transferring the voltage output from the pixel sensor to multiple pixels in the ROC, each with its respective capacitance. In addition, the digitization of the charge signal detected by the ROC pixel can also be emulated by applying a *charge-to-TOT* transfer function, allowing to include effects of charge thresholds and non-linearities in the read-out digitization electronics. Such transfer function can be added in the simulation in the same way as the *charge-to-voltage* transfer function.

In order to verify the described coupling simulation and the capacitive transfer module, a detector assembly (H35DEMO sensor coupled to a FE-I4 ROC, named W19_o2) that has shown non-uniform signals during a test-beam campaign (at FTBF - Fermilab 2017) was chosen for comparison. First, a cross-section measurement was performed on the sample in order to measure the relative position of the chips. The sample was placed inside a cylindrical container with resin, as shown in Figure 7.20a, and once the resin was cured the sample was polished on both sides until both cross-sections of the chip were clearly visible. Both cross-sections are 1.5 cm apart. Figure 7.20b and 7.20c shows the pictures of the extremities of one cross-section, where it is possible to see the gap becoming larger along the 2cm cross-section.

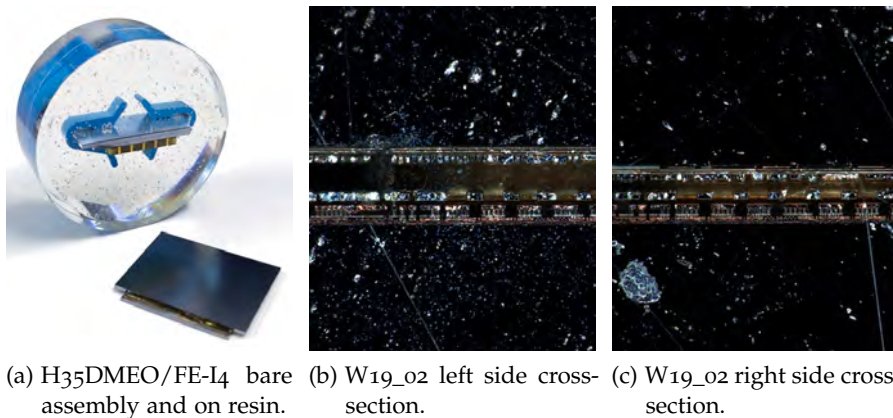


Figure 7.20: W19_o2 sample on resin and cross-section pictures.

With the gap between the chips measured along both cross-sections, it is possible to calculate the angles, for the column and row directions, between the chips. Figure 7.21 shows the measured gap points

of both cross-sections, along the H35DEMO/FE-I4 bottom and top rows. The bottom surface represents the chip at the bottom of the cross-section pictures (in this case the H35DEMO), while the top surface is the adjusted plane passing through the position points measured for the gap between the H35DEMO and the FE-I4.

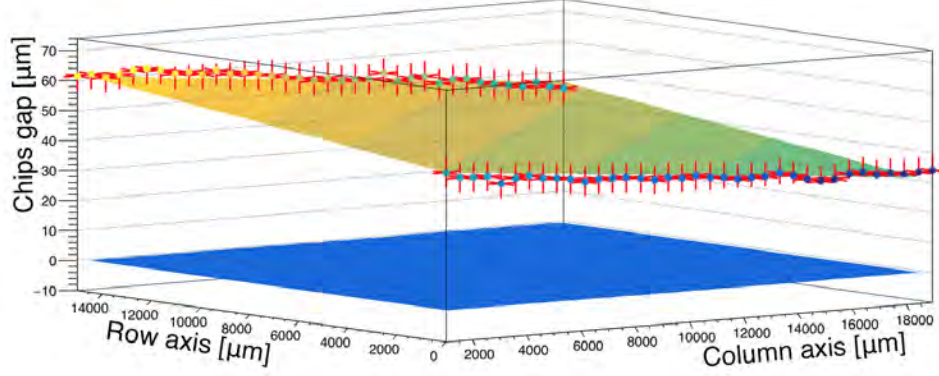


Figure 7.21: Profile of the gaps between the chips.

The cross-section measurements indicated that the gap along the assembly diagonal increased about $30 \mu\text{m}$. The angles between the chips are extracted from the adjusted plane equation and the angle calculated along the column and row direction is $-800 \mu\text{rad}$ and $1000 \mu\text{rad}$, respectively. The same angle was used in the *Capacitive Transfer* module in the AllPix² simulation.

The AllPix² simulation was configured with a proton beam of 120 GeV with a Gaussian profile, as the beam from FTBF, illuminating perpendicularly the detector. The coupling capacitances used are the coupling simulation results shown on Section 7.3.3.2, while the *charge-to-voltage* transfer function, shown in Figure 7.22a, was extracted from a preliminary post-layout simulation of the H35DEMO circuitry during prototype design phase available in the H35DEMO documentation [123]. The charge digitization by the FE-I4 ROC was simulated with a *charge-to-TOT* transfer function based on an ATLAS IBL module charge-ToT calibration, shown in Figure 7.22b.

Figure 7.23 shows the ToT distribution over the pixel matrices for the data and for the simulation. The pixel ToT was calculated as the mean ToT of each individual pixel distribution, accounting only sin-

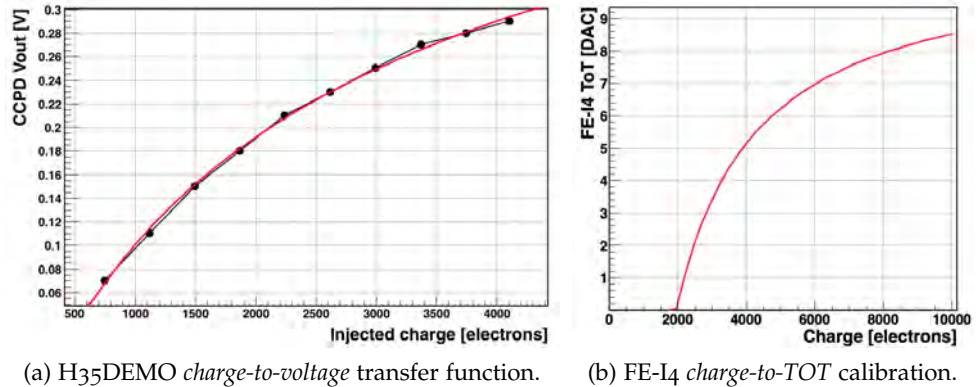
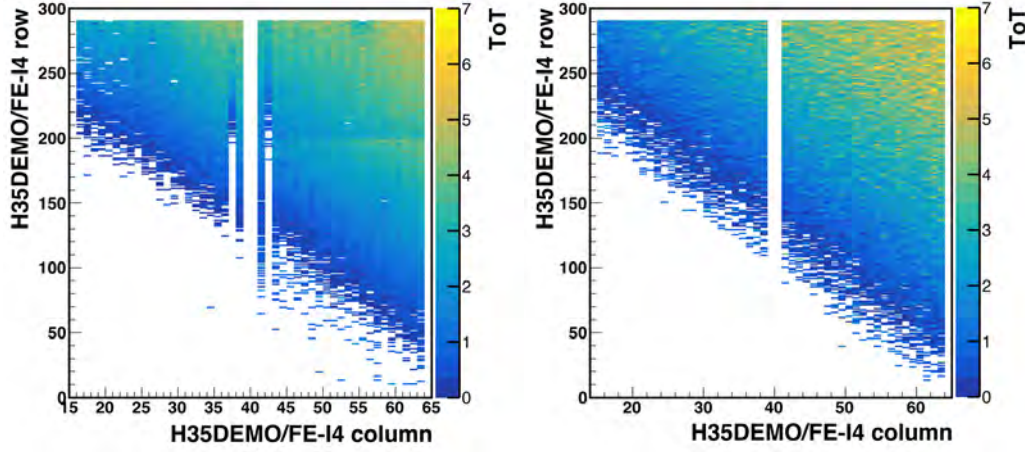


Figure 7.22: Transfer functions used for the capacitive transfer simulation.

gle pixel clusters. The similarity between the images already indicates a good agreement of the simulation with the real data.



(a) W19_02 mean pixel ToT data.

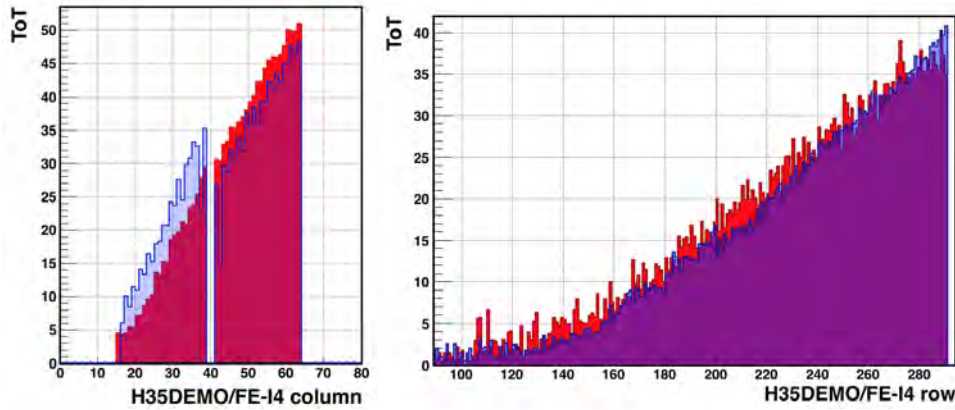
(b) Mean pixel ToT simulation.

Figure 7.23: W19_02 mean ToT map data (left) *vs* simulation (right).

In order to be able to properly compare the ToT gradient, a projection of the ToT map for the simulation and for the data was made along the column and row directions. To reduce statistical fluctuations along the columns and rows, the projection comprises 11 rows [225-235] or 9 columns [35-45] and, therefore, the ToT value on each histogram bin is the sum of all the pixels being projected.

Figure 7.24a shows the projection of rows 225 to 235 on the column axis. The blue histogram represents the measured ToT data and the ToT discontinuity in the middle columns is due to the different amplification electronics implemented for H35DEMO ANA1 and ANA2, where ANA2 yields smaller amplified signals. As the simulation does not take into account the H35DEMO electronic processing, the simulation (in red) shows a continuously increasing ToT with similar ToT gradient and range.

Figure 7.24b shows the projection of columns 35-39 (ANA1) and 41-45 (ANA2) along the row axis and it shows that a good agreement between data and simulation is also achieved in the row direction.



(a) ToT projection of 11 rows.

(b) ToT Projection of 9 columns over the row axis.

Figure 7.24: ToT comparison between data (blue) and simulation (red).

The apparent linear increase is counter-intuitive in view of the capacitive nature of the coupling (where $C \sim 1/d$, as shown in Figure 7.13), but it is needed to have in mind that other non-linearities, such as the transfer charge functions introduced previously, which will create a cumulative effect on the final measured ToT.

The good agreement between the data and the simulation shows that this chain of simulation can be used to predict the effect of bad assembly parallelism on the performance of the detector.

7.4.2.1 Simulation limits

Even with the good agreement between data and the simulation, it is important to note that the model developed here is a first approximation that can be used to predict the response for assemblies with tilted chips.

The first approximation regards the total charge signal collected on each sensor pixel, which in the AllPix² framework is defined by the amount of charge-carriers that are created and propagate reaching a minimum, configurable, distance of the collection implant of the pixel, while a proper (and more challenging for implementation) simulation of the total charge collected would be by using the Shockley–Ramo theorem, already described on Chapter 4 (currently being implemented in the simulation framework). The minimum distance required for the charge to be accounted as collected was defined as 75 μm on the simulation performed, based on edge-TCT scans at the same sensor bias high-voltage of 25 V [129].

In addition, the electric field responsible for the propagation of the charges (and, ultimately, the final amount of charge that arrives at the minimum distance to the pixel) is approximated to a linear electric field (like a parallel-plate capacitor), while more detailed electric field simulated with finite element TCAD tools should be used to accurately simulate the charge carrier propagation towards the pixel implants. Therefore, for the correct sensor charge collection and signal creation simulation, the sensor electric field must be accurately simulated, in addition to the weighting potential, so the Shockley–Ramo theorem can be properly used.

The second approximation is on the used transfer function for the *charge-to-voltage* on the H35DEMO. The transfer function was extracted from a simulation performed during chip design and the values on the real device are likely to change as function of many parameters, such as specific on-chip DACs configured differently during simulation and data acquisition, temperature and so on. Nevertheless, the function used provides a good approximation of the general behaviour of the voltage output as function of the collected charge in the sensor. In a similar way, the transfer function used to translate the induced charge on the FE-I4 ROC into a digitized ToT value was created based on the response of a random IBL module.

The dielectric constant of the glue, responsible for the strength of the signal transmission, is assumed to be constant over the assembly, which can differ if there are bubbles trapped between the chips or if the glue density is not constant, changing the effective dielectric constant of the coupling, or if there is a strong dependence on the signal frequency over the desired range.

Having these considerations in mind, the results shown previously indicate that the capacitive coupling and capacitive signal transfer can be simulated, providing good predictions of the coupling and calibration effects.

7.5 ALLPIX² MESH CONVERSION TOOL

An important aspect in silicon pixel detector performance is how the charges, created upon radiation interaction with the sensor, will propagate through the sensor bulk. The movement of the charges is driven by the electric field in the sensor volume as the electric field will drift the charges towards the pixel collection implants, generating an electric signal that can be measured by the detector read-out system. Observables such as collected charge, cluster size and track/hit residual, depend on how the charges drift and diffuse through the sensor.

The sensor electric field can be accurately simulated using the finite element method with TCAD³ software, such as Synopsys [149] or Silvaco [150]. TCAD simulations model semiconductor fabrication, simulating fabrication process steps (such as diffusion and ion implantation), as well as the semiconductor device operation, simulating the behaviour of the electrical devices based on fundamental physics, such as the doping profiles of the devices.

As the simulation performed in COMSOL, meshes are needed in TCAD simulations in order to provide a description of the sensor implant geometry, where the electric field will be calculated. Meshes can be separated into two categories: Unstructured and structured meshes. Both types are illustrated in Figure 7.25. Unstructured meshes, as the one shown in Figure 7.25 (left) illustrating the meshing of a coast line, are formed by triangular elements, being highly non-uniform but flexible to fit in complex shapes. Nevertheless, while an unstructured mesh is most appropriate to model the sensor implant geometry, it comes with a few disadvantages if used to calculate the charge propagation inside the AllPix² simulation framework.

Without a regular structure, each mesh cell must be identified by a unique number and the amount of cells surrounding a given mesh node is not necessarily constant. Therefore, the numeration of the neighbouring elements, not necessarily sequentially identified, to a given node cell must also be stored, increasing the complexity of the mesh description. Therefore, in order to propagate the charge carriers through an unstructured mesh, a large computational process is

³ Technology Computer-Aided Design

needed while calculating the trajectory of the charges. This issue can be overcome with the use of a regular grid (or structured) mesh, as the one shown in Figure 7.25 (right).

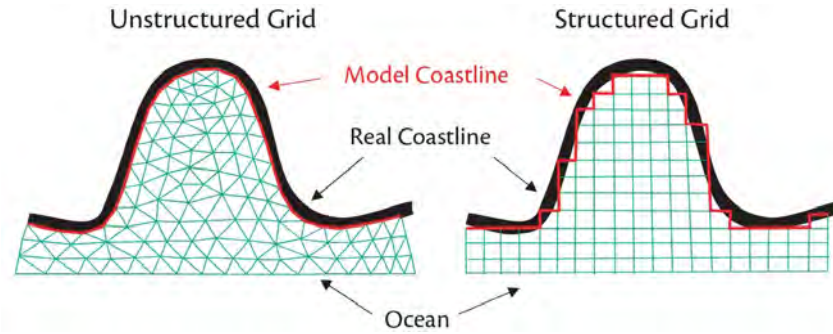


Figure 7.25: Adjusted model (red) of an unstructured grid (left) and an structured grid (right) to a coastal embayment (black)[151].

A structured mesh divides the domains into an assembly of quadrilateral cells and the mesh node positions can be represented by i, j, k indices. In contrast to an unstructured mesh, the nodes are surrounded by the same number of elements, with a regular connectivity, and the nearest neighbours can be immediately identified by knowing the node indices. Nevertheless, it has the disadvantage of the difficulty of keeping accuracy in complex shaped domains - a problem that can be overcome with the use of a dense grid mesh, which will require more memory for the mesh storage, but without the additional cost of larger computational process needed for the propagation.

The results from the TCAD simulations, such as the electric field magnitude and direction over the simulated volume, are stored on each mesh node (being named vertex data). Therefore, in order to convert an unstructured mesh into a regular grid mesh, an interpolation is needed as the new mesh points will not necessarily fall into the same position as the original mesh nodes.

7.5.1 Barycentric coordinates and interpolation

Starting with the 2D case, an unstructured mesh is composed of triangles. Therefore, it is appropriate to use barycentric coordinates. Barycentric coordinates express the position of a point P located on a triangle ABC ($\triangle ABC$) using three scalars, $(\zeta_A, \zeta_B, \zeta_C)$. Figure 7.26 illustrates a random point located inside the $\triangle ABC$ with the colors red, green and blue as vertex data. Following it will be demonstrated how new "vertex" data can be calculated on any point P located inside the $\triangle ABC$ using its barycentric coordinates.

The barycentric coordinates can be associated with the areas of the sub-triangles formed by the new point P and the original A , B and C vertices. For this reason, barycentric coordinates can also be called areal coordinates. Its possible to see in Figure 7.26 that as the point P gets closer to the vertex A (red), the area of the $\triangle BCP$ gets larger,

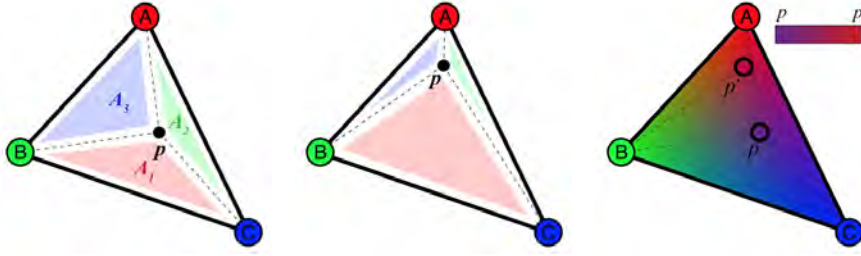


Figure 7.26: $\triangle ABC$ with color as vertices data and two random points P and P' being interpolated.

and the value associated to P gets closer to the value stored in the vertex A. Having this in mind, the coordinates can be defined as:

$$\zeta_A = \triangle_{BCP}^{Area} / \triangle_{ABC}^{Area} \quad \zeta_B = \triangle_{ACP}^{Area} / \triangle_{ABC}^{Area} \quad \zeta_C = \triangle_{ABP}^{Area} / \triangle_{ABC}^{Area} \quad (7.10)$$

Following this definition the normalization of the barycentric coordinates, meaning $\zeta_A + \zeta_B + \zeta_C = 1$, is guaranteed as the sum of the areas of the three sub-triangles must be equal to the total area of the $\triangle ABC$. This further implies that only two coordinates already define the position of P , as expected from a 2D coordinate system, with the third one being defined as $\zeta_C = 1 - \zeta_A - \zeta_B$, for example. Subsequently, the point is within the $\triangle ABC$ if $0 \leq \zeta_{A,B,C} \leq 1$. If any one of the coordinates is less than zero or greater than one, the point is outside the triangle⁴. If any of them is zero, P is on one of the lines joining the vertices of the triangle.

The same concept can be extended into the 3rd dimension. Unstructured 3D meshes are mainly composed of linear tetrahedral (\triangle) elements, as the $\triangle ABCD$ shown in Figure 7.27. The position of a tetrahedron point may be specified by a set of four dimensionless numbers, $\zeta_A, \zeta_B, \zeta_C, \zeta_D$.

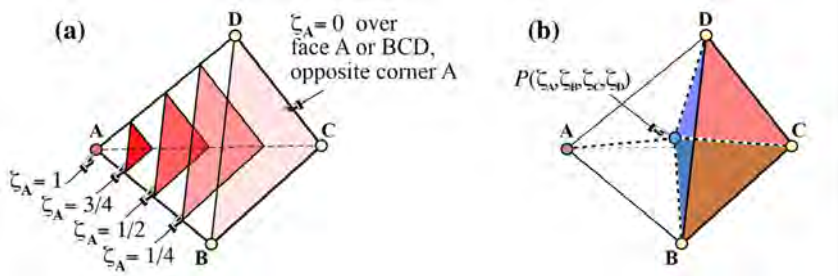


Figure 7.27: ABCD tetrahedron with the visualization of ζ_A coordinates and sub-tetrahedron BCDP. Image adapted from [152].

The value of ζ_A , for example, is 1 at the tetrahedron vertex A and 0 at the other 3 vertices, including the entire opposite face. It varies linearly with distance as one traverses the distance from the corner to that face, as shown in Figure 7.27(a). As an extension to the 2D case, the barycentric coordinates for the 3D case can be defined using the volume ratios between the tetrahedrons. In this way, $\zeta_X = V_X / V_{total}$,

⁴ Areas with opposite sign are possible as the calculations are done by vector cross-product, which depends on the vector orientations

also resulting in normalized coordinates $\zeta_A + \zeta_B + \zeta_C + \zeta_D = 1$. Here, V_X denotes the volume of the sub-tetrahedron spanned by the point P and the face opposite to the X corner, as illustrated for ζ_A with the coloured $\triangle BCDP$ in Figure 7.27(b), and V_{total} is the $\triangle ABCD$ volume.

Any linear function F that assumes the values $F(A) = A$, $F(B) = B$ and $F(C) = C$ at the vertices of a triangle (and $F(D) = D$ on a tetrahedron) may be interpolated into any point $P(\zeta_A, \zeta_B, \zeta_C, \zeta_D)$ in terms of its barycentric coordinates:

$$F(P) = A \cdot \zeta_A + B \cdot \zeta_B + C \cdot \zeta_C (+D \cdot \zeta_D) \quad (7.11)$$

This is known as barycentric interpolation. If the interpolated point coincides with one of the vertices, then the associated value is simply the data on that vertex.

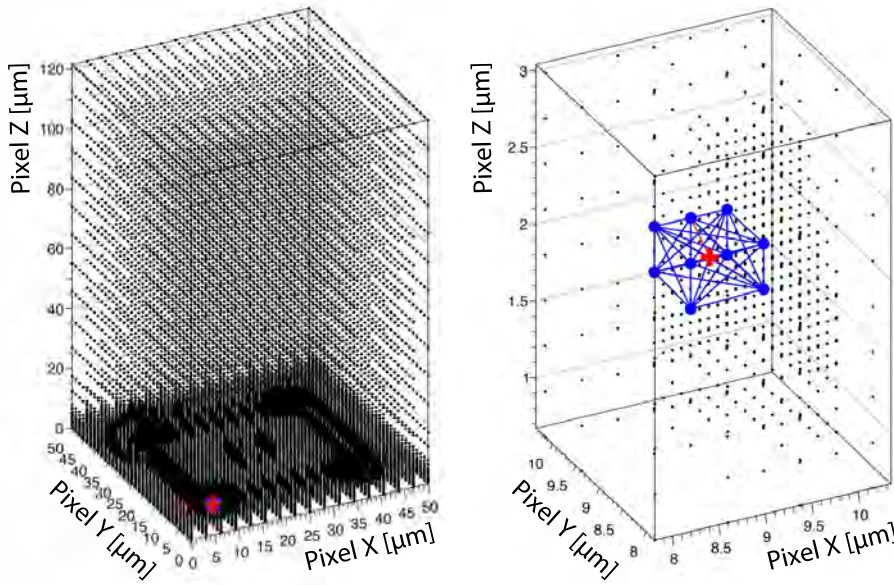
7.5.2 Implementation in AllPix²

The tool developed to perform the mesh conversion, using barycentric interpolation, for the AllPix² simulation framework can be found in [153]. It can also be compiled and installed independently of the AllPix² framework, if desired. First, the mesh used in the TCAD framework must be exported in the *DF-ISE*⁵ format, composed by two files: the grid file, with the mesh points coordinates and mesh elements (lines, faces and domains) relations; and the dataset file, containing the simulated quantities (vertex data) for each mesh node point. The mesh is imported using a *DF-ISE* file reader, creating a 2D or 3D mesh point-cloud that will be used for the interpolation of the new regular grid mesh, as described in the previous section.

As fine grained meshes tend to yield more accurate simulations, mesh clouds can normally contain over 100k nodes with indices that are randomly distributed over the geometry volume. While interpolating the new regular mesh it is needed to look through the original mesh point-cloud in order to find the closest nodes forming a tetrahedral (in 3D meshes, or triangles in 2D simulations) surrounding the new mesh node being interpolated. As the mesh is not structured, all nodes must be tested in order to verify if they are within a threshold distance (or search radius) and, in order to avoid large computational time for the interpolation, a strategy using a *leaf based* search on regularly spaced partitions (*octree*) of the mesh cloud volume is used [154].

Figure 7.28a shows an example of a mesh point-cloud, composed by $\sim 70k$ points, used for the simulation of a single $50 \times 50 \mu\text{m}^2$ pixel on a planar silicon sensor $120 \mu\text{m}^2$ thick. The non-uniform distribution of the mesh nodes can be seen clearly close to the pixel implant, at $Z < 10 \mu\text{m}$. Figure 7.28b shows in details a smaller part of the same mesh, indicating a node of the new regular mesh to be interpolated (in red) and the closest nodes in the original point-cloud (in blue).

⁵ Text based file format of the ISE software company TCAD suite.



(a) Example of a mesh point-cloud with over 70k points. (b) Mesh point-cloud with interpolated point (red) and first neighbours (blue).

Figure 7.28: Pixel cell mesh points (black) with a single extra point (red) to be interpolated (a) and zoom into point-cloud for detail of surrounding points (b).

If the 4 closest neighbours are co-planar (or 3 for 2D, being co-linear), or if the formed tetrahedron doesn't contain the point P being interpolated, the given set of points can not be used for the interpolation as the point P would be described by negative, or larger than 1, barycentric coordinates. Therefore, a selection on the neighbours found must follow to find the appropriate tetrahedron for the vertex data interpolation.

The conversion tool was implemented as a C++ library with triangles and tetrahedrons as objects with dedicated functions to calculate the areas and volumes, establishing if the found nodes can be used for the interpolation of the new point. The Eigen library [155] was used for the calculation of the areas and volumes via the *Jacobian* matrix of the triangle and tetrahedron, easily defined using the coordinates of the 4 mesh nodes. The tetrahedron volume is defined as

$$V = \frac{1}{6} \det(\mathbf{J}) = \frac{1}{6} \det \begin{bmatrix} 1 & 1 & 1 & 1 \\ x_1 & x_2 & x_3 & x_4 \\ y_1 & y_2 & y_3 & y_4 \\ z_1 & z_2 & z_3 & z_4 \end{bmatrix}$$

while, for 2D, the Jacobian matrix is defined without the last matrix row and column, and the triangle area is defined as $\frac{1}{2} \det(\mathbf{J})$. Having in mind that $\det(\mathbf{J})$ is a *signed* quantity (depending on the ordering of the nodes while forming the tetrahedron or the triangle), the interpolated point P is said to be inside the interpolation area/volume if,

and only if, its barycentric coordinates ζ_X are larger than 0, smaller than 1, and all have the same sign. The interpolation algorithm tries to perform the interpolation using the tetrahedron with the smallest volume possible (by using the 4 closest nodes in the point-cloud). If the closest neighbours can not be used for interpolation, different ways are implemented in order to use further nodes and permute the tetrahedron vertices, until an appropriate tetrahedron is found.

7.5.3 Mesh conversion performance

During the simulation of an event (one particle interacting with the sensor), AllPix² groups the charges created for the propagation through the sensor volume in order to save computing time, instead of propagating each individual electron-hole pair among the thousands created. For the charge group propagation, the trajectory of each group is calculated through several steps across the sensor electric field. On each step, configurable by selecting the desired time step and spatial precision, the electric field is retrieved at the charge group position on the given instant, in order to calculate the group mobility and the group future position in the sensor. This calculation is done multiple times, stepping the charge group until it reaches the collection implant or the (configurable) charge integration time finishes.

To retrieve the electric field value on a given location in the sensor volume, from the original point-cloud mesh, the electric field interpolation would be needed for each propagation step, which would require a large computational power and would lead to longer simulation time as the neighbour search (in the large point-cloud) and the further interpolation requires several computational steps. With the conversion of the mesh point-cloud into a regularly spaced grid mesh, the electric field value can be spatially retrieved by using the new mesh i, j, k indices, which computationally is a "cheap" task that doesn't require a lot of time, as accessing the content of an 3D array.

In Figure 7.30, the blue plot shows a distribution of the time required to search the closest neighbours in the original mesh (Figure 7.28) for a given point to be interpolated, for all the new nodes on a regularly spaced 25x25x75 grid mesh (with a total of 46875 nodes). The red plot shows the search time plus the time needed to calculate the interpolation for each point in the new regular grid mesh. The times were recorded, using the C++ standard *chrono* library, by measuring the elapsed time⁶ between the start and end of the calculations, using the *now()* function of the *system_clock* class.

The first peak in the blue distribution shows that 70% of the new mesh points take less than 10 μs to have its neighbours found, while for the interpolation $\sim 50\%$ of the points take between 10 and 100 μs , with the remaining $\sim 50\%$ takes more than 100 μs . The complete

⁶ Computer system-wide real time wall clock, running on a 3.2 GHz4 core Intel i5-6500 CPU with Scientific Linux CERN 6.10 as operational system.

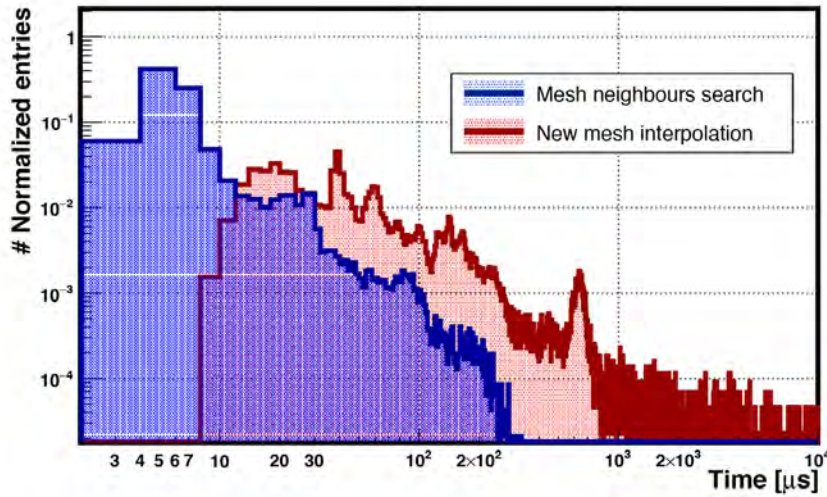


Figure 7.29: Time needed for neighbours search (blue), new point interpolation (red).

mesh conversion - $\sim 70k$ mesh point-cloud into $\sim 45k$ points grid - took approximately 10 minutes.

In order to evaluate the advantage of using the grid mesh, the interpolation algorithm was implemented into the propagation module in order to retrieve the electric field from the original TCAD mesh, via the barycentric interpolation, for each propagation step.

A typical simulation event using the grid mesh takes about 30 ms to run, independently of the incident position of the particle on the pixel and executing thousands of propagation steps. The first consequence of this *on-the-run* interpolation is that, just as the conversion of the mesh into a regular grid takes different times depending on the node position, the time needed for the propagation of the charges through the sensor depends on the distribution of the nodes on the original TCAD mesh. As expected, with the more complex retrieval of the electric field, the simulation time for a typical event (perpendicular particle incidence close to the pixel center) increased to 400-500 ms, with some events, happening in some regions of the pixel with complicated meshing, taking up to 30 seconds to be simulated.

The use of a regular grid mesh shows its advantage here, as during the mesh conversion complicated points to interpolate must be interpolated just once, while if the interpolation is done *on-the-run* several steps around the same complicated point are done, increasing the event simulation time considerably. Therefore, the use of the grid mesh provides simulation times at least 10x faster when compared with the interpolation being performed on each propagation step, and 1000x faster for some events depending on the location of the charge creation.

The barycentric interpolation algorithm is powerful enough to interpolate an infinite amount of points in between points (from the original mesh) separated by a large distance. Therefore, an advantage of the use of a regular mesh is that, as the electric field is retrieved from the grid mesh by using its i, j, k indices, to have a fine grained

grid mesh, with pitch as small as the minimum element size in the original mesh, does not make the computational process more time-consuming. To have a fine pitch regular grid mesh helps to keep the details of the original field, although with the disadvantage of the need of a larger memory to store the higher number of nodes.

In order to show that the quality of the electric field is kept during the conversion from the TCAD mesh into the grid mesh, Figure 7.30 shows a comparison of the electric field magnitude at the center of a generic pixel along the sensor depth, with the values from the TCAD simulation in black and the interpolated values in red. The pixel mesh volume was $28 \times 28 \times 15 \text{ } \mu\text{m}^3$ (with about 45k points) and, in order to compare values directly simulated from the TCAD software, the original mesh had a dedicated set of points forming a line from the bottom to the top of the sensor, at the center of the pixel, to explicitly calculate the electric field in this region. The interpolated grid mesh was created with $500 \times 500 \times 500$ nodes and the values were extracted from the center of the grid (from bins $250 \times 250 \times 0$ to $250 \times 250 \times 500$).

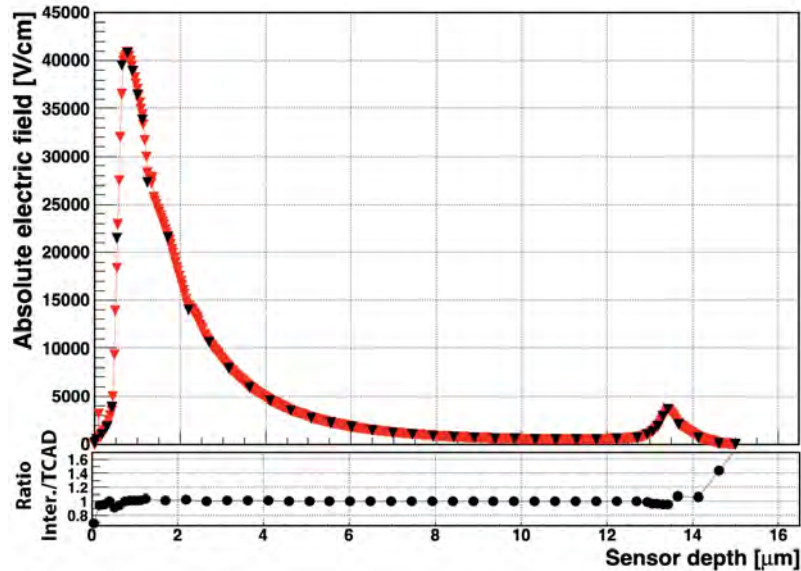


Figure 7.30: Comparison between original TCAD electric field (black) and electric field from interpolated grid (red).

The bottom ratio plot in Figure 7.30 shows that the interpolation has good agreement from $0.1 \text{ } \mu\text{m}$ up to $14 \text{ } \mu\text{m}$, while the interpolated value deviates up to 40% when the interpolation approaches the boundaries of the original mesh. The interpolation can lead to misleading values close to the boundaries of the mesh point-cloud as all the closest neighbours can be arranged at the 2D edge of the mesh, making it necessary to use a point that is further apart from the edge, possibly introducing a distant value into the interpolation and creating an edge effect in the interpolation.

HV-CMOS TEST-BEAM RESULTS

Test-beam measurements represent the ultimate tests of the detector prototypes. These are performed using a known beam illuminating the Devices Under Test (DUTs), recreating similar conditions as the detectors will face on the real experiment, such as particle hit rate and temperature and/or radiation conditions.

In order to reconstruct the particle trajectories hitting the DUT it is needed to measure the particles, preferentially, before and after the DUT, so the track position can be interpolated into the DUT position. For that a, so-called, particle beam telescope is used. A particle telescope generally consists of multiple planes of position sensitive detectors. With the spatial position of the particle beam along the telescope, the trajectory of the particles can be reconstructed, allowing to measure characteristics of the DUT, such as spatial resolution and detection efficiency.

For the reconstruction of the particle trajectories measured by the telescope planes an off-line reconstruction software, named Proteus, is used.

8.1 TEST-BEAM DESCRIPTION AT CERN SPS

As mentioned on the first part of this thesis, the acceleration structures that inject high energy protons into the LHC are also used by other beam users. Some of these users are the Secondary Beam Areas (SBA), such as the experimental East Area [156], in which beam lines are derived from the 24 GeV/c primary beam from the PS accelerator, using the beam for irradiation of devices, for example, or as the experimental North Area (NA) with multiple beam lines, described in more detail in the following paragraphs.

The beam lines at the NA are produced by the incidence of the SPS high-intensity primary 450 GeV proton beam onto each of the three primary targets T2 (H2 and H4 beam lines), T4 (H6, H8 beam lines and P42/K12 beam for the NA62 experiment[157]), and T6 (with the M2 beam line for the NA58/COMPASS experiment[158]) located at purpose-built target areas, near the surface but deep enough to be radiation-shielded by the landscape. Figure 8.1 shows a diagram of how the primary proton beam arrives at the NA and is subdivided into diverse beam lines. Upon the interaction of the primary proton beam with a target a shower of secondary particles is created and it is further filtered and steered into the different beam lines, which can contain electrons, hadrons (pions, kaons and protons), muons or a combination of these particles.

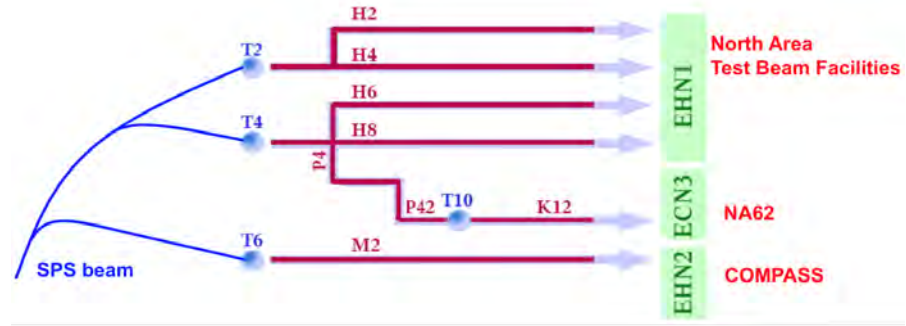


Figure 8.1: Beam from SPS into NA targets and following beam lines.

Sophisticated beam line equipment allows the selection of the type, polarity and energy of particles as well as the beam intensity. The so-called *wobbling station* ensures that sufficient particles of the requested type and energy are sent towards each beam line in a way consistent with the requirements of the other beam lines derived from the same primary target. Dipole magnets are used to guide the particles through the tunnels towards the relevant experimental areas and also to introduce dispersion, necessary to achieve momentum selection. Smaller dipoles (trim magnets) allow corrections to the beam steering. Quadrupoles help to control the beam size and dispersion along the beam line. Together with movable slits, called Collimators, they define the acceptance of the beam line in momentum and angle phase-space.



Figure 8.2: Illustration of SPS beam and EHN1 beam lines..

The beam lines H2, H4, H6 and H8 are located in the Experimental Hall North 1 (EHN1), while the other lines and experiments are located in different buildings. Figure 8.2 shows the EHN1 building with an illustration of the beam coming from the SPS accelerator and Figure 8.3 shows a picture of the interior of the EHN1 building with its four beam lines.



Figure 8.3: Picture of the EHN1 interior with beam lines identification.

The beam from the SPS is delivered in so-called super-cycles and its cycles can change depending on the SPS beam delivery request from the beam-line users. The super-cycle contains one or more spills, each typically 4.8 seconds long, during which beam is extracted towards the NA targets with a particle time distribution as uniform as possible and a super-cycle can take between 30 and 60 seconds. Figure 8.4 shows a typical super-cycle from the SPS.

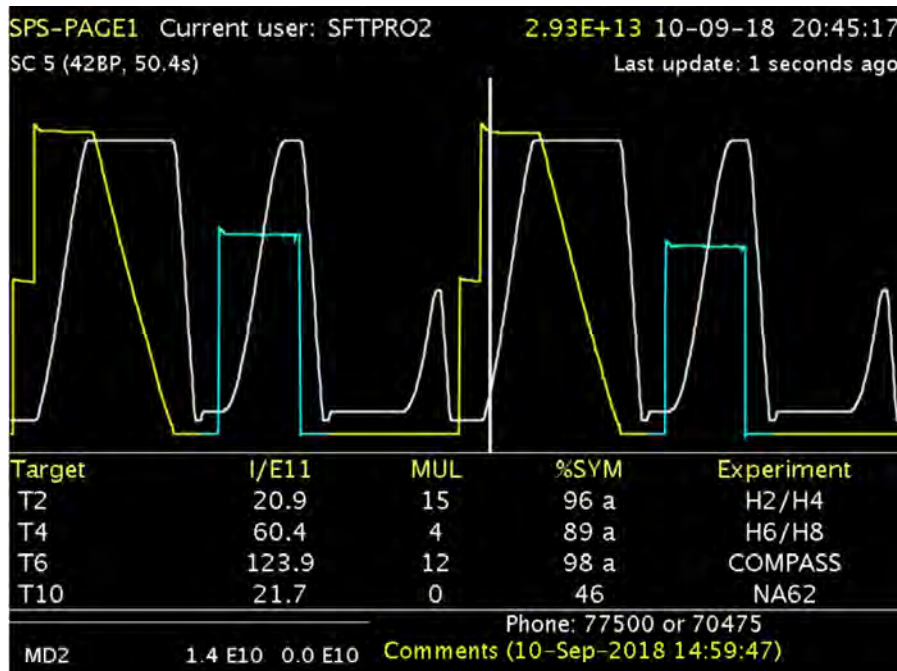


Figure 8.4: The SPS super-cycle overview page showing a typical operation mode of the SPS with two fills and slow extractions towards the test beam areas[159].

The white curve shows the current on the main dipole magnets of the SPS extraction system, responsible for inject the beam into the NA, while the yellow curve shows the SPS beam instantaneous in-

tensity. The cycle of the yellow curve shows the SPS beam intensity increasing with two injections from the PS, followed by the increase of the magnet current (in white) which is then kept constant for the slow extraction of the beam, seen as the decrease of the SPS beam intensity (falling edge of the yellow curve). After the beam extraction the magnet returns to its idle position so a new beam can be injected into the SPS for a new cycle. As mentioned previously, the SPS is also used to accelerate and inject the beam to other users, what happens between the beam extractions to the NA.

Information about the beam is available on the Vistar SPS Page-1, as shown in Figure 8.4, and a complete description can be found in [160]. As an example: the yellow number at the top shows the SPS beam intensity; at the bottom, the $I/E10$ column indicates the intensity as the number of protons sent towards each primary target, in units of $10^{11} \text{ protons/spill}$, and MUL indicates the beam multiplicity (ratio between the numbers of charged particles detected upstream/-downstream of the target¹).

8.2 FERMILAB TEST-BEAM FACILITY

Fermilab's Wilson Hall



During the technical shut-down period of the CERN accelerators, the test-beam measurements were performed at the test-beam facility available at the Fermi National Accelerator Laboratory (Fermilab). Fermilab hosted the DØ[161] and CDF[162] experiments, which measured $p\bar{p}$ collisions from the Tevatron accelerator²[163]. As the LHC, the Tevatron used a complex of accelerators, shown in Figure 8.5, in order to accelerate the particles, with other users of the beam acceleration, such as the Fermilab Test-Beam Facility (FTBF)[164], shown in Figure 8.6, with the MCenter and MTest lines.

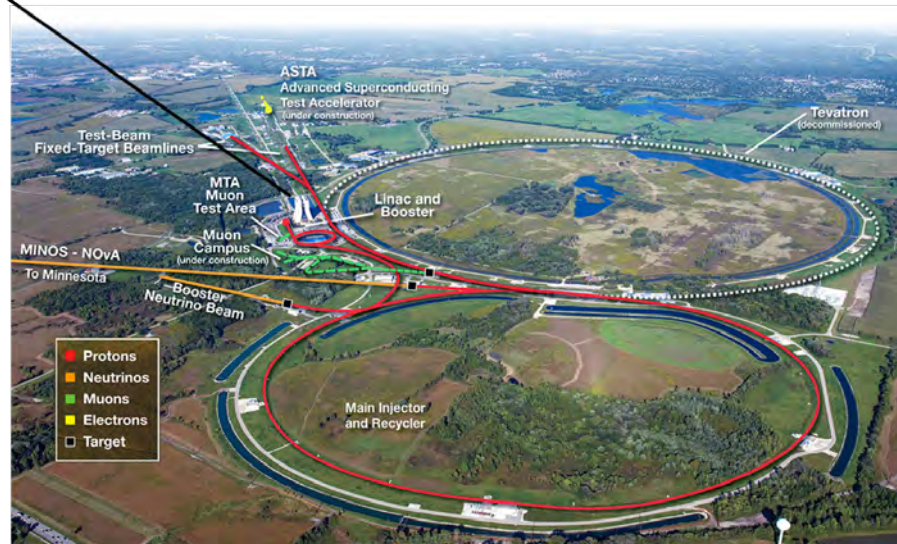


Figure 8.5: Fermilab acceleration complex. Image from [165].

- ¹ This ratio depends on the length of the target, on the acceptance of the downstream detector and on calibration factors for the monitors.
- ² Decommissioned in September 2011.

The acceleration chain starts with 750 keV H^- ions being extracted from a source and injected into the Linac. The Linac accelerates the ions to 400 MeV, and then extracts them to the Booster Accelerator. As the ions are injected into the Booster, the electrons are stripped off leaving 400 MeV protons to circulate in the Booster, which will accelerate them to 8 GeV. At this point the protons are extracted to the Main Injector, which will perform the last acceleration step, accelerating the beam to 120 GeV. Then, the protons are steered from the Main Injector into the so-called Meson line, where there are two movable aluminium targets in order to generate the secondary beam to be used in the test-beam areas.

As the targets are movable, there are multiple operation modes, each providing a specific beam. A primary proton beam at 120 GeV is possible, with a maximum intensity of 500k protons/spill³, as well as a secondary π^+ beam with energies from 8 to 60 GeV, electrons from 1 to 32 GeV, or a mix of π p and κ from 200 MeV up to 1 GeV, available only as a tertiary beam. The measurements performed at FTBF were done on the MTest beam line using 120 GeV protons with a $\Delta p/p \approx 2\%$.



Figure 8.6: Fermilab Test-Beam Facility (FTBF) building with the MCenter and MTest beam lines.

8.3 THE UNIGE FE-I4 TELESCOPE

Particle telescopes can be seen as a small section of an experiment vertex/tracker detector (one module of each layer) with the difference of, instead of surrounding the beam pipe and being illuminated by particles with divergent trajectories, it surrounds a DUT and is illuminated by a parallel beam (approximately).

In order to test several prototypes under study for the ATLAS ITk upgrade, as well as test devices from other projects, and with the

³ Counted by a beam instrumentation scintillator.

availability of modules from the ATLAS IBL construction, the UniGE FE-I4 particle telescope [166] was built at University of Geneva. The telescope uses 6 IBL planar modules, composed of two FE-I4 ROCs coupled to a single silicon sensor (shown in Figure 3.19).

The telescope, as a small experiment detector, is composed of several sub-systems: mechanical parts for the detector support; electrical sources with High-Voltage (HV) and Low-Voltage (LV) capabilities; detector refrigeration; trigger control and read-out systems; and so on. A description of the systems will follow in the next sections.

8.3.1 Telescope modules

Each IBL double module is mounted on an aluminium frame, which is then fixed on an alignment and support rail (telescope arm), together with other (two) telescope planes. To minimize multiple scattering as the beam traverses the detector, the aluminium frame is opened in the detector region. The aluminium frame also supports the module flex, which contains the wire-bonds for communication with the module (plus some passive components) and the module Adapter PCB, which interfaces the detector control/data lines and HV input to the DAQ system. Figure 8.8 shows an illustration of a complete telescope plane and some pictures of the module assembly.

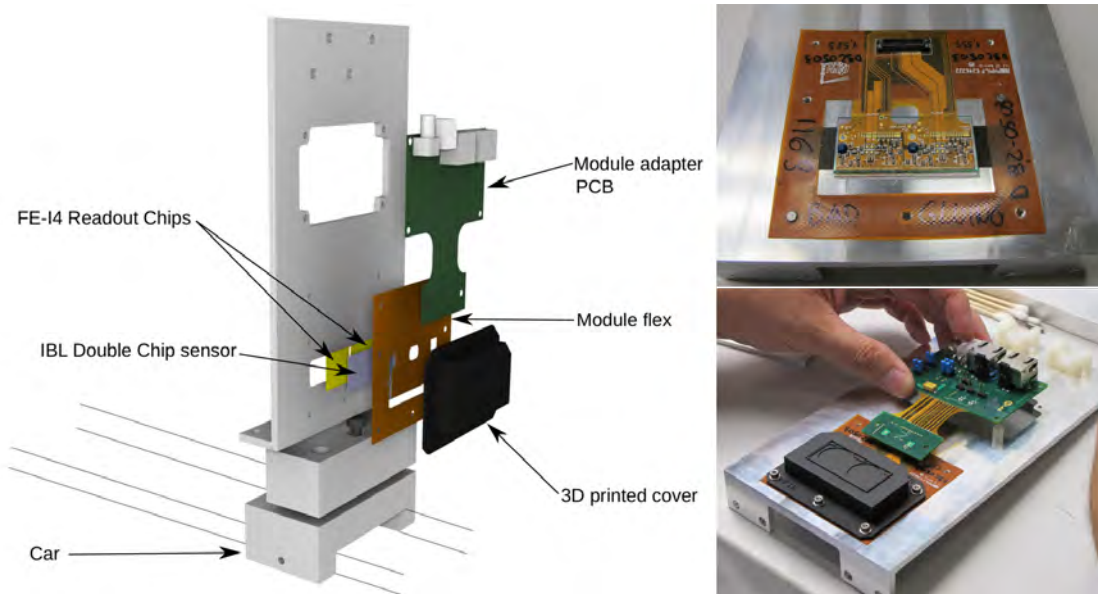


Figure 8.7: (Left) 3D render of a telescope plane. (Top-right) Glueing of the IBL module sensor and flex into telescope plane frame. (Bottom-right) Picture of the complete telescope plane [167][168].

Each sensor ($200\ \mu\text{m}$ thick n^+ -on-n silicon) is bump-bonded to two FE-I4 ROC and is composed of 160×336 pixels ($2 \times 80 \times 336$ FE-I4) with a pixel pitch of $250 \times 50\ \mu\text{m}$. Due to the inactive edge on the FE-I4 ROC, the innermost pixel columns in the sensor have a pitch of $450\ \mu\text{m}$ to bridge the larger gap between the two FE-I4 pixel matrices.

8.3.2 Telescope structure

The telescope is composed of 6 IBL module planes which are, typically, arranged in two 40 cm long telescope arms (where the planes can be freely positioned). As the sensor pixels have a rectangular aspect ratio, the tracking resolution is not the same in the column and row axes. In order to mitigate this problem, the middle plane of each arm is rotated by 90° around the beam axis, ensuring a comparable spatial resolution in the beam transversal direction. The two telescope arms, each with 3 telescope planes, can be seen in Figure 8.8. Both telescope arms can be moved separately to accommodate DUT setups with a width between 20 and 40cm, thus ensuring a positioning of the innermost planes as close as possible to the DUT.

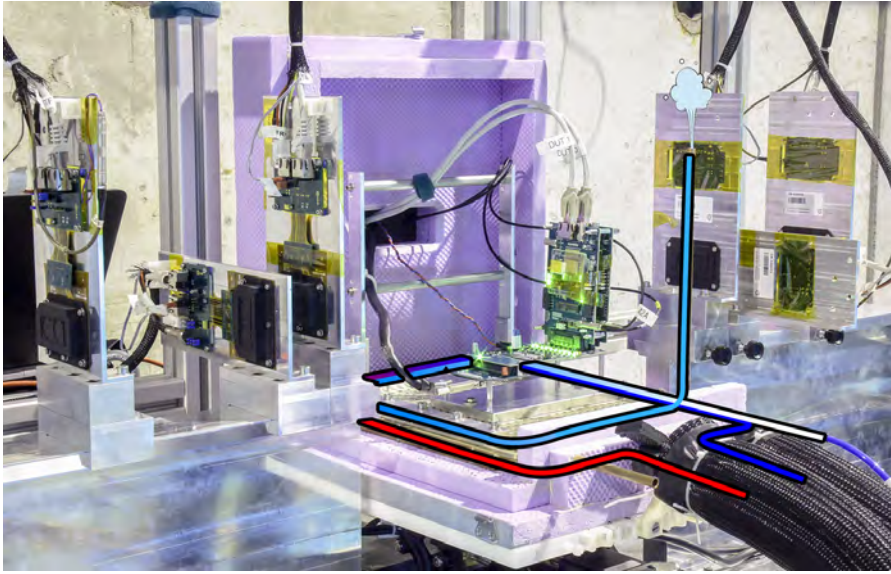


Figure 8.8: Picture of the 6 telescope planes and the DUT box opened. In addition, the coloured lines indicates the cooling pipe (with a cold input and warmer output) and the gas pipe with input at room temperature and colder outlet.

An hermetic container for the DUT (called DUT box) is placed between the two telescope arms, and is also shown in Figure 8.8. The DUT box is mounted on two stages in order to properly position the DUT transversally with respect to the particle beam. In addition, the environmental condition (temperature and humidity) inside the DUT box is monitored and controlled with the use of a silicon-oil based chiller and a gas (typically dry N_2) inlet.

The refrigeration is illustrated in Figure 8.8, with blue color indicating cooler temperatures. The cold silicon oil goes inside the DUT box and circulates in a copper tube in thermal contact with the DUT support plate (also made of copper), cooling it down. With the silicon-oil refrigerated down to -60°C the temperature on the base plate goes down to -46.1°C , further cooling components that are in thermal contact with it. In addition, a second copper pipe runs at the periphery of

the base plate, close to the silicon-oil pipe, with a constant (dry) gas flow into the DUT box. The gas released into the box is also cooled down, helping to decrease the atmospheric temperature, while keeping it dry. Temperatures as low as -26.6°C have been achieved on the CCPDV4 prototype while operation [169].

The whole system is mounted on a 8" thick optical breadboard, supported by four pressurized (at 2.5 bar) dampers to isolate the telescope structure from possible mechanical vibrations in the experimental area. In addition, a patch panel, shown in Figure 8.9, is used as an interface between the equipment on on the telescope and the rest of the system (facilitating the system assembly/installation process). A new rounded DUT box mounted on a rotation stage, allowing to take data while rotating the DUT (allowing to extract more characteristics of the DUTs), and with similar cooling as mentioned previously, was implemented by the time of the end of this thesis.

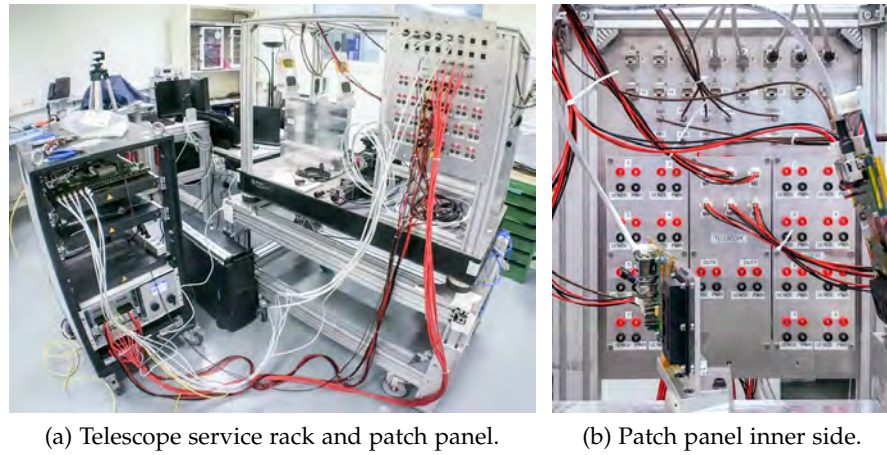


Figure 8.9: Telescope systems connections.

A movable half height rack, visible on the left side of the picture in Figure 8.9a, hosts the detector control and read-out systems, the power supply unit, the environmental monitoring systems, stage controllers and a network switch. Figure 8.10 illustrates the main telescope blocks.

8.3.3 Data Acquisition System

The DAQ system is a modification of the readout system, based on the HSIO/RCE system⁴, designed for the IBL during development phase. The general layout is shown in Figure 8.11. It is composed of three main blocks: the High-Speed Input Output (HSIO); the Reconfigurable Cluster Elements (RCEs); and the ATLAS Trigger and Data Acquisition (TDAQ) framework.

The HSIO is a custom-made readout board based on the Xilinx Virtex-4 FPGA. It hosts a large number of I/O (Input-Output) data channels and interfaces them, via Multi-Gigabit Transceivers (MGTs), with the higher level processing RCE units. It implements the low

⁴ Custom-made system designed at SLAC (Stanford Linear ACellerator Laboratory)

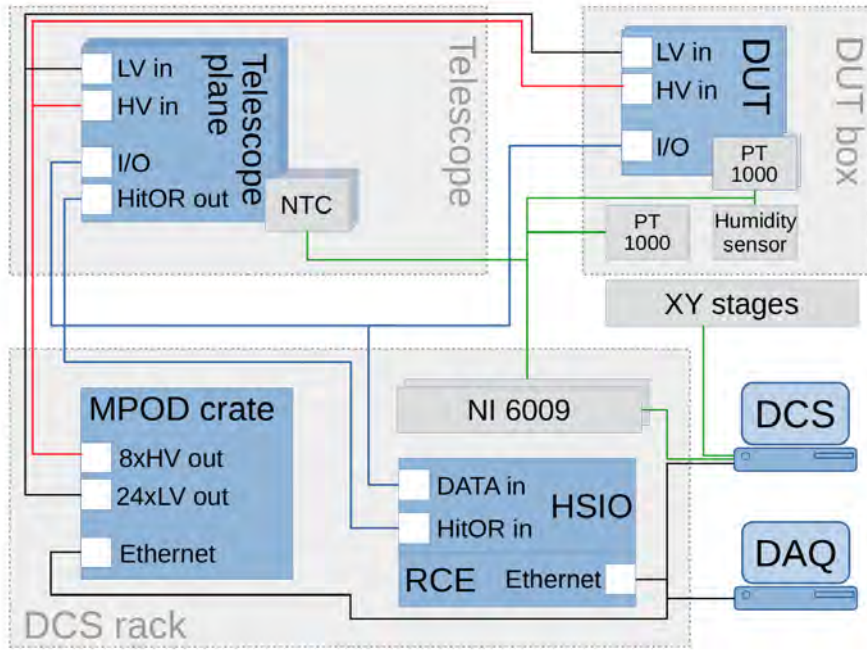


Figure 8.10: System blocks of the telescope setup [166].

level command and data protocols for the FE-I4, dispatching commands coming from the RCE, and buffering the data from the FE-I4s connected to it. The HSIO is also responsible for the clock and triggers that are distributed globally to all detector front-ends.

In case of the FE-I4 telescope, the HSIO is used in conjunction with the CosmicBoard: a second custom-made PCB that is connected to the HSIO via an ACTA Zone-3 connector. The CosmicBoard interfaces up to 16 telescope planes with the HSIO system using Ethernet RJ-45 sockets, driving the Clock (CLK) and Command (CMD) output

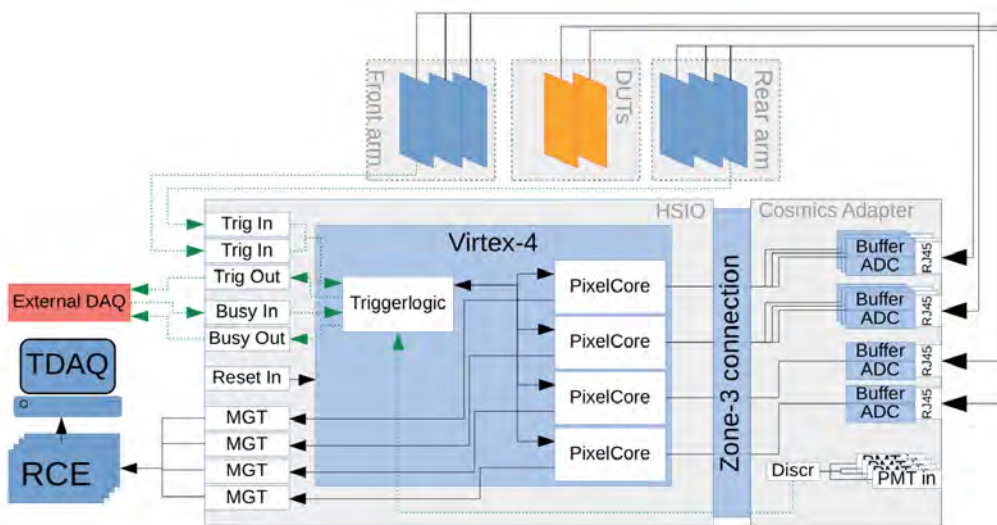


Figure 8.11: Telescope DAQ system. Shown are the data and trigger (green dashed lines) connections between the detectors, the low level (HSIO) and high level (RCE, PC) readout system [167].

lines and the data input line, needed for the FE-I4 operation. In addition the CosmicBoard has four LEMO inputs that are connected to discriminators, generating signals (from external detectors, as scintillators for example) that can be used for read-out triggering.

The RCE is a generic computational unit based on a 350 MHz PowerPC System-On-Chip (SOC), which can handle up to 24 lanes of high-speed serial I/O with speeds up to more than 40Gb/s per channel. An RTEMS Real-Time kernel runs as operational system, with software packages responsible for defining the actual tasks of the system uploaded as part of the boot-up procedure. The RCE configures the HSIO and sends commands to the interfaced front-ends. Four RCEs share the workload of reading out the six telescope planes + DUTs, histogramming and transferring the raw front-end data coming from the HSIO, via Ethernet, to the DAQ PC.

The DAQ PC is a standard x86_64 computer running on a Linux OS. The ATLAS TDAQ [170] system is installed and used for communication and data handling, communicating with the RCEs via Ethernet protocol. Custom-made software allows the per-plane (such as threshold or pixel masks) and global configuration (such as the trigger mode and delays) using human-readable configuration files. Two softwares are used to operate the telescope system: the *CalibGui*, used to perform calibration scans on the FE-I4 devices; and the *CosmicGui*, used to take and store the data from pixel hits.

The CalibGui is used to run scans for full calibration and validation of the FE-I4, including basic functional tests of the analogue and digital parts of the pixel cells, threshold and ToT response equalisation. Before data taking the telescope planes are tuned, ensuring the FE-I4 modules are configured in a known and optimal state.

After chips configuration the data taking is done with the CosmicGui software. Acquisition parameters can also be configured within the software. Trigger delays, front-end latency values and readout window lengths can be set separately for the telescope planes and DUT, in order to accommodate possibly different response times of the controlled devices. During data taking an online monitor provides real-time hit maps, correlation plots between the hit positions of neighbouring planes, timing and charge information plots.

The CosmicGui is also responsible for the selection of the trigger scheme to be used, which comprises several inputs that can be combined using logic operators. There are three trigger schemes: the cyclic trigger; the scintillators mode; and the HSIO mode. The cyclic trigger issues a trigger signal and command periodically, every multiple of 25 ns, and it is used mainly for debugging purposes. The scintillators mode is intended to be used with (scintillator) detectors connected to the signal input available at the CosmicBoard.

The HSIO mode is the one typically used in the telescope during data taking. It uses two digital input lines (LEMO) available at the HSIO board, which can be used individually or combined via AND or OR operators, in order to detect trigger signals. In the telescope

setup these digital inputs are used to read-out the HitOR signal coming from one or two telescope planes. In a typical operation the HitOr signal of the first and last planes are used in coincidence for the trigger of the telescope read-out.

As the HitOr signal from each pixel in the full matrix can be set individually, it is possible to define an arbitrary region-of-interest (ROI) trigger window, which is especially useful for devices smaller than the telescope's acceptance, maximizing the amount of triggered events with particle tracks in a specific region of interest (usually as big as the DUT acceptance). This capability is shown in Figure 8.12 where the ATLAS logo was converted into a HitOr pixel mask and was applied into the pixel matrix during test-beam.

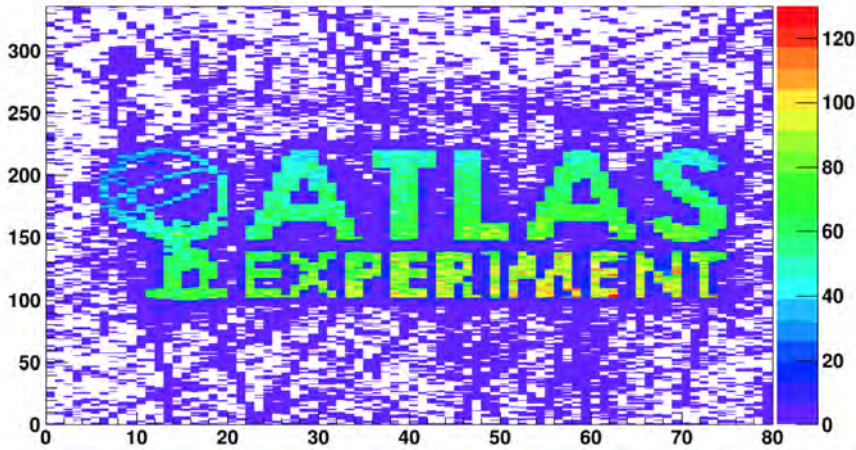


Figure 8.12: Hit map of the first telescope plane in a data set with a complex ROI mask derived from the logo of the ATLAS Experiment. The low occupancy background around the logo originates from delta electrons and nuclear interactions with the sensor.

8.3.3.1 DUT integration

The FE-I4 read-out chip is widely used by the ATLAS Pixel community for future sensor R&D. DUTs with the FE-I4 as ROC are read out exactly like telescope planes, and the integration of these DUTs is straight-forward. Non-FE-I4 based DUTs are not implemented in the RCE readout and have to be read-out by their own dedicated readout system. In this case there are two schemes, illustrated in Figure 8.13, for synchronising the data streams coming from the telescope and the external DUTs, ensuring a correct stream history for proper event merging in the off-line analysis.

In the first scheme, called *Trigger/Busy scheme*, the telescope triggers itself (using the first and last plane HitOr signals for example) and sends a trigger signal (TTL or CMOS) to the external DAQ system. The DUT DAQ then raises a busy signal, that halts further triggers by the telescope, while it reads out the DUT. Once the DUT read-out is completed, the busy signal is lowered, enabling the telescope DAQ to issue further trigger signals.

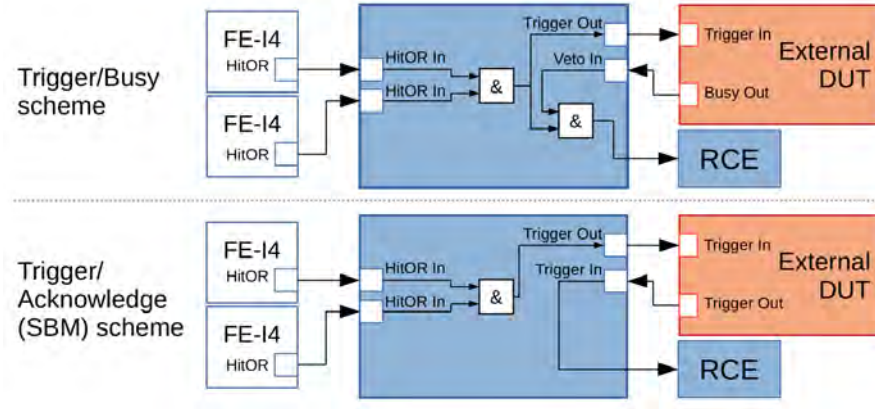


Figure 8.13: Trigger schemes for non-FE-I4 DUTs, ensuring synchronised data streams to be merged off-line for analysis [166].

The second scheme, *Trigger/Acknowledge scheme*, is more DUT-like driven. Here, the HSIO evaluates the trigger inputs and send a trigger flag out to the external DAQ, without triggering the telescope read-out. If this DUT system is ready for data taking it starts its DAQ and acknowledges the trigger signal to the RCE, which starts the read out the telescope. This is the more robust scheme, as it checks for the system readiness, before starting the readout.

8.3.4 Power supply

In order to have a versatile system capable of supplying power to multiple systems with diverse requirements, a system with mixed LV and HV modules is used. The used WIENER MPOD mini-crate is a compact 19" chassis that is equipped with four power supply cards in the 6U Eurocard format. The MPOD can be monitored and controlled locally or remotely, via Ethernet, CAN bus or USB 2 interfaces.

For the HV biasing of the (6) telescope planes and (up to 2) DUT sensors, an 8 channels ISEG EHS-8210n-F 1 kV HV module is used, providing a maximum output of 1000V (8 mA max. current). For general LV power lines, such as to be used for the ROC powering, two 8 channels WIENER MPV 8008D LV modules are installed (with 16 channels in total), supplying voltages up to 8 V at 10 A per channel. An additional WIENER MPV 8210D LV module can provide up to 120 V and 100 mA max. current. All channels have a floating ground and are monitored in terms of output voltage and current.

The interface between the HV module with the patch panel is done via Super-HV (SHV) cables. At the patch panel, the SHV connectors are converted to LEMO outputs, which are then connected to the telescope planes and DUTs. The other (LV) modules uses two 37-pin sub-D connectors as output (one sub-D for 4 channels). Each LV channel uses 4 lines (positive and negative powering and sensing lines) and the cable used for the interface splits the lines in the sub-D connector,

on the module side, into groups of 4 banana connectors to be plugged into the patch panel. On the patch panel 6 LV channel connectors are converted into a 4-pin Molex connector, dedicated for the LV power of the telescope planes, while the other 18 LV channels are left for the telescope users and their DUTs with banana connectors.

8.3.5 Auxiliary systems

The temperature of each telescope module, measured through a Negative Temperature Coefficient (NTC) temperature sensor attached to the corresponding flex-hybrid, is continuously recorded by a National Instruments (NI) USB-6009 OEM multi-channel (14-bits resolution) USB DAQ device. A second NI DAQ device is used to monitor the environmental conditions by reading additional PT1000 temperature and humidity sensors located at several locations inside the DUT box and close to the DUT.

The position of the DUT box can be controlled in the XY-plane (perpendicular to the direction of the beam) by means of two high-precision linear stages equipped with stepper motors, with an absolute position accuracy of approx. $2\mu m$. An OES ALLEGRA-2-10-02 two-axis programmable control system driver is used to control the stages. The controller has a serial interface for remote control.

The chiller typically used for the cooling of the DUT box is an HUBER UNISTAT 705, capable of a minimum silicon-oil cooling temperature of $-75^{\circ}C$, consuming a maximum current of 14 A. The chiller can also be remotely controlled via a serial interface.

A network switch is also presented on the rack in order to organize and control the different networks connecting the telescope, DCS and DUT sub-systems. Also, a remote controlled power strip is used in order to facilitate the debugging and recovery of the system, in case of any failure, by allowing to remotely plug out and back in the system equipments⁵.

8.3.6 Slow Control Software

A standard x86 laptop running on an Windows OS acts as control for the MPOD crate, the linear stages and chiller, while recording the temperature and humidity data using the NI ADCs. The slow control software has been developed using the NI LabVIEW 2012 Professional Development System in an object-oriented programming approach. The program Graphical User Interface (GUI) is shown in Figure 8.14.

Upon startup, the various devices described above are probed and connected to the interface. The slow control software establishes an HTTP connection to the DAQ PC to access the current run number of the telescope DAQ. The communication with the MPOD mini-crate is made using the SNMP protocol. The stages controller is interfaced

⁵ Solution for 99.99% of the problems encountered during data taking operation.

with the DCS framework via a RS-232 serial port and the chiller can be controlled remotely via its RS-232 or RS-485 serial socket. The NI ADCs are connected via USB to the laptop and NI provides LabVIEW drivers that are used for the interface with the DCS layer.

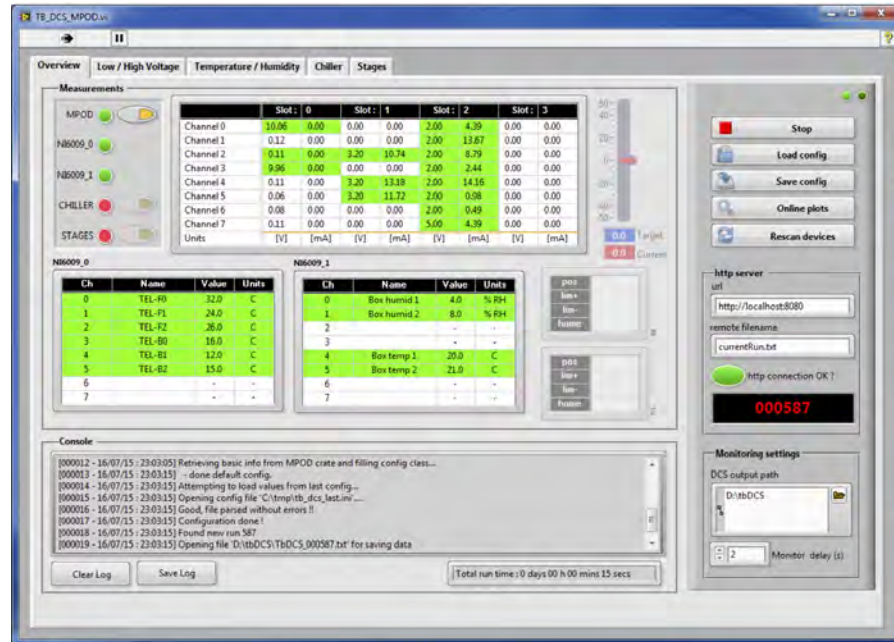


Figure 8.14: DCS GUI. The Overview tab shown provides a summary of all the different data measurements and the device status.

The control of the power supply enables per-channel current limits, voltage-ramp speeds, etc. Various program parameters (e.g. channel names, PS current limits and composition of channel-sequences) can be defined in text configuration files. An output file is created for each run. Data is recorded in a simple ASCII format with a user-defined delay, typically set to a few seconds.

All the infos concerning the several systems of the telescope - such as HV and LV channel status, position of the stages or temperature of the telescope planes and/or DUT - are available on the first tab/page of the DCS GUI, while more detailed informations and parameters controls are available on the different tabs, each responsible for one specific system.

8.3.7 Telescope characteristics

The FE-I4 telescope was characterised at the CERN SPS H8 beamline (180GeV π^+) in 2014 and 2015. During multiple testbeam periods, full size FE-I4 as well as small-area ($\sim 3 \text{ mm}^2$) sensors were tested. Sample data sets of several million triggers were used for analysis.

In all events reconstructed, 96.1% had only a single track traversing the telescope, while 3.7% were two track events[166]. The rest of the events had more than two tracks and up to eight tracks were recon-

structed on a single event. Although the SPS aims for providing a mostly constant beam intensity, of typically $\sim 100\text{kHz}$ during a spill, high intensity bursts can occur.

Due to the time resolution of the FE-I4 chips of 25ns , particles in such events cannot be differentiated by time of arrival. Tracks which pass close to each other therefore cannot be reconstructed reliably and are discarded. A typical requirement on the tracks for analysis is the detection of the traversing particle by all six telescope planes, which is the case for 96% of the reconstructed tracks, with 3.2% of the tracks formed by particles detected at 5 planes. This cut on the tracks yields an average detection efficiency per plane of 99.4%[\[166\]](#).

8.3.7.1 Trigger rate

The speed of the telescope has been verified in operation with different readout parameters, such as the number of DUTs and the readout window widths.

A readout window of 100 ns length (or four LHC Bunch Crossings (BC)) for the telescope was found to be sufficient to collect all hits[\[167\]](#) from the planar silicon sensors. Reading-out only the telescope planes with 4 BCs windows, the telescope DAQ achieves a trigger rate of about 18 kHz , establishing an upper limit for the telescope data taking rate. A higher trigger rate would require the exclusion of telescope planes, but at the expense of a reduced spatial resolution.

When adding one or two FE-I4 based DUTs to the readout with the full readout window of 16 bx (400 ns), the trigger rate reached up to approximately 6 kHz . Small devices that geometrically cover only a fraction of the telescope's acceptance profit greatly from the Region Of Interest (ROI) trigger. In case of a 3 mm^2 device, such as the CCPDv4 chip, $\sim 98\%$ of the tracks recorded by the telescope do not cross the DUT region. By restricting the read-out of events with tracks traversing a projected area of the DUT (+ small margin) on the first and last planes of the telescope, the amount of measured events with hits on the DUT increased from 2% to about 70%. A summary of the effects of the different DUT geometries and the ROI trigger can be found in [\[167\]](#).

A new DAQ system is being developed in the ATLAS TDAQ framework, named FELIX (Front-End Link eXchange), and integration tests with the telescope show an increase to 400 kHz trigger rate, being a probable upgrade for the telescope in the near future [\[171\]](#).

8.3.7.2 Spatial resolution

The UniGE FE-I4 telescope spatial resolution is defined as the errors of the track fit parameters interpolated at the position of the DUT. As the track fit depends on the hit position measurement and its precision, the accuracy in the position of the telescope planes and the granularity of the sensors defines its resolution, in first order.

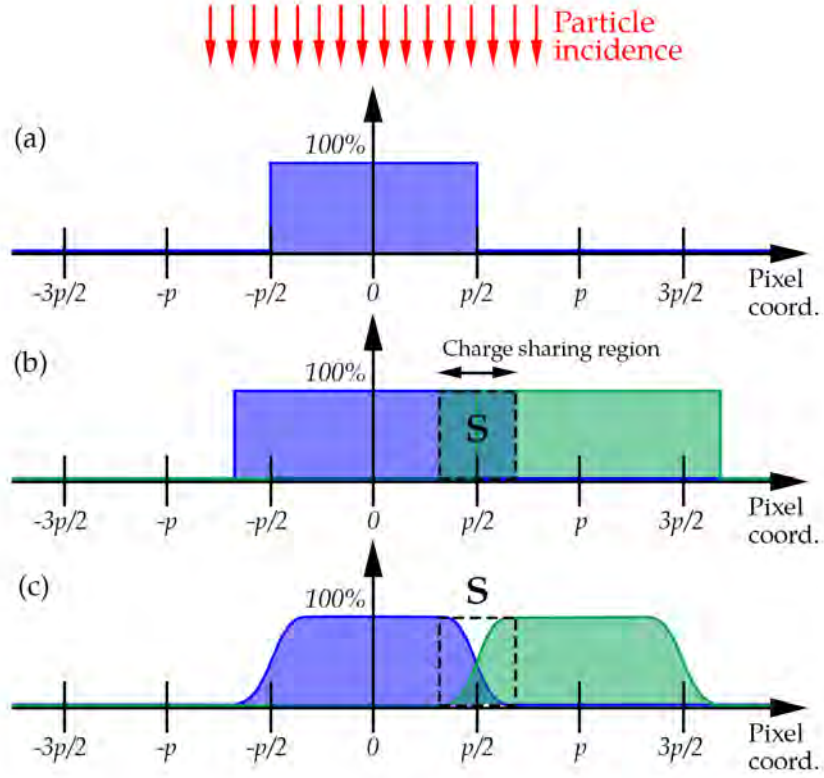


Figure 8.15: Signals in two adjacent pixels as function of the impact position. A) Detector with binary readout without charge sharing; B) binary readout with charge sharing; C) Pixel with analogue charge readout.

The hit position resolution of a pixel detector can be determined, in first order, by the pixel size. The single hit resolution (σ) of an idealized pixel detector is a box-like response with width given by the pixel pitch (p). For an 1D pixel centred at 0 and assuming a uniform density of incident particles and its detection $D(x) = 1$, only particles with incidence between $-p/2$ and $p/2$ can be detected, as shown in Figure 8.15(a). The average difference between the incidence position, x_i , and the measured hit position, x_m can be written as:

$$\sigma^2 = \frac{\int_{-p/2}^{p/2} (x_i - x_m)^2 D(x_i) dx_i}{\int_{-p/2}^{p/2} D(x_i) dx_i} = \frac{\int_{-p/2}^{p/2} x_i^2 dx_i}{\int_{-p/2}^{p/2} dx_i} = \frac{p^2}{12} \quad (8.1)$$

Equation 8.1 defines that the intrinsic resolution of a pixel detector is $p/\sqrt{12}$, in each of the two spatial dimensions measured. For the FE-I4 detector, with a pixel pitch of $250 \times 50 \mu m^2$, 8.1 yields a single hit resolution of

$$\sigma_x = 72.2 \mu m \quad \text{and} \quad \sigma_y = 14.4 \mu m. \quad (8.2)$$

During the particle interaction with the sensor, two (or more) pixels can be triggered by the same particle, originating the (so-called) pixel cluster. The occurrence of clusters with more than one pixel improves

the resolution. This is usually the case when a particle passes through a region, as indicated by s in Figure 8.15(b), where the movement of the charges created can induce a charge signal in more than one pixel.

If the pixels only output digital⁶, and for the events triggering two pixels, one expects a resolution of $s/\sqrt{12}$, and for the events triggering only one pixel, $(p-s)/\sqrt{12}$. The spatial resolution can be improved with an analog readout of the pixel, allowing to measure the total charge created on the sensor. Such a situation is displayed in Figure 8.15c.

With a charge measurement from the pixel, a charge weighted cluster center-of-mass (CM) can be estimated. By knowing the fraction of charge shared between the two pixels, one expects a resolution better than $s/\sqrt{12}$, while for the events triggering only one pixel the resolution is still limited by $(p-s)/\sqrt{12}$. For this reason, it is desirable to artificially boost the size of the clusters, by tilting the sensors for a non-perpendicular beam incidence (for example), generating larger clusters and a more accurate cluster CM position weighting.

The distance between the position of the track projected on a given plane and the calculated particle position from the hit cluster is named *residual*. For a single pixel cluster, ideally, the residual distribution should be square-shaped, with a size equal to the pixel pitch, convoluted with a Gaussian distribution accounting for the track reconstruction resolution. Figure 8.16 shows the residual distribution, in the horizontal (X) and vertical (Y) directions, for the telescope's innermost plane of the front arm, with a ToT-weighted cluster CM.

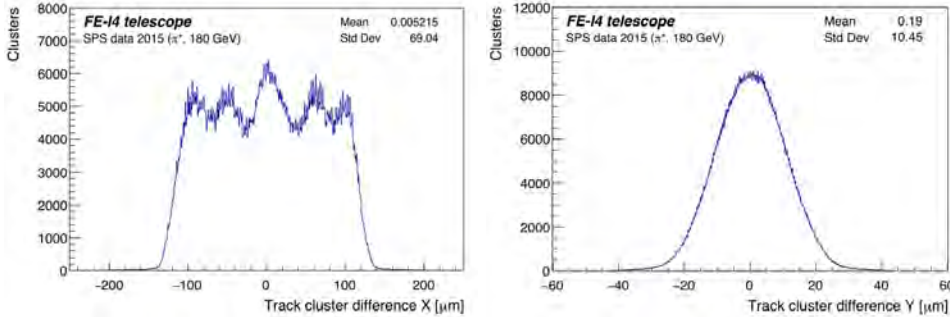


Figure 8.16: Residual distribution in X (left) and Y (right) directions for the third telescope plane [166].

The vertical distribution follows the expected shape of the convolution of a box function with a Gaussian distribution, with the Gaussian contribution dominating due to the telescope's resolution and the small pixel size ($50\mu\text{m}$). The horizontal distribution shows a box structure with width of about $240\mu\text{m}$, convoluted with a Gaussian function (smoothing the box edges) and an additional five peak structure. This peak structure is a geometric effect resulting from the increased granularity along the long size of the pixel, brought by the rotated middle planes of the telescope arms [167].

⁶ Digital in the sense that the hit information only indicates if there was (or not) a hit detected above a given threshold.

Both distributions are centred around zero with a standard deviation (SD) of $\sigma_{x,res} = 69.0\mu m$ and $\sigma_{y,res} = 10.5\mu m$, being smaller (indicating a better resolution) than the values previously estimated by Eq. 8.1. This is attributed to the charge sharing effect, which for the telescope sensors leads to around 20 % of clusters containing more than one hit, as shown in Figure 8.17.



Figure 8.17: Distribution of the cluster sizes for a random telescope plane.

The sigma of the residual distribution accounting only single pixel clusters, therefore, should converge to the theoretical value predicted on Equation 8.1. Nevertheless, the most-probable area for a particle hit to produce a one pixel cluster is smaller than the actual pixel size, being confined to the geometrical center of the pixel (as further away from neighbouring pixels avoiding charge sharing), leading to a reduced effective pixel size and, thus, an increased resolution for single pixel (SP) clusters, with the SD of their residual distributions $\sigma_{x,res,SP} = 70.2\mu m$ and $\sigma_{y,res,SP} = 10.6\mu m$ [167]. This indicates an effective pixel area (generating mainly single pixel clusters) of approximately $243 \times 36 \mu m^2$ (instead of $250 \times 50 \mu m^2$), meaning a charge sharing region surrounding the pixel periphery of about $7 \mu m$ (or 2.8%) in the pixel long axis and $14 \mu m$ (28%) on the pixel short distance.

Finally, the telescope resolution, defined as the pointing resolution at the DUT location, can be calculated from the errors of the track fit projected to the position of the DUT z . The telescope pointing resolution at a given position Z along the beam-axis is given by [168]:

$$\sigma^2(z)_{x,y} = \sigma_{O(x,y)}^2 + Z^2 \cdot \sigma_{s(x,y)}^2 + 2Z \cdot C(\sigma_O, \sigma_s)_{x,y} \quad (8.3)$$

with $\sigma_{O(x,y)}$ being the uncertainty on the track's origin (in the x and y directions), σ_s is the uncertainty on the track's slope and $C(\sigma_O, \sigma_s)$ the covariance matrix of the track parameters. Although the tracking algorithms (described in the next sections) do not directly account for alignment imprecisions and multiple scattering, these uncertainties

are present in the distribution of the calculated hit positions and consequently are absorbed in the fit parameter uncertainties. This leads to a pointing resolution at the center of the telescope of

$$\sigma_{x,DUT} = 11.7\mu m \quad \text{and} \quad \sigma_{y,DUT} = 8.3\mu m \quad (8.4)$$

In order to verify the possible consequences of multiple scattering in the final telescope resolution, an AllPix simulation using a 180 GeV π^+ beam and including the different materials in the telescope plane module was performed [168]. The simulated geometry included six planes of the telescope + an additional plane as DUT, placed at the middle of the telescope. A scattering angle of 14.8 mrad was calculated, leading to a deflection of $\sim 12 \mu m$ for a configuration with a total length of the telescope of 80 cm [167]. Since the telescope plane hit resolution is in the order of $70 \times 10 \mu m$, the multiple scattering might be neglected.

These values were compared to the prediction of the analytical model for broken line fitting as introduced in reference [58], which assumes a parallel beam illuminating perpendicularly the sensors (idealized with thickness small compared to the distance between different sensors), and includes multiple scattering in the detector material. For the telescope geometry the model returns a value of $13.0 \mu m$ (horizontal) and $9.4 \mu m$ (vertical), which underestimates the telescopes performance by about 12%. The reason for this discrepancy can be found in the resolution enhancing charge-sharing effect, which is not accounted for in the model, and has a bigger effect in the resolution than the multiple-scattering. Therefore, straight tracks can be assumed at the SPS test-beam[168].

8.3.8 Telescope automation

When characterising a DUT, a large phase-space of configuration parameters (such as HV, threshold, feed-back currents and etc) must be covered in order to provide a full picture of the DUT properties. Having in mind a trigger rate in the order of 5 kHz, and a desired data sample with $> 2M$ events, for statistical relevance, a single point in the DUT configuration-space can take at least 1 hour (for 2M triggers), if the test-beam is not interrupted for technical reasons (such as DAQ or beam failure). Therefore, to scan a complete configuration space for a single DUT can take one day, considering an interrupted data taking shift.

With the large amount of DUTs to be tested, each with specific configuration requirements, to keep the data taking continuously running is a task that has a high man-power cost. Therefore, the DAQ system was improved in a way that it is easy to have a full control of the system completely remotely, so no operator needs to be physically at the test-beam, with the exception of when it is needed to change a DUT or for specific system debugs. In addition, as the data-taking is always susceptible to human error (such as wrongly setting

a determined value or lack of logging)⁷, an effort was done for the automation of the data-taking process.

As most components of the telescope setup are connected via Ethernet an automation scheme was implemented including logging and alert messages in case of system problems. The core of the automation framework is a Python based scan supervisor which can communicate with all relevant components of the DAQ and DCS system. Figure 8.18 shows the control and data flow in the automated test beam runs. It runs a configurable scan loop that comprises the change and control of settings, running and monitoring the actual data taking, reporting to a log file and, upon finishing a parameter sweep, analysing the collected data to provide a continuous data quality monitoring.

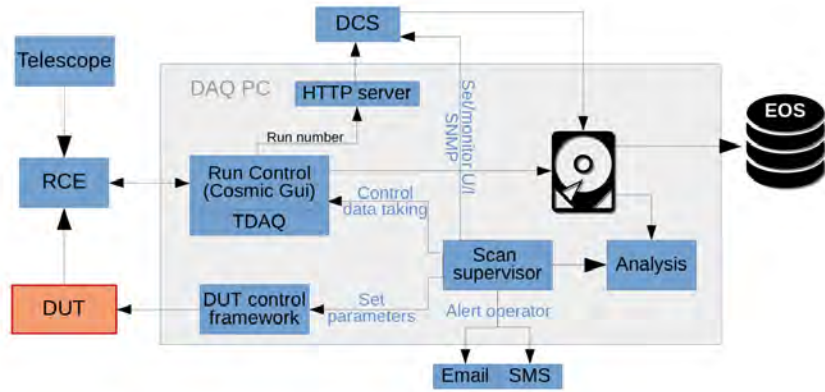


Figure 8.18: Scheme of the control and data streams in the automatic data taking with the FE-I4 telescope [167].

On-DUT parameters are set by directly sending commands to the DUT controlling software framework, with specific communication protocols, while bias voltages provided by the Wiener crate are modified via Simple Network Management Protocol packages. Data is taken with the telescope specific DAQ system which is invoked in a sub shell and monitored by means of interpreting log files and exit codes. Upon finishing a run or at the occurrence of an error, the operator is informed by email and/or SMS and can react promptly.

All data is saved locally on the DAQ PC and can be further backed-up in the CERN's central storage EOS. In addition, the following track reconstruction software can also be invoked once the runs are finished, allowing to quickly check the data quality in order to evaluate if the next scan point can start or if the data needs to be re-taken.

8.4 TRACK RECONSTRUCTION SOFTWARE - *proteus*

A track reconstruction software is needed in order to identify particle trajectories from the collection of hits detected by each telescope plane. For the work performed on this thesis the raw telescope data is handled by the Proteus [172] reconstruction software.

⁷ Especially during over-night shifts.

Proteus is an open-source object oriented framework, written in modern C++, aiming for modularity in order to easily implement multiple algorithms to condition diverse data formats for proper analysis. Currently Proteus is able to handle the data types from the UniGE FE-I4 telescope, from the TimePix3 SPIDR DAQ system[173], and from the EUDAQ library[174]. It is therefore composed of specialised algorithms for data handling, synchronisation, setup description, reconstruction and analysis. All data are stored in ROOT file format, with the geometry description and configuration of the framework given in text configuration files.

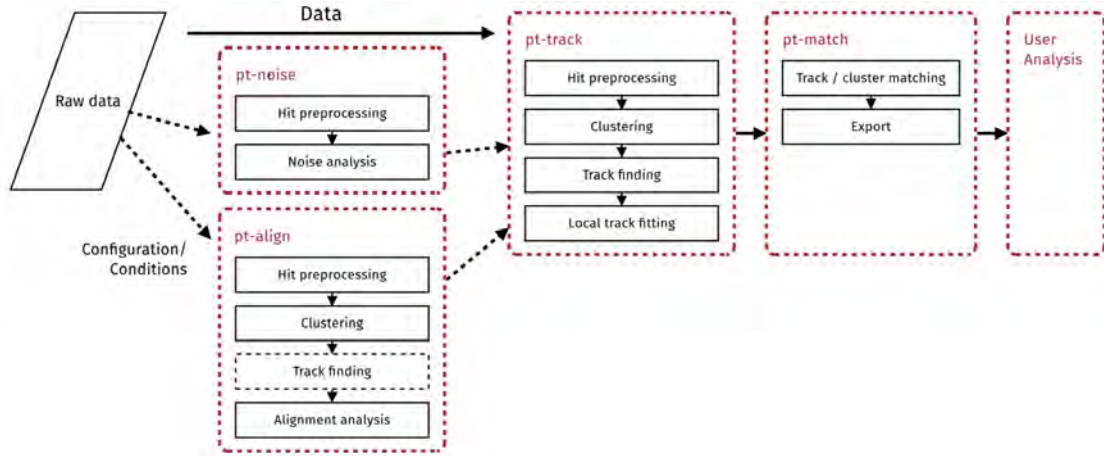


Figure 8.19: Data flow in Proteus.

The usual work-flow from raw data to results is shown in Figure 8.19, and is described in the following sections. Two data processors are available to be used before the track reconstruction. The first is named *pt-align*, responsible for scanning the data for noisy pixels and creating a mask to not account noisy pixels in the reconstruction. Following the noise mask, the nominal telescope geometry can be corrected, in order to account possible misalignments from the nominal telescope description, using the *pt-align* algorithm. This step, for example, can be skipped if the given geometric description is already accurate, as is the case for simulations where the geometry is well known or if the alignment was already performed for a given run and the subsequent ones don't have any modification on the telescope setup. After the track reconstruction, performed by *pt-track*, the *pt-match* is used in order to match (or not) clusters measured on the DUT with the tracks found. Further analysis may follow with user specific scripts to extract further information provided from the matched clusters.

8.4.1 Noise mask and clustering

Detectors are rarely free of noise, especially after irradiation, and noisy pixels are unsuited for characterization as they can disturb alignment and analysis algorithms. Therefore, a noise masking al-

gorithm calculates a per-pixel occupancy and excludes a pixel from further analysis if the pixel passes a given counting threshold.

In order to cope with non-uniform beam profiles, such as the one shown in Figure 8.20a, Proteus calculates an expected local occupancy (Figure 8.20b) at the position of the analysed pixel via a kernel density estimator. The pixel's occupancy is then stated as local significance, shown in Figure 8.20c, which yields a robust cut variable.

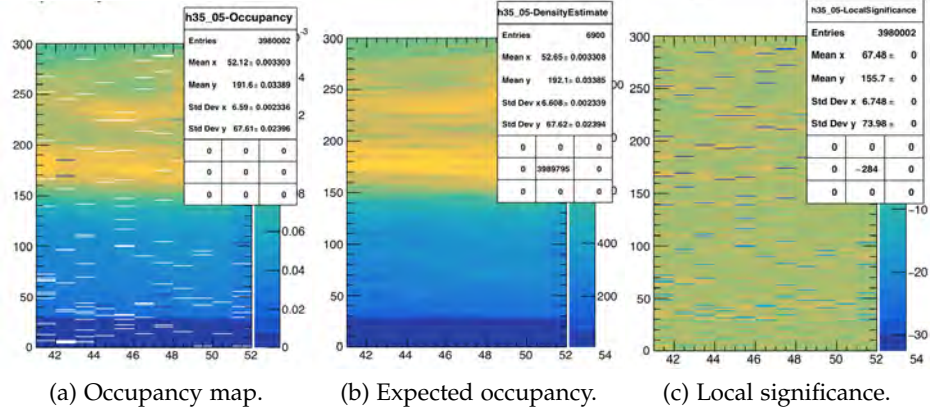


Figure 8.20: Noise masking process: raw occupancy map (a); the calculated expected occupancy (b); and the pixels local significance (c).

Pixels triggered by the same particle, composing a pixel hit cluster, have to be identified in order to calculate the actual hit position. A recursive procedure starts with a random hit as seed of the cluster and adds all neighbouring hits to it until no further hits in the vicinity of the cluster are found (although a maximum distance for the next neighbour can be defined to cope with broken clusters, which can occur if a pixel from a given cluster is masked).

For clusters consisting of more than one pixel, the actual hit position on the sensor has to be reconstructed. The basic method, called binary or digital hit making, uses the barycentre (or geometric centre) of the pixels with hits:

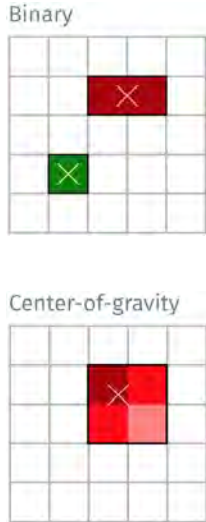
$$(x, y)_{digitalcluster} = \frac{1}{N} \left(\sum_i^N x_i, \sum_i^N y_i \right) \quad (8.5)$$

On the telescope planes, the integrated charge deposited on each pixel is accessible through the ToT as measured by the FE-I4. This allows us to improve the cluster position resolution by weighting the contribution of each hit by the associated deposited signal:

$$(x, y)_{analogcluster} = \left(\frac{\sum_i^N x_i \cdot Q_i}{\sum_i^N Q_i}, \frac{\sum_i^N y_i \cdot Q_i}{\sum_i^N Q_i} \right) \quad (8.6)$$

8.4.2 Telescope software alignment

For precise tracking of particles down to the level of 10 microns precision, the relative position between detector planes of the telescope has to be accurately known, as well as the beam profile (such as slope



and divergence). Even with the telescope mechanical parts being built with high precision machining, an alignment precision under $100\ \mu\text{m}$ is not easily achievable for such systems where human mechanical interventions happen constantly. Therefore, the reconstruction software performs an offline measurement of the possible deviations and accounts for them during the track reconstruction.

Starting with the positions and rotations of the planes measured by an initial telescope survey, the nominal geometry of the system is corrected via two steps. The first is responsible for a first coarse alignment, shifting the detector perpendicularly to the beam with a precision in the order of the pixel pitch, while the second method has the power of also correct for possible rotation misalignments with a precision in the order of the telescope tracking resolution.

The first (coarse) alignment uses the hit correlation distributions calculated between consecutive telescope planes, with the first plane fixed and defined as origin of a global coordinate system to which the position of the planes is referenced. Given a parallel beam, and perfectly aligned detectors, the hit correlations would form a straight line through the origin with a slope equal to the ratio of the pixel pitches. Detector misalignment perpendicular to the beam is inferred by the correlation offset, while deviations from the calculated slope are directly proportional to rotations.

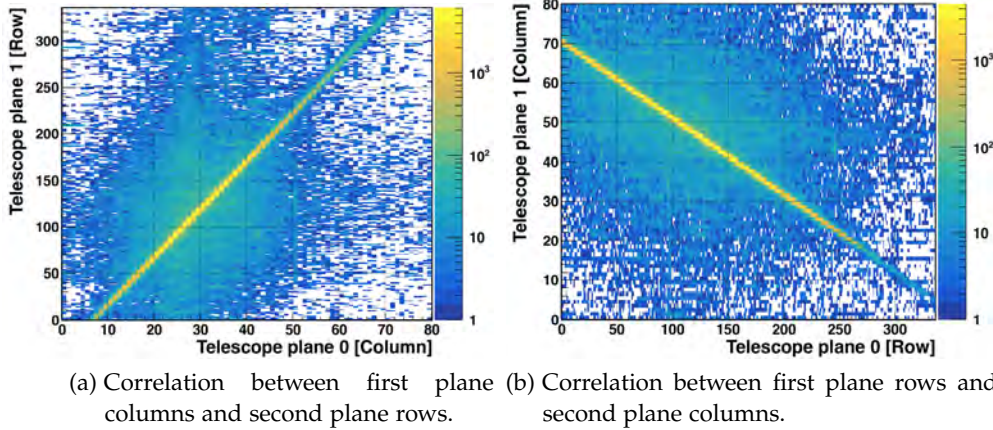
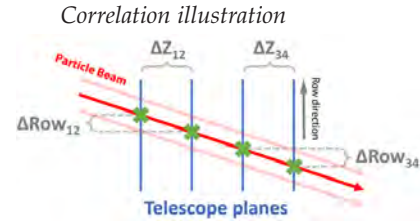


Figure 8.21: Correlation plots between first and second telescope planes, before software alignment.

Figure 8.21 shows the hit correlations between the column and row directions of the first and second telescope planes, extracted from the online monitoring plots from CosmicGui. As consecutive planes in the FE-I4 telescope are rotated by 90° , the correlation between the planes must be correlating the column (or row) of the plane N with the row (or column) of plane $N + 1$ ⁸. The correlation line is clear on both plots of Figure 8.21, and the visible background is from scattered particles and/or noise hits⁹.

⁸ With the exception of the two most innermost telescope which are vertically oriented, but facing opposite directions

⁹ The slope in Figure 8.21b is inverted as the monitoring plots don't take into account the orientation of the planes.

To further refine the alignment, as the track position is directly influenced by the position of the given plane being aligned, a fine tuning procedure is performed based on unbiased residuals¹⁰. The measured residuals ε_x and ε_y in the local coordinates of the plane are calculated by a projection of the (misalignment) displacement Δx , Δy and $\Delta\gamma$ on the reconstructed hit position (x, y) :

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & -x \\ 0 & 1 & y \end{bmatrix} \cdot \begin{bmatrix} \Delta x \\ \Delta y \\ \Delta\gamma \end{bmatrix} \quad (8.7)$$

In Equation 8.7, Δx and Δy represents the perpendicular displacement with respect to the beam axis, and $\Delta\gamma$ represents the rotation around the beam axis¹¹. The linear system of equations in Eq. 8.7 is under-determined, as it has fewer equations than unknowns, but can be approximately solved by requiring a χ^2 minimization as:

$$\begin{aligned} \Delta x &\sim \varepsilon_x(1 - x^2) + \varepsilon_y xy \\ \Delta y &\sim \varepsilon_y(1 - y^2) + \varepsilon_x xy \\ \Delta\gamma &\sim \varepsilon_y x - \varepsilon_x y \end{aligned} \quad (8.8)$$

The minimization runs iteratively over several steps, where the calculated displacement is applied to the initial geometry before the next step. The evolution of the detector position parameters through 50 alignment steps is shown in Figure 8.22, where it is possible to see that after 40 steps the alignment converges to a stable position.

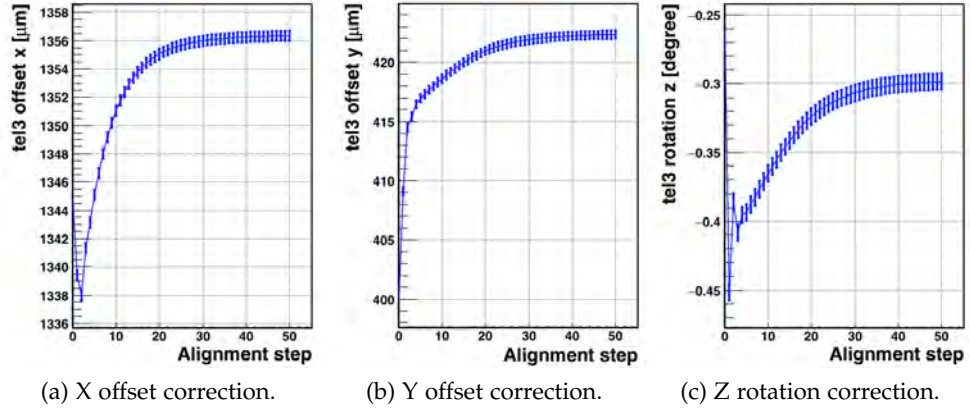


Figure 8.22: Evolution of the geometry parameters - (a) horizontal displacement; (b) vertical displacement; (c) rotation around the beam axis - over 50 alignment iterations.

8.4.3 Track fitting and DUT cluster matching

Once the positions of the telescope planes are well known, the tracks can be accurately reconstructed. Starting from a seed cluster, usually

¹⁰ Unbiased residuals are obtained by excluding the plane under consideration from the track reconstruction.

¹¹ Valid for small angles approximation.

on the first plane, the tracking algorithm searches for clusters on consecutive planes within a user-defined projection solid angle, as illustrated in Figure 8.23. The angle is chosen according to the scattering angle on the telescope planes and, therefore, should be chosen according to the characteristics of the beam-line used.

If multiple clusters are found within the search region, the track search bifurcates and continues in both cluster directions. Candidate tracks containing the largest number of associated clusters, or with the least linear regression χ^2 , are kept. The algorithm has good performance handling data with large amounts of scattering given a low track density, clearly separating tracks without ambiguities of cluster/track assignment. Once all tracks are reconstructed, a χ^2 cut is used to filter those tracks which are disturbed largely by scattering or nuclear interaction with the telescope planes.

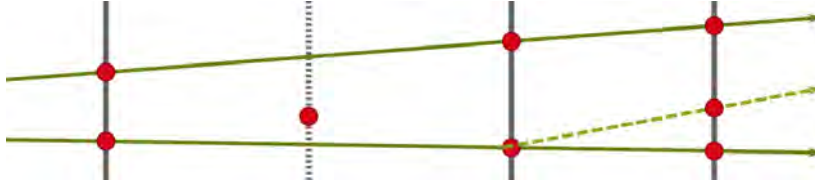


Figure 8.23: Illustration of the track finding with hits in the telescope planes.

The DUT must also have its position corrected by the software in order to provide accurate results. Therefore, the same steps performed for the telescope alignment are done for the DUT. This is usually done right after the telescope alignment and before the track finding.

The final step of the data process is to find hit clusters on the DUT and decide if these, if any, are generated by real particle interaction with the sensor. In order to associate the DUT-cluster to a track, we extrapolate the fitted track to the DUT and restrict the match to clusters within a certain distance, defined as:

$$d = \sqrt{(x_{track} - x_{DUT})^2 + (y_{track} - y_{DUT})^2} \quad (8.9)$$

where $x, y_{track, DUT}$ are the extrapolated positions of the track, in DUT-local coordinates at DUT position, and of the DUT-cluster coordinates. A minimum value for d is required in order to match a track associated to a DUT-cluster. This minimum distance cut is dependent on spatial resolution of the DUT and a typical value is the largest pixel pitch on the given DUT. With the DUT clusters matched to tracks, it is possible to define the detector global efficiency as:

$$\epsilon = \frac{N_{matched}}{N_{total}} \quad (8.10)$$

where $N_{matched}$ is the number of tracks with a matched cluster on the DUT and N_{total} is the total number of reconstructed tracks. With the association of DUT clusters to the tracks it is possible to extract further characteristics about the DUT, such as in-pixel efficiencies and timing resolution, depending on the required analysis of each DUT.

The work done during this thesis, due to finite time, was restricted to test-beam prototype tests in the ATLAS ITk framework. Results for the prototypes investigated by and for CLIC can be found in [75] and [119].

Between the end of 2015 and 2018 three different devices (introduced in Chapter 5) were investigated and characterized, in the ATLAS ITk upgrade, before and after irradiation using the UniGE FE-I4 telescope at the CERN SPS H8 and at the Fermilab MTest beam lines. These are: the CCPDV4, coupled to a FE-I4 read-out ASIC; the H35DEMO, with its analog matrices also coupled to a FE-I4; and the ATLASpox, the first full scale monolithic HV-CMOS prototype.

For the possible operation in the future ATLAS ITk, the detector prototypes were extensively tested in order to evaluate their performance concerning hit detection efficiency, good spatial precision and fast time stamping of the particle interactions. The tests were performed in different operational conditions in order to assure the detector performance over the experiment life time.

In the HL-LHC operation, the ATLAS ITk will face collision environments with up to 200 pile-up events every 25 ns. Therefore, it is essential to be able to assign the different track to the correct bunch crossing (BC) time window. This requirement imposes the utilisation of fast shaping and fast readout. This imposes an in-time cumulative efficiency of 99% within 2 BCs, before irradiation, and 95% in 2 BCs after irradiation.

The relevant fluences for the application in the upgraded ATLAS Inner Tracker (ITk) at HL- LHC (target integrated luminosity of 3000 fb⁻¹) range between about 2×10^{14} (for the outer strip layers), 1×10^{15} (outermost pixel layer), 4×10^{15} (pixel layer 1¹) and 1×10^{16} n_{eq}/cm^2 (pixel layer 0¹). The most relevant range for the ATLAS HV-CMOS pixel demonstrator project is in the region of the outermost pixel layer, i.e. around 1×10^{15} n_{eq}/cm^2 .

9.1 CCPDV4

In 2015 and 2016, multiple CCPDV4 samples (coupled to the FE-I4 ROC), un-irradiated and irradiated up to 5×10^{15} n_{eq}/cm^2 , were characterised with the UniGE FE-I4 telescope at the SPS H8 beam line. For the CCPDV4 the configuration and control, such as threshold tuning, was done with the CaRIBOu system, being the first time the CaRIBOu system was used. Although the CaRIBOu system is able to read-out the FE-I4 ROCs, in order to avoid off-line merging of the DUT and

¹ Assuming replacement after 1500 fb⁻¹.

telescope data streams, the DUT ROC was read-out by the telescope DAQ, as a normal telescope plane.

The substrate resistivity available at the production period for the 180 nm process was in the range of 10-20 Ωcm , leading to a depletion depth of about 10-15 μm , simulated for bias voltages between 80 and 150V.

The CCPDv4 is the fourth small detector of a series of HV-CMOS devices designed as prototypes towards a monolithic device that can be operated fully depleted by biasing the chip substrate. During technology characterization, it was decided to use the FE-I4 for the read-out of the prototype as the FE-I4 is a well known chip, already extensively characterized during the ATLAS IBL commissioning. In this way it is possible to disentangle sensor characteristics from the electronics read-out. The sensor (shown in Figure 5.10) has a total size of $\sim 2.4 \times 2.9 \text{ mm}^2$ and a thickness of 250 μm .

Regarding the sensor characteristics, in a simplistic way, the matrix of the Deep N-wells can be seen as a classical planar $n^+ - in - p$ pixel sensor. However, due to the low resistivity of the sensor substrate, the thin layers of depleted silicon would yield a most probable charge of only about 800-1200 electron-hole-pairs², being a detection challenge for classical pixel readout chips with low threshold settings, typically, in the order of 1000-1500 electrons.

As the HV-CMOS process allows for electronic circuits to be implemented, within the deep n-wells, in-pixel amplification is possible and can be used to amplify the signal to a suitable amplitude for a discriminator or directly for a readout chip. Therefore, as the sensor devices allow signal handling, it was decided to capacitively couple the sensors to the ROC, as described in Chapter 2, avoiding the expensive bump bonds and allowing smaller pixel pitches to be tested. As consequence, the HV-CMOS sensor device needs to be configurable, by a set of registers and DACs, in order to tune its analog and digital circuits for a proper signal processing. In this way, not only the sensitive properties of the sensor region of the device can be characterized before/after irradiation, but also the electronic circuits can be already evaluated.

The CCPDv4 contains several pixel flavours, each with different design in order to evaluate different aspects of the HV-CMOS device. Out of the different pixel flavours, this study focused on the performance of the so-called STime-type pixels, considered as the baseline implementation for an ATLAS ITk candidate pixel architecture in ams H18 technology.

Each STime pixel on the HV-CMOS sensor features a size of only 33 μm by 125 μm , containing a two-stage amplifier and a discriminator (referenced to a global threshold), with a 4-bit in-pixel Tune-DAC, allowing a per-pixel threshold tuning. To match the FE-I4 pixel size of 50 μm by 250 μm , the HV-CMOS pixels are grouped together in groups of three, forming a macro-pixel with 100 \times 125 μm pitch (as

² Considering a vertically penetrating MIP.

already discussed in Section 2.3.2). While the CCPDV4 also allows the adjustment of the pixel output towards the ROC, encoding of the hit pixel's coordinate within the macro-pixel, this feature was not used during this study and, hence, the test-beam analysis was performed on the macro-pixel level.

9.1.1 Threshold tuning

The voltage reference given to all pixel discriminators is globally distributed across the pixel matrix, assuring that all matrix is set to the same threshold. Nevertheless, small threshold variations can still occur from possible mismatches in the discriminator electronics due to imperfections during production. In order to mitigate the local threshold variation a 4-bit DAC (named Threshold DAC, or TDAC) is connected to each pixel discriminator. The TDAC will shift the effective voltage seen by the discriminator, helping to equalize the threshold over the pixel matrix. The adjustment of each pixel TDAC in order to achieve the smallest threshold variation is commonly referred as tuning or equalization.

To start with, the control of the threshold is done by adjusting voltage levels which can be calibrated into a charge value. In order to perform a voltage-to-charge calibration and have an absolute scale for the threshold (given in electrons e^-), a setup using a ^{55}Fe radioactive source illuminating the sensor, biased at 80V and at room temperature, was used. The ^{55}Fe spectrum was recorded by measuring, with an oscilloscope, the output signal of a single pixel after the amplification stage. The resulting calibration factor is $\sim 8.6 e^-/\text{mV}$ [175].

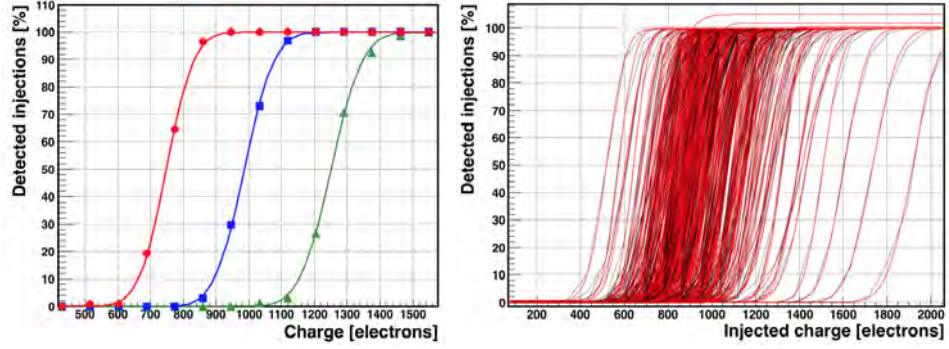
The tuning procedure consists in injecting each pixel with a known charge and measuring the fraction of times that the injection pulses fired the pixel discriminator. The CaR board contains an adjustable pulser that can be connected to individual pixel inputs on the CCPDV4 and, via de CaRIBOu DAQ software, the amplitude of the charge injected is scanned. Each pixel is injected individually and the output of the pixel discriminator is routed out of the chip and connected to a counter implemented on the same FPGA board used for the CaRIBOu system. In this way, the CCPDV4 tuning is performed completely independent of the FE-I4 ROC.

The ideal response of the charge injection scan should be a step function where the step transition happens when the injected charge is equal to the threshold value. As electronic circuits are always prone to electronic noise, this ideal response is convoluted with a Gaussian function, yielding a S-shaped curve that can be defined as:

$$S = N + \frac{N}{1 + e^{-\sigma(x-\mu)}} \quad (9.1)$$

The response of a charge injection scan for a given pixel, measured for different TDACs values, is shown in the Figure 9.1a. The markers on the plots represent the fraction of detected pulses, from N injections, for each charge injected, while the continuous lines represent

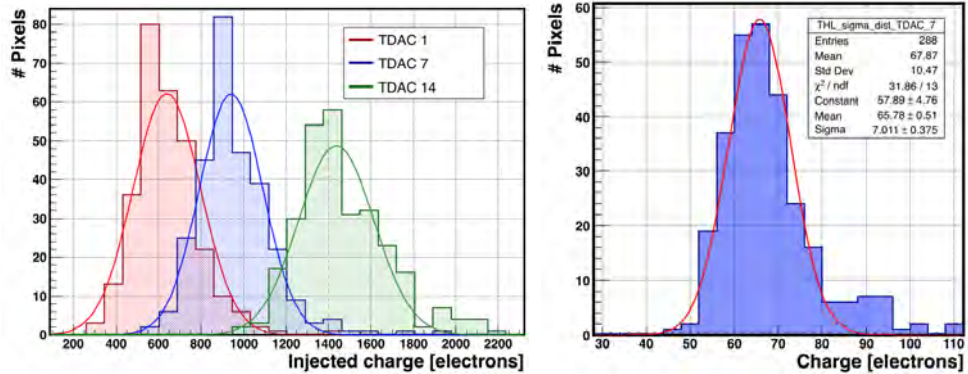
the fit from an error function. The pixel scan with TDAC = 1 is shown in red, TDAC = 7 in blue and TDAC = 14 in green. Figure 9.1b shows the response of the 288 STime pixels scanned with the same TDAC = 7 with the S-curve fit shown in red. The matrix S-curve scan shows that within the same TDAC, the threshold dispersion-range values that a single pixel has with the lowest and highest TDAC setting (as the pixel shown in Figure 9.1a).



(a) Single pixel S-curve measurement for TDAC 1, 7 and 14. (b) Overlaid S-curves measured with TDAC = 7 for the 288 pixels in the STime matrix.

Figure 9.1: Single pixel S-curve for different TDACs (1, 7 and 14) and STime pixels S-curves with TDAC = 7.

From the S-curve fit it is possible to extract each pixel threshold μ , defined as the charge value at which the S-curve reaches 50%. The threshold dispersion of all the pixels is shown in Figure 9.2a for TDACs 1, 7 and 14. As for the single pixel threshold shift, the effect of higher TDAC values is also seen as a shift in the mean threshold measured over the pixel matrix, with mean at about $620 e^-$ for TDAC = 1, $940 e^-$ for TDAC = 7 and $1430 e^-$ for TDAC = 14, with dispersion ranging from 130 to $170 e^-$. In addition, from the pixel S-curve fits it is also possible to measure how smeared the step function is by the σ of a gaussian fit. The distribution of the adjusted S-curve σ is shown in Figure 9.2b, indicating an electronic noise level (Equivalent Noise Charge, or ENC) in the order of $65 e^-$, and has shown to be constant as function of the TDAC, as expected.



(a) STime pixels threshold distributions for TDAC 1, 7 and 14. (b) S-curves σ (ENC) distribution for a single TDAC.

Figure 9.2: Threshold (a) and equivalent noise charge (b) distributions.

Each pixel TDAC is calculated with an interpolation of the threshold distributions *versus* the TDAC values and by retrieving the TDAC value that would yield a targeted threshold. The calculation of the target matrix threshold is done by evaluating the mid-point between the threshold distributions with different TDACs. Therefore, an important aspect for a successful tuning is the achievable dynamic range, and linearity, of the pixel thresholds with different TDAC values. Ideally, a separation of 4σ ($2\sigma_{TDAC=1} + 2\sigma_{TDAC=14}$) is desired for threshold distributions with the lowest and highest TDAC values. A second DAC, named VNDAC, is used for the adjustment of the TDAC range. Figure 9.3 shows the curve of the mean measured threshold versus each TDAC value for each VNDAC set. It shows that a larger dynamic range can be achieved with higher VNDAC values, at the expense of the non-linearity of the mean threshold and TDAC dependence.

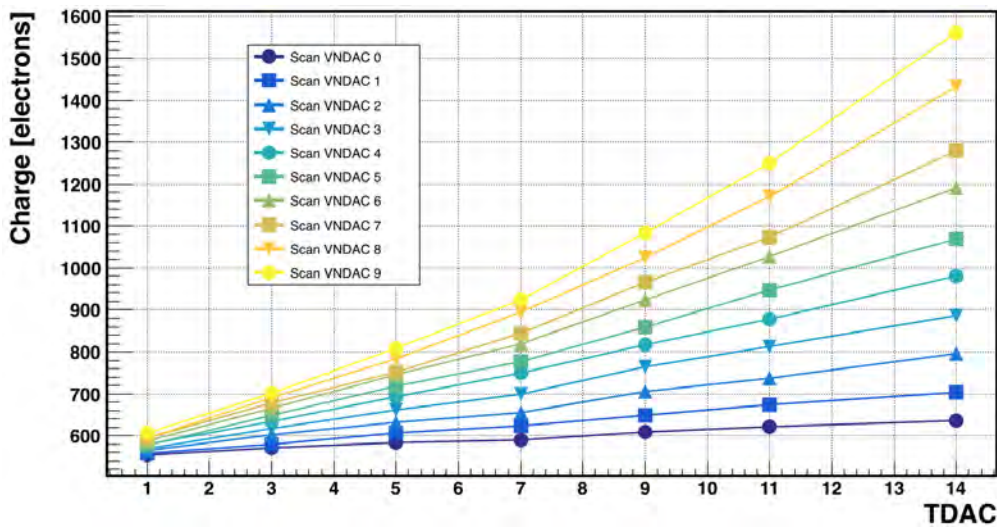


Figure 9.3: TDAC scan for different VNDAC values.

To have a linear variation of the mean matrix threshold as function of the TDAC values is an advantage as any TDAC value would be accurately interpolated to return the desired targeted threshold, allowing a good tuning to be performed with the charge injection scan with only two TDAC values. If higher values of VNDAC are used, the non-linearity between threshold and TDAC will have an effect in the interpolation, requiring more TDAC values to be used and, consequently, requiring more time needed for the tuning. A satisfactory tuning result was achieved using VNDAC = 5 and scanning only 3 TDAC values (1, 7 and 14).

The tuning result is shown in Figure 9.4, with the pixels threshold distribution for the un-tuned matrix in blue (TDAC = 1) and in red (TDAC = 14) and with the tuned threshold distribution in black. The effect of the tuning is visible by analysing the width of the threshold distribution. From a Gaussian fit of the different distributions, the σ values found for the matrix before tuning are about 120 and 140 e^- , for TDAC 1 and 14 respectively. After the tuning the measured σ is in the order of 25 e^- , representing a significant improvement when

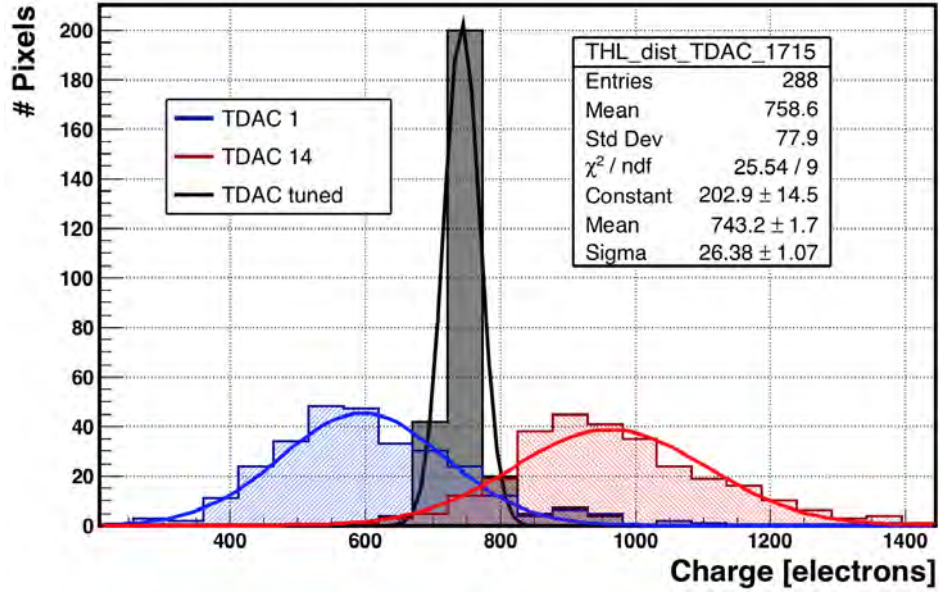


Figure 9.4: Threshold distribution for TDAC = 1 (blue), TDAC = 14 (red), and for the equalized matrix (black).

compared with the matrix before the tuning. This narrow distribution allows to lower the global threshold of the CCPDv4 without outliers pixels becoming noisy.

9.1.2 Un-irradiated results - SPS H8 - 2015

The results shown here were measured at the SPS H8 beam-line along the year of 2015. All the measurements were performed at room temperature ($\sim 20^\circ\text{C}$) and are published in [175].

9.1.2.1 Residuals

Due to the small size of the HV-CMOS sensor, limiting the amount of tracks that can be used for the DUT alignment, the alignment algorithm had no sensitivity to correct for the in-plane rotation and, hence, only the translations perpendicular to the beam axis was corrected. In order to increase the amount of tracks reconstructed by the telescope that also hit the small DUT, a ROI mask was used in the telescope trigger planes, selecting only tracks that traverse the specified DUT region. In addition, as the CCPDv4 sends a digital pulse to the FE-I4, the ToT information available from the ROC pixel read-out has no use here. Therefore, the binary clustering algorithm was used and only (DUT) single cluster track events were selected. Figure 9.5 shows the unbiased residual distributions measured along the column and row directions.

The R.M.S. of the residual distributions are in reasonable agreement with the intrinsic resolutions expected for the macro-pixel, along the X ($125\ \mu\text{m}$) and Y ($100\ \mu\text{m}$) directions, $\sigma_x = 125/\sqrt{12} = 36.1\ \mu\text{m}$ and $\sigma_y = 100/\sqrt{12} = 28.9\ \mu\text{m}$, respectively.

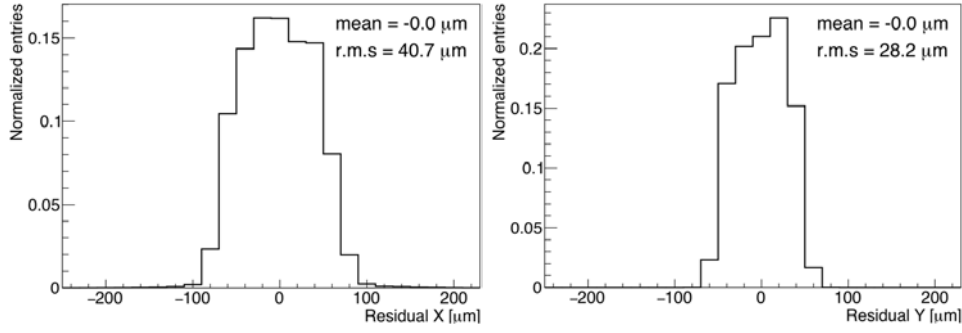
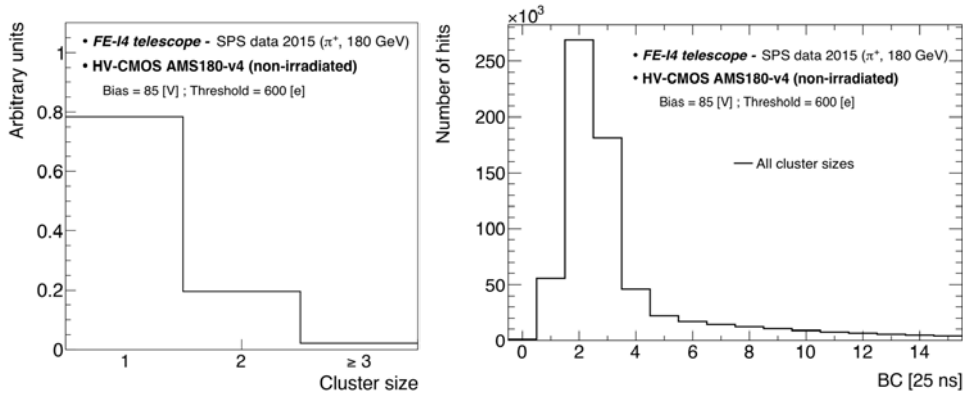


Figure 9.5: Normalized residual distributions of the DUT along the X (left) and Y (right) directions [175].

9.1.2.2 Clusters and timing

The cluster size, an effective measurement of charge sharing, is shown in Figure 9.6a for the DUT nominal operation (85V bias-voltage and 600 e⁻ threshold). At the SPS test-beam the track incidence was practically perpendicular to the detector planes. From all the DUT-clusters matched to a reconstructed track, $\sim 78\%$ of the events are composed by single-pixel clusters, while clusters formed by two pixels were observed in $\sim 20\%$ of the cases, and clusters with sizes of three or more pixels was less than 2%, similarly to the cluster sizes measured for the telescope planes.

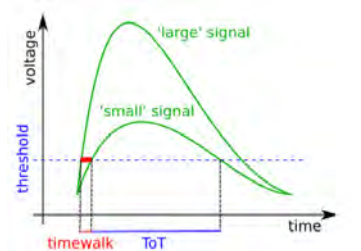


(a) Normalized cluster size distribution for normal beam incidence (b) Timing distribution of the DUT hits in units of 25 ns for all cluster sizes.

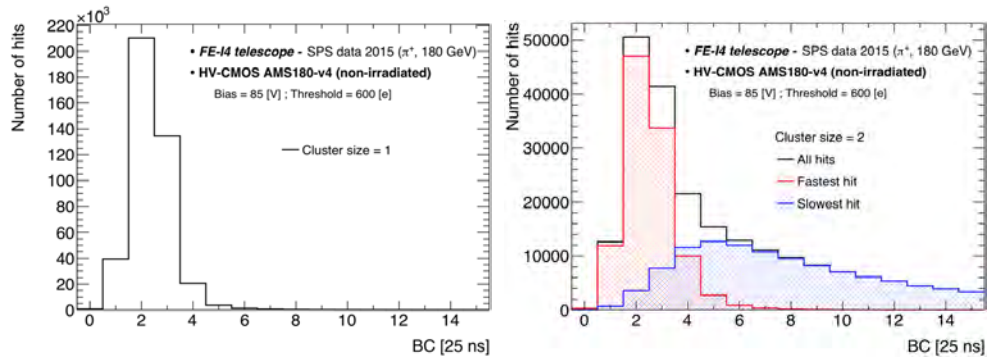
Figure 9.6: Cluster sizes (a) and timing (b) distributions [175].

Figure 9.6b shows the timing distribution in units of BC (25 ns), defined by the difference in the time measurement of the hit recorded at the DUT with respect to the trigger, for all cluster sizes. In the case of two hit clusters, where the charge detected by each pixel is smaller due to a known time-walk effect from the amplifier [168] it is expected that the hit time-of arrival measured from the pixel with smaller charge signal is detected is larger than that of the pixel with higher charge (see lateral image). The long tail of the cluster timing distribution shows the late (slow) hits.

Time-walk effect illustration, when signal with low amplitudes are detected later.



In order to better assess the timing performance of the CCPDv4 prototype, the timing distribution was split into single pixel clusters and clusters with two pixels, where the timing of each pixel can also be visualized separately. Figure 9.7a shows the timing distribution of clusters with only one pixel, confirming that the long tail for later times from the distribution with all clusters comes from clusters with size > 1 . Figure 9.7b shows that the fastest hit in the cluster has a similar distribution as the single pixel clusters, while the second hit on the cluster shows a much broader timing distribution with larger time values. This analysis confirms that the slowest signals in the tail of the distribution of Figure 9.6b correspond to the diffused charge in large multiplicity clusters. Therefore only the fastest hit of multi-pixel clusters will be considered for the analysis shown here.



(a) Timing distribution of the DUT hits for single pixel clusters. (b) Timing distribution of the measured time of each of the two pixels in the cluster is shown.

Figure 9.7: Timing distribution, in 25 ns bins, for single pixel clusters (a) and two-pixel clusters (b) [175].

9.1.2.3 Detection efficiency

In Figure 9.8a the efficiency contribution with respect to the detection time is plotted for different values of the bias voltage. The shape of the distributions are similar to that already shown in Figure 9.7a, with most particles being detected within 2 bins. The dispersion decreases with rising bias voltage and the mean is shifted towards earlier times. Both observations can be explained by the fact that with higher biasing voltage the electric field in the sensor is increased, improving the signal time with faster charge collection.

The cumulative efficiency versus integration time is shown in Figure 9.8b, illustrating the necessary integration time to achieve a certain efficiency. For this plot the efficiency contributions were accumulated, starting at the maximum efficiency bin and proceeding by adding the neighbouring bins sorted by their value. At 85V bias voltage, an efficiency higher than 90% is achieved after three BCs, with the efficiency reaching a plateau after five BCs.

Figure 9.9 shows the effect of the threshold on the timing distribution for a bias voltage of 80V. It shows a clear dependence of hit

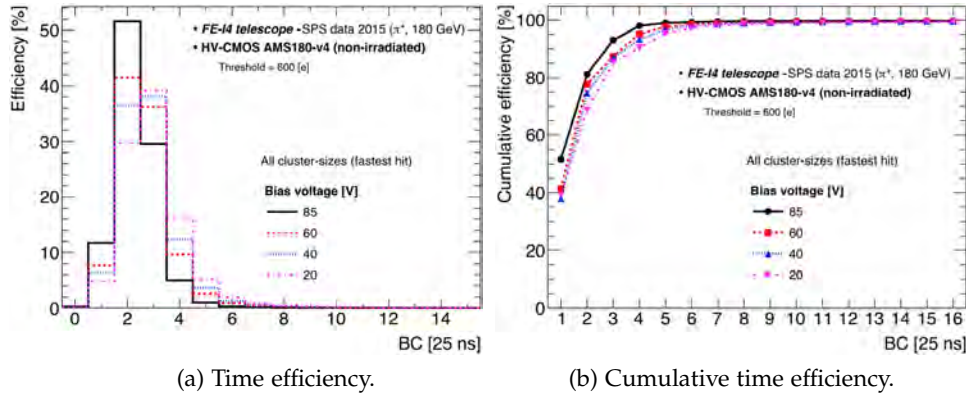


Figure 9.8: Efficiency (a) and cumulative (b) efficiency versus hit timing for different bias settings [175].

detection latency with the threshold, which again is an indicator of the time-walk of the amplifier signal. In case of a constant rise time for all signal sizes, a reduction of threshold would only yield an increase in efficiency. It is observed here that the timing distribution spread is improved, with higher efficiency being achieved earlier in time, when the threshold is reduced to 386 e^- . Nevertheless, as will be described in the following paragraphs, with lower threshold levels the electronic noise starts to dominate, decreasing the efficiency performance of the detector .

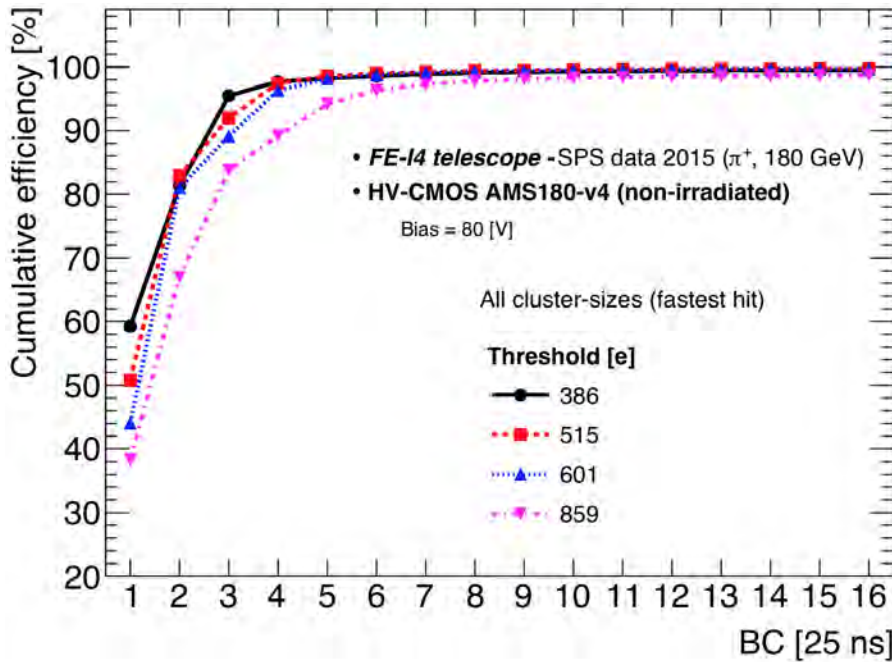
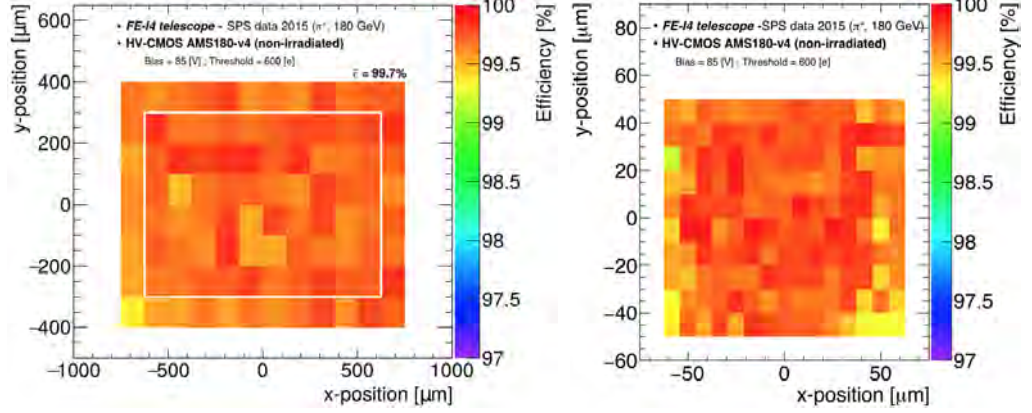


Figure 9.9: Cumulative efficiency (25 ns bins) for different thresholds [175].

By counting how many hits were detected by a given pixel and referencing it to the total amount of tracks traversing the pixel region, it is possible to calculate the efficiency of single pixels. Figure 9.10a shows the efficiency map resulting from the 16 BCs integration, for

a bias voltage of 85V and a threshold of 600 e^- . An average global efficiency of $\epsilon = 99.7\%$ is obtained when filtering out the outermost columns and rows, in order to avoid edge-effects due to the finite telescope resolution.



(a) CCPDv4 efficiency map. The average global efficiency excludes the edge pixels.

(b) In-pixel efficiency.

Figure 9.10: Efficiency distributions for the complete pixel matrix and projected into (3 CCPDv4 pixels with effective $125 \times 100 \mu m^2$) [175].

Thanks to the achieved pointing resolution of the FE-I4 telescope being smaller than the read-out pixel size, by projecting the STime pixels into one macro-pixel (3 CCPDv4 pixels with a total area of $125 \times 100 \mu m^2$) it is possible to evaluate the efficiency in sub-pixel regions. Figure 9.10b displays the in-pixel efficiency map, which shows a slight reduction of the efficiency towards the edges, hinting at charge sharing. Figure 9.11 shows the relative contributions to the efficiency from different cluster sizes. The high efficiency in the central region of Figure 9.10b results from events where the cluster size is exactly one ($\sim 78\%$ of the cases). Events with a cluster size of two ($\sim 20\%$ of the cases) contribute mainly to the edge regions, as expected from charge sharing between neighbouring pixels.

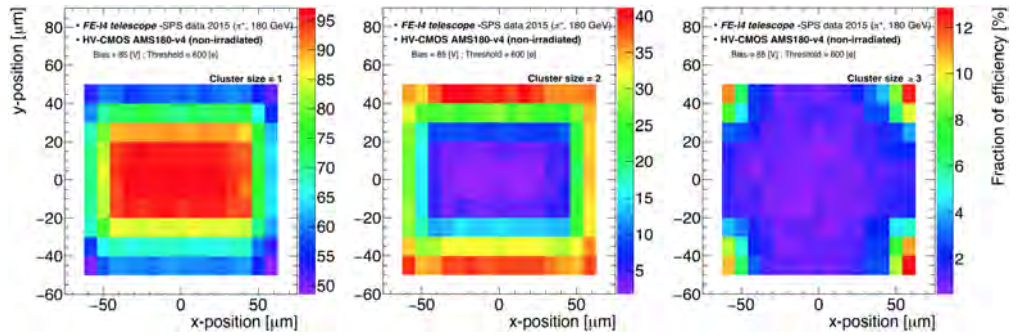


Figure 9.11: Relative contributions to the efficiency inside a macro-pixel according to their cluster sizes (single pixel (left), two pixels (center) and ≥ 3 (right) [175].

The efficiency as a function of the discriminator threshold is shown in Figure 9.12a for a bias voltage of 80V. Three distinct operational

regimes can be identified and their approximate edges marked by red lines. As expected, for a low threshold, the detector cannot be operated properly due to pixels with noise levels above the threshold, while pixels with too large threshold would not be able to detect events with low energy deposition. The region for which the efficiency is higher than 99.5% is between 385 and 690 e^- . The relatively large width of the plateau is a consequence of the good tuning of the pixel matrix, yielding a threshold dispersion of only $\sim 25 e^-$, while with the $\sim 150 e^-$ dispersion from the un-tuned matrix the plateau would be smaller as the threshold level would have to be increased to avoid noisy pixels, getting closer to the value where the signal generated borders the threshold.

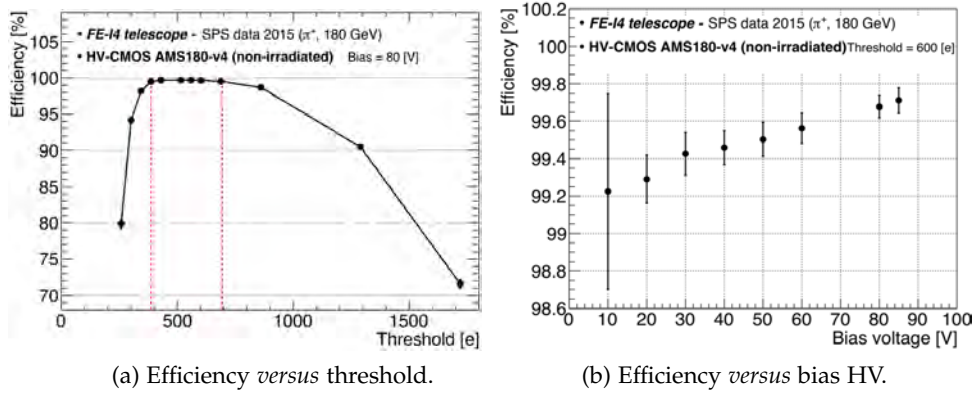


Figure 9.12: Efficiency as a function of the threshold and of the bias voltage [175].

The efficiency as a function of the sensor bias voltage is shown in Figure 9.12b for a threshold of 600 e^- . The large statistical uncertainty for the first data point is due to a mistake during data taking where the ROI triggering was not activated so that only a small fraction of the recorded tracks passed through the sensor. Even for a bias voltage as low as 10V the detector is highly efficient with over 99% detection probability as it is expected from a diffusion-dominated signal. The performance increases, as expected, with higher voltages as the depletion zone grows around the collection deep N-well, enlarging the effective pixel sensitive volume.

9.1.3 Irradiated results - SPS H8 - 2016

The intended application for HV-CMOS sensors requires very high radiation tolerance. One sample was irradiated with 18 MeV protons at the Bern Cyclotron Laboratory and then measured in a testbeam after $1.3 \times 10^{14} n_{eq}/cm^2$ and, after a second irradiation step, also at $5 \times 10^{14} n_{eq}/cm^2$. Two other samples were irradiated, by reactor neutrons at the JSI TRIGA reactor (Ljubljana), one sample at $1 \times 10^{15} n_{eq}/cm^2$ and the second at $5 \times 10^{15} n_{eq}/cm^2$. During the test-beam measurements the DUTs were cooled down to about $-28^\circ C$ to suppress the leakage current due to the bulk damage. The results are published in [176].

Discriminator thresholds of all samples were equalised by means of the CaRIBOu system. However, as NIEL effects from irradiation induce a high leakage current and thus noise, the minimum achievable threshold varies between the samples. In order of increasing fluence, global thresholds of 0.07V(~ 600 e), 0.08V(~ 690 e), 0.09V(~ 770 e), 0.1V(~ 860 e) were set. The threshold values in electrons are mere approximations as a calibration was not possible as described earlier.

9.1.3.1 Residuals

The residual distribution in both pixel directions is shown in Figure 9.29. It is possible to see that the spatial resolution (approximated by the distribution RMS) is comparable with the resolution achieved before irradiation.

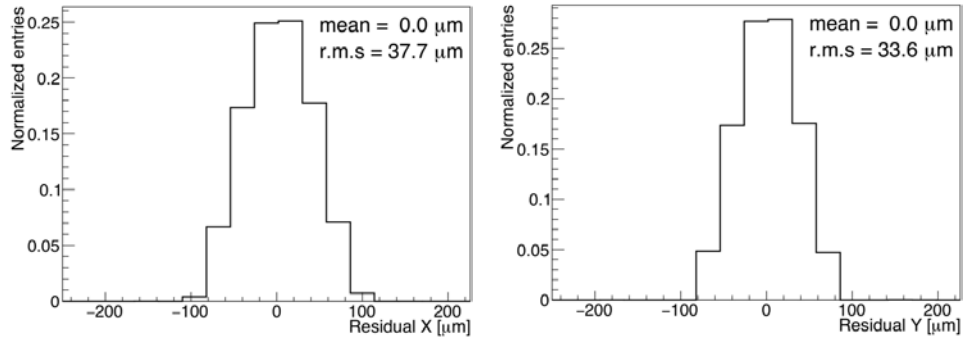


Figure 9.13: Normalised residual distributions of the $1 \times 10^{15} n_{eq}/cm^2$ DUT along the column (left) and row (right) directions [176].

9.1.3.2 Cluster size and timing

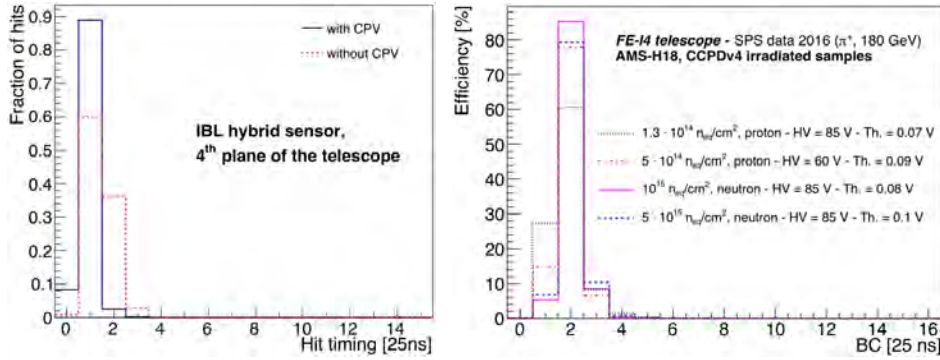
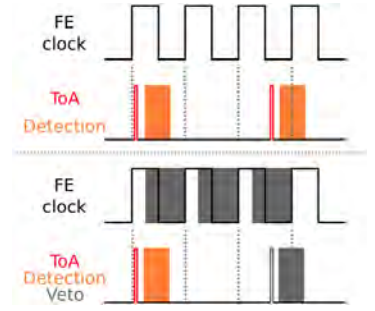
Due to the smaller depletion depth and to the creation of charge traps in the sensor bulk, suppressing the charge diffusion through the sensor, smaller cluster sizes are expected. Table 9.1 shows this to be true, with the fraction of clusters with 2 pixels being reduced to only a few % after irradiation. This effect, however, can be mitigated artificially by tilting the sensor, increasing the particle path through the sensor, or by the use of magnetic fields to shift the charge drift during collection. This solution helps to enlarge the cluster size without the addition of pixel hits with late signal time-of-arrival.

Table 9.1: Cluster size fractions, in percentage, for different fluences.

Fluence [n_{eq}/cm^2]	0	$1.3 \cdot 10^{14}$	$5 \cdot 10^{14}$	$1 \cdot 10^{15}$	$5 \cdot 10^{15}$
Cluster size = 1 [%]	78.3	97.0	95.8	97.8	96.1
Cluster size = 2 [%]	19.6	2.8	3.8	2.0	3.4
Cluster size > 3 [%]	2.1	0.2	0.4	0.2	0.4

The SPS H8 beam has no pronounced timing structure over the 5 s long spill. Therefore, there is in general no coincidence between the time of arrival (ToA) of the particle and the FE clock, leading to an artificial smearing of the timing distribution. In order to mitigate this effect, a Clock-Phase Veto (CPV)[167] was implemented during the measurements with the irradiated samples. Here, only particles that are detected in a tunable interval of 6.4 ns of the FE clock-phase can issue a trigger, similarly to the particle collisions detected at ATLAS where the FE-I4 clock is synchronized with the LHC beam crossing. The effect of the veto for one of the telescope planes is depicted in Figure 9.14a. With the CPV, remaining timing delays are likely to be caused by either slow charge collection and/or time-walk effect.

CPV illustration. Late triggers in the FE-I4 clock cycle are discarded, emulating a bunched particle beam [167].



(a) Timing distribution of a telescope plane with and without the Clock-Phase Veto. (b) Timing distributions for the four irradiated CCPDV4 samples at the operational bias voltages [176].

Figure 9.14: Effect of the telescope CPV on a telescope plane and CCPDV4 timing distribution.

The efficiency contribution with respect to the timing bin was calculated and is shown in Figure 9.14b. The timing resolution of the detector improves with irradiation up to $1 \times 10^{15} n_{eq}/cm^2$, leading to an efficiency larger than 85% for one BC, being comparable with the IBL telescope module shown in Figure 9.14a, and larger than 95% over three BCs, decreasing to 80% in one BC at $5 \times 10^{15} n_{eq}/cm^2$. This can be explained by the acceptor-removal effect, which increases the charge signal generated after irradiation, mitigating time-walk effects.

The effect of the signal size can be found in the timing distribution versus bias voltage shown in Figure 9.15a. As the diffusion component after $1 \times 10^{15} n_{eq}/cm^2$ is negligible and only the fastest hits in multi-hit clusters are considered, this plot directly shows the performance of the amplifier with signal size. The in-pixel mean timing map in Figure 9.15b demonstrates further that the late hits originate from the sides of the macro-pixel.

Some more insight can be gained when looking at the timing distribution for different applied bias voltages (Figure 9.15a) and at the average timing of an event depending on the track's in-pixel position

(Figure 9.15b). As expected, the events registered without any applied bias voltage are slow and very broad in their timing. The time resolution gradually increases with the increasing electric field causing faster collection. The in-pixel mean timing map indicates that central events – below or near the deep N well – are collected faster, while events at the edges of the pixel are on average slower. The CCPDv4 sensors are biased from the front side as there is no backside contact. TCAD simulations indicate that this may lead to regions of low electric field strength, supporting our measurements.

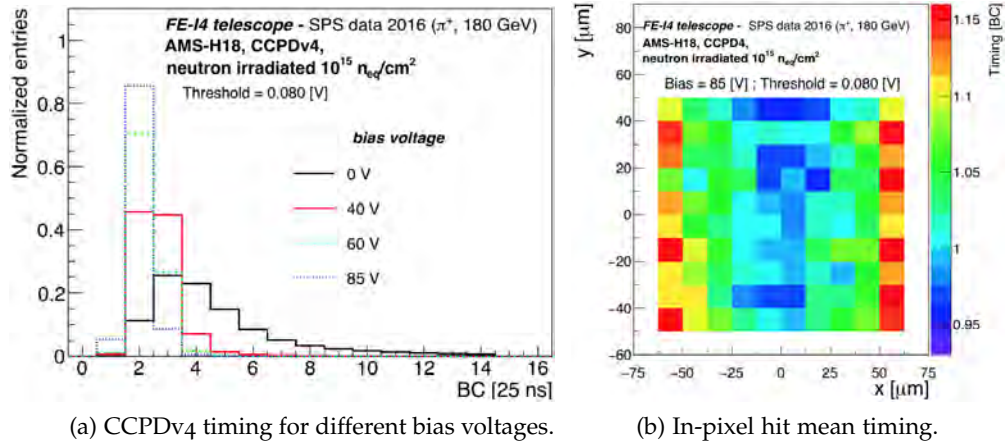


Figure 9.15: CCPDv4 timing for four values of bias voltage (a) and In-pixel timing map showing the mean timing of the event as depending on the track position inside the pixel (b) [176].

9.1.3.3 Detection efficiency

The hit efficiency for the STime pixels in the sample irradiated with $10^{15} n_{eq}/cm^2$ at a bias voltage of 85V and using a threshold of 80 mV is shown in Figure 9.16a. It can be seen that an homogeneous and high efficiency of 99.7% is reached across the whole matrix.

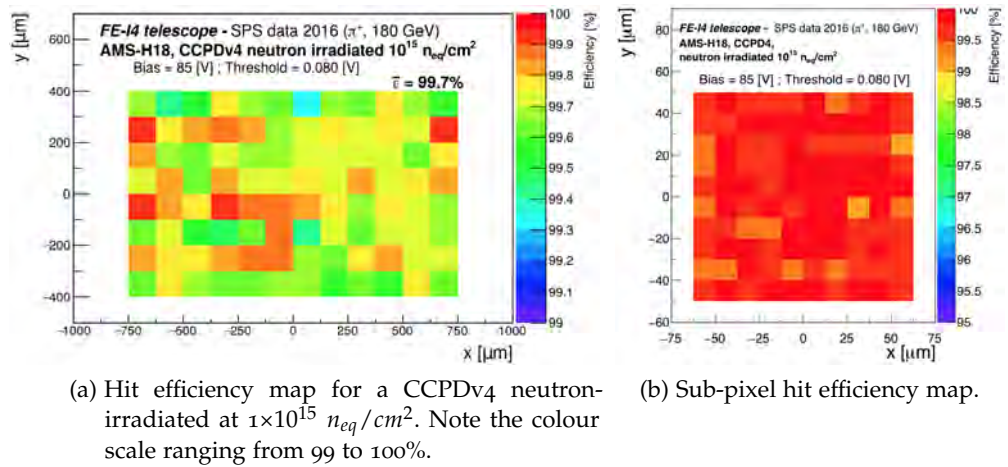


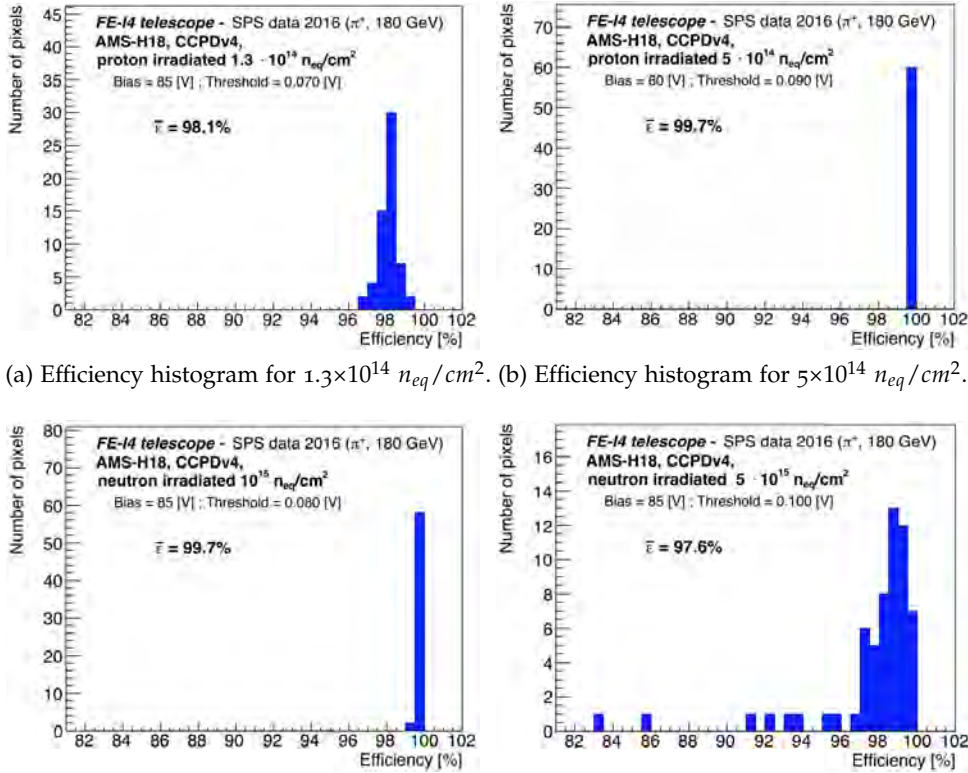
Figure 9.16: Efficiency for a sample neutron-irradiated at $1 \times 10^{15} n_{eq}/cm^2$ [176].

By plotting the hit efficiency within sub-pixel regions, shown in Figure 9.16b, it was found that there is no significant loss of hit efficiency in any region of the pixel, demonstrating a very uniform response of the macro-pixel with no visible structures at the level of 1%.

The average efficiency here is calculated by not accounting tracks with reconstructed trajectories within $20\text{ }\mu\text{m}$ of the DUT edges, avoiding possible edge effect due to mis-reconstructed tracks because of the finite telescope resolution ($\sigma \sim 10\text{ }\mu\text{m}$). For samples irradiated with fluences of 1.3×10^{14} , 5×10^{14} , 1×10^{15} and $5 \times 10^{15}\text{ } n_{eq}/\text{cm}^2$, the measured average hit efficiencies are 98.1%, 99.7%³, 99.7% and 97.6%, respectively.

The distribution of the efficiencies calculated for each pixel is shown for each irradiation step in the histograms of Figure 9.17. First visible aspect is that the $1.3 \times 10^{14}\text{ } n_{eq}/\text{cm}^2$ sample had a lower efficiency than the next two higher irradiated ones. This is attributed to the low charge collection region seen by TCT[101]. For the highest fluence of $5 \times 10^{15}\text{ } n_{eq}/\text{cm}^2$, it can be seen that there are several outlier pixels, most probably originating from individual deteriorated circuits. It is possible that in future improved designs these could be recovered by extending the operating point of internal DACs, but this would require further detailed studies at circuitry level.

- 3 Here a working point at a bias voltage of only 60V was chosen as the sample was noisy at the higher bias voltage of 80V



(a) Efficiency histogram for $1.3 \times 10^{14}\text{ } n_{eq}/\text{cm}^2$. (b) Efficiency histogram for $5 \times 10^{14}\text{ } n_{eq}/\text{cm}^2$.

(c) Efficiency histogram for $1 \times 10^{15}\text{ } n_{eq}/\text{cm}^2$. (d) Efficiency histogram for $5 \times 10^{15}\text{ } n_{eq}/\text{cm}^2$.

Figure 9.17: Hit efficiency histograms for different fluences of protons (upper row) and neutrons (lower row) [176].

As with the un-irradiated sample, bias-voltage and threshold scans were performed to study the dependency of the hit efficiency. The result for the HV bias scan is shown in Figure 9.18. It can be seen that for the bias voltage, a plateau is reached after about 40V, but in particular the very low and very high fluences profit from going to the highest possible bias voltages before the onset of breakdown (i.e. about 85V). This is probably due to the fact that the depletion zone is thin compared to that of passive hybrid pixel sensors and its increase with bias voltage contributes significantly to the hit efficiency. At the middle fluences of the irradiation (5 and $10 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$) the acceptor removal effect helps increasing the sensor depleted volume (see Section 4.3.2), not requiring the highest bias voltage to achieve an high detection efficiency. Values for the lowest bias voltage show a decrease in efficiency with fluence, which is expected as the diffusion component deteriorates rapidly with irradiation. After the highest fluences however, this effect cannot fully counteract trapping and the efficiency cannot be sustained. For the sample irradiated with $5 \times 10^{14} \text{ n}_{eq}/\text{cm}^2$ the reduced efficiency at 80V is due to the increasing noise at the highest bias voltage.

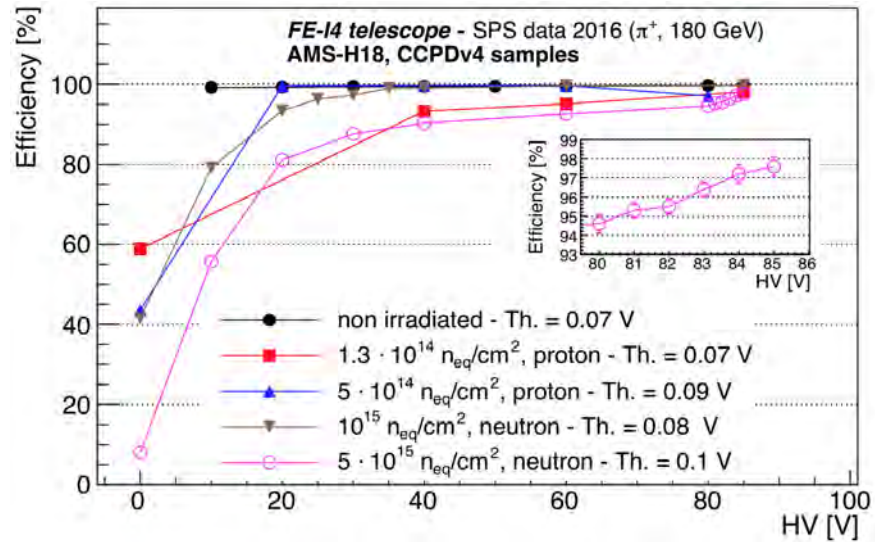


Figure 9.18: Average hit efficiency as a function of applied bias voltage. The insert shows the sudden increase in efficiency between 80 and 85V, which could be attributed to charge multiplication [176].

For the highest fluence, a rapid increase of efficiency close to its breakdown voltage was observed. The insert in Figure 9.18 shows its behaviour between 80 and 85V. In highly irradiated (above $10^{14} \text{ n}_{eq}/\text{cm}^2$) planar and 3D pixel sensors, it has been demonstrated that the high electric field combined with trapping due to radiation damage can lead to charge multiplication due to impact ionisation when sufficient high voltage is applied to the sensors [177]. Here free charge carriers can obtain enough energy to ionise atoms on impact, leading to an amplification of the signal collected and consequently an increase in noise and leakage current for the passage of a particle.

With regard to the threshold scans, Figure 9.19 shows that for high threshold, as for the un-irradiated samples, there is a loss of efficiency due to events with low charge signals not being detected. For low threshold values, once more, the discriminators are becoming noisy lowering the signal-to-noise ratio together with the efficiency. In between, plateaus of stable efficiency appear with the highest width for the intermediate fluences. This is expected from observations of the HV scan as the highest signal after irradiation can be found for values where the charge trapping is compensated by the acceptor removal effect. In the low threshold region, the minimum threshold, before the reduction in efficiency due to noise, rises with fluence (0.06V, 0.06V, 0.07V, 0.09V) which can be explained by the high levels of bulk leakage current after irradiation. This especially limits the 1.3×10^{14} and $5 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ samples as they suffer from low signal sizes.

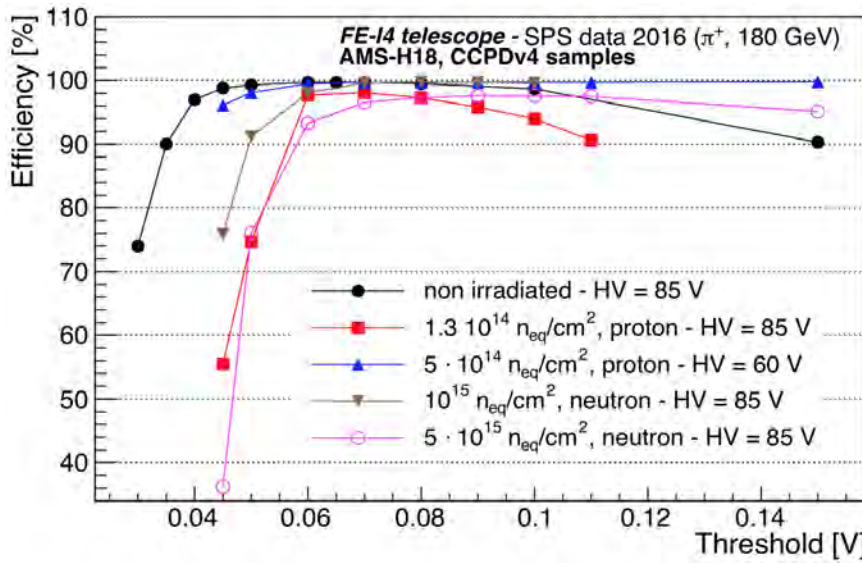


Figure 9.19: Average hit efficiency as a function of threshold voltage [176].

9.2 H35DEMO - SPS H8 AND FTBF - 2017

The H35DEMO is a prototype designed and produced in order to further evaluate the performance of HV-CMOS devices with a focus on the effect of higher resistivity substrates, as a better charge collection performance is expected from sensor bulks with higher resistivities. The H35DEMO prototype was designed and produced in 4 different resistivities: $20 \text{ } \Omega\text{cm}$, $80 \text{ } \Omega\text{cm}$; $200 \text{ } \Omega\text{cm}$; and $1000 \text{ } \Omega\text{cm}$.

The H35DEMO is the first large scale (FE-I4 size) HV-CMOS device and it comprises 4 independent pixel matrices (described in Section 2.3.3). Two matrices couple to the FE-I4 chip for read-out and contain only analog circuits. These matrices are investigated in the work described here, allowing for the evaluation of the effect of different substrate resistivities on the detector performance. The results shown here are published in [178].

The other two matrices are fully monolithic devices, and were investigated in a collaboration with the IFAE (Barcelona) using the UniGE FE-I4 telescope. A dedicated read-out system, also based on the Xilinx ZC706 FPGA board, was developed by IFAE and was integrated to the FE-I4 telescope using the busy/trigger scheme. The results are very encouraging⁴, achieving a minimum threshold of $1300 \pm 130 e^-$ and a noise level in the order of $180 \pm 26 e^-$, which yielded a noise occupancy $< 2 \times 10^{-7}$ in 25 ns, with less than 1% of masked pixels. An efficiency of $> 99\%$ was measured, with data produced at FTBF, before irradiation for all tested samples (20,80 and 200 Ωcm) with thresholds in the range between 1300 and 1800 e^- . A 200 Ωcm sample was irradiated up to $10^{15} n_{eq}/cm^2$ with neutrons at JSI and measured at SPS H8. An efficiency also above 99% was measured at a bias of 160V and threshold at $1800 \pm 200 e^-$, with a noise level of 278 ± 31 electrons [179].

The CaRIBOu system was used for the slow control of the analog matrices of the H35DEMO prototypes. During the data taking the DUTs were maintained at about 25°C with the help of the telescope DUT box. The analog matrices provide an output signal, to be transmitted to the ROC pixel, that is proportional to the collected charge in the sensor bulk. Therefore, a weighted center-of-gravity clustering is possible to estimate the hit position. For the analysis, only tracks with clusters on all six telescopes planes and a $\chi^2/d.o.f.$ below 5 are considered. The distance cut for a DUT cluster and telescope track match is 250 μm along each pixel axis.

Samples of three different resistivities (80, 200 and 1000 Ωcm) were studied with bias voltage from 0 to 160V and FE-I4 thresholds from 1000 to 4000 e^- , as shown on Table 9.2. The Analog 2 matrix of the 1000 Ωcm sample was not measured due to an early increase in leakage current below the breakdown voltage as mentioned on Section 3.1. The threshold values quoted on the table refers to the threshold applied on the FE-I4 ROC. As the charge detected by the H35DEMO is amplified and sent to the ROC pixel via a capacitive injection, threshold values on the FE-I4 do not illustrate the real charge collected on the sensor.

⁴ Having in mind that the technology used has larger node size and, as consequence, less electronic circuits will fit on a given pixel size, in comparison with the aimed 180 nm technology.

Table 9.2: Summary of measurements performed on the H35DEMO prototypes in test beam.

Resistivity	Matrix	Bias voltages	Threshold [e^-]
80 Ωcm	Analog 1	0 to 160V	1500, 2000
200 Ωcm	Analog 1	0 to 160V	2500, 3000, 4000
200 Ωcm	Analog 2	0 to 140V	2000, 2500, 3000, 4000
1000 Ωcm	Analog 1	0 to 160V	1500, 2000, 2500, 3000

9.2.1 Residuals

As most clusters contain only one pixel, the spatial resolution of the prototypes is mainly determined by the pixel pitch. Figure 9.20 shows a typical unbiased residual distribution for a 200 Ωcm sample operated with a bias of 160V and 2000 e^- threshold. The function used models the typical box-shaped response of a pixel with width l , convoluted with a Gaussian curve accounting the telescope resolution σ . As the particle beam illuminating the sensor is not uniform, the fraction of background events is dependent on the sensor, resulting in the tilt observed on the residual plots.

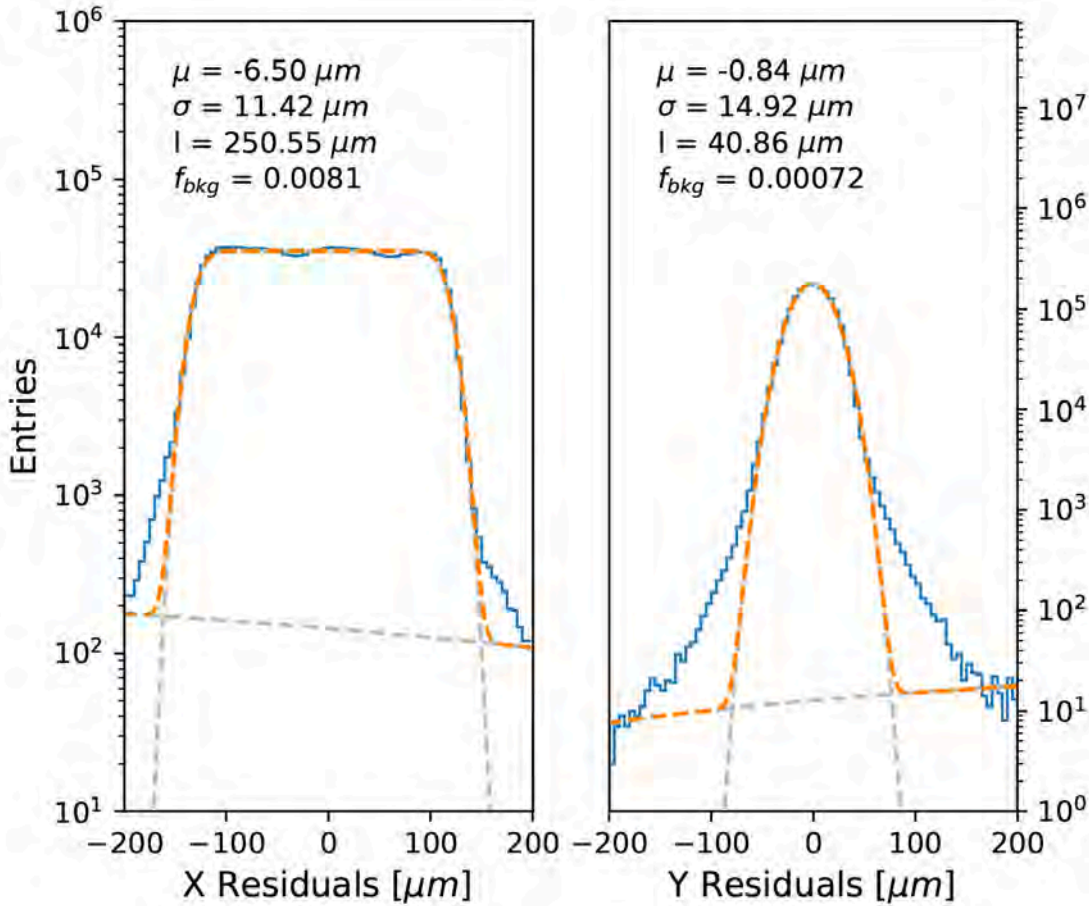


Figure 9.20: Unbiased residual for a 200 Ωcm sample, 160V bias voltage, 2000 e^- threshold, analog matrix 1 (blue). Fit of a gaussian convoluted with a box function (orange). μ is the mean of the distribution, σ the width of the Gaussian, l the width of the box and f_{bkg} the fraction of background events [178].

The fitted pixel size, along the column axis, is in good agreement with the real size, while the adjusted size along the pixel row direction is smaller than the real value due to the larger charge-sharing along this direction, causing the tail of the distribution.

9.2.2 Cluster sizes and timing

The effect of different substrate resistivities on the behaviour of the H35DEMO prototype can also be observed through the changes of cluster properties. Figure 9.21 shows the typical cluster size measured for the high-gain matrix (matrix with highest detection efficiency). For all resistivities, the dataset is dominated by clusters containing only one pixel. This is due to the large size of the pixel ($250 \times 50 \mu m$) and the small depletion depth expected ($< 50 \mu m$).

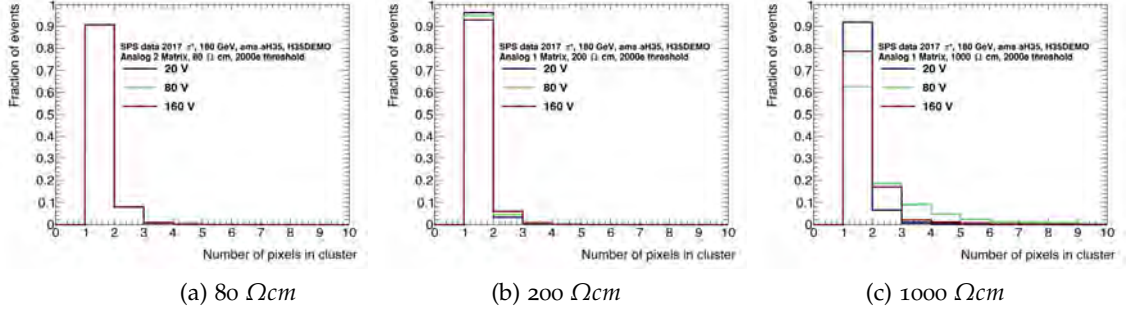


Figure 9.21: Cluster size versus bias voltage and different substrate resistivity for 2000 e^- threshold [178].

At higher resistivity, the influence of a large depletion depth can be observed in Figure 9.21c, and two competing phenomena are visible. The charge deposited deeper in the bulk will drift for a longer time than the charge deposited close to the electrodes, while the increased electric field in the bulk increases the charge speed, making the charge drift time smaller. This second effect is enhanced as the bias voltage is applied on an electrode surrounding the collection diode. As the depletion depth reaches values larger than the electrode to N-Well distance ($10 \mu m$), the behaviour of the diode diverges from that of a planar diode. It can be observed in Figure 9.21c that the charge sharing producing larger clusters is maximal at an intermediate bias voltage of 80V.

The resistivity of the substrate should also have an effect on the rise time of the signal and the amount of charge generated. Figure 9.22 shows the dependence of the timing resolution of the H35DEMO for different bias voltage and resistivity for the second high-gain matrix.

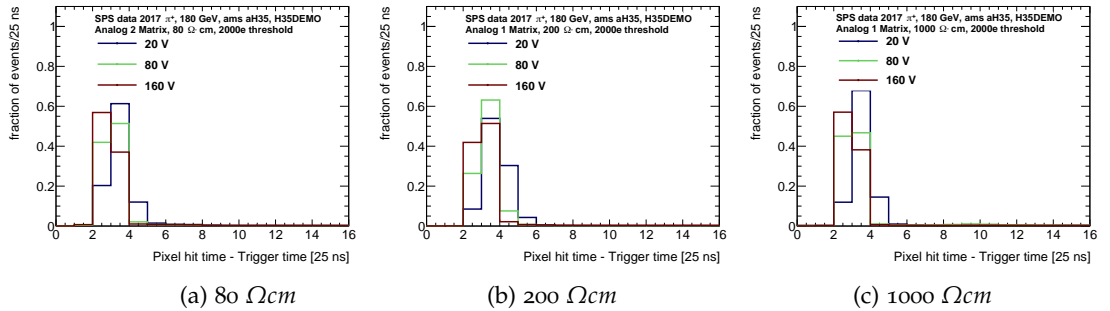


Figure 9.22: Signal arrival time distributions in 25 ns bins versus bias voltage and different substrate resistivity for 2000 e^- threshold [178].

No significant variation of the distribution was observed in the other matrices. It was not possible to adjust the delay of the clock for the FE-L4 ASIC to optimise the binning of the timing distribution. No clear dependence of the timing resolution on resistivity, gain or presence of the Deep P-Well can be observed. However, in all cases, the timing distribution is constrained to less than 50 ns for bias voltages over 80V. This indicates that the timing resolution is dominated by the intrinsic jitter of the preamplifier and not by the sensor signal shape.

9.2.3 Comparison of pixel flavours

The H35DEMO analog matrices contain six flavours of pixels with different gain, feedback and biasing schemes. The purpose of these variations is to determine the best scheme to ensure a low noise and a high-efficiency operation of the pixel. The Deep P-Well, a deep implant located below the high voltage implant influences the pixel input capacitance and therefore the noise and rise time of the signal. Enclosed Layout Transistors (ELT) are used to make the circuitry more radiation tolerant to ionising dose but will negatively affect the gain and rise-time of the pulse generated by the circuitry. The gain, as determined by the feedback capacitor in the pixel amplifier, will affect the noise and the detection efficiency, for a given injection charge.

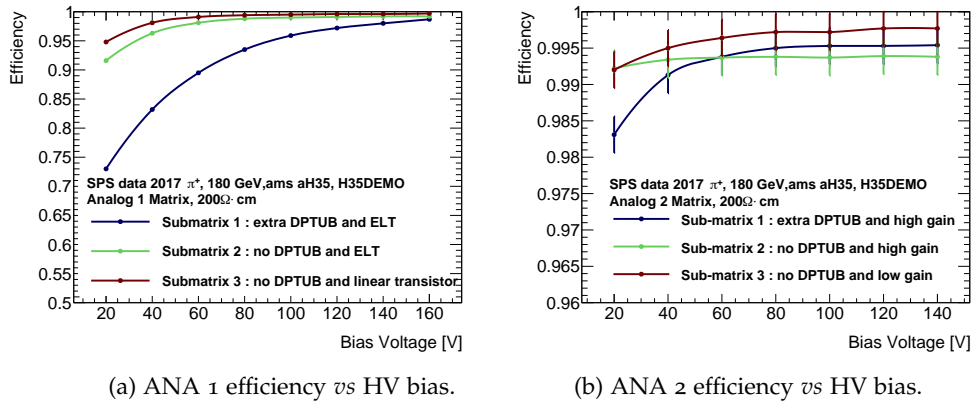


Figure 9.23: Detection efficiency as a function of bias voltage for the three sub-matrices of analog matrix 1 (left) and analog matrix 2 (right) for a 200 Ω cm sample for a threshold of 2000 e^- [178].

Figure 9.23 shows the detection efficiency for all sub-matrices of the analog matrices of the 200 Ω cm sample, as a function of the bias voltage applied to the sensor. Figure 9.23a shows that the use of an ELT in the feedback circuitry of the pixel (sub-matrix 2) doesn't impact significantly the pixel detection efficiency when compared with the pixel flavour using linear transistors (sub-matrix 3). The most significant effect is however linked to the addition of the Deep P-Well implant to the high-voltage implant, degrading the detection efficiency in both analog matrices. The addition of capacitance between the Deep N-Well and the biasing contact due to this implant affects the gain and rise-time of the amplifier and should be avoided for particle detection.

In Analog matrix 2, for the three cases, efficiency is well above 99% in the conditions of figure 9.23b.

9.2.4 Detection efficiency

The particle detection efficiency is a key parameter to determine the usability of high-resistivity substrate CMOS sensors. This parameter is influenced by the signal strength and the gain of the preamplifier. Figure 9.24 shows the bias voltage scan performed for the individual matrices for different thresholds settings of the FE-I4. A clear dependence of the efficiency on the substrate resistivity for comparable

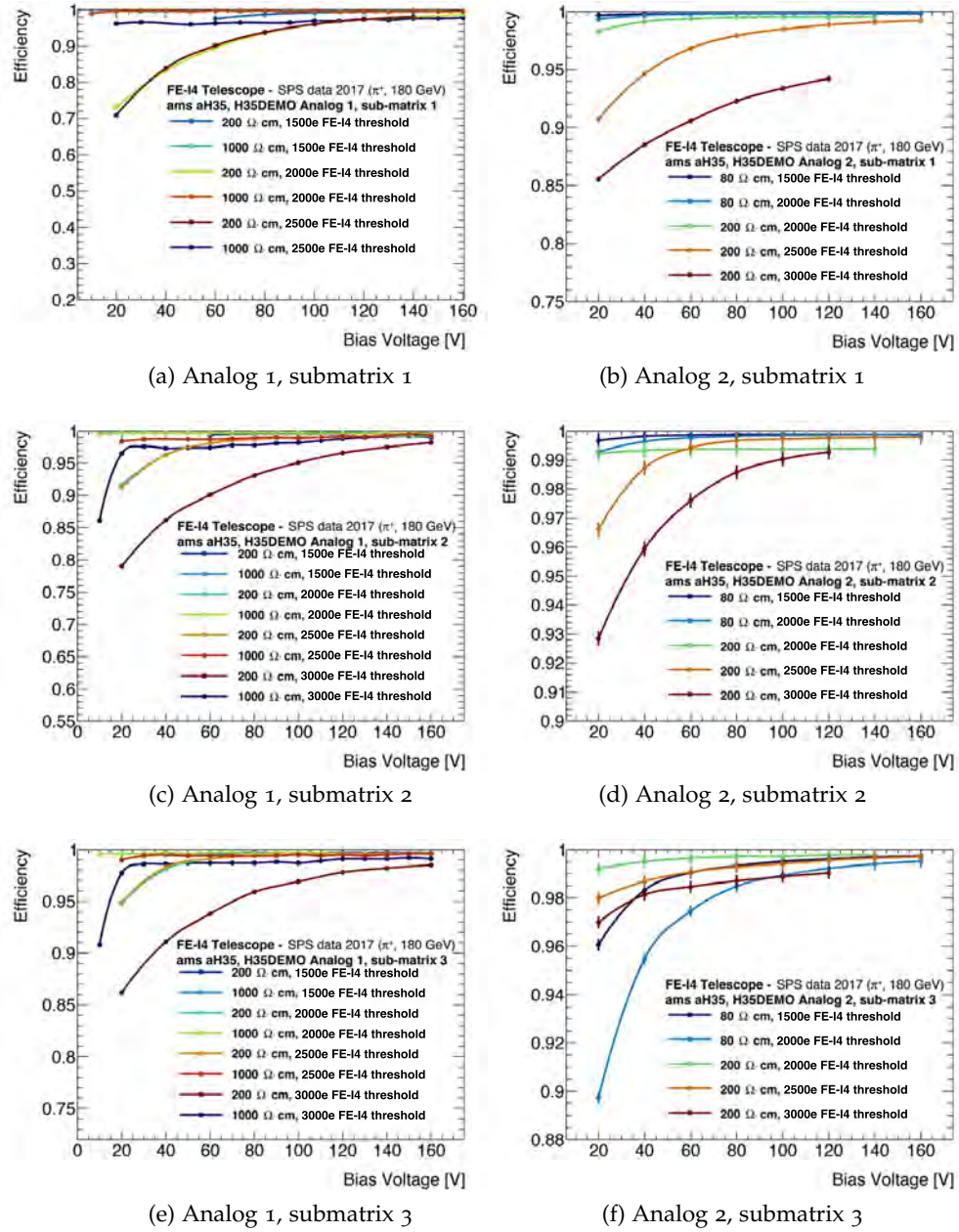


Figure 9.24: Efficiency of 80, 200 and 1000 Ωcm resistivity substrates for the different sub-matrices as a function of bias voltage and FE-I4 detection threshold [178].

thresholds can be observed. The higher the resistivity, the smaller the bias voltage needed to obtain a good detection efficiency, in agreement with our expectation. Excellent detection efficiency superior to 99% can be achieved for all resistivities studied with a threshold of 2000 e^- , corresponding to approximately 1500 e^- signal in the H35DEMO sensor, assuming 3.5 fF coupling capacitance and a gain of $1/15\text{ mV/e}^-$.

Figure 9.25 shows the efficiency for each pixel of the second high-gain matrix for each of the three resistivities, taken at 2000 e^- FE-I4 threshold and 160V bias voltage. These results show, after careful tuning of the glueing method, a good detection uniformity over the matrix has been achieved. This demonstrates a good uniformity of the pixel's electrical behaviour within the columns and good uniformity of the glue interface and preamplifier properties. The left column for analog matrix 2 and right column for analog matrix 1 shows low efficiency due to the proximity with the pixels of the monolithic NMOS and CMOS matrices, which can compete for the charge signal.

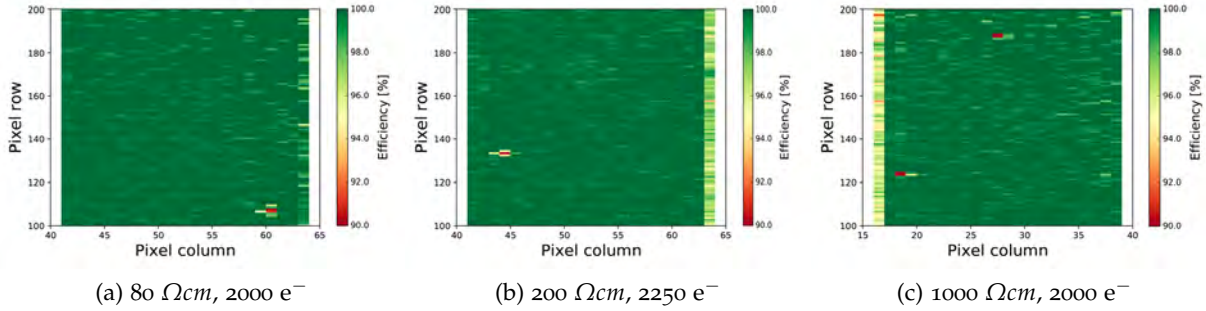


Figure 9.25: Efficiency for the analog high-gain sub-matrices at 160V for different substrate resistivities [178].

Figure 9.26 shows the in-pixel efficiency measured for the high-gain matrices for different resistivities and HV bias. Figures 9.26 a), c) and e) show the efficiency at low bias voltage, where intra-pixel regions with low efficiency are visible, more evident for the lower resistivity substrate. TCT measurements [129] have confirmed that lower depletion volumes are achieved with lower resistivity substrates, when compared with an higher resistivity substrate at the same HV bias. This effect can be observed as the inefficient region between pixels as shown in Figure 9.26a. All samples could be operated with efficiency above 99% when sufficient bias was applied, as shown in Figures 9.26 b), d) and f).

In light of the results obtained during this test beam campaign, the following observations can be made: The use of ELT in the feedback circuitry does not affect significantly the performance of the amplifier, as shown in Figure 9.23a; The extra deep P-Well (DPTUB) should not be used, placed under the P-Well providing the contact to the substrate, in order to reduce the input capacitance of the preamplifier. Figure 9.23 shows that a higher efficiency is achieved without the DPTUB; High-Gain is required to achieve good detection efficiency

over a large range of bias in these conditions, as results from the second analog matrix have shown; The time resolution of the sensor is limited by the amplifier design but is not affected significantly by the gain or feedback transistor used; A threshold of about 1500 e^- must be applied to ensure good detection efficiency superior to 99% for all resistivities when the discriminator is to be implemented in the pixel, for monolithic integration (2000 e^- equivalent in FE-I4).

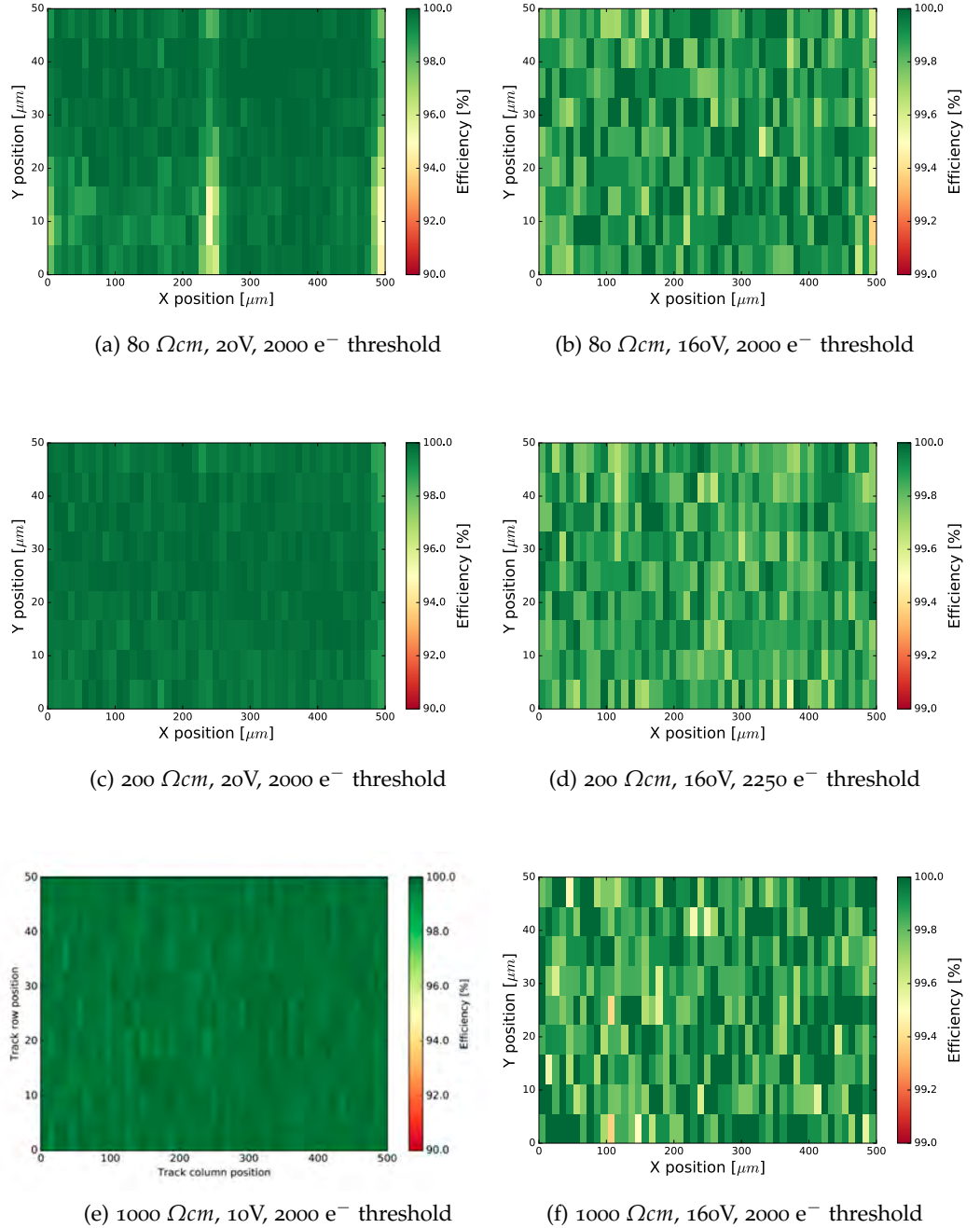


Figure 9.26: 2x2 In-pixel efficiency for 80, 200 and $1000\ \Omega\text{cm}$ resistivity substrates for sub-matrix 2 (Analog 2 for 80 and $200\ \Omega\text{cm}$, Analog 1 for $1000\ \Omega\text{cm}$) [178].

9.3 ATLASPIX

The ATLASpix results shown here were measured between the October 2017 and October 2018. At the end of 2017 the device was put on the beam-line at SPS for the first time and its read-out was performed with an independent and dedicated system based on a commercial Xilinx Nexys FPGA board in combination with a custom control and readout board developed at KIT, requiring an off-line synchronization of the DUT and telescope data. The system was integrated with the telescope DAQ using the Trigger/Busy scheme. By the time, the device was tested by the University of Geneva team as well as by the CLICdp collaboration (using the TimePix 3 telescope at the SPS H6 line) and by Heidelberg colleagues at DESY[180] test-beam using 3 MuPix8 [181] reference layers for tracking.

At the beginning of 2018 the ATLASpix was starting to be integrated to the CaRIBOu read-out system and a 200 Ωcm non-irradiated ATLASpix sample was tested at FTBF, where a short scan of HV bias and thresholds was performed. In June 2018 the ATLASpix started to be tested, again, at CERN SPS H8 beam-line, with the ATLASpix finally fully integrated with the CaRIBOU system. A few measurements were done with the same non-irradiated sample, and then the focus was turned to the performance of irradiated devices. By the time of the conclusion of this thesis, systematic scans were being performed on multiple irradiated devices, although only the results of one irradiated sample will be shown here.

It is expected that the performance of the ATLASpix is similar to the CCPDv4 results as both were designed and produced in the same technology. Hence, differences are expected to come from the different resistivities, which are available for the ATLASpix prototypes, and from the read-out chain which is performed by the ATLASpix itself, instead of the FE-I4 in case of the CCPDv4.

A preliminary threshold to charge calibration was performed using a ^{55}Fe source and a calibration factor of $1620\text{ e}^- / 0.164\text{ V}$ was found. Having in mind that the effective threshold is referenced to a base line voltage of 0.8 V, a threshold of (for example) 0.9 V is effectively a threshold of 100 mV, corresponding to approximately 1000 electrons.

As the CCPDv4, the ATLASpix also contains a tuning DAC in order to equalize the effective pixel threshold across the pixel matrix. Nevertheless, while performing the tuning of the chip it was noticed that the TDAC values set on the pixels were not being in fact applied to the thresholds. A possible explanation for that is the size of the RAM cells that hold the TDAC values are smaller and with a different grounding scheme, in comparison with the CCPDv4, and might be not working properly. This possible bug is to be fixed on the following version of the ATLASpix. Therefore the results shown here are for a matrix with un-tuned pixel thresholds.

9.3.1 Cluster size, residuals and timing

A cluster-to-track matching cut of $250\ \mu\text{m}$ along both dimensions is used to associate telescope reconstructed tracks to ATLASpox clusters. Figure 9.27 shows the cluster size distribution for the $200\ \Omega\text{cm}$ with 60V as bias and threshold set at 0.875 V measured at FTBF. It is possible to see that $\sim 90\%$ of the clusters are composed by a single pixel; about 9% is 2-pixel clusters; and the remaining 1% composed by clusters with 3 pixels or more.

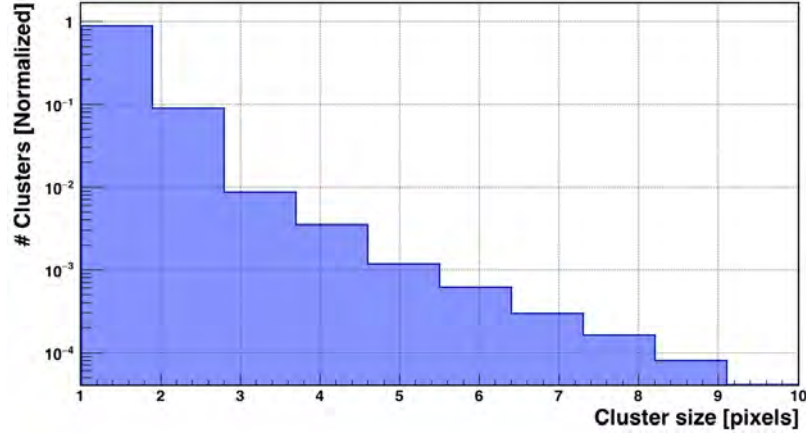


Figure 9.27: ATLASpox cluster sizes (normalized) measured for a $200\ \Omega\text{cm}$ sample biased at 60 V and threshold at 0.875 V.

The measurements performed by the CLICdp collaboration at SPS H6 beam line, using the TimePix3 telescope with about $2 \times 2\ \mu\text{m}^2$ spatial resolution (at the DUT position), investigated the cluster sizes according to the track hit position within the pixel, $130 \times 40\ \mu\text{m}^2$, as shown in Figure 9.28. It shows that hits generating 2-pixel clusters comes mostly for tracks close to the pixel borders along the pixel short distance ($40\ \mu\text{m}$), indicating an effective region for charge-sharing of $\sim 4\ \mu\text{m}$.

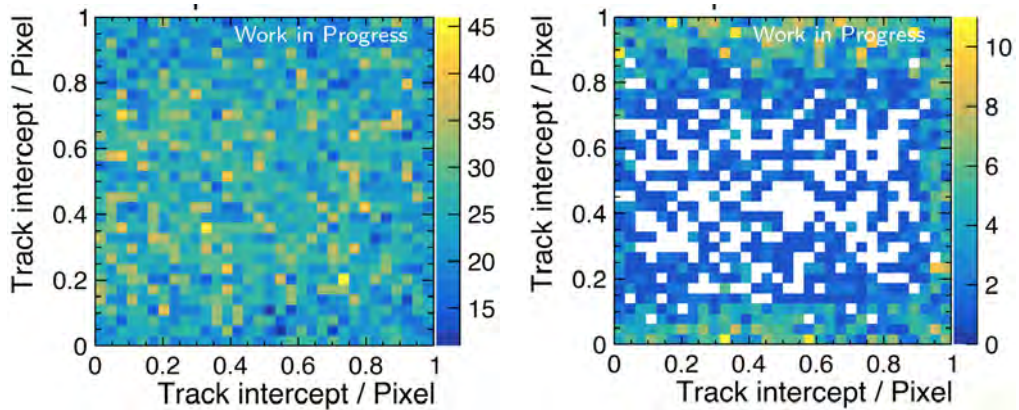


Figure 9.28: Distribution of track hits within a pixel for single (left) and two pixels (right) clusters.

Figure 9.29 shows the residuals between reconstructed track position and estimated cluster position on the device-under-test, also

measurement at FTBF. The fitted function models the expected box-shaped response from a pixel, with width l , convoluted with a Gaussian function in order to account the telescope resolution σ .

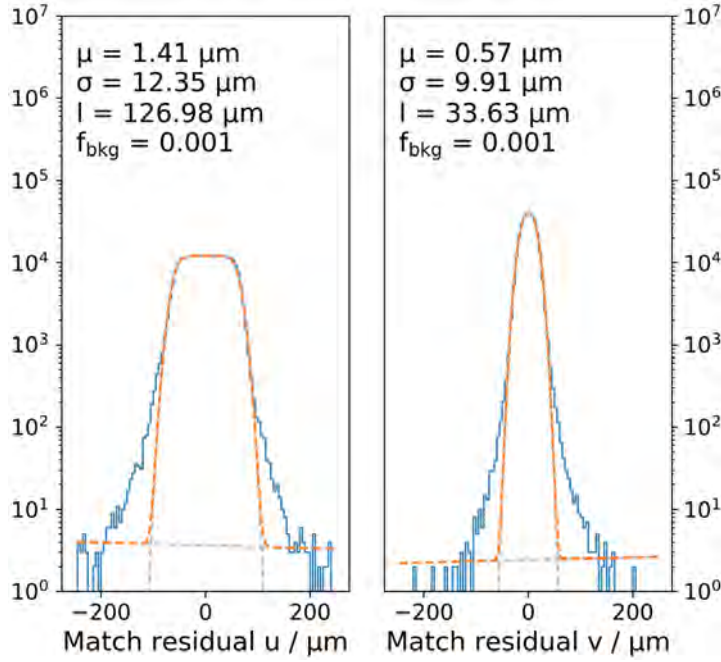
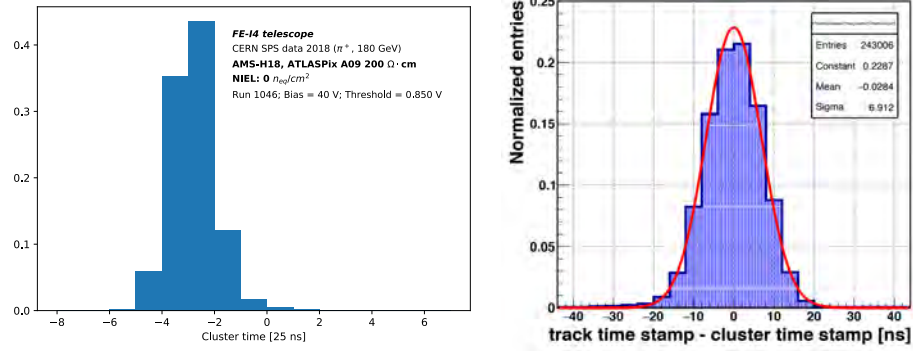


Figure 9.29: Residual distributions, for the direction along the columns (left) and rows (right,) for the 200 Ωcm sample biased at 80 V and threshold at 0.875 V.

The fitted pixel width, $l \sim 127 \mu m$, along the long u direction is consistent with the $130 \mu m$ pitch. Along the short direction v the fitted width, $l \sim 34 \mu m$, is smaller than the $40 \mu m$ pitch as a result of the charge sharing region of about $4 \mu m$ at the pixel bottom and top edges, as shown in Figure 9.28. In both cases the back-ground fraction f_{bkg} due to mismatches or noise hits is negligible and its tilting angle is due to the non-uniform beam profile.

Regarding the timing measurements, the result shown here for the un-irradiated sample was obtained at the SPS H8 test-beam, as during the test-beam at FTBF the hit timing information was not properly available from the CaRIBOu system. At the SPS H8 test-beam the ATLASpix was running with a slow clock of 80 MHz, providing the timing residuals (difference between telescope trigger time and measured hit time on DUT) shown in Figure 9.30a. It is possible to see that about 80% of the detected hits are detected within 2 BCs (or 50 ns), being comparable with the timing measured with the CCPDv4.

In parallel to the ATLASpix measurements with the UniGE FE-I4 telescope (at SPS H8), the CLIC team also investigated the ATLASpix properties using the Timepix3 telescope, permanently installed in the SPS H6 area. In addition to the already expected time-walk effect, during measurements it was also verified that there was a strong dependence on time-walk and the pixel row address. In order to evaluate the timing capabilities of the prototype, both effects were analysed and corrected for. Figure 9.30b shows the timing distribu-



(a) Timing residuals of ATLASpIX at 40V and threshold = 0.85V, running at 80MHz. (b) ATLASpIX timing measured with the Timepix3 telescope at SPS.

Figure 9.30: Timing distributions measured for the ATLASpIX with the UniGE FE-I4 telescope(a) and on the CLIC Timepix3 telescope (b) with row and time-walk correction.

tion achieved after row-address and time-walk correction with the ATLASpIX threshold at ~ 480 electrons (bias HV at -75 V). It shows that a nice timing stamping resolution under 7 ns is achievable.

9.3.2 Detection efficiency

As done for the previous prototypes, the pixel efficiency across the matrix is shown in Figure 9.31 for two runs of the 200 Ωcm ATLASpIX sample performed at FTBF. Here, the pixel efficiency is calculated as the total number of DUT clusters divided by the total number of tracks, binned at the area of each pixel. Here, the first and last columns are excluded, together with the last row, to avoid edge effects. The first ~ 25 bottom rows were outside the telescope acceptance and no tracks are reconstructed in this region. An average pixel

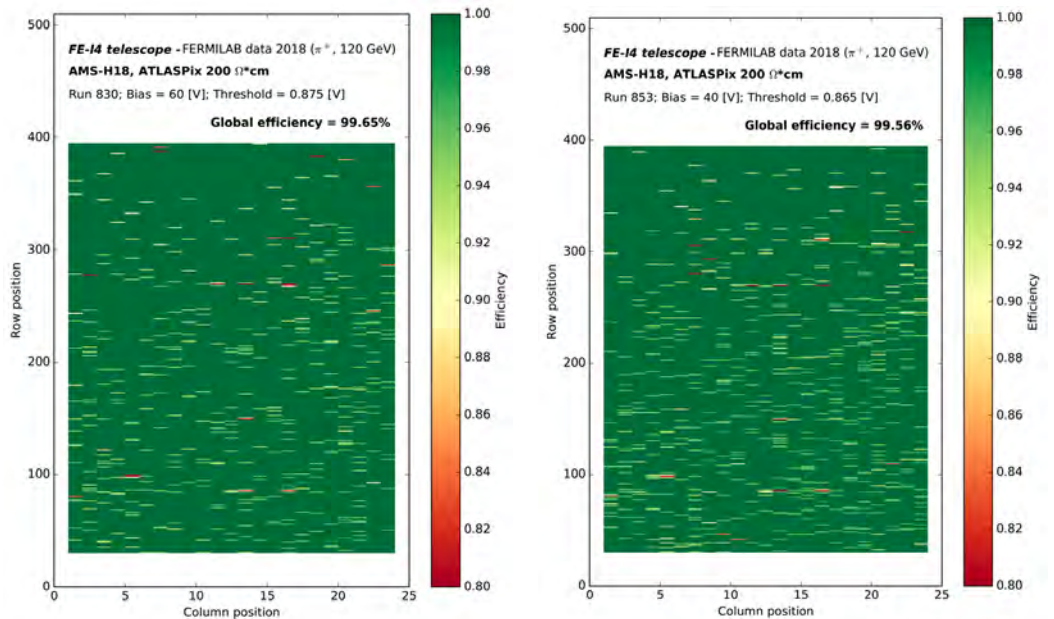


Figure 9.31: Efficiency maps for two runs performed at FTBF.

efficiency of 99.65% is found for the run performed at 60 V and 0.875 V threshold (approximately 740 e^-). Figure 9.32 shows the pixel efficiency distribution, where it is possible to see that most of the pixels have an efficiency between 90 and 100 %.

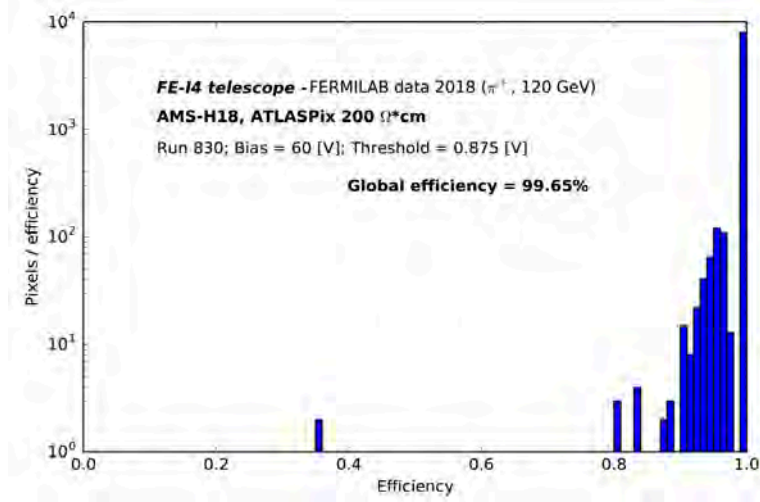


Figure 9.32: Pixels efficiency distribution for the 200 Ωcm sample at 60V and 0.875V threshold ($\sim 740 e^-$).

With the good pointing resolution of the FE-I4 telescope, the efficiency map was projected into 2x2 pixels with a binning larger than the telescope resolution. The in-pixel efficiency for the run performed at FTBF with 99.65% (60V and $\sim 740 e^-$ threshold) is shown in Figure 9.33.

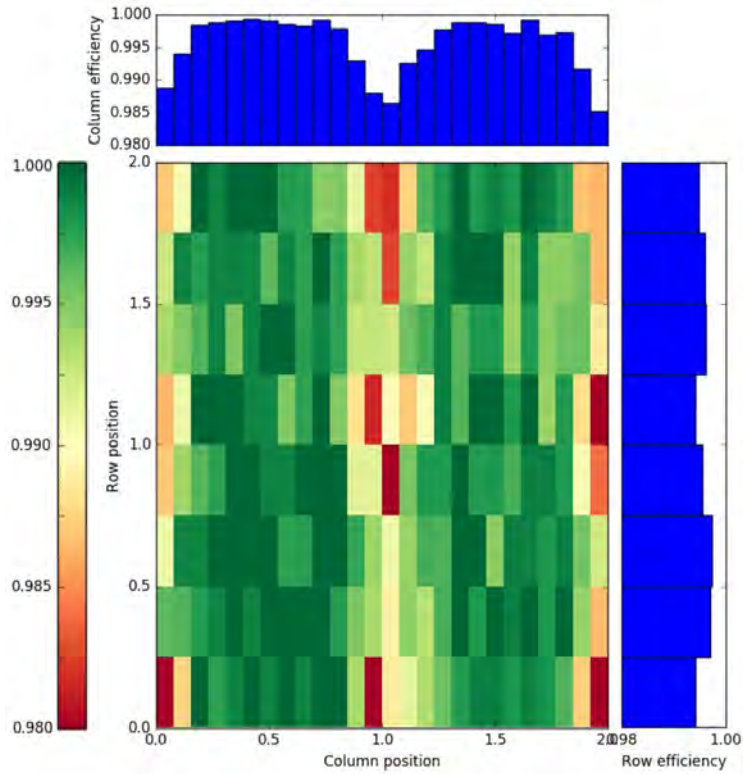
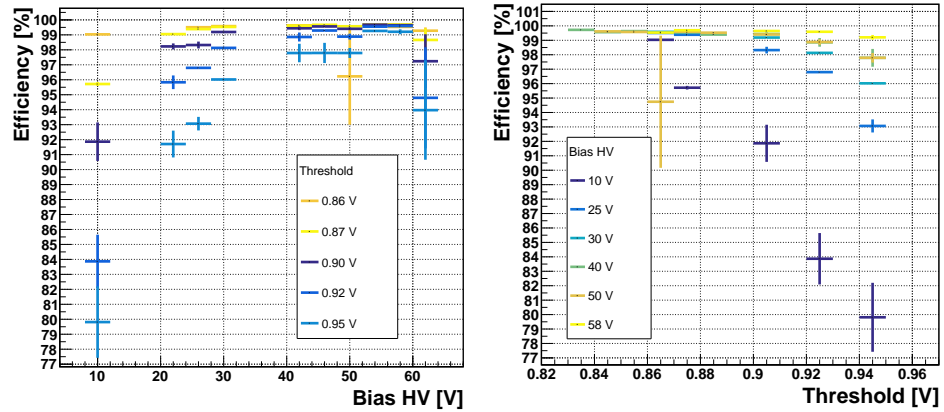


Figure 9.33: In-pixel efficiency for the 200 Ωcm sample at 60V and $\sim 740 e^-$ threshold.

It is possible to see that the detection inefficiency comes from the regions between pixels. These corner regions with low efficiency can possibly be mitigated with higher bias voltages, back sensor biasing (homogenising the electric field in the sensor bulk), or lower threshold values.

Figure 9.34a shows the ATLASpix scan in the bias voltage, for different thresholds configured, as measured at CERN SPS. Higher efficiencies are achieved by the increase of the high voltage applied to the sensor. The measurements show that with a sufficient low threshold it is possible to achieve an efficiency above 99% with a bias voltage of only 10 V. The efficiency for bias voltages above 60 V started to decrease, most probably due to the increase in the sensor leakage current.



(a) Efficiency *vs* bias high voltage, for different threshold settings. (b) Efficiency *vs* configured threshold, for several bias voltages.

Figure 9.34: ATLASpix bias high voltage and threshold efficiency scans.

Figure 9.34b shows the efficiency as function of the threshold, ranging from 860 mV to 950 mV (or ~ 740 to $1500 e^-$), for several high voltages applied to the sensor bulk. Comparing with the CCPDv4 scan results, where 3 distinct threshold operation regions with a plateau between 385 and 690 e^- can be seen, the threshold scan for the tested ATLASpix 200 Ωcm doesn't show an efficiency plateau for the lower threshold values, possibly due to the fact that the matrix threshold was not tuned, making the efficiency always decrease from a threshold at 860 mV ($\sim 740 e^-$).

9.3.3 Irradiation results

By the time of the conclusion of this thesis, systematic scans on a 200 Ωcm ATLASpix sample, irradiated with neutrons at the JSI reactor to a dose of $10^{15} n_{eq}/cm^2$, started to be done at SPS H8 beam line.

With the increase of the device irradiation, the sensor breakdown voltage increased, allowing to achieve higher bias voltages than before irradiation. The cluster sizes are comparable with the un-irradiated sample shown in Figure 9.27, with $\sim 90\%$ of the clusters containing a single pixel. The measurements performed on this irradiated sample

were ran on a faster clock of 160 MHz, yielding a time-stamp of 6.25 ns. The timing measured for the 200 Ωcm irradiated with neutrons at $10^{15} \text{ n}_{eq}/\text{cm}^2$ with bias voltage at 85 V and threshold of 0.88 V (corresponding to ~ 800 electrons⁵) is shown in Figure 9.35.

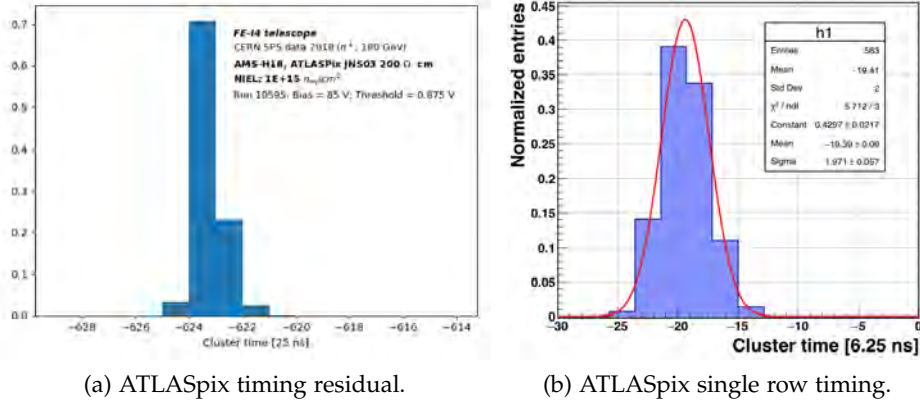
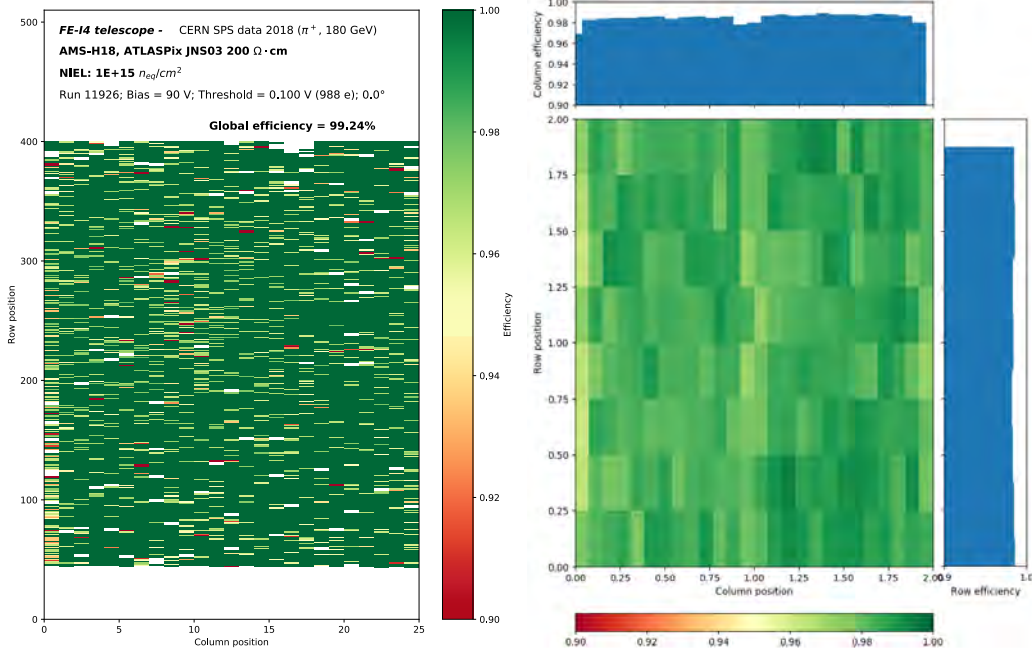


Figure 9.35: Timing distributions measured for the full ATLASpix matrix (a) and for a single row (b).

Figure 9.35 shows that about 70% of the hits are detected in one BC, while $> 90\%$ of the hits are detected within two BCs (50 ns). A dependence of the timing measured with the row address was again measured and, to evaluate the performance that the detector can achieve with a row timing correction, the timing residuals for the middle row is shown in Figure 9.35. A σ deviation of 12 ns was measured from a Gaussian fit, being consistent with the achieved timing before irradiation and with the CCPDv4 prototype.



⁵ Using the calibration factor measured for an un-irradiated sample.

The detection efficiency mapped over the pixel matrix is shown in Figure 9.36 for the full matrix (left) and projected into a 2x2 pixel matrix (right). As for the un-irradiated results, the bottom rows of the ATLASpIx matrix are outside the acceptance of the telescope.

An average efficiency of 99.24% is achieved and, by excluding from the calculation pixels with less than 10 entries, masked pixels and its first neighbours, the efficiency is $> 99.5\%$. The in-pixel efficiency shows no strong efficiency dependency of the hit position within different in-pixel regions.

The pixels efficiency distribution is shown in Figure 9.37. It is possible to see that most of the pixels have efficiency close to 100%, while a few pixels have efficiency $< 85\%$. Possibly, these outlier pixels can be recovered with the threshold tuning, which was not performed on the ATLASpIx prototype as already mentioned before.

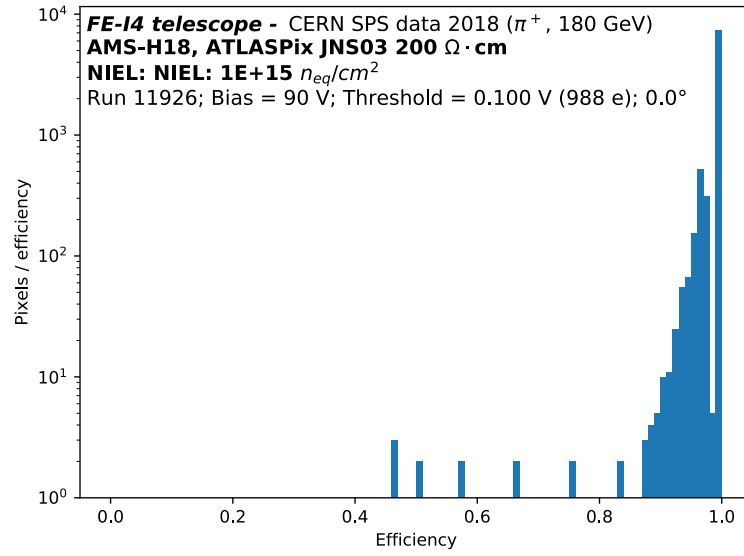


Figure 9.37: Pixels efficiency distribution for the 200 Ωcm sample irradiated at 10^{15} neq/cm^2 (80V bias; $\sim 1000 \text{ e}^-$ threshold).

9.4 SUMMARY OF THE RESULTS

To provide a clear picture of the performance of the several HV-CMOS prototypes shown here, a summary regarding the main aspects investigated follows.

9.4.1 General aspects

The prototypes spatial resolution has shown to be dependent on the pixel pitch and on the size of the pixel clusters, as expected. With a pixel pitch as the ATLASpIx prototype ($130 \times 40 \mu\text{m}$), for example, a better spatial resolution can be achieved when compared with the ATLAS IBL modules (with pixel pitch of $250 \times 50 \mu\text{m}$).

Due to the small extension of the depletion region in the sensor bulk (in between 10 to $50 \mu\text{m}$, depending in the bias HV and substrate

resistivity), the signal generated by a MIP particle (generating ~ 80 electron/hole pairs/ μm) is usually much smaller when compared with a planar sensor (with depletion extending completely through the sensor bulk). Therefore, a small threshold is needed to achieve a good signal-to-noise ratio. The CCPDv4 prototypes has shown great capability in tuning the matrix threshold, achieving thresholds as low as $520 \pm 30 \text{ e}^-$ in test-beam runs, while the monolithic ATLASpdx (without tuning) could be operated without noise with threshold at $700 \pm 200 \text{ e}^-$ before irradiation and $\sim 1000 \text{ e}^-$ after irradiation.

The results of the different substrate H35DEMO resistivities investigated show that high efficiencies can be achieved at lower bias voltages when using higher substrate resistivity. In addition, as shown by the H35DEMO timing plots, little influence from the substrate resistivity was seen on the signal rise time, in agreement with TCT measurements [129], indicating that the timing resolution is determined mainly by the pixel electronics design.

9.4.2 Timing measurements

The prototypes have shown timing resolution comparable with the current ATLAS IBL modules. For the CCPDv4 prototypes before irradiation an efficiency $>90\%$ is achieved integrating the hits in 3 BCs (75ns), with room for improvement from time-walk correction or a synchronized beam measurement. After irradiation, and with the implementation of the telescope CPV, an efficiency of $\sim 95\%$ within 3BCs was measured. This can be explained by the acceptor-removal effect which increased the charge signal generated after irradiation, mitigating time-walk effects.

A first investigation of the timing performance of the ATLASpdx was performed. The results are comparable to those of the CCPDv4 prototype. Before irradiation $\sim 90\%$ efficiency is achieved within 2 BCs. After irradiation the timing performance improved, similarly to CCPDv4, where $>90\%$ of efficiency is achieved for 2 BCs. In addition, it was found that the ATLASpdx timing is affected by time-walk effect and hit row address, indicating that with calibrated corrections the timing performance can be improved significantly.

9.4.3 Detection efficiency

Prototypes have been measured with different thresholds and HV bias voltages in order to determinate the detector operational configuration for a high detection efficiency. The tests performed with the CCPDv4 prototypes have shown an efficiency of up to 99.7% with a biasing voltage of 85V and a threshold of 600 e^- before irradiation. The efficiency after irradiation was found to be maximized between fluences of 5×10^{14} and $10^{15} \text{ n}_{eq}/\text{cm}^2$, where a detection efficiency of 99.7% was measured.

An efficiency above 99% was also measured for all H35DEMO substrate resistivities, when a high bias voltage is applied. Regarding the pixel electronics design, the most significant effect on the efficiency is linked to the addition of the Deep P-Well implant for the high-voltage implant, degrading the detection efficiency in both analog matrices, while the use of ELT or linear transistors don't have a significant impact on the pixel performance.

The full monolithic ATLASpix has also shown high detection efficiency. The measured efficiency for a $200\ \Omega\text{cm}$ sample, at 60V and threshold at $\sim 740\ \text{e}^-$, is 99.65%. After an irradiation dose of $10^{15}\ n_{eq}/\text{cm}^2$ an efficiency of 99.24% is measured. These results can be used to confirm the possibility to use HV-CMOS for detectors in collider experiments, since they exhibit similar performance to the detector technology currently implemented in the ATLAS experiment.

CONCLUSIONS

HV-CMOS prototypes have been investigated for a possible usage at the outer pixel layers of the ATLAS ITk upgrade, which will cover a large surface area requiring a large number of modules to be produced. Monolithic devices offer great advantages as no hybridization step needs to be done, saving time and cost and facilitating the pixel modules production. Traditional monolithic detectors, based on CMOS technology, don't fulfil the ITk requirements regarding timing and radiation hardness. Therefore, new detector devices are being investigated using the commercial HV-CMOS technology. In addition to the ATLAS upgrade, the detector proposal for the future CLIC experiment also foresees a possible use of HV-CMOS devices as sensors for capacitively coupled pixel detector modules. In this context, multiple HV-CMOS prototypes were designed and characterized in order to evaluate their performance.

An advantage of this new technology, when comparing with traditional CMOS, is the capability of sustaining high bias voltages applied to the device bulk without compromising the operation of the device transistors. It was verified that, for different HV-CMOS prototypes, break-down voltages above 100V can be achieved, while keeping a low leakage current ($<1 \mu A/cm^2$), providing an high electric field in the sensor bulk assuring a fast drift charge collection and, consequently, fast particle signals providing a good timing measurement. This aspect of the HV-CMOS devices is comparable with what is achieved in traditional planar silicon sensors.

To use HV-CMOS devices as sensors for the production of CCPDs, a precise and accurate flip-chip assembly procedure is needed to guarantee a homogeneous pixel coupling across the matrix. Systematic tests on flip-chip assemblies have shown that pixel pads alignment precision $<2 \mu m$ is achievable while keeping a planarity between the chips in the order of a few hundreds μrad . Finite element simulations of the pixel coupling has shown that the cross-coupling between neighbouring pixel pads is 2-4%, for a pixel pitch of $35 \mu m$, while for larger pixel pitch (such as $50 \times 50 \mu m$ on the H35DEMO) the cross-coupling decreases to 0.4%. In addition, it was verified that the possible uncertainty from the flip-chip process should affect the direct pixel coupling by about 5%. The cross-coupling in detectors with small pixel sizes can be mitigated with the use of a guard-ring. The simulation has shown that the use of a guard-ring around the pixel pads can reduce by a factor of 8 the cross-coupling effect.

The prototypes measured at test-beams (with the UniGE FE-I4 telescope), have shown good performance, and proved to be a valid candidate to be used for the ATLAS ITk upgrade. The CCPDv4 proto-

type, only available with substrate resistivities of 10-20 Ωcm and read-out by the FE-I4 ASIC, was used to investigate the radiation hardness of the device bulk at the expected ITk fluences. Before irradiation, and at optimal bias of 85V and 600 e^- threshold, the detection efficiency measured is 99.7%, a performance similar to the planar sensors used at the ATLAS IBL. Irradiated samples were also tested with fluences of 1.3×10^{14} , 5×10^{14} , 1×10^{15} and $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$, yielding an average hit efficiency of 98.1%, 99.7%, 99.7% and 97.6%, respectively. The CCPDv4 timing resolution at $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ shows an efficiency of >85% for one BC, being comparable with the IBL telescope module, and >95% over three BCs.

The investigation of the effect of the substrate resistivity on the performance of the detector and the evaluation on the feasibility of building large area HV-CMOS sensors was done with the H35DEMO prototype, also coupled to a FE-I4 ASIC. In addition, with the large size of the device allowing multiple pixel flavours to be designed and tested, different pixel circuits were tested. The results of this investigation shows that detection efficiencies larger than 99% can be achieved for all resistivity values studied. Higher resistivity results in larger signals and better efficiency at lower bias voltages. In addition, the time resolution of the different prototypes has shown little dependence on the substrate resistivity, indicating that the timing resolution is determined by the preamplifier itself, with little influence from the signal strength and varying rise time.

The ATLASpax prototype is the first large area monolithic HV-CMOS prototype designed and tested. By the time of this thesis only 200 Ωcm samples were tested. Before irradiation and at 60V and $\sim 740 \text{ e}^-$ threshold, the timing and efficiency performance are similar to those of the CCPDv4. Detection efficiency of 99.65% was measured, with a timing resolution in the order of 12 ns. After neutrons irradiation up to $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$, an efficiency of 99.37% is achieved (at 85V and threshold $\sim 1000 \text{ e}^-$) with a timing resolution still of 12 ns.

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