Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

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Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

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Abstract. The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment. TileCal is a sampling calorimeter with steel as absorber and scintillators as active medium. The scintillators are read-out by wavelength shifting fibers coupled to photomultiplier tubes (PMTs). The analogue signals from the PMTs are amplified, shaped, digitized by sampling the signal every 25 ns and stored on detector until a trigger decision is received. The High-Luminosity phase of LHC (HL-LHC) expected to begin data taking in 2026 requires readout electronics suitable for a 1 MHz trigger rate, higher ambient radiation, and for better performance under high pileup. Both the on- and off-detector TileCal electronics will be replaced during the shutdown of 2024-2025. PMT signals from every TileCal cell will be digitized and sent directly to the back-end electronics, where the signals are reconstructed, stored, and sent to the first trigger level at a rate of 40 MHz. This will provide better precision of the calorimeter signals used by the trigger system and will allow the development of more complex trigger algorithms. Changes to the electronics will also enhance the data integrity and reliability of the system. Three front-end board options were built and investigated both in laboratory and in several beam test campaigns. The final version has been chosen after evaluating the results. A hybrid *Demonstrator* for the new readout architecture and compatible with the present system has been developed, adopting the new chosen front-end option. The *Demonstrator* is undergoing extensive testing and is planned for future insertion in ATLAS.

1. Introduction

TileCal [1] is the central hadronic calorimeter of the ATLAS experiment [2] at the Large Hadron Collider (LHC) at CERN. TileCal was designed to achieve high performance in the energy reconstruction of hadrons, jets, tau-particles and missing transverse momentum. It is a sampling calorimeter using steel plates as passive absorber and plastic scintillator tiles as active material. The TileCal detector is composed of three cylinders subdivided azimuthally into 64 wedge modules each. Two readout sections of the central cylinder form the Long Barrel (LB) sides (LBA, LBC), while the other two cylinders, located on each side of the LB, are called the Extended Barrel (EB) sections (EBA, EBC). The light produced by each scintillating tile is collected by two wavelenght shifting (WLS) fibers and fed to readout Photo-Multipliers (PMT). WLS fibers are grouped in bundles coupled to the PMTs to define TileCal cells with projective geometry as shown in Figure 1. The modules in the LB are equipped with up to 45 PMTs whereas 32 PMTs are needed to read out the EB modules. The PMT blocks, including fiber bundle head, light mixer, and PMT, and the on-detector electronics are installed in mechanical structures, called super-drawers, housed inside girders in the outermost part of the modules.

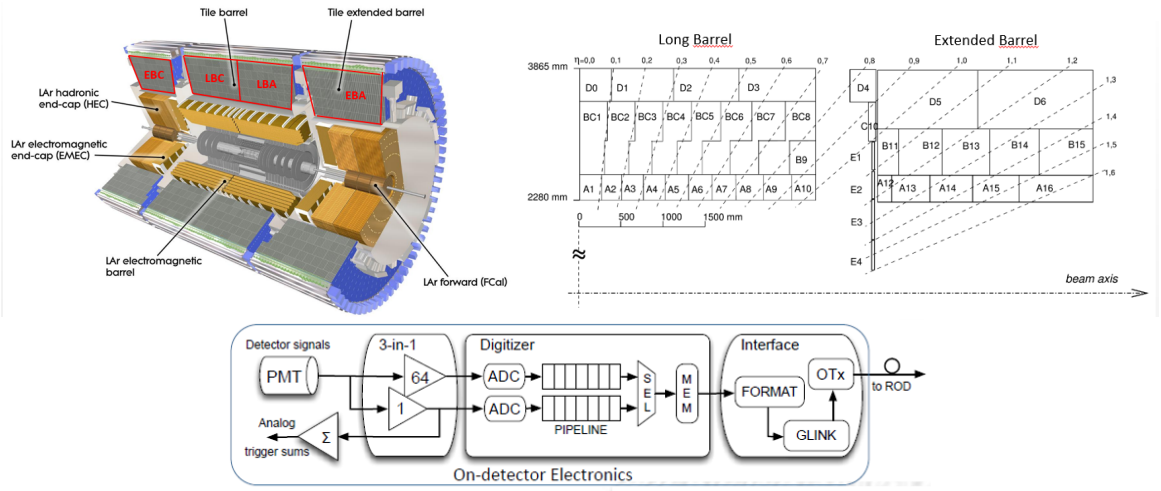

Figure 1. ATLAS calorimeters (top-left) and TileCal longitudinal cross-section with individual cell geometry and labelling (top-right), and current diagram of the readout system (bottom)

A total of 9852 PMTs are used to readout the TileCal cells. The PMT signals are amplified, shaped, and digitized at 40 Msps (Mega Samples Per Second) using a clock synchronous with the LHC beam crossing. The digital samples are stored in pipeline memories during the Level-1 trigger latency (2.5 μs). PMT analog signals are analog summed and transmitted to the Level-1 Calorimeter system. The digital samples corresponding to the events selected by the Level-1 trigger system are transmitted through optical fiber to the off-detector ReadOut Drivers (RODs) [3] at a maximum average rate of 100 kHz. The main tasks of the RODs, executed in Digital Signal Processors (DSPs), are energy and time reconstruction, synchronization of detector and trigger data, busy handling and data compression. Data are processed within 10 μs and transmitted to the High Level Trigger (HLT) system of ATLAS [4]. The present TileCal readout architecture is shown in Figure 1.

At High Luminosity LHC (HL-LHC), the instantaneous luminosity will increase up to $7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$, producing about 200 p-p collisions per bunch crossing with a corresponding increase of the particle flux through TileCal (up to about 80 Gy for 4 ab^{-1} integrated luminosity). Replacement of the readout electronics is mandatory because the current readout architecture is not compatible with the new fully digital Trigger/DAQ (Data AcQuistion) system of ATLAS. The demanding requirements for trigger and data flow rates at HL-LHC and the ageing of the present electronics due to operation time and to radiation require an upgraded readout.

All other detector components (steel absorbers, scintillating tiles, fibers and almost all the PMTs) will not be replaced. Studies to assess the detector optics robustness are in progress.

2. Upgrade of the TileCal readout electronics

Some general concepts for detector upgrades of the LHC experiments were adopted in the design of the new TileCal readout system such as the use electronic parts tolerant to the expected radiation level and the design of a readout architecture suitable to sustain the higher trigger rate (> 1 MHz) and the larger event buffer (latency > 10 μs). Some main guidelines were adopted: move buffers and pipelines off detector, read out data at 40 MHz (LHC bunch-crossings frequency), and improve reliability through redundancy to limit the impact of component failures.

The new readout concept is based on the choice to have a new modular geometry of the

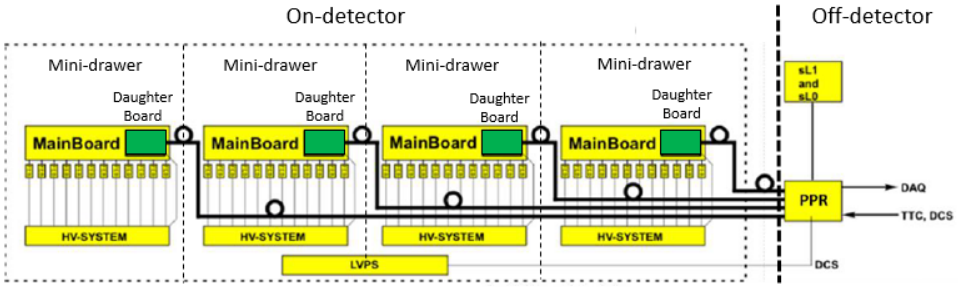

Figure 2. Block diagram of the TileCal upgrade readout architecture.

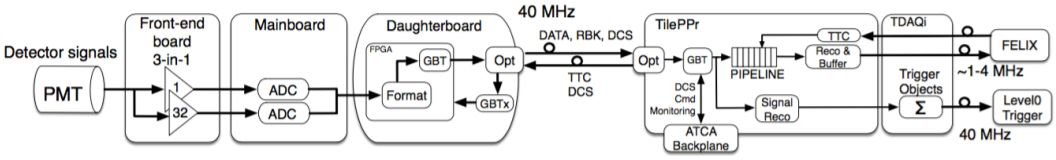

Figure 3. Sketch of the TileCal upgrade readout electronics for HL-LHC.

mechanics hosting the PMT blocks and the readout electronics. The 45 (32) PMTs in a long barrel (extended barrel) module are located into 4 (3) identical mini-drawers, each hosting up to 12 PMTs. The mini-drawer geometry to readout each individual TileCal module is shown in Figure 2.

A Main Board (MB) is placed on top of each mini-drawer structure. It receives the PMT analog signals from the front-end boards (FEB) and digitizes them. The digitized data are sent to a Daughter Board (DB). The MB also provides the control of the High Voltage. The DB synchronizes the digitized data and sends them to the Pre-Processor (PPr) via optical links. The DB also distributes the timing, control and configuration signals received from the PPr. The PPr, located off-detector, communicates with all the DBs, organizes data in pipelines, implements data reduction, and transmits the data selected by the trigger to FELIX (Front-End LInk Exchange), the future ATLAS digital DAQ and Trigger system [5]. It also receives the timing and control signal from the LHC and from ATLAS, and distributes the commands for the DCS system. More detailed descriptions of the individual components are given in the following subsections. A sketch of the full readout chain for the HL-LHC upgrade is shown in Figure 3. A special version of the upgrade electronics, called *Demonstrator*, was built to readout at the test beam a spare module of TileCal. In this case, full trigger and readout compatibility with the present architecture was kept for allowing to compare the performance of the two architectures.

2.1. Front-End Board

Three FEBs were proposed and tested. One board, called *3-in-1* [6], is the evolution of the present FEB and it is assembled with radiation hard discrete components. The two other options implement different designs based on custom ASIC chips. One board, called *QIE* [7], splits the PMT anode current in four channels corresponding to different ranges and associated to a gated integrator with a 7-bit ADC. The other ASIC (Application-Specific Integrated Circuit) option, called *FATALIC* [8], has a current conveyor with gain ratios 64:8:1 followed by an RC shaper and a 12-bit ADC per gain. Both ASIC options have a 17-bit combined dynamic range. The FEB card selection process was completed before the submission of the TileCal TDR [9]. The *3-in-1* option was chosen because it provides the best accuracy for the minimum bias integrator

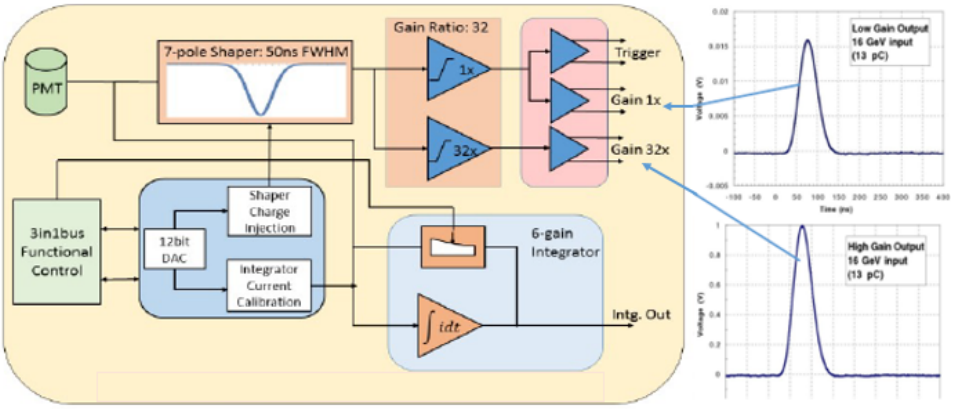

Figure 4. Diagram of the *3-in-1* card (left) and waveforms of the bi-gain channel outputs (right).

and luminosity scan, coupled with the fact that it is based on a well proven design. A functional diagram of the *3-in-1* card is shown in Figure 4.

The PMT output is split into two paths for fast and slow signal processing. The fast signal processing includes a 7-pole passive LC shaper with 1KHz - 12.5 MHz bandwidth. The shaped signal is amplified in parallel with two gains with 32:1 ratio. The high-gain channel covers an input dynamic range of 0-25 pC suitable for processing the low energy particle signals. The low gain channel covers an input dynamic range of 25-800 pC to process signals generated by high energy hadrons. Both low and high gain amplifiers send the analog signals to the MB for digitization. For compatibility with the current Level-1 trigger, an analog trigger sum is also included on the *3-in-1* card version for the *Demonstrator*. Shaped signals are digitized with 12-bit, 40 Msps ADCs in the MB and the combined bi-gain system achieves input dynamic range of 17 bits. A 12-bit DAC is used for response calibration with charge injection cycles controlled by a 40-conductor digital bus in LVDS signal standard.

2.2. Main Board and Daughter Board

The Main Board associated to each mini-drawer is divided into four sections, each served by one Altera Cyclone IV FPGA. Each section handles the signals from 3 PMTs. A quarter of the MB functional block diagram (one section) is shown in Figure 5.

The FPGA controls low gain and high-gain ADCs, including input bias voltage levels, and serves as a communication hub between FEBs and DB. Each FPGA of the MB communicates to the DB with a dedicated SPI port. Two timing signals that initiate the low-gain and high-gain CIS calibrations are also provided. The digitized data from the low-gain and high-gain channels are sent to the DB on a dedicated serial bus without FPGAs involvement. The integrator ADC data is readout directly by the DB via a standard I2C bus.

To digitize three PMT bi-gain signals in a section, 6 channels of 40 Msps 12-bit ADCs and 3 channels of 50 kHz 16-bit ADCs for the slow integrators are used. Converted data are sent to the DB at 560 Mbps (14-bit $\times$ 40 Mbps) with redundant serial link (80 Gbps).

The MB is physically divided into two equal parts with independent powering from Point-Of-Load (POL) regulators receiving +10V from Low Voltage Power Supplies (LVPS) with independent bricks connected in "Diode-Or" to reduce single point failure effects.

The DB [10] is plugged on the MB through a 400-pin connector. The DB receives timing, trigger and control (TTC) signals and slow control commands from the Back-End Pre-Processor

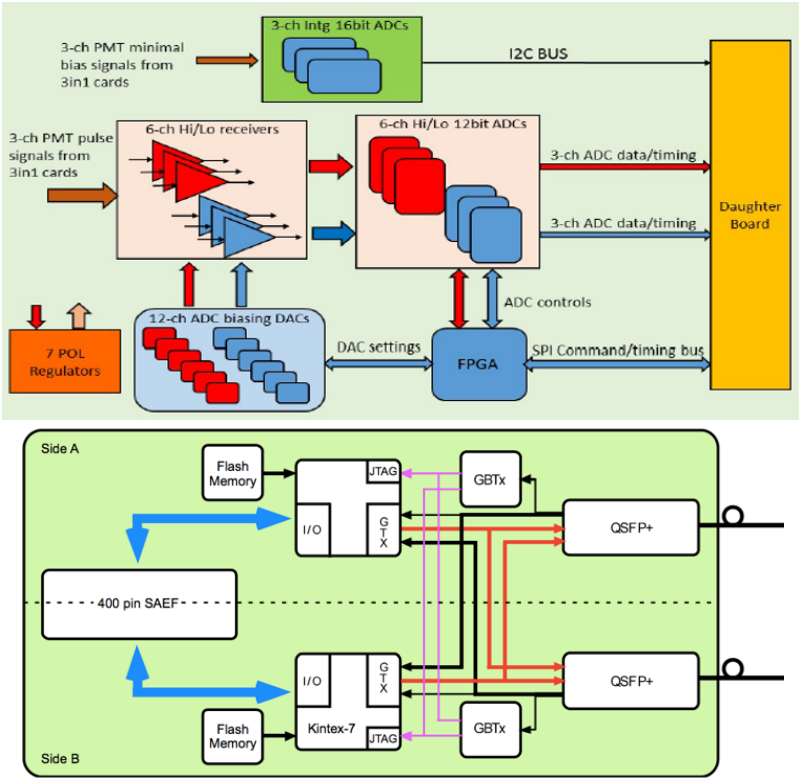

Figure 5. Block diagrams of the Main Board (top) and of the Daughter Board (bottom).

module. TTC signals and commands are distributed to the MB and to High Voltage board located underneath the mini-drawer mechanical structure. Digitized data received from the MB are packed with the integrator and monitoring data and transmitted to the TilePPr through a pair of redundant 9.6 Gbps GBT links per side. The functional block diagram of the DB is shown in Figure 5.

The DB is divided in two sections which can be operated independently, each section serving up to 6 FE channels. In the DB version V4 used at present in the *Demonstrator*, the interface with the PPr is implemented through redundant Quad Small Form-factor Pluggable (QSFP) connectors and the system is managed by two Xilinx Kintex-7 FPGAs. Two GBTx chips are used to manage the system clock and FPGA remote configuration. In the latest DB version V5, FPGAs are replaced with the powerful Xilinx Kintex Ultrascale+ model and the two QSFP connectors are replaced with four 850 nm multi-mode Small Form-factor Pluggable (SFP) connectors.

2.3. Back-End Electronics

The TileCal upgrade Back-End (BE) electronics consists of a Pre-Processor (PPr) and of an interface (TDAQi) with the ATLAS Trigger and Data Acquisition system (FELIX). PPr and TDAQi are hosted in a customized ATCA carrier. The design of the full scale PPr is being finalized and it is intended to serve eight TileCal modules (Super-Drawers, SD) as shown in Figure 6. It will contain four Compact Processing Modules (CPM) with a main FPGA each, and one TDAQi Rear Transition Module (RTM) with a FPGA used for managing the new digital trigger. Communication with FELIX will be ensured with optical transceivers with multimode fibers.

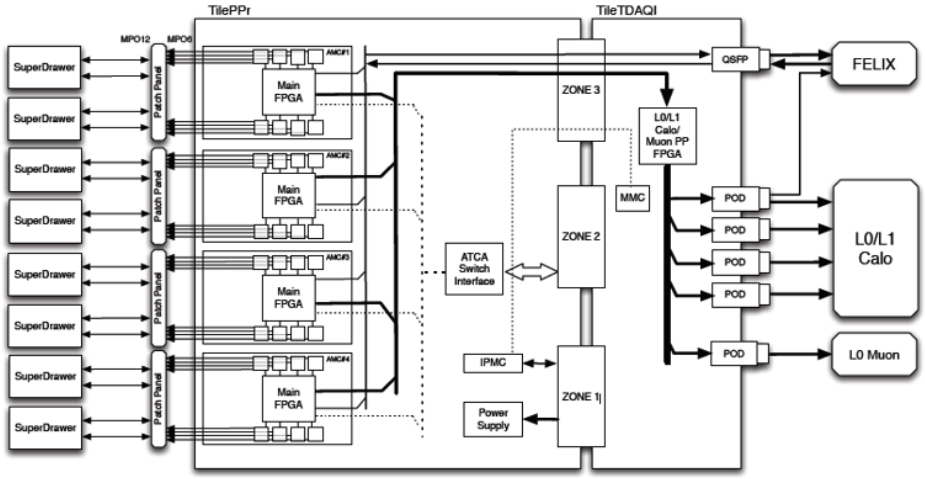

Figure 6. Functional Block diagram of the Back-End electronics.

Two prototype PPrs [11] are in use in the *Demonstrator*, each serving one SD and corresponding to 1/8 of the full scale PPr. They have been extensively tested during data taking at the test beams with integration to the FELIX system. The prototype PPr receives the digitized data from four Daughter Boards at 40 MHz through the four QSFP modules requiring a total input bandwidth of 160 Gbps. Data are unpacked and stored in the circular pipeline memories of the Readout FPGA. Upon reception of a Level-1 trigger Acceptance (L1A) signal, the TilePPr collects the data for the selected event from the pipelines and transmits them to the FELIX system (16 samples, 2 gains) and to the legacy RODs (7 samples, 1 gain) with the proper format keeping backward compatibility with the current ATLAS DAQ system.

Other functions performed by the CPMs are the remote configuration of the FE electronics FPGAs and the data calibration and processing for cell energy reconstruction in real time every bunch crossing. Additional functionality of the TDAQi RTM is the calculation of the trigger objects by defining trigger towers with different size in pseudorapidity and azimuthal angle.

3. High Voltage and Low Voltage power supplies

Two options for the High Voltage Power Supplies (HVPS) are under evaluation at the moment. They have different locations of the distribution and monitoring electronics.

Option 1: *Remote* control system (baseline) bulk HVPS and regulators will be installed in the ATLAS service cavern. This solution requires 100 m long HV wires for each individual PMT. Advantages are easy maintenance and no radiation hardness issues. A 12-channel prototype is used at the test beams. HV cables with higher density wire bundles from different companies are under evaluation. Challenge is fitting and routing in the detector volume large cable bundles with big HV connectors.

Option 2: *Internal* control system (back-up): bulk HVPS are located in the underground service cavern, but regulators are placed on-detector. Individual channel control is operated through the Daughter Board. Advantage is the reduced number of HV cables (only one HV cable per module (SD)), but maintenance is much less easy with no accessibility during normal operations.

Low Voltage distribution for the upgraded detector is made by a three stage power system based on the current Low Voltage Power Supplies (LVPS) design. Improvements with respect to the present system are better reliability, lower noise, improved radiation tolerance, and a

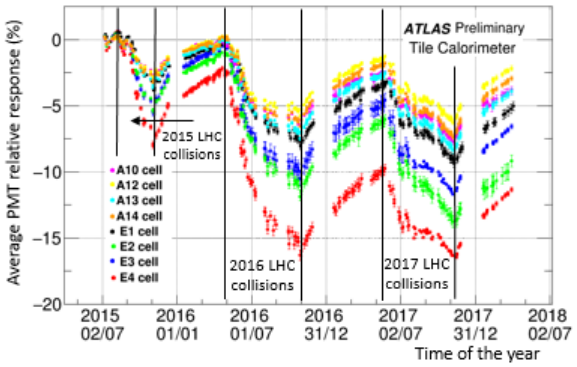

Figure 7. Relative variation of the average response of the PMTs reading out the most exposed TileCal cells [12].

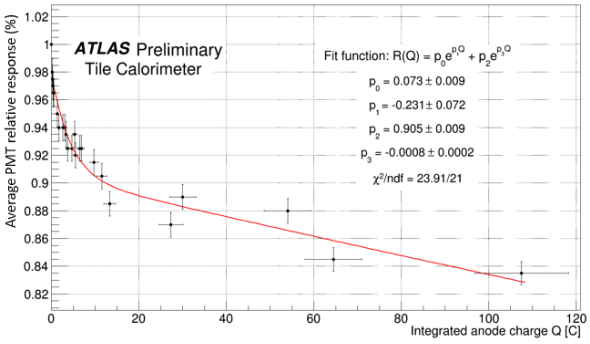

Figure 8. Relative variation of the average response of the PMTs reading out the most exposed TileCal cells as a function of the integrated anode charge [12].

smaller number of connections. Only one DC level (+10V) and POL regulators are needed for feeding all local circuits. Two individual *bricks* per mini-drawer are used. Redundancy is actuated by the control in the Main Board of the brick pairs arranged in diode OR. Voltage control and monitoring is done through the new ATLAS slow control system. Eight bricks (1 SD) are assembled in a box located in the TileCal SD extension called finger. Each individual brick requires remote on/off control.

4. PMT robustness studies

Actions to prevent loss in detector perfomance due to the ageing of the optics are also considered part of the TileCal upgrade program. We restrict here to the photo-detectors robustness studies and replacement plans. Full replacement of the readout PMTs of TileCal is not foreseen, no relevant variation of the PMT response was seen so far during LHC run 2 for the main part of the PMTs. The time evolution of the response was studied for the PMTs reading out the most exposed cells of the barrels and of the special scintillators located in the gap between the detector sectors. The PMT response to laser excitation measured in calibration data samples shows a reproducible pattern (Figure 7). A down-drift of the PMT response is observed at the beginning of each p-p collision period, while a partial recovery is seen when no beams circulate in the accelator during shut-down periods.

The response variation is expected to depend on the amount of integrated PMT anode charge and on the rate of charge integration (anode current). To make a prediction of what one can expect in terms of response loss for the PMTs reading out the most exposed cells which will integrate some 600 C after the completion of the HL-LHC program, a plot of the response loss was built as function of the anode integrated charge. Using the conversion tables luminosity-integrated anode charge obtained by looking to the integrator response of the FE electronics and plotting the average response loss at the end of each collision period during run 2, the plot shown in Figure 8 was obtained. The considered cells integrated a different amount of anode charge in the same time period.

Driven by only visual inspection of the plot, a two-exponential model was made for the PMT response loss as a function of the anode integrated charge. No difference on the slope parameters was found within the errors, dominated by the PMT-to-PMT response variation, if the model for the fit is changed into an exponential plus a straight line. The loss slow rate was measured to be 0.08% per Coulomb. It was decided to replace for HL-LHC data taking all PMTs expected to loose more than 25% in response. Based on the model described above, only a fraction of

the PMTs (about 10% of the full 10,000 unit sample), reading out the most exposed cells in the inner layer will be replaced with the latest and improved version of the same PMT type. The better performance in terms of response loss and quantum efficiency of the latest PMT version, model Hamamatsu R11187, was measured at the bench.

5. Conclusions

A wide R&D program for the new TileCal readout electronics for HL-LHC is progressing well. Prototypes of all elements of the full readout chain for the HL-LHC upgrade are intensively tested exploiting a *Demonstrator* reading out a TileCal spare module. Test beam results are used for continuous tuning of the new versions of each component of the Front-End and Back-End electronics. The design and the production of a full-size protoype of the Pre-Processor with the interface to the future ATLAS Trigger/DAQ system will be ready before insertion of the *Demonstrator* in TileCal which is foreseen for the next LHC Long Shutdown (2019).

Radiation hardness tests for all elements of the system are on-going and close to be completed. The design of the new super-drawer mechanics is completed, prototypes are available, including a different option for the Extended Barrel and a new drawer extraction system.

Studies on PMT lifetime and robustness are in progress, the response evolution was modeled based on the available calibration data. Projections to the HL-LHC era were made leading to the decision of replacing the present PMTs reading out the most exposed cells with a same geometry model and improved robustness.

In general, high reliability of the upgraded system will be achieved through redundancy, modularity, and increased robustness against irradiation effects.

Acknowledgments

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