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HIGH-RESPONSE PLC-BASED MACHINE PROTECTION SYSTEM DEVELOPMENT AND PERFORMANCE FOR SRILAC

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Abstract

The RIKEN linear accelerator (RILAC), which is among the injectors for cyclotrons at the radioactive isotope beam factory (RIBF), was upgraded by installing a superconducting RILAC (SRILAC) to search for superheavy elements with element numbers 119 and above. Prior to conducting the SRILAC upgrade, the machine protection system in RILAC was constructed using simple relay circuits. However, most of the accelerators at RIBF other than RILAC have been equipped with machine protection systems using Mitsubishi MELSEC-Q programmable logic controllers (PLCs) since 2006. They follow a mechanism that was triggered an anomalous signal to drive the beam chopper to stop the beam, and are called beam interlock systems (BIS). Machine protection was required in the SRILAC project to prevent vacuum deterioration of the superconducting cavity owing to changes in the beam envelope. Thus, we developed an FA-M3 PLC-based system to realize a BIS with high response performance at a lower cost than conventional systems. This system was characterized by implementing both relatively slow response and I/O requiring high response performance. For example, in the case triggered by an anomalous signal from the electromagnet power supply, the simulation of the beam envelope indicated that the response performance was relatively slow, with a few milliseconds being sufficient.

INTRODUCTION

One of the injectors in the RIKEN radioactive isotope beam factory (RIBF) is the RIKEN linear accelerator (RILAC) [1]. RILAC serves as an injector for the RIBF and provides beams for standalone experimental courses. Experiments are underway to search for superheavy elements with atomic numbers greater than 119, facilitated by an upgraded project. The primary upgrades to the RILAC include two significant improvements. The first is the installation of a new 28 GHz superconducting electron cyclotron resonance ion source (ECRIS) upstream, which enhances the beam intensity [2]. The second upgrade involves the implementation of a superconducting linear accelerator (SRILAC) downstream of the existing RILAC cavities to boost the beam energy [3]. Because of the increased beam intensity and energy from the upgrade, minor errors in the accelerator components could easily cause significant problems for the experimental equipment and the RIBF beamline downstream of SRILAC.

In addition, issues with superconducting cavities, such as quenching owing to vacuum deterioration caused by beam loss, must be avoided. Therefore, the machine protection system (MPS), a mechanism for protecting hardware from the beam, must be more advanced. In response to these requirements, an MPS was developed to operate SRILAC.

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PREVIOUS SYSTEM

Before the SRILAC project, the RILAC interlock system was implemented using hardware composed of mechanical relays. Consequently, the response performance of the previous system was not high, typically on the order of tens of milliseconds. In contrast, at RIBF facilities other than the RILAC, an interlock system based on the MELSEC Q-series programmable logic controller (PLC) is employed as the MPS [4]. This system prevents hardware failures caused by deviations in the beam trajectory from its normal orbit by driving a beam chopper located just downstream of the ECRIS in response to abnormal signals from components, such as power supplies, RF systems, and vacuum systems. In addition to the beam chopper, the system outputs signals to insert the Faraday cups depending on the type of input signal. This system is referred to as the beam interlock system (BIS), and its response time is of the order of 10 ms.

SYSTEM REQUIREMENT

The following system requirements have been established to develop the MPS for the SRILAC project. The system is designed to minimize the complexity of both hardware and software. In addition, human and machine protection systems are clearly separated, with the core logic of the system following the RIBF BIS. The selected hardware prioritizes long-term maintainability. Furthermore, all stages of system development and operation are handled by the team to facilitate system upgrades and rapid troubleshooting. The development of the upper-level system is based on the experimental physics and industrial control system (EPICS) channel access (CA) protocol, which is the standard control protocol at RIBF. For example, with abnormal RF signals, the system achieves a performance that exceeds the typical response of the capabilities of conventional PLC-based system such as RIBF BIS and drives the beam chopper.

SRILAC BIS SPECIFICATIONS

Controller

When selecting hardware for the SRILAC BIS, the goal was to develop and operate the system entirely within a team, thereby ensuring long-term maintainability. Consequently, the decision was made to construct the system

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using the FA-M3 series PLC, which has a proven track record at the RIBF [5-8] and is familiar to the team. Owing to concerns regarding reaching the upper limit of several internal registers, F3SP76-7S, the highest-performing sequence CPU module available at the time of system construction, was selected. The main BIS sequence was implemented on F3SP76-7S, whereas the upper-level system, including the user interface, was implemented using EPICS. To achieve this, a Linux CPU (F3RP71) [9] was installed in the second slot of the PLC-based module to create a multi-CPU configuration.

Communication

In the previous system, an interlock was designed with stations equipped with sequential CPU modules communicating via FL-net for CPU-to-CPU communication [10]. However, even in the smallest configuration (two stations), a communication-induced delay of several milliseconds was observed that increased with the number of I/Os. Therefore, CPU-to-CPU communication was avoided in the SRILAC BIS. Instead, the main unit of the CPU module communicates with seven subunits via an optical FA bus. This configuration facilitated mutual information exchange between the FA-M3 series units and the construction of a remote I/O system. The system employed a loop configuration using optical fibers to create a redundant FA bus network (Fig. 1). Further, based on the cable length, number of modules, and loop type, the I/O refresh time caused by the FA link in this configuration was theoretically calculated to be approximately 300 µs.

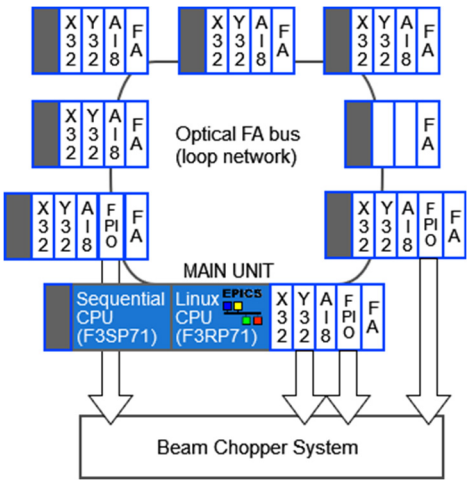

Figure 1: System chart of SRILAC BIS with optical FA bus network with redundancy

Sequence

Machine protection in the SRILAC operation was realized by the SRILAC BIS as a central part of the output of the SRILAC BIS to the beam chopper switch, and by inputting the interlock signals output by each system, such as the low-level RF and electromagnet power supply, to the SRILAC BIS (Fig. 2). When an abnormality was detected, the chopper stopped the beam and Faraday cups were inserted simultaneously. These sequences followed the RIBF BIS.

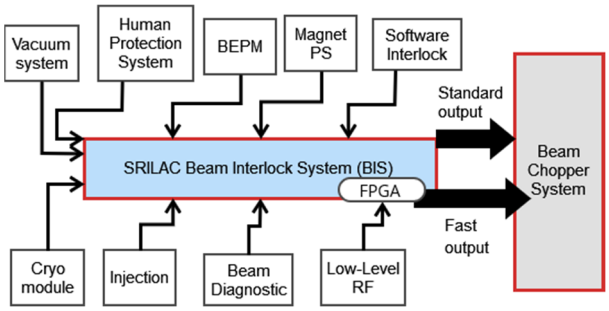

Figure 2: Flow chart of the entire system machine protection for SRILAC operation.

Standard I/Os

The input module used as the standard I/O was F3XD32-3F [11] as digital inputs and F3AD08-6R [12] as analog inputs. For the output module driving the beam chopper, the F3YD32-1H [11] was chosen owing to its catalog-specified response speed of less than 0.1 ms. For the output related to driving the Faraday cup, where a fast response time is unnecessary, F3YD32-1P [11] with a response speed of less than 1 ms was selected. These modules are referred to as standard I/O. For standard I/Os, the PLC units and numbers of input points are totally 280 points which combine digital and analog inputs.

High-Response I/Os

Typically, PLCs have a system response time of several milliseconds. FPGA are often selected for systems that require response times in the microsecond range [13]. In SRILAC operations, a high-speed response is necessary to stop the beam in response to error signals triggered by unstable RF phases from a low-level RF system. Thus, to achieve a high-speed response within a BIS based on the FA-M3 series, a field-programmable high-speed I/O module (F3DF01: FPIO module) [14] was selected, and the interlock logic was implemented in the FPIO module.

The FPIO module contained an FPGA (AMD Spartan-6 LX) [15] with 24 input and output points each as high-speed I/Os. A total of three FPIO modules are installed, and they mainly receive interlock signals from Low-Level RF. Because this logic can be implemented without passing through the sequence CPU module, it can be processed in parallel without being affected by the scan time of the program running on the sequence CPU module. In this system, settings such as enabling/disabling each input signal of the FPIO module were configured via the D or I register from the EPICS CA client. For high-response I/Os,

SYSTEM PERFORMANCE

The response times of standard I/Os were measured. The test condition involved the input of a 100 Hz interlock signal into the F3XD32-3F of Subunit #6, and the response time was defined as the time required for the output to be generated from the chopper switch connected to the main unit (Fig. 3). The results confirmed that the system operated with an average response time of 6 ms.

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Comparatively, the response time of the high-response I/Os was significantly shorter. In this test, a 100 Hz interlock signal was input into the FPIO module installed in the main unit, and the response time was defined as the time required for the output to be generated from the chopper switch. The result was approximately 78 µs, thus demonstrating a substantial improvement over the standard I/Os.

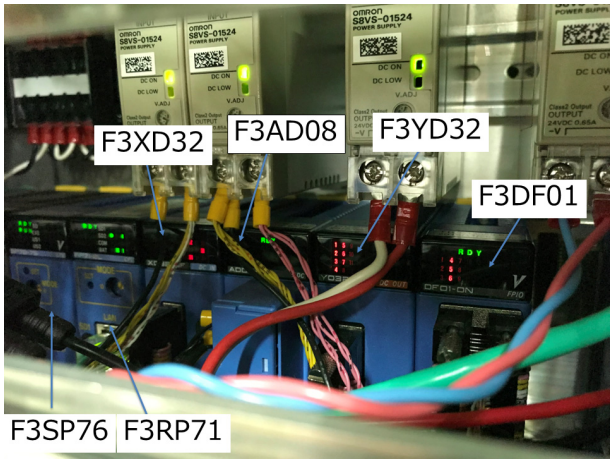

Figure 3: Photograph of the SRILAC BIS main unit.

VERIFICATION OF I/O PERFORMANCE

The SRILAC BIS includes both standard I/O and FPGA-based high-response I/O modules. When error signals are triggered by a low-level RF system, driving the beam chopper with standard I/Os may not be sufficiently fast, potentially leading to vacuum degradation within the superconducting cavity. Therefore, the error signals from a low-level RF system should be handled using high-response I/Os. Conversely, for triggers from electromagnetic power supplies, the response time of standard I/Os is expected to be sufficient. To verify this, magnetic field measurements at the quadrupole electromagnet upstream of SRILAC (Fig. 4) and beam dynamics simulations were conducted to assess the standard I/O performance. Figure 5 shows the decay of the magnetic field when an external interlock signal was input into the electromagnetic power supply, causing it to shut off. The current through the quadrupole electromagnet was 32 A before the external interlock signal was input.

The electromagnetic power supply received an external interlock signal and sent it to the SRILAC BIS as soon as the power supply was turned off. Assuming a time of 10 ms, the SRILAC BIS required 16 ms to stop the beam, because standard I/Os operate with an average response time of 6 ms. The results showed that the magnetic field after 16 ms, corresponding to the stopping of the beam by the standard I/Os, was equivalent to a current value of 94 % before the input of the external interlock signal. Using the beam dynamics simulation software TraceWin [16, 17], the simulation estimated the beam loss to be approximately 0.1 % when the current changed from 32 A, which was the actual operating current during the experiment, to 30 A. Because this beam loss is minimal, it can be concluded that the error

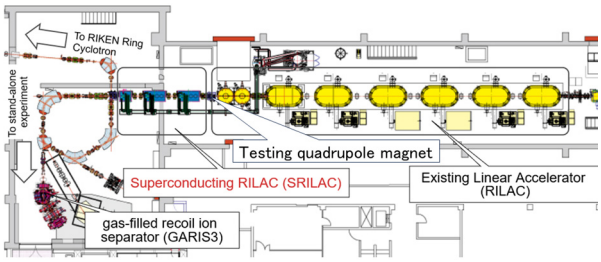

Figure 4: Placement of the quadrupole electromagnet for verification of I/O performance.

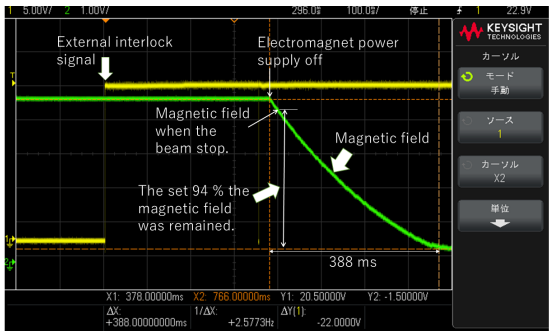

Figure 5: Screenshot of an oscilloscope measuring the decay of the electromagnet's magnetic field after inputting the external interlock signal and turning-off the electromagnet power supply.

signals from the electromagnetic power supply can be sufficiently managed using standard I/Os. Similarly, when signals from vacuum-control gate valves were input to the SRILAC BIS and the beam was stopped upon closing the gate valve, it at least 20 ms were required to close the gate valve. This indicated that standard I/Os are also sufficient in this case.

CONCLUSION

The MPS was constructed for the SRILAC operation. The SRILAC BIS was developed as a core component of the system and operates by receiving interlock outputs from other systems. After the interlock outputs were fed into the SRILAC BIS, the beam chopper and Faraday cup were driven based on the preset logic, thereby facilitating rapid beam stopping. With a response time of approximately 6 ms and standard I/O, the performance of the PLC-based system was satisfactory. In addition, to achieve response speeds of less than 100 µs, which were difficult with conventional PLC-based systems, an FPIO module was introduced, and FPGA internal logic was developed separately from the sequence CPU. By January 2020, the SRILAC beam commissioning had been completed [18], and the control system, including the MPS, had been operating without issues [19]. The new developed system enables us to provide the beam for experiments to search superheavy elements [20, 21].

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REFERENCES

[1] M. Odera *et al*., "Variable frequency heavy-ion linac, RILAC: I. Design, construction and operation of its accelerating structure", *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. 227, p. 187, 1984. doi:10.1016/0168-9002(84)90121-9

[2] T. Nagatomo *et al.*, "New 28-GHz superconducting ECR ion source for synthesizing new super heavy elements of Z > 118", in *Proc. ECRIS'18*, Catania, Italy, Sep. 2018, pp. 53-57. doi:10.18429/JACoW-ECRIS2018-TUA3

[3] K. Yamada *et al.*, "Construction of superconducting linac booster for heavy-ion linac at RIKEN Nishina Center", in *Proc. SRF'19*, Dresden, Germany, Jun.-Jul. 2019, pp. 502-507. doi.org/10.18429/JACoW-SRF2019-TUP037

[4] M. Komiyama *et al*., "Recent update of the RIKEN RI beam factory control system", in *Proc. ICALEPCS'17*, Barcelona, Spain, Oct. 2017, pp. 427-430. doi:10.18429/JACoW-ICALEPCS2017-TUPHA028

[5] M. Komiyama *et al*., "Upgrading the control system of RIKEN RI beam factory for new injector", in *Proc. ICALEPCS'09*, Kobe, Japan, Oct. 2009, paper TUP084, pp. 275-277. https://jacow.org/icalepcs2009/papers/TUP084.pdf

[6] M. Komiyama *et al.*, "Recent development of the RIKEN RI beam factory control system", in *Proc. PCaPAC'18*, Hsinchu City, Taiwan, Oct. 2018, pp. 66-68. doi:10.18429/JACoW-PCaPAC2018-WEP15

[7] A. Uchiyama *et al.*, "Control System Renewal for Efficient Operation in RIKEN 18 GHz Electron Cyclotron Resonance Ion Source", *Rev. Sci. Instrum.* vol. 87, p. 02A722, 2016. doi:10.1063/1.4934614

[8] A. Uchiyama *et al.*, "Design of reliable control with star topology fieldbus communications for an electron cyclotron resonance ion source at RIBF", in *Proc. PCaPAC'18*, Hsinchu City, Taiwan, Oct. 2018, pp. 105-108. doi:10.18429/JACoW-PCaPAC2018-WEP30

[9] EPICS Device and Driver Support for Yokogawa's F3RP71 and F3RP61, https://github.com/EPICS-F3RP61

[10] M. Komiyama *et al*., "Recent Updates of the RIKEN RI Beam Factory Control System", in *Proc. ICALEPCS'19*, New York, NY, USA, Oct. 2019, pp. 383. doi:10.18429/JACoW-ICALEPCS2019-MOPHA073

[11] Yokogawa General Specifications, "FA-M3 Basic Input/Output Modules", GS 34M06G01-01E, https://web-material3.yokogawa.com/GS34M6G01-01E.us.us.pdf

[12] Yokogawa General Specifications, "FA-M3 Analog Input Modules", GS 34M06H11-04E, https://web-material3.yokogawa.com/GS34M06H11-04E.pdf

[13] R. Schmidt, "Machine protection and interlock system for large research instruments", in *Proc. ICALEPCS'15*, Melbourne, Australia, Oct. 2015, pp. 537-542. doi:10.18429/JACoW-ICALEPCS2015-TUC3I01

[14] Yokogawa Hardware Manual, IM 34M06C11-01E, https://web-material3.yokogawa.com/IM34M06C11-01E.pdf

[15] AMD Spartan TM 6 FPGAs, https://www.amd.com/ja/products/adaptive-socs-and-fpgas/fpga/spartan-6.html

[16] TraceWin, https://www.dacm-logiciels.fr/tracewin

[17] T. Nishi *et al*., "Development of non-destructive beam envelope measurements using BPMs for low beta heavy ion beams in SRF cavities", in *Proc. HB'23*, Geneva, Switzerland, Oct. 2023, pp. 284-289. doi:10.18429/JACoW-HB2023-WEA4I1

[18] N. Sakamoto *et al.*, "Operation experience of the superconducting linac at RIKEN RIBF", in *Proc. SRF'21*, East Lansing, MI, USA, Jun.-Jul. 2021, pp. 315. doi:10.18429/JACoW-SRF2021-MOPFAV005

[19] A. Uchiyama *et al.*, "Control system of the SRILAC Project at RIBF", in *Proc. ICALEPCS'21*, Shanghai, China, Oct. 2021, pp. 147-152. doi:10.18429/JACoW-ICALEPCS2021-MOPV015

[20] K. Yamada *et al.*, "Operational experience for RIKEN superconducting linear accelerator", in *Proc. SRF'23*, Grand Rapids, MI, USA, Jun. 2023, paper MOIXA04, pp. 30-37. doi.org/10.18429/JACoW-SRF2023-MOIXA04

[21] N. Sakamoto *et al*., "Performance of the super-conducting RIKEN heavy-ion linac at the RIKEN Radioactive Isotope Beam Factory", presented at the LINAC'24, Chicago, IL, Aug. 2024, paper THPB053, this conference.