ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP28

# DESIGN OF BEAM POSITION MONITORING INTERLOCKING PROTECTION SYSTEM

R. X. Tian [1,3,†], J. X. Wu[1,2], Z. X. Li[1,3], K. W. Gu[1,2], J. J. Su[1,2], F. F. Ni[1], Y. Wei[1], H. M. Xie[1,2], L. L. Li[1], Y. Zhang[1,2], G. Y. Zhu[1,2]
[1]Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Lanzhou University, Lanzhou, China

*Abstract*

The machine protection system guarantees the safe operation of the HIAF in different operating modes and prevents damage to the online equipment in the event of a failure. Beam current data such as beam current position and phase is an important basis for analyzing and diagnosing accelerator faults. In this paper, the beam position and phase interlock monitoring system were designed by the authors. The system is based on circular buffer and AXI4 protocol to realize the transmission and storing of interlock data and locking of interlock status. Laboratory tests show that the system could save the beam position, beam phase, SUM signals and amplitude of sensed signal with interlocking before and after 8 ms and latch the interlock status of 25 channels. The system was deployed at the CAFe-LINAC (LINear ACcelerator) in March 2024 and completed online measurements.

## INTRODUCTION

The HIAF (High Intensity Heavy-ion Accelerator Facility) [1-4] is a new-generation heavy-ion accelerator research device with international leading level. It could provide the highest peak flow of low-energy heavy-ion beams in the world. In order to avoid radiation damage to on-line equipment in the event of a malfunction and to increase the availability of the entire installation. The Beam Position and Phase Interlock Protection System monitors physical quantities such as the horizontal position of the beam, the vertical position, the SUM signal (beam intensity), the beam intensity and the beam width of the pulsed beam. The system would send an interlocking signal to the MPS (Machine Protection System) [5-7] before a fault occurs or in the shortest possible time after a fault occurs. Simultaneously，the beam data would be saved in the local computer. The system provides a reference for beam commissioning, machine studies and beam structure analysis.

## SYSTEM DESIGN

The beam position and phase interlocking protection system have two main functions: one is the locking of the state during interlocking; the other is the saving of data during interlocking. The monitored state quantities in the system are shown in Table 1. Whether the ADC (Analog-to-Digital Converter) sampling value is saturated or not directly affects the accuracy of the position calculation algorithm, so the ADC conversion value is likewise monitored in the system. The beam current strength that SUM signal, is too large to cause equipment damage [8-9]. For example, the intercept probe Faraday with high current strength in the continuous beam current is very easy to be destroyed [10].

This affects the normal operation of the beam current diagnostic system. The monitoring of the phase is the monitoring of the beam energy. The deposition of energy could lead to rapid melting of material, damage to equipment and vacuum disruption. A shift in the beam position could also cause a pipe breakdown with destruction of the vacuum in a short period of time. The drastic reduction in beam transfer efficiency means that beam losses are significant, resulting in costly repairs and disruption of scientific progress for co-workers.

Table 1: Monitored State Quantities

| State Quantity | state | note |
|---|---|---|
| ADC raw value | saturation | 4 channels |
| beam intensity | high | H1 & H2 |
| beam intensity | low | H1 & H2 |
| phase | high | H1 & H2 |
| phase | low | H1 & H2 |
| horizontal position | high | H1 & H2 |
| horizontal position | low | H1 & H2 |
| vertical position | high | H1 & H2 |
| vertical position | low | H1 & H2 |
| transmission efficiency | high | H1 & H2 |
| transmission efficiency | low | H1 & H2 |

In the system, the interlocking status of the monitored state quantities is latched and transmitted to the ARM (Advanced RISC Machine) and then published to the user interface through the network. Figure 1 shows the block diagram of the entire system.

In addition to the locking of state quantities, the beam data before and after the occurrence of the interlock is also very important. The beam data could be analyzed to determine why failures occur and could also be used to predict failures. The authors used BRAM (Block Random Access Memory) as a buffer to store beam data in real time, including beam position, beam current intensity, beam phase and the sensed amplitude and phase of the four probes of the detector. The BRAM of the Zynq UltraScale+ MPSoC XCZU9EG is only 40.9 Mb, so the system could only store 8.192 ms of beam data at this stage.

†email: tianrx1028@impcas.ac.cn

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP28

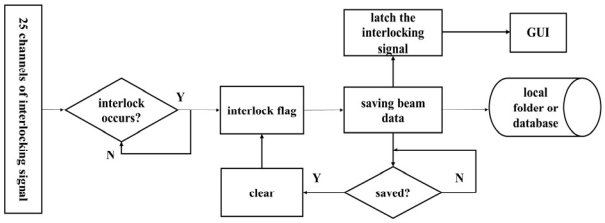


Figure 1: Block diagram of the system.

## *State Latching*

Whether or not interlocking of the monitored physical quantity occurs is done by the FPGA (Field Programmable Gate Array) algorithm [10]. Once the interlock occurs the FPGA side will generate a low-level signal of 3 to 10 μs as shown in Figure 2. The system realizes 3~10 μs state amount latch and transfer it to ARM side.

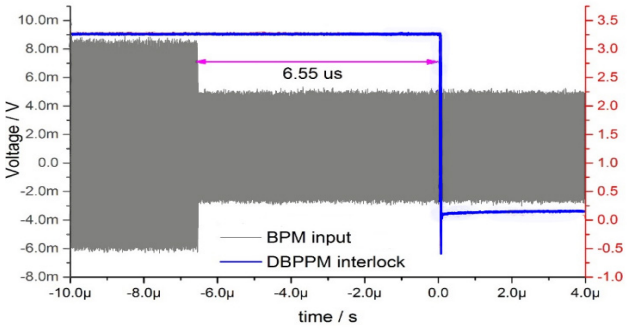


Figure 2: Interlocking signal.

Since all the interlocking states are semaphores, the lightweight on-chip protocol AXI-Lite is used in this system to transmit them to the ARM side. AXI-Lite is a simplified version of the AXI (Advanced eXtensible Interface) protocol with a transfer length of 1. It is mainly used for IP core initialization and for transferring small batches of data. AXI is a bus protocol that is the most important part of the AMBA (Advanced Microcontroller Bus Architecture) 3.0 protocol proposed by ARM, which is an on-chip bus geared toward high performance, high bandwidth, and low latency. It is an on-chip bus for high performance, high bandwidth, and low latency. The state locking algorithm is done in the FPGA and the timing diagram is shown in Figure 3.

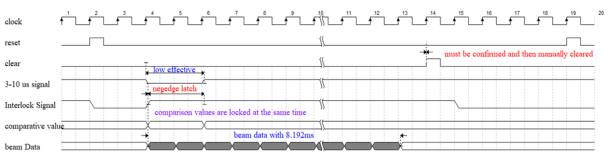


Figure 3: Timing diagram for status lock.

As shown in Figure 3, the clock is 200 MHz as the transmission clock of the AXI bus. The interlock signal reverts to a low level regardless of state when the system is reset. The falling edge of the 3-10 μs signal generated at the FPGA part is valid and latched into the register. The difference compared to the threshold is latched at the same time. The saving of beam data is initiated at the same time, which would be described in detail in the next section. The interlock state must be confirmed after the data is saved and then manually released.

The 25 monitored physical quantities adopted the same method to latch the interlocked state quantities. Finally, the state quantities and comparison values are transferred to the ARM side through a customized read-only AXI IP (Intelligent Property) core.

## *Saving of Beam Data*

Data such as beam position, beam phase and beam intensity before and after interlocking are very important, especially for the analysis of faults and early warning of faults. In the paper, the cyclic buffer method is used to realize the storage of data before and after interlocking. The schematic diagram of the working principle of the loop buffer is shown in Figure 4.

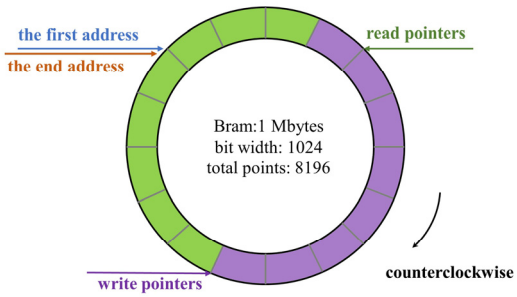


Figure 4: One read and one write pointer schematic to a circular buffer.

The circular buffer works as follows: (1) The loop buffer is always in the write state when no interlock occurs; (2) The address is locked and sent to the ARM side when the interlock occurs; (3) The write state continues until the write pointer is offset 4096 from the locked address; (4) The ARM side starts reading data and the read pointer should be at the point where the lock address is offset 4096 forward; (5) Clear the interlock flag and enter the cyclic write state again. The flowcharts for the write and read states of the cyclic buffer are shown in Figure 5 and Figure 6 respectively.

The beam position and phase monitoring interlock system is an expansion and upgrade of the embedded system. That is equivalent to an interrupt program throughout the BPM's embedded system. When an interlock (interrupt) occurs, the system enters the interrupt handling program. The system would start to save beam data. At the end of the interrupt program, the duty officer must manually clear the interlock flag and enters the normal data output and post-processing program.

# MEASUREMENT RESULT

## *Test Results in Laboratory*

The test platform was successfully built under laboratory conditions to obtain the test results. At the same time, the burst mode of the signal source is used to generate a pulse

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP28



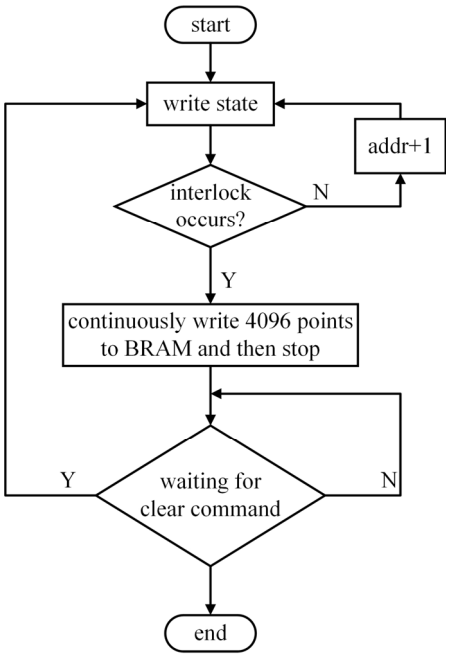


Figure 5: Flowchart of the write state of a cyclic buffer.

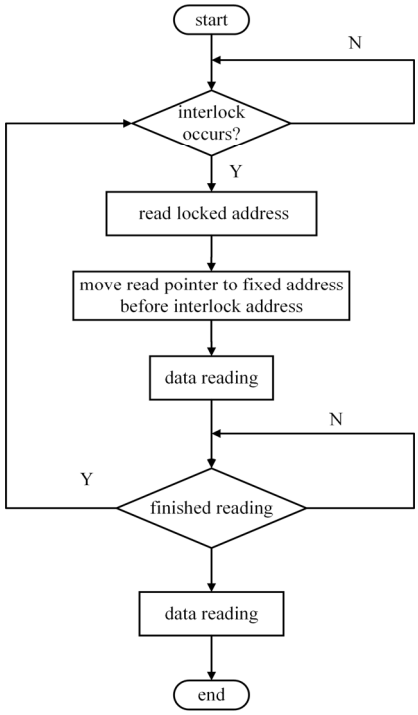


Figure 6: Flowchart of the reading state of a cyclic buffer.

wave to cause a position interlock. The latching function of the interlock state and the saving function of the beam current data could then be tested under laboratory conditions. The system is online more than half the time running in trigger mode. A simulated trigger mode is needed under the laboratory to test the functionality of this system. RIGOL DG4162 Function and Arbitrary Waveform Generator has 2 channels. Each channel has a synchronized output. The functionality of the system could be tested in trigger mode. This allows testing of the state interlocking of the triggered modes and the saving of the interlocked beam data under laboratory conditions. The test results of the interlock data are shown in Figure 7 and Figure 8. The test curves show that the system can accurately store beam current data to a local folder.

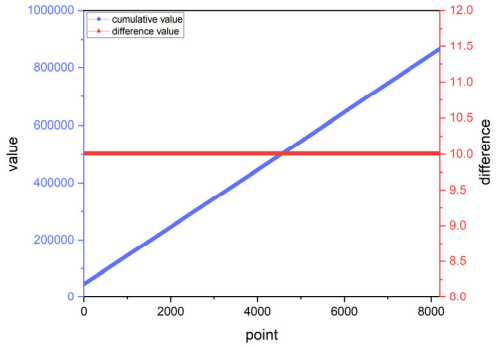


Figure 7: Test results with accumulators.

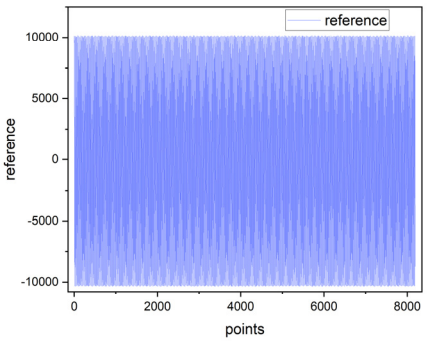


Figure 8: Reference signal waveform after trigger mode chaining.

## *Online Test Results*

Functional testing of online interlock status was completed in March 2023 with SS-BPM at the linear accelerator device CAFe in Lanzhou. CAFe operates in continuous mode with particles of 40Ar12+ and an energy of 224.2 MeV Monitoring of beam current strength, horizontal and vertical position of the first harmonic in trigger mode. When the BPM system generates an interlock, the interlock signal is transmitted to the machine protection system and cuts off the beam flow to protect the equipment. Figure 9 shows the SUM signal exceeding the threshold at 17:34:34. The status latch is shown accurately on the Figure 10 user interface. In addition, this interlock signal is transmitted in real time to the machine protection system, as can be seen from the interface at time 17:34:35.

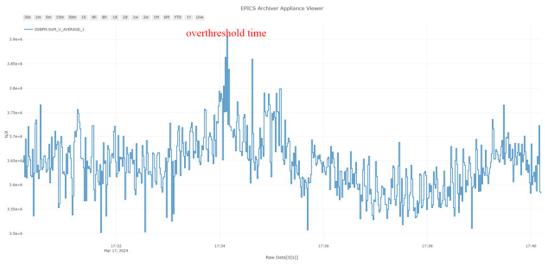


Figure 9: Waveform curve of the SUM signal of the monitored quantity SS-BPM (including interlocking moments).

ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-TUP28

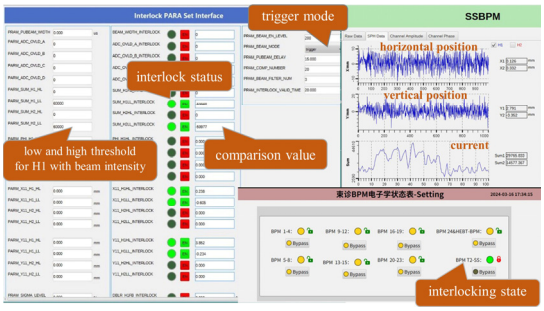


Figure 10: Online testing interface.

## CONCLUSION

In this paper, the authors introduce a present a method for locking states and an algorithm for saving beam data. The method could realize the state locking of 25 monitored quantities and the saving of beam data up to 8.192 ms. That also could meet the preservation of injector single pulse waveform data in the HIAF injection mode. The system was verified online in March 2024 through the state locking function, realizing real-time interlocking and equipment protection of beam position and beam intensity. The saving of interlock data was similarly tested in the laboratory, including sine wave and cumulative number. Due to the limitation of BRAM resources in hardware platform, this method could only store beam data for about 8 ms. The next work is to develop the DDR based data storage function, which is the system could store beam current data for a longer period like 2.5 seconds of data.

## ACKNOWLEDGEMENTS

The authors would like to give special thanks to the staff of the Beam Feedback Department, Institute of Modern Physics, Chinese Academy of Science, for their kind help in the beam commissioning and electronics tests.

## REFERENCES

[1] J. C. Yang *et al.*, "High Intensity heavy ion Accelerator Facility (HIAF) in China", *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 317, p. 263–265, 2013. doi:10.1016/j.nimb.2013.08.046

[2] J. C. Yang, L. T. Sun, and Y. J. Yuan, "Status of the HIAF Accelerator Facility in China", in *Proc. Cyclotrons'22*, Beijing, China, Dec. 2022, paper MOAI01, pp. 1-5. doi:10.18429/JACoW-CYCLOTRONS2022-MOAI01

[3] F. C. Cai *et al.*, "Beam loading effects and microwave instability in the booster ring of a high intensity heavy-ion accelerator facility", *Phys. Rev. Accel. Beams*, vol.23, p. 064402, 2020. doi:10.1103/PhysRevAccelBeams.23.064402

[4] B. Wu *et al.*, "The design of the Spectrometer Ring at the HIAF", *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. 881, p. 27–35, 2018. doi: org/10.1016/j.nima.2017.08.017

[5] A. Nordt, A. Apollonio, and R. Schmidt, "Overview on the Design of the Machine Protection System for ESS", in *Proc. IPAC'14*, Dresden, Germany, Jun. 2014, pp. 472-475. doi:10.18429/JACoW-IPAC2014-MOPME045

[6] K. H *et al.*, "Interlock and protection systems for superconducting accelerators: Machine protection system for LHC", in *Proceedings from WAO'01*, Villars sur Ollon, Switzerland, 28 January - 2 February 2001:170-178, CERN. http://doc.cern.ch//archive/cern-rep/2001/2001-002/p140.pdf

[7] R. Schmidt *et al.*, "Protection of the CERN Large Hadron Collider", *New J. Phys.*, vol. 8, p. 31, 2006. doi:10.1088/1367-2630/8/11/290

[8] Z. Y. Li *et al.*, "FRIB Fast Machine Protection System: Engineering for Distributed Fault Monitoring System and Light Speed Response", in *Proc. of LINAC2016*, East Lansing, MI, USA, p. 25-30, 2016. doi:10.18429/JACoW-LINAC2016-THPLR046

[9] Y. Wei *et al.*, "Development of a non-intercepting weak beam current measurement electronics for Heavy Ion Accelerator Facility in Lanzhou", *Rev. Sci. Instrum.*, vol. 95, p. 064701, 2024. doi:10.1063/5.0202920

[10] F. F. Ni *et al.*, "A new digital beam position and phase measurement implementation based on a field programmable gate array for the high intensity heavy-ion accelerator iLinac", *Rev. Sci. Instrum.*, vol. 93, p. 063301, 2022. doi:10.1063/5.0089407