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Production testing of the COLUTA ADC ASIC for the ATLAS HL-LHC Liquid Argon calorimeter readout

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Abstract: The COLUTA (COLumbia-University of Texas at Austin) ASIC is an 8-channel, 15-bit, 40 million samples per second (MSPS), analog-to-digital (ADC) converter designed for the high-luminosity LHC (HL-LHC) upgrade of the Liquid Argon (LAr) calorimeter readout electronics. The production version of the ADC meets and exceeds the specifications for the analog performance and the HL-LHC radiation tolerance. Radiation tolerance test procedure and the results of the irradiation test on pre-production lot chips will be discussed. The production testing will be performed by a custom-designed robotic test setup which will test 80,000 chips required for the upgrade. The chip performance results, and the chip quality information are stored in a local and centralized database. Results from robotic chip-testing of the production lots will be described, along with the yields of the chips which meet the specifications for the upgrade.

Keywords: Analogue electronic circuits; Calorimeters; Front-end electronics for detector readout; Radiation-hard electronics

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1 Introduction

The LAr calorimeter at the ATLAS experiment [1] has an extensive hardware and software upgrade program to cope with the high instantaneous luminosity and the large number of proton-proton interactions per bunch crossing expected at the HL-LHC. During HL-LHC, the expected instantaneous luminosity will be 5–7 times the nominal LHC luminosity and the average number of interactions per bunch crossing will be 3–4 times the nominal LHC interactions [2]. The calorimeter will upgrade its on-detector and off-detector electronics to meet the ATLAS physics goals in the demanding conditions of the HL-LHC. The Phase-I trigger electronics upgrade [3] will enhance the physics reach of the experiment during the Run-3 data-taking period (years 2022–2025). The Phase-II trigger electronics upgrade will provide a fine-granularity readout while maintaining the trigger requirements during HL-LHC operation. A detailed block diagram illustrating the architecture of the upgraded readout electronics is shown in figure 1. The Phase-I upgrade, shown in the bottom part of the figure, includes the LTDB and LDPB boards. The Phase-II upgrade, shown in the top part of the figure, upgrades the full readout chain as well as the calibration system of the on-detector electronics.

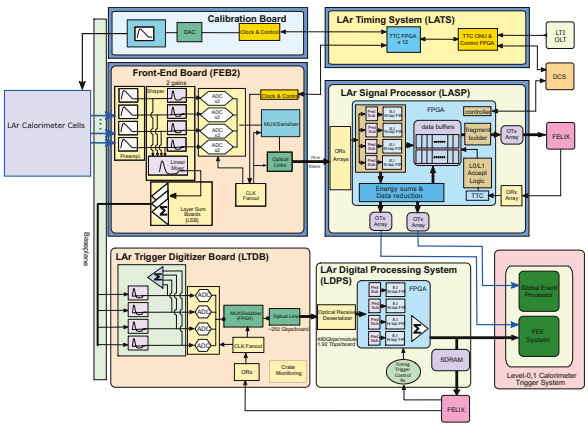

Figure 1. Schematic of the on- and off-detector electronics for the HL-LHC.

The Phase-II on-detector electronics will be installed on a new front-end board, dubbed "Front-End Board 2 (FEB2)", that will replace the current FEB boards. Similar to the current FEB, each FEB2 will handle 128 calorimeter channels, with 1524 FEB2 boards required to read out the entire calorimeter. Custom-designed electronics on the FEB2 will amplify, shape, and digitize the analog calorimeter signals over two overlapping gain scales and a dynamic range of 16 bits at the rate of 40 MHz. The digitized signals will be sent via optical links to the off-detector electronics.

2 COLUTA ADC

The COLUTA ADC is a custom, eight-channel, 15-bit ADC fabricated in 65 nm CMOS, operating at a sampling frequency of 40 MHz. Each channel features Multiplying DAC (MDAC) and Successive Approximation ADC (SAR) quantization core followed by the Digital Data Processing Unit (DDPU) that determines and applies the MDAC and SAR calibration constants and formats the output data [4]. The digitized data are transmitted serially at a nominal rate of 640 Mbps whose electrical interface is compatible with that of the lpGBT [5].

The ADC is expected to continue to perform reliably throughout the operation of the HL-LHC. For the expected total integrated luminosity of 4000 fb^{-1}, the LAr electronics are required to be radiation tolerant to Total Integrated Dose (TID), Non-Ionizing Energy Loss (NIEL), and Single Event Effects (SEE) listed in table 1.

Table 1. Radiation hardness requirements for on-detector electronics.

ASIC	TID [kGy]	NIEL [n_{eq}/cm^2]	SEE [$h_{>20\,MeV}/cm^2$]
ADC	1.4	4.1×10^{13}	1.0×10^{13}

The COLUTA ADC radiation hardness measurements were performed at a proton-beam facility at the Massachusetts General Hospital. The ADC exceeds the radiation tolerance requirements and is operational well beyond the HL-LHC required dose. Further details about the radiation hardness measurements are explained in section 3.

3 Radiation hardness measurements

Radiation hardness measurements of the COLUTA ADC were performed at the Francis H. Burr Proton Therapy Center at the Massachusetts General Hospital (MGH). The ADC is irradiated with 225 MeV proton beam with TID up to or greater than the HL-LHC required dosage. The goals of the radiation testing are to test the radiation tolerance of the ADC and measure the cross section of single event upsets (SEUs). Five chips selected randomly from the pre-production lot were tested at MGH on 28th and 29th October 2023. As shown in figure 2, the chip was placed at one end of the ~ 50 cm long board, while the other active elements, including the FPGA, were placed at the other end. During irradiation, the radiation-sensitive elements were protected with lead shielding.

To monitor the general health of the chip during irradiation the current draw and the temperature readings of the chip were measured *in situ*. During irradiation the ADC was monitored for configuration corruption by reading back the ADC configuration bits every five minutes. Upon a failed read back the corrupted configuration was recorded and the ADC was reconfigured. For all of the five boards under test, a total of 3 triple-redundant configuration bits were corrupted, corresponding to a cross section of $(2.27 \pm 1.31) \times 10^{-18}\,cm^2$/bit.

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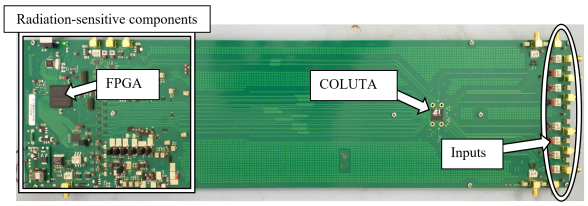

Figure 2. Elongated board designed for radiation testing. The radiation-sensitive components such as the FPGA are located on one corner and the chip-under-test is located on the opposite end.

The chip also includes a counter to measure the frequency of upsets of the individual D flip-flops (DFFs); three DFFs compose one triple-redundant configuration bit. The counter (SCSEU) records instances where one of the three DFF is not in agreement with the other two. The integrated SCSEU counts are shown in figure 3. The cross section of the DFF corruption rate (averaged over all irradiated boards) is $(4.20 \pm 0.03) \times 10^{-10}\,\mathrm{cm}^2$.

To measure the SEU cross section, the chips were monitored for erroneous ADC codes (e.g. due to a flip of a SAR bit) while the chip was being irradiated. 2^{22} (4.2M) digitized samples from each channel were recorded and the output was histogrammed with the FPGA. Multiple histograms for each channel were recorded during the testing to collect statistically significant sample of candidate histograms with and without SEUs. A single-event upset would appear as a large deviation from the expected value. Specifically, an SEU is identified as a single ADC sample that is at least two counts away (on either side) from any other sample in the distribution. The SEU cross section (averaged over all irradiated boards) is $(1.37 \pm 0.07) \times 10^{-10}\,\mathrm{cm}^2$. The rate of SEUs is linearly dependent of the average proton rate, as shown in figure 3.

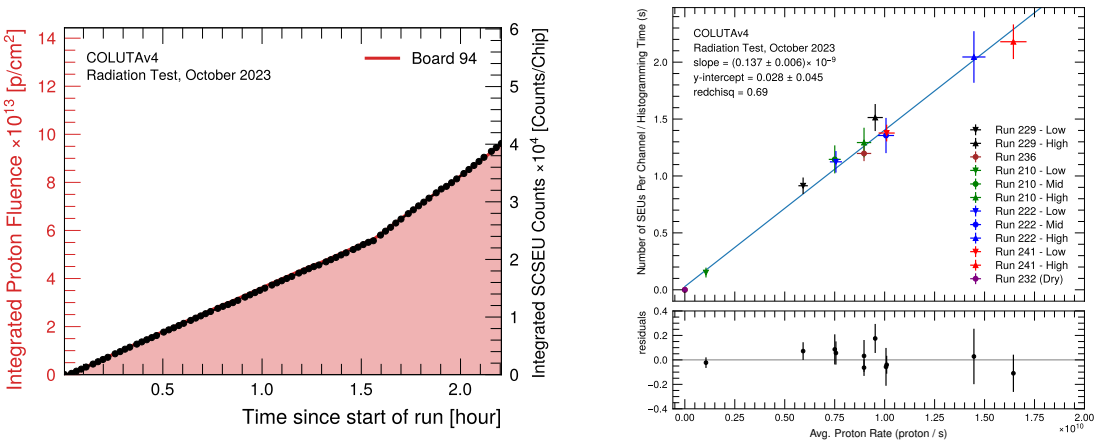

Figure 3. Left: TID and integrated SCSEU counter as a function of the run time. Right: rate of SEUs as a function of the average proton rate.

4 ADC Quality Assurance/Quality Control (QA/QC) testing

The QA/QC testing will be performed on about 80,000 COLUTA chips to be installed on 1524 FEB2 boards. The testing is performed with a custom-designed, automated robotic setup shown in figure 4. A clean room houses a Selective Compliance Articulated Robot Arm (SCARA) surrounded by eight

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JEDEC trays and one custom-designed QA/QC testboard. A photointerrupter sensor, vacuum cup gripper, and a camera are attached on the robot arm. Each JEDEC tray consists of 189 wells which house either an untested or a tested and graded chip. For QA/QC testing, the robot test stand is loaded with four filled JEDEC trays housing untested chips and four empty JEDEC trays to sort the tested and graded chips. Each chip-under-test is picked from the well using the vacuum gripper, moved to a staging area where the QR code printed on the chip is decoded using the camera on the robot arm. Once the QR code is decoded, the chip is moved from the staging area and socketed on the QA/QC testboard. The photointerrupter sensor performs fault checking to verify that the chip is socketed properly. After a successful socketing the chip is powered and a series of measurements are performed to qualify the chip. The result of each test is used to compute the performance or "grade" of the chip and the chip is unsocketed and sorted into the respective JEDEC tray based on the chip grade. The aforementioned testing procedure is repeated until there are no chips left to test.

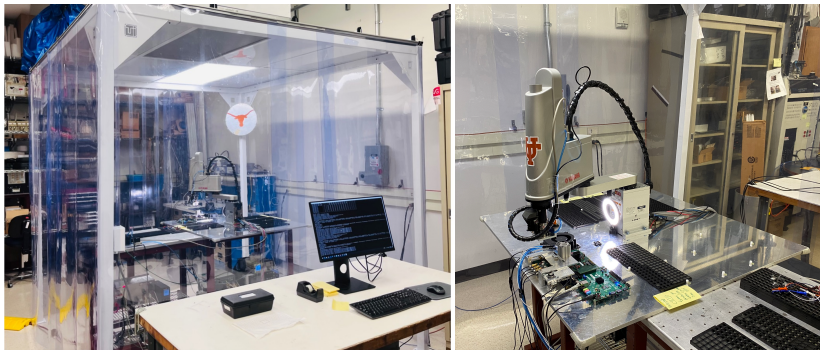

Figure 4. Clean room and the robot test stand to perform automated QA/QC testing.

The COLUTA QA/QC testing is performed on a custom-designed testboard which has eight identical channels to uniformly measure the analog performance of each COLUTA channel. 1000 pre-production chips were tested and qualified using the first version of the QA/QC testboard, shown in figure 5, with an observed yield of >90% during optimal testing conditions. Out of the 1000 tested chips, 500 chips are installed on prototype FEB2 boards. The second version of the QA/QC testboard, as shown in figure 5, improves on the design of the first version with better uniformity of the analog inputs.

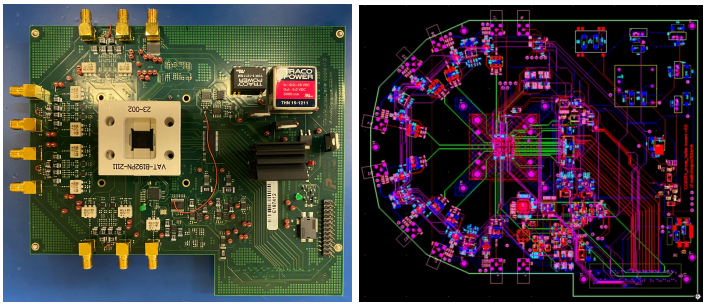

Figure 5. Left: photograph of the first version of the QA/QC testboard. Right: schematic of the second version of the QA/QC testboard.

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Two sets of QA/QC tests are performed on each chip: “Dead-or-Alive” and “Performance” tests. The dead-or-alive tests measure the chip health and the ability to configure and readout all COLUTA channels. The test is a quick evaluation of the chip performance to discard dead or non-functional chips. So far, no dead chips have been observed in the 1000 pre-production chips. The performance test is a detailed series of analog measurements to evaluate chip performance and assign chip grade. In the performance test the chip health, chip power, and analog performance of the eight channels are measured to determine the chip quality and assign a chip grade. During the performance test each channel is calibrated and the calibrated constants are evaluated against the ideal constants. The analog performance for each channel is determined by measuring the INL/DNL, the mean and width of the baseline, and the ENOB from digitizing a sine wave at full-scale input.

The tested chip is graded based on the analog performance of each of the eight channels. The channel with the lowest analog performance is used to assign the final chip grade, ensuring the selection of the best analog performance chips for the FEB2. The tested chips are assigned one of three grades: “meets specs.”, “does not meet specs.”, “not functional”. The chips graded “meets specs.” will be installed on the prototype and production FEB2 boards.

Under optimal testing conditions, a yield of >90% is observed from the 1000 pre-production tested chips. Figure 6 shows the evolution of cumulative chip grade and the evolution of the chip yield during the month of chip testing in August 2023.

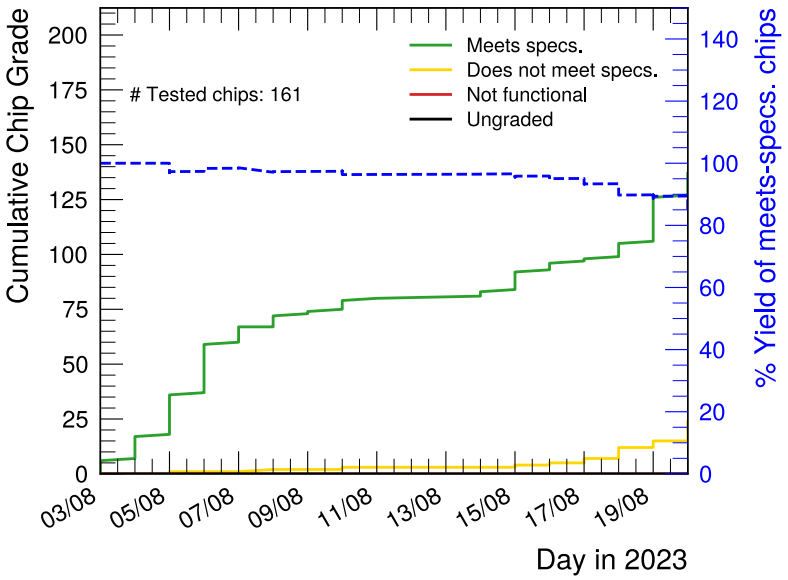

Figure 6. Cumulative chip grade and yield of tested chips as a function of test day in 2023.

5 Summary and conclusion

The COLUTA is a custom-designed ADC for the HL-LHC readout electronics for the ATLAS LAr calorimeter. The production version of the ADC meets and exceeds specifications for the analog performance and the HL-LHC radiation tolerance requirements. Five randomly selected chips from the pre-production lot were irradiated beyond the required HL-LHC dosage. Each chip was fully functional

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after irradiation and no latch-ups or single-event functional interrupts were observed. The production testing of 80,000 ADC chips will be performed using an automated, robotic setup. A custom-designed QA/QC testboard with identical analog inputs will measure uniformly the performance of each ADC channel. The chips will be tested on a set of measurements and the chip quality will be evaluated using the results of the chip performance tests. Preliminary testing of 1000 pre-production chips provides a >90% yield of meets specifications chips under optimal testing conditions.

Acknowledgments

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