ISBN: 978-3-95450-249-3 ISSN: 2673-5350 doi: 10.18429/JACoW-IBIC2024-WEP55

# HIGH-SPEED ADC AND HIGH-SPEED DAC MicroTCA.4 AMC-RTM PAIR FOR A MULTIPLE OF DIAGNOSTICS AND FEEDBACK IMPLEMENTATIONS

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*Abstract*

We present the MicroTCA.4 electronics modules, an AMC-RTM pair, for direct sampling of wideband signals with high-speed ADCs, versatile digital signal processing with the AMD RFSoC, and driving of wideband signals with high-speed DACs. The Zynq UltraScale+ RFSoC Gen 3 at the core of this system was primarily designed for telecommunication and especially software-defined radio (SDR) but also found other applications in various scientific experiments, which we will discuss in this paper. This component not only allows for the implementation of multiple diagnostics but also enables the creation of wideband feedback systems, thanks to the driving capabilities of its DACs.

This work presents a hardware architecture and shows how the modules can be set up and configured. The performance and functionalities are discussed, with particular attention paid to system noise, which is essential for high-precision scientific research.

## INTRODUCTION

Modern ADC and DAC technology development allow high-frequency sampling clocks and the measurement/generation of wideband low-noise signals. Due to improved signal processing capabilities, more and more applications are simplifying their hardware by getting rid of analog down converters, shifting the measured signal bandwidth to baseband, and using the direct sampling technique. In this paper, we present two MicroTCA.4 modules, i.e. DAMC-DS5014DR and DRTM-MBFB-FE (see Fig. 1), referred to as later the AMC and the RTM. They are interconnected over Zone 3 Class RF1.1. The AMC can also be used with any other RTM (designed according to Class RF1.1) needed for special analog processing, which is not covered by any assembly version DRTM-MBFB-FE.

## AMC MODULE

### *Zynq UltraScale+ RFSoC Gen 3*

The core component for the AMC module is the RFSoC. The module offers low-noise ADCs with a high-sampling rate of 5 GS/s, with a wide input bandwidth of 6 GHz, and low-noise DACs with a high sampling rate of 10 GS/s, which are attractive components for a multiple of scientific applications. Additionally, the RFSoC includes plenty of digital resources and two different classes of ARM processors for versatile processing implementations. The detailed description of the RFSoC IC can be found in [1].

### *Analog Front-End and Back-End*

In the AMC, various assembly options are designed to use the entire ADC/DAC bandwidth, including DC or AC coupling. The DC coupling requires an active front-end component based on a fully differential amplifier, which produces significant harmonics, especially at frequencies more than about 2.5 GHz, and other nonlinear products of input signals. If the measurement of a DC component is not needed and the input signal is >10 MHz, it is best to use the passive front-end based on an RF balun. The measured signals can be provided by the front panel or the Zone 3 connector. This is detailed further in the "Class RF1.1 Zone 3" section.

### *Communication Interfaces*

Data can be transferred over the standardized AMC connector (see [2]) or the front panel connectors. Ports 4-15 of the AMC connector are connected to three of the FPGA's quad GTY transceivers. One quad GTY is used for PCIe 4.0 x4 (64 GT/s) that provides communication with all other AMC modules over the MCH root complex. The rest of the GTYs are connected to other AMC modules over low-latency point-to-point links (depending on the AMC backplane). Optionally, two quad GTYs can be used for PCIe 4.0 x8, but the number of point-to-point links is reduced. Ports 17-20 are MLVDS lines dedicated to timing and trigger distribution, which are critical for time-stamping data in scientific research.

The fourth quad GTY is connected to the QSFP28 optical transceiver and is accessible from the front panel. It can be used for applications such as PCIe 4.0 x4 or 100 GbE communication. USB-C connector on the front panel with USB 3.2 Gen 1 and DisplayPort.

### *Memory*

The AMC module includes a few volatile and non-volatile memory units connected to the PL and PS banks of the RFSoC. The available non-volatile memory for fast data processing are a PS DDR4 (16 GB, 64 bit x 2400 MT/s) and two PL DDR4 (16 GB, 64 bit x 2666 MT/s each). The non-volatile memory storing the firmware, configuration data, and calibration parameters are QSPI Flash, micro SD card, and 16 GB eMMC.

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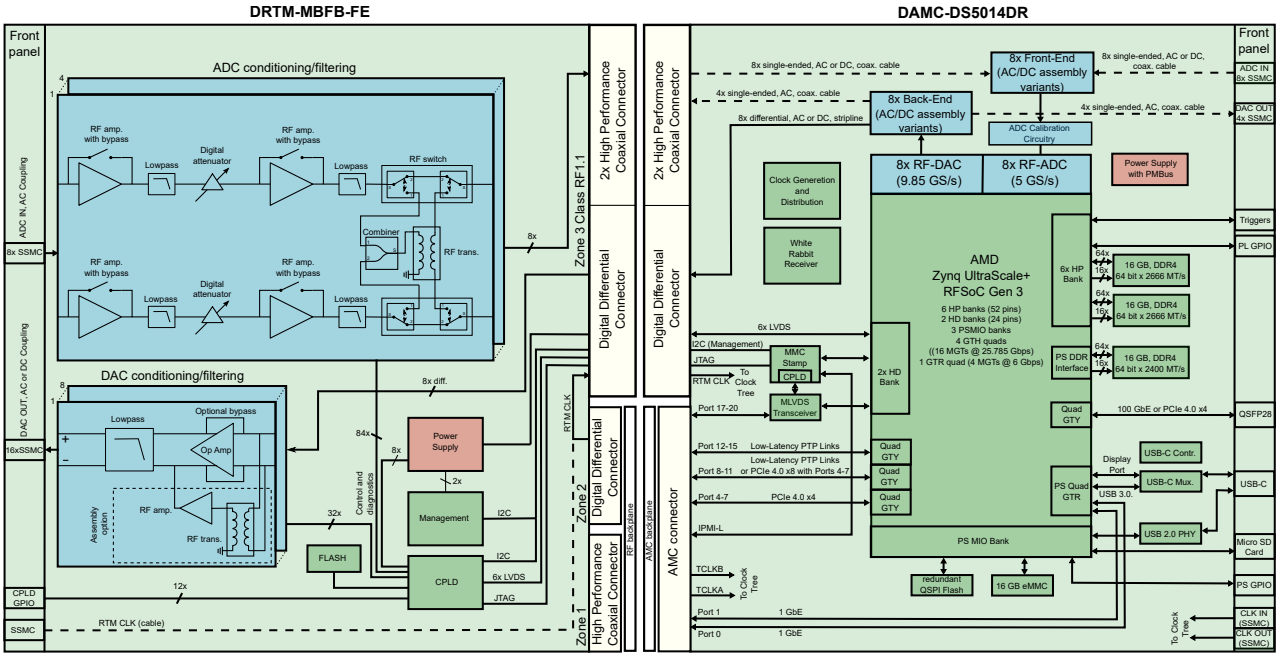


Figure 1: Simplified block diagram of the DRTM-MBFB-FE and DAMC-DS5014DR pair.

### *Clock Tree*

The AMC module requires a robust clock tree to ensure data sampling, processing, and transmission ICs work correctly. The clock tree is generally divided into two sections, called the digital and the analog clocks. The analog clock section generates a high-performance, low-jitter clock for sampling ADCs and DACs. The digital clock section provides clocks to all other components.

An onboard temperature-compensated crystal oscillator (TCXO) on the AMC is designed to serve as a reference clock for the AMC in standalone operations. However, in most cases, the external reference clock is used, since the AMC needs to be synchronized with an experimental facility. The external reference clock can be provided from different sources, such as the front panel, AMC backplane (TCLK A/B), or Zone 3 Connector (RTM Clock). All onboard oscillators are phase-locked to the reference clock. The PLLs can have multiple configurations that cover most of the applications' requirements.

High-precision phase and timing measurements, such as those in bunch arrival time detectors, are susceptible to sampling clock jitter. This motivates the option to provide the ADCs with a sampling clock directly from an ultra-low-noise external RF source, such as a high-performance signal generator. This solution reduces the additive $1/f$ noise of the detector. However, the noise floor remains unchanged since it is dominated by internal ADC front-ends. The same situation concerns DACs while generating low phase noise signals. Amplitude measurements are not sensitive to clock jitter. Therefore, external clock sources do not improve the amplitude detector SNR.

### *ADC Calibration*

Each ADC in the RFSoC is built on multiple sub-ADCs in an interleaving architecture. The nature of the interleaving process requires an intricate calibration algorithm to obtain the best dynamic range performance from the ADC. Reference [1] details the method of calibrating the ADC and its impact on ADC performance. The AMC includes special circuitry that allows automatic ADC calibration without the need for any external electronics. This simplifies the usage of the AMC, especially when access to the measurement systems is difficult or impossible.

## RTM MODULE

The RTM is a universal RF analog circuit for the conditioning and filtering signals provided to the ADCs and for the conditioning and filtering of signals from DACs.

The eight ADC channels (single-ended input, single-ended output, AC coupling) have the bandwidth from 10 MHz up to 6 GHz (for different assembly versions), and the net gain from −25 dB up to 20 dB adjustable in steps of 0.25 dB. It is possible to use special features like combining two channels, e.g. for a pilot tone calibration or splitting one channel into two ADCs for channel parallelization, which can be used for noise reduction or redundancy purposes. These special features can be automatically activated by changing the settings of the RF switches.

The eight DAC channels (differential input, differential output, DC coupling) have a bandwidth from DC up to about 2.5 GHz. However, their performance, i.e. the input reflection and channel-to-channel isolation, degrades with frequency due to the Zone 3 differential connector limitations. If the isolation better than 60 dB is required, then the signals

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| | | Digital Clock IO | Digital Fixed IO | Digital Clock Input | Digital User IO | | Differential DACs | | | MTCA.4 Management | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| J30 | | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| - | F | AMC-CLK- | OUT1-/D8- | RF-CLK3- | DAC7- | D5- | DAC4- | D2- | DAC1- | TMS | TDO |
| + | e | AMC-CLK+ | OUT1+/D8+ | RF-CLK3+ | DAC7+ | D5+ | DAC4+ | D2+ | DAC1+ | TDI | TCK |
| - | d | RF-CLK2- | OUT0-/D7- | RF-CLK1- | D6- | DAC5- | D3- | DAC2- | D0-CC- | SCL | SDA |
| + | c | RF-CLK2+ | OUT0+/D7+ | RF-CLK1+ | D6+ | DAC5+ | D3+ | DAC2+ | D0-CC+ | MP | PS# |
| - | b | RF-CLK0- | AMC-TCLK- | RTM-CLK- | DAC6- | D4- | DAC3- | D1- | DAC0- | PWRB2 | PWRB1 |
| + | a | RF-CLK0+ | AMC-TCLK+ | RTM-CLK+ | DAC6+ | D4+ | DAC3+ | D1+ | DAC0+ | PWRA2 | PWRA1 |

| | | Single Ended Analog Signals | | |
|---|---|---|---|---|
| J31 | | 3 | 2 | 1 |
| | B | ADC-IN7 | DAC-OUT1 | DAC-OUT3 |
| | A | ADC-IN6 | DAC-OUT0 | DAC-OUT2 |
| J32 | | 3 | 2 | 1 |
| | B | ADC-IN1 | ADC-IN3 | ADC-IN5 |
| | A | ADC-IN0 | ADC-IN2 | ADC-IN4 |

Figure 2: Zone 3 Class RF1.1 pin assignment J30, J31 and J32 connector, AMC side view.

generated by DACs should not be faster than 1 GHz. The "DC" DAC channel outputs can also be used as single-ended outputs with limited performance regarding common-mode distortions.

The DAC channels can also be configured (assembly option) as single-ended, AC coupled - they implement RF baluns and low-noise RF amplifiers instead of fully differential amplifiers.

## CLASS RF1.1 ZONE 3

The AMC and RTM are interconnected via coaxial and differential connectors specified in the Zone 3 Class RF1.1 (see Fig. 2), which is being published soon. This Class is a modification of the Class RF1.0 (published in [3]), where the gigabit transceiver pins are substituted with DAC outputs and, additionally, they are "scattered" with the digital IO pins for better DAC-to-DAC isolation. The coaxial connectors J31 and J32 provide twelve high-performance and high-isolation interconnections that cover the maximum bandwidth of 6 GHz [4].

## FIRMWARE

To lower the barrier for developers using the DAMC-DS5014DR board, DESY provides an open-source FPGA example firmware code. The primary objective of this firmware is to encapsulate all board-related logic (e.g. PCIe, MPSoC configuration, DDR, etc.) within a ready-made Board Support Package (BSP), allowing users to concentrate on a superficial application layer where they can integrate their algorithms and begin using high-speed ADC/DAC data. The BSP is configurable to accommodate various application use cases. Additionally, an embedded Linux image can be created using Yocto, supported by this example code. The entire codebase is constructed using DESY's open-source FPGA framework, FWK [5], which is actively maintained by the MSK group at DESY.

## APPLICATIONS

The RFSoC was initially designed for versatile telecommunication and SDR applications. Additionally, it is extensively utilized in scientific research. The detectors, including wideband ADCs, measure signal phase, amplitude, and frequency, which carry information about some physical properties, like changes in a cavity field, motion of a target, bunch position, bunch phase, bunch charge, and others. Moreover, combining the wideband DACs, FPGA, and the processing unit can be used as actuators in feedback loops to control the experiment property.

Some applications that will use or plan to use the DAMC-DS5014DR (with or without DRTM-MBFB-FE) are briefly mentioned below:

- **Transverse Multi-Bunch Feedback (PETRA IV)** Suppression of the fast (on the ns-scale) bunch-by-bunch transverse position variations with the high-resolution of 1 µm [6].
- **Phasemeter (LISA)** A high signal bandwidth (>2 GHz) and high tracking bandwidth (>2 MHz) multi-channel phasemeter for tracking changing laser frequencies for the laser interferometry [7].
- **Kicker Pulser (EuXFEL, FLASH, PETRA IV)** Diagnostics of short rise time pulses from the kicker pulser.
- **X-Ray Gas Monitors XGMs (EuXFEL, FLASH)** Diagnostics of bunch-resolved photon energy [8].
- **BAC (REGAE)** Beam Arrival Time Cavity (BAC) for the precise arrival time measurements for the very low charge operation below 1 pC, [9].
- **LLRF (MYRRHA)** Direct sampling of the cavity coupled-out RF signals for the field amplitude and phase stabilization.
- **Timing System (PETRA IV)** Correction of the timing reference signal with respect to the bunch arrival time.

## SELECTED PERFORMANCE RESULTS

The core component of the AMC, i.e. RFSoC Gen 3, has hundreds of different settings and configurations that can be used in different applications. Hence, more than a comprehensive performance evaluation is needed, and

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special tests should be done on each case. The critical parameter for most of the applications is residual phase noise and additive amplitude noise of ADCs, which was evaluated for 1 GHz sine wave sampled with 5 GS/s clock (see Fig. 3 and Fig. 4).

The DACs have following parameters: white phase noise PSD <−162 dBc/Hz, residual timing jitter about 26 fs RMS (from 100 Hz to 100 MHz), white amplitude noise PSD < −167 dBc/Hz, additive amplitude noise about 0.021 % (from 10 Hz to 40 MHz), which was evaluated at 1.5 GHz.

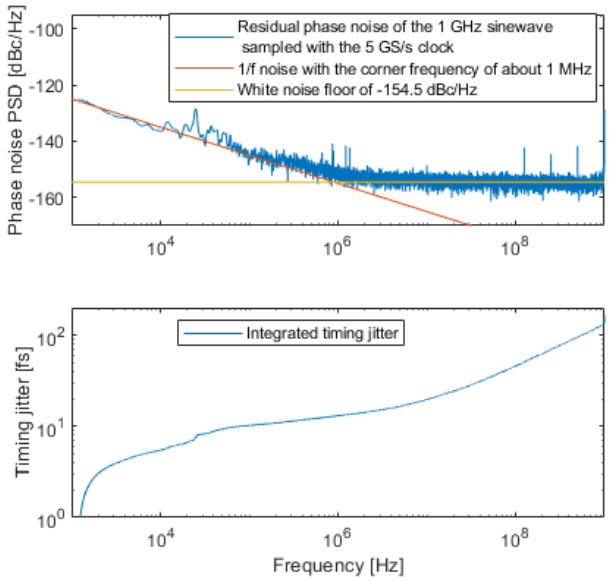


Figure 3: Residual phase noise PSD and timing jitter of the ADCs measured with the 1 GHz sine wave sampled with the 5 GS/s clock.

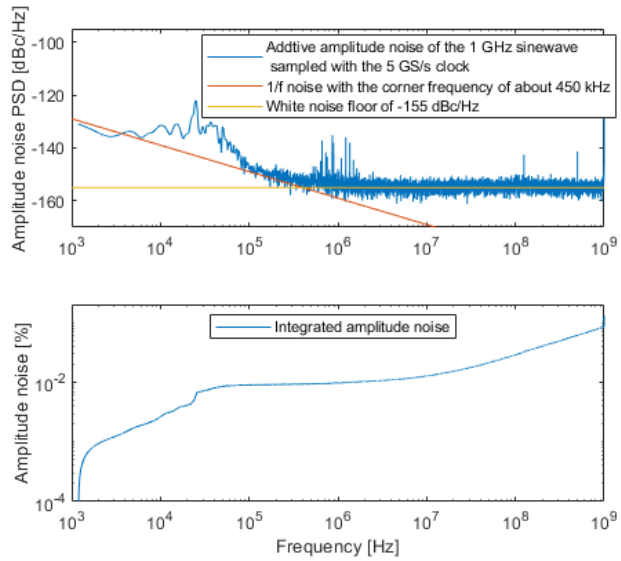


Figure 4: Additive amplitude noise PSD and integrated amplitude noise of the ADCs measured with the 1 GHz sine wave sampled with the 5 GS/s clock.

A spur-free power supply composed of 3-stage low-noise voltage converters is crucial to achieve the above results.

## CONCLUSION

We have designed two MicroTCA.4 modules, i.e. DAMC-DS5014DR and DRTM-MBFB-FE, as universal devices that can be used in diverse scientific applications. Because of the unification of the RF analog converters and digital resources in one chip and the developed firmware (board support package), they feature high performance, flexibility, and ease of use.

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