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RECEIVED: November 15, 2016

ACCEPTED: January 11, 2017

PUBLISHED: February 14, 2017

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS,
26–30 SEPTEMBER 2016,
KARLSRUHE INSTITUTE OF TECHNOLOGY (KIT), KARLSRUHE, GERMANY

Development of a rest gas ionisation profile monitor for the CERN Proton Synchrotron based on a Timepix3 pixel detector

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ABSTRACT: A fast non-destructive transverse profile monitor, named PS Beam Gas Ionization monitor (PS- BGI), is under development at CERN for the Proton Synchrotron (PS). This monitor infers the beam profile from the transverse distribution of electrons created by the ionisation of rest gas molecules by the high energy beam particles. The distribution is measured by accelerating the electrons onto an imaging detector based on Timepix3 (TPX3). This detector consists of hybrid pixel detector assemblies mounted on a ceramic carrier board and flexible printed circuit cables which have been developed specifically for operation in an ultra high vacuum environment.

KEYWORDS: Beam-line instrumentation (beam position and profile monitors; beam-intensity monitors; bunch length monitors); Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons)

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1 Introduction

The Proton Synchrotron Beam Gas Ionization monitor (PS-BGI) is a device to measure the beam transverse profile in the PS. It uses the electrons produced by the beam/rest gas interaction to infer the beam size. In this context, rest gas refers to the residual gas present in the PS beam pipe. The electrons are translated from their emission point to the detector using an electro magnetic field and the beam profile is then reconstructed using the position and timing information of the electron-hits on the detector. The project is part of the PS LHC Injector Upgrade (LIU), itself part of the High Luminosity LHC (HL-LHC) project. Its objective is to provide profile measurements of the beam or its individual bunches every 1 ms with a relative error of 1 %. The rate at which the BGI can provide new profiles is mainly affected by the rest gas composition, vacuum pressure and beam parameters (e.g. intensity, current).

PS-BGI features a novel type of detection system based on Timepix3 Hybrid Pixel Detectors (HPD's) [1]. This technology allows for a direct detection of the electrons, without the need for gas injection or Multi-Chanel Plate (MCP) amplification and for a profile acquisition at speeds of several kHz. However, the detector has to be in the close proximity of the beam in order to work as expected. This adds the complexity of having the device inside the beam vacuum and exposure to radiation.

This contribution focuses on the development of the PS-BGI detector and the imaging detector in particular. The readout system and support systems (e.g. power supply) are not discussed in this article. The mechanical design and operational requirements of the PS-BGI instrument are described elsewhere and are only briefly mentioned here [2, 3]. The first assembled PS-BGI prototype is presented in figure 1. The design follows the SPS and LHC BGIs by having the device entirely mounted onto a rectangular flange. Two rectangular electrodes are used to shape the electric field. A -20 kV potential is applied to the top electrode while the rest of the field cage is grounded. An ion trap, on the top electrode, prevents the emission of secondary electrons onto the detector. The bottom electrode covers the detector assembly and protects it from the beam wake-field by

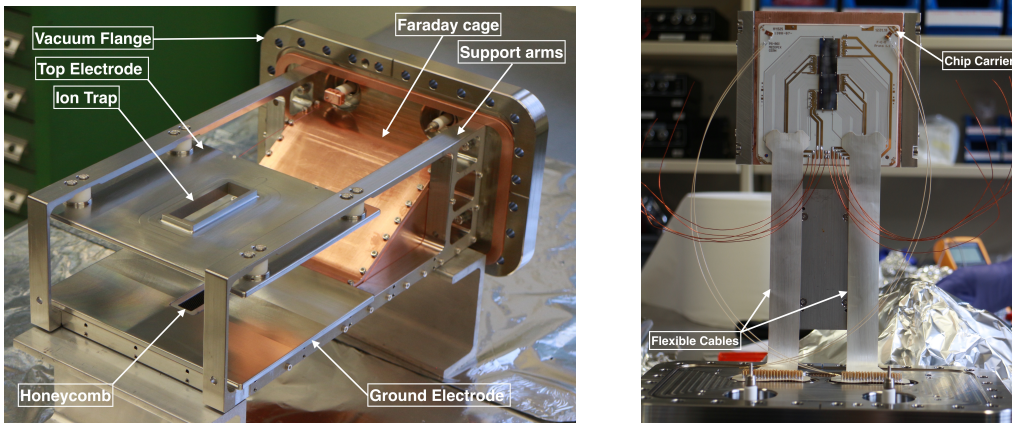


Figure 1. Left: first assembled PS-BGI prototype. Right: the Imaging detector during assembly.

forming a faraday cage with the rest of the BGI. An opening in the bottom electrode is provided by a steel honeycomb to allow the electrons to reach the detector whilst also providing protection from the beam wake-field.

2 PS-BGI detector

The PS-BGI imaging detector has been developed to operate inside the primary PS vacuum under a pressure of 10^{-9} mbar and an expected radiation dose per year of 10 kGray. It is composed of four TPX3 placed on a ceramic carrier board. This board routes the TPX3 signals to two sets of connectors, while the power traces are directly brazed to copper wires. A pair of flexible cables connect the ceramic carrier board to D-SUB connectors on the vacuum feedthrough flange. The ceramic board is connected to a cooling circuit via an intermediate ceramic support. This assembly is used to evacuate the heat generated by the TPX3 during operation and provide additional cooling for the silicon sensors. The good field region for the detector is $50 \times 50 \text{ mm}^2$ and the maximum thickness allowed by the magnet aperture for the detector and cooling circuit is 12 mm. The signal feedthroughs are standard D-SUB 78 and D-SUB 26.

2.1 Timepix3 and silicon sensors

Timepix3 is a pixelated readout chip developed by the Medipix3 collaboration [4]. It has a detection area of 14 mm^2 Containing 256×256 pixels with a $55 \mu\text{m}$ pitch. It features two readout modes; event driven and frame based and can provide the Time of Arrival (ToA) and Time over Threshold (ToT) for each individual pixel. Additionally the TPX3 can be used in a more classic photon counting mode where only the number of hits above threshold and integrated ToT (iToT) are recoded. The ToA has a resolution of 1.56 ns and the minimum threshold was measured at ~ 500 electrons or $\sim 2 \text{ keV}$ in silicon [1]. A single Timepix3 can detect and readout up to 80 MHit/s. Each hit is contained in a 60-bits package and is readout on one of eight Scalable Low-Voltage Signalling (SLVS) differential links. Each link can transmit up to 640 Mbit/s, bringing the total data rate to 5.12 Gbit/s for a single Timepix3 chip.

The arrangement of the TPX3s in the imaging detector is presented in figure 2. The number and placement of pixel detectors is defined by the beam position uncertainty (pipe center ± 25 mm). Four TPX3 chips in a row perpendicular to the beam direction allow to image the beam at any time during the acceleration cycle. The total detection area of the detector is $14 \times 56 \text{ mm}^2$ with 262k pixels. Each TPX3 is bonded to an individual silicon edgeless sensor. These sensors are $100 \mu\text{m}$ thick and each pixel contains a P implant in a N bulk (P on N). The silicon surface is not metalized in order to allow low-energy electrons to reach the silicon and they are operated fully depleted in order to maximize detection efficiency. This type of sensor was selected after a series of tests conducted with a demonstrator instrument [2].

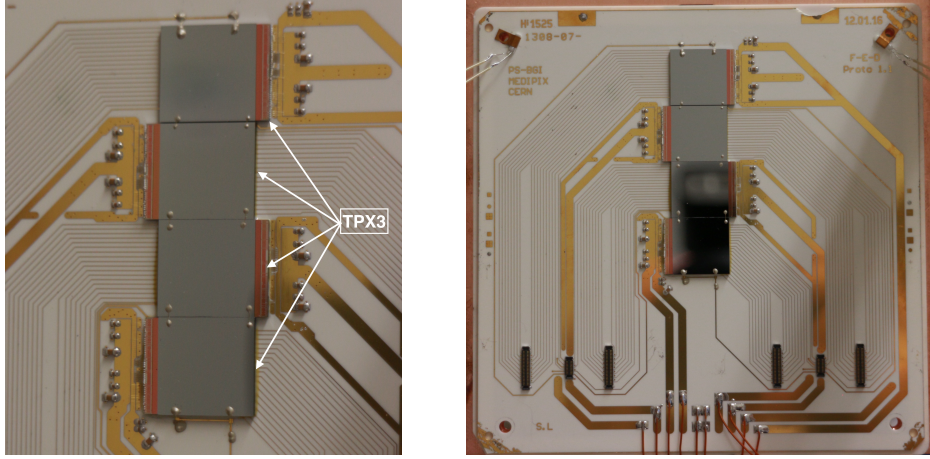


Figure 2. Left: TPX3 assemblies monted on the chip carrier. Right: ceramic chip carrier board.

It is estimated that the signal from the beam will be in the order of 40 MHit/s (electrons), with each ionization electron having an energy close to 10 keV. This estimate is based on the measured vacuum pressure, gas composition inside the PS beam line, electro-magnetic field in the good-field region and the detection area. However, the noise level in the PS is unknown as such a detector was never operated in close proximity to the beam. Noise sources might include; direct losses from the beam, secondary electron emission and activated material close to the detector. Due to these uncertainties, the optimal mode of operation for the detector has yet to be defined.

2.2 Chip carrier

The chip carrier is a ceramic circuit board. Its role is to electrically connect the TPX3s to the readout electronics as well as to provide a physical support for the assemblies. The ceramic carrier is also part of the cooling system (discussed in section 2.4). The main features of this board are its compatibility with the PS vacuum and radiation tolerance. The chip carrier is shown in figure 2.

The board has two metal layers built around a $114.3 \times 114.3 \times 0.389 \text{ mm}^3$ aluminium oxide substrate (99.9 % Al_2O_3). Compared to conventional PCB substrates, the ceramic is used to reduce the total outgassing from the board. It also has the added benefits of being radiation tolerant and is readily available for circuit board manufacturing. The top layer is used to route the signals and power, wirebond the TPX3s and secure them onto the board. The bottom layer is used for the ground and some routing for the power traces. All signals are routed on the top layer in order to reduce

design complexity, further reducing design and manufacturing time. Moreover, not using vias enhances signal integrity. Most of the wirebond pads on the TPX3 have a $73\ \mu\text{m}$ pitch. Considering that the chips are bonded using wedge-wedge aluminum wirebonds, it is important to keep the bonding pads on-chip as aligned as possible with the pads on the ceramic, which necessitates a minimum trace width/spacing of $30\ \mu\text{m}$ on the ceramic. This feature size is achieved by a sputtering thin film deposition technique. Both metal layers have a Ti/Cu/Ni/Ag metalization with the copper layer being $12\ \mu\text{m}$ thick. Ti is the sputtered layer, the other layers are chemically grown. The copper thickness is required to limit the voltage drop on the power traces. To further limit outgassing no soldermask is applied.

The differential pairs are matched to a 100 ohm impedance and their physical parameters are obtained using 2D field solvers. Crosstalk is mitigated by large spacing between the pairs.

The board comprises the four TXP3 assemblies, their decoupling ceramic capacitors and low-profile connectors. Despite the fact that TPX3s can be daisy chained, each TPX3 assembly is operated independently. This configuration was selected in order to increase the overall reliability of the detector as well as simplifying its design. Each Timepix3 assembly is glued to the ceramic using a thin layer of non electrically conductive low outgassing epoxy. The bias voltage is connected from the ceramic to the sensors by manually placed gold wires. These wires are connected on either side of the Timepix3 row for the chips on the outside and from sensor to sensor for the chips in the center. The wires are secured by a small drop of conductive epoxy. This specific procedure is necessary due to the absence of a metallic layer on top of the sensors, which precludes the use of a standard wirebonding technique to attach the bias wires to the sensor. The Timepix3 requires decoupling capacitors to stabilize its input voltages. These capacitors are by design oversized in order to mitigate the effects of radiation induced degradation [5, 6]. Moreover, due to the limited vertical clearance between the top of the ceramic and the field shaping ground electrode (1mm), the largest capacitors have to be placed on the bottom side of the board. The connectors are also selected to fit within the vertical clearance and are only 0.6 mm when stacked. The limited number of components used on this board is mainly due to the fact that no other components could be easily converted for use in vacuum (direct die bonding on ceramic).

Two boards were assembled and tested for vacuum compatibility. The results show an outgassing rate, after 10h of pump down at room temperature, of $3.5 \times 10^{-6}\text{mbar} \cdot \text{l/s}$ and $1.8 \times 10^{-6}\text{mbar} \cdot \text{l/s}$ and both boards are within CERN acceptance limits for the Residual Gas Analysis (RGA). The large difference in outgassing rate comes from the fact that each board uses a different epoxy to secure the TPX3 assemblies.

2.3 Flexible cables

The flexible cables are a pair of flexible printed circuit boards. Their role is to connect the ceramic carrier to the flange feedthroughs. The cables route every digital and analog signals to and from the TPX3, as well as the bias voltage required for the silicon sensors. A set of cables is presented in figure 3.

Each cable has two metal layers built around a $50\ \mu\text{m}$ thick Liquid Crystal Polymer (LCP) substrate. This substrate is selected for UHV operation. LCP has the advantage of being virtually hermetic, absorbing very little gas when exposed to air and therefore degassing very little when placed in vacuum. This allows for direct vacuum operation without requiring a bake-out procedure

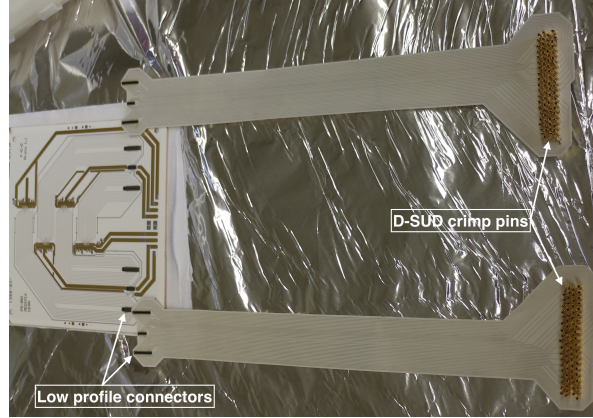


Figure 3. Left and right flexible cables with a blank chip carrier board.

or specific storage environment. The PCB stack is limited to two metal layers in order to avoid the use of a bonding layer between substrates. The top layer is used for the signal ground-plane while the bottom layer is used for the signal microstrips. Every differential pair is matched to a 100 ohm differential impedance. The physical parameters for the traces were obtained by simulating the traces in 2D field solvers. The design also accounts for crosstalk, intra-pair phase alignment and signals losses. Moreover, in order to limit signal reflections, no vias are used for the differential pairs.

The connection to the chip carrier board is done via three low profile connectors. These are mounted on the bottom side of the cable. The connection to the flange is done by directly brazing D-SUB crimp pins to the cable. Excess flux from the assembly was removed by a feral cleaning step.

One fully assembled cable was tested for vacuum compatibility. The measured outgassing rate, after 10h of pump down at room temperature, is 2.2×10^{-6} mbar · l/s and the cable RGA is within CERN acceptance limits.

2.4 Cooling system

A cooling system is required as it is impossible to rely on radiation to cool the detector while being operated inside of the PS vacuum. A liquid cooling system is therefore used to remove the 12W of heat generated by the four TPX3 chips and to reduce the effects of radiation damage on the silicon sensors [7].

The cooling system comprises a steel pipe brazed to a base copper plate, a support ceramic assembly and chip carrier board. Heat flows vertically from the TPX3s through the carrier board and ceramic support to then reach the copper plate where it is evacuated by the chilled liquid. The copper plate is specially designed to fit the ceramic support and the carrier board.

The ceramic support is a thin ceramic substrate brazed to a copper bar. Its main functions are to mechanically support the carrier board, electrically insulate it from the rest of the detector and provide a thermal link between the carrier board and the copper plate. It attaches to the copper plate by a set of screws, while the carrier board rests on the ceramic part. In order to enhance the thermal contact between the two ceramics, a thin gold foil is placed in between the ceramic carrier and support boards. The carrier board is then compressed against the ceramic support by a set of screws. This foil acts as a Thermal Interface Material (TIM) and effectively removes any voids due

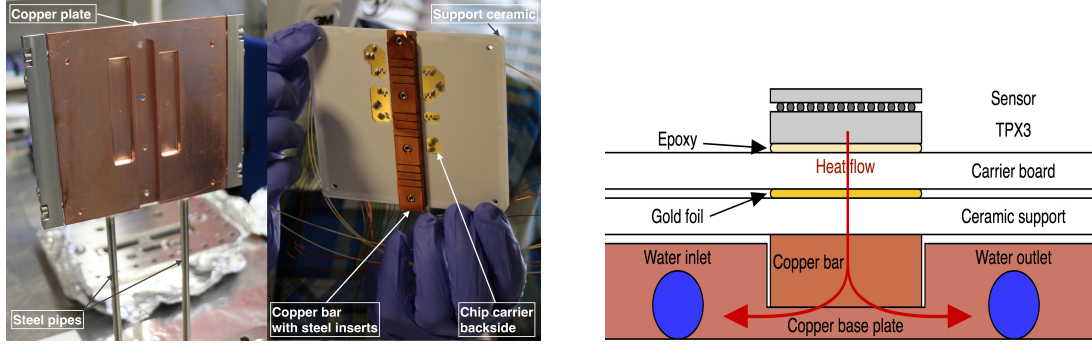


Figure 4. Left: base copper plate and ceramic support attached to the chip carrier. Right: cross-section of the cooling system.

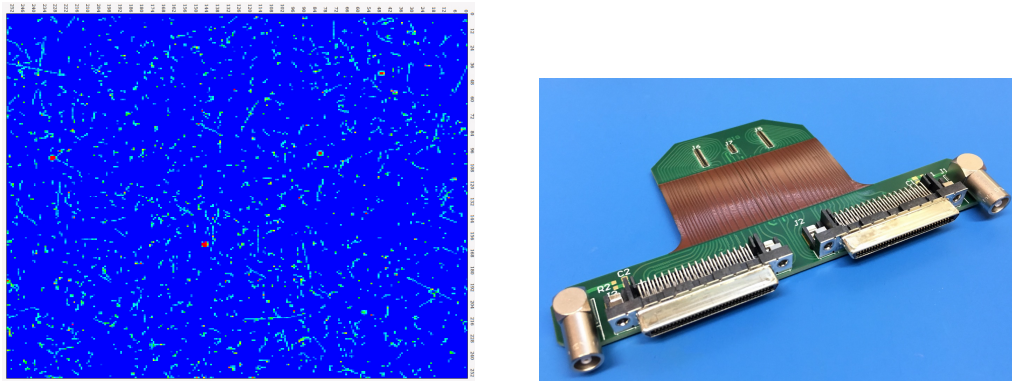


Figure 5. Left: data collected by the first chip carrier using cosmic rays. Right: rigid-flex PCB adapter for SPIDR.

to the ceramic surface roughness. Gold is preferred over other material due to its softness, vacuum compatibility and high melting point. Softness reduces the amount of force required to fill the voids in the ceramics and its high melting point removes the risk of the material suddenly vaporizing in case of catastrophic failure. This solution allows the detector to be replaced, if need be, without having to change the whole cooling system.

2.5 Detector testing

When assembled, the carrier boards are tested using the SPIDR readout system [8]. SPIDR is connected to the chip carrier using a flex-rigid PCB adapter that was developed for this purpose. This allows to verify if the assembly was successful and if any of the TPX3s were damaged during the assembly process. So far only the first produced chip carrier has been tested and some data was acquired using cosmic rays. The interface PCB and an example of cosmic ray data acquired with the first chip carrier are shown in figure 5.

3 Conclusion

A vacuum compatible electron detector for the PS Beam Gas Ionization monitor has been designed and manufactured. The preliminary vacuum and functional test results are encouraging and prove

that the hybrid pixel detector technology can be used in the primary vacuum of a particle accelerator. A prototype PS-BGI will be installed in the PS during winter 2017 with the aim of testing the operation of the Timpix3 chips in the accelerator environment.

Acknowledgments

The authors would like to thank: Michael Campbell, Jerome Alozy, Xavi Cudie, Alexandre Gerardin, Didier Steyaert, Yannick Coutron, Romain Ricol, Emilien Rigutto, Karol Scibor, Alice Michet, Jose Somosa, Wilhelmus Vollenberg, Claude Rinaldi and Sylvain Kaufmann.

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