A low noise high gain differential amplifier for bolometric detector

A. Reza[1],* V. Vatsa[2,3], M. S. Pose[1], A. Mazumdar[2,3], A. Garai[2,3], H. Krishnamoorthy[2,3], G. Gupta[1], R. Pachuau[1], V. Nanal[1], and R. G. Pillay[4]

[1]*DNAP, Tata Institute of Fundamental Research, Mumbai - 400005, INDIA*
[2]*INO, Tata Institute of Fundamental Research, Mumbai - 400005, INDIA*
[3]*Homi Bhabha National Institute, Anushaktinagar, Mumbai - 400094, INDIA*
[4]*Department of Physics, Indian Institute of Technology Ropar, Rupnagar – 140001, India*

Introduction

A tin cryogenic bolometer detector operating at 10 mK (*TIN.TIN* - The INdia based TIN detector) is being developed to study neutrinoless double-beta decay (NDBD) in ^{124}Sn [1]. The detector uses a neutron transmutation doped (NTD) Ge sensor, kept at 10 mK inside a cryogen free dilution refrigerator (CFDR), to detect the change in temperature due to an incident photon/charged particle. In the present readout scheme, output signal from the cold NTD Ge sensor is taken out of the CFDR and the signal is amplified at room temperature using a commercially available differential amplifier (FEMTO DLPVA-100-F). The large parasitic capacitance of the long cables, connecting the cold sensor to the differential amplifier at room temperature, leads to signal integration. The long cables are also vulnerable to external EMI pickups. To reduce these effects, a low noise cryogenic source follower amplifier with unity voltage gain has been designed and tested at 120 K [2]. The cryogenic amplifier will be used as a front-end stage in the bolometer readout circuit. The amplifier will be mounted on the 40K stage of the CFDR system and it will be kept in a thermal environment with an operating temperature of 120 K. For further amplification at 300 K, a low noise high gain differential amplifier has been designed and tested.

In this paper, we present the design and test results of a low noise high gain differential amplifier for the sensor readout circuit in a bolometer detector. Voltage gain (A_V), input voltage noise density (e_n) and common mode rejection ratio (CMRR) of the amplifier is measured at 300 K and its results are reported.

*Electronic address: **ashifreza86@gmail.com**

Circuit description of the amplifier

The circuit schematic of the low noise high gain differential amplifier is shown in Fig. 1. The differential amplifier consists of two stages. The first stage is a JFET based low gain differential amplifier, implemented using a general purpose low noise Si JFET (2SK879). All the supply voltages for FET biasing are filtered using a low-pass RC circuit. The output of the first stage differential amplifier is then applied to a low noise high gain instrumentation amplifier (INA103) from Texas Instruments. INA103 has a very low noise characteristic of 2 nV/√Hz at 10 Hz. It also offers a variable voltage gain in the range of 0 – 60 dB by selecting the gain setting resistor R_G. It also provides adjustment of the output offset voltage using a 10 kΩ potentiometer connected to the negative power supply (V-). The amplifier is fabricated on an FR4 glass epoxy PCB as shown in Fig. 2.

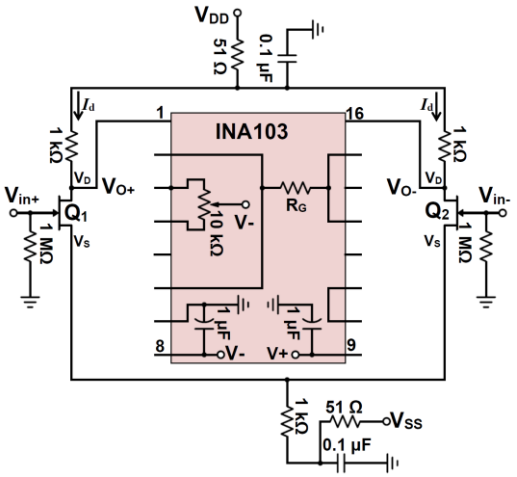

Fig. 1 Circuit schematic of the two stage differential amplifier

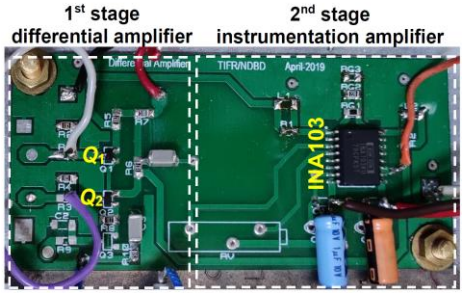

Fig. 2 Fabricated differential amplifier PCB

Testing and results

The DC bias voltages for the FETs are supplied using a data acquisition (DAQ) card from National Instruments (PXI-6232). Biasing voltages (V_+ = +15 V, V_- = -15 V) for INA103 is supplied using a DC voltage source. To measure A_V, a LabVIEW code is developed which sweeps the frequency of input signal in the range of DC – 100 kHz and acquires the amplifier's output data. A_V of the amplifier is defined as,

$$A_V = A_{V1} + A_{V2} = A_{V1} + \left(1 + \frac{6000}{R_G}\right) \quad (1)$$

While voltage gain for the first stage (A_{V1}) is controlled by the bias parameters I_d and V_{DS} ($V_{DS} = V_D - V_S$) of both the FETs, voltage gain for INA103 (A_{V2}) is decided by the selection of R_G. A typical frequency response of the amplifier for two values of R_G are shown in Fig. 3, which shows almost flat frequency response in our desired frequency band of DC – 100 kHz.

e_n of the amplifier is measured by shorting the input of the amplifier and measuring the output noise voltage using the PXI card. For the bias setting of I_d = 2 mA and V_{DS} = 2 V, e_n ~ 4.2 nV/√Hz is obtained as shown in Fig. 4.

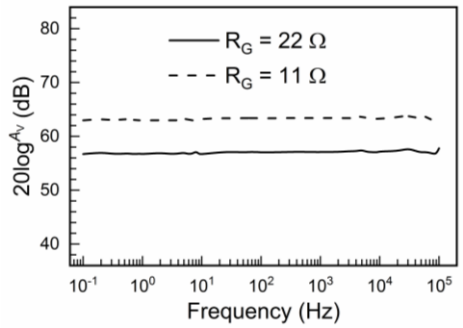

Fig. 3 Measured frequency response for different R_G. Bias setting: I_d = 2 mA, V_{DS} = 2 V.

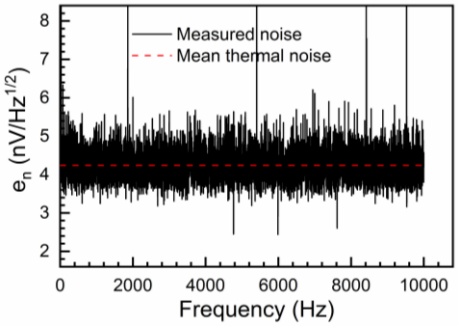

Fig. 4 Measured input voltage noise density for R_G = 11 Ω. Bias setting I_d = 2 mA, V_{DS} = 2 V.

Table 1: A_V, e_n and CMRR for different bias settings with R_G = 11 Ω

Bias points (I_d, V_{DS})	A_V (dB)	e_n (nV/√Hz)	CMRR (dB)
0.5 mA, 2.0 V	*59.4*	*5.8*	*70.7*
1.0 mA, 2.0 V	*61.7*	*4.8*	*63.8*
2.0 mA, 2.0 V	*63.2*	*4.2*	*59.5*
2.0 mA, 4.0 V	*64.3*	*4.0*	*66.1*

The measured A_V, e_n and CMRR for different bias settings are listed in Table 1. For a fixed R_G of 11 Ω, slight variation in A_V is observed due to changes in A_{V1} at different bias settings. It is also observed that e_n is sensitive with the variation in I_d. For a fixed V_{DS} of 2 V, e_n ~ 5.8 nV/√Hz is obtained which further reduces to 4.2 nV/√Hz at a higher I_d of 2 mA. There is little effect of variation in V_{DS} on e_n. Although e_n improves with the variation in I_d from 0.5 mA to 2 mA, CMRR of the amplifier reduces from 70.7 dB to 59.5 dB at higher I_d. Increasing V_{DS} to 4 V offers a better CMRR of 66 dB for I_d = 2 mA.

Acknowledgements

We thank Mr. S. Mallikarjunachary and Mr. K. V. Divekar for assistance during the measurement. We also acknowledge the support of *TIN.TIN* and INO collaboration.

References

[1] V. Nanal, Eur. Phy. J. Conf. **66**, 08005 (2014).

[2] A. Reza et al., 18th International Workshop on Low Temperature Detectors, 2019.