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Development of CMOS Sensors for Electron Microscopy

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Abstract: In this work, we show the design and preliminary characterization of an image sensor with 64x64 pixels and its associated hardware and software needed to use the chip. The aim of the chip is to be used as a sensor for TEM electron microscopy. First measurements were done using X-Rays to characterize the chip and to test the whole system (ASIC, Software, and Hardware). The chip was tested with electrons inside an Electron Microscope at Thermo Fisher and it's functioning was checked. The chip was able to stand 50 Mrad of X-Ray and 3.6 Mrad of electrons total dose without decreasing considerably the performance.

Keywords: Radiation-hard detectors, Solid state detectors, Radiation damage to electronic components, Radiation-hard electronics

Contents

1 Introduction

The current prototype for the proposed sensor was developed in 180nm AMS HV-technology [1] with a 64x64 pixel matrix and a rolling shutter readout for detection of High Energy Particles (HEP).

This project aims to test the sensor to evaluate the feasibility of using it as a sensor inside an electron microscope. The sensor characteristics needed, depends on the application, that is why it is complicated to give specific numbers, however, approximate values are shown in Table 1.

Table 1. Specs of sensors on electron microscopy [2–4]

	Diffraction Imaging	Life Science	Material Science
Pixel Array	< 1k x 1k	> 4k x 4k	> 1k x 1k
Dynamic Range	Single-electron up to 10^5 e/pix/frame	Single-electron detection	20 ~ 200 e/pix/frame
Radiation Hardness (~1 year use)	~20 Grad	~20 Mrad	~1 Mrad
Framerate [fps]	>1000/s	>40/s	>100/s

The sensor consists of a matrix of pixels and the associated electronics. The pixels exploit deep n-wells on p-substrate diodes. Secondary particles are collected on the deep n-wells which include the front-end pixel electronics. Due to the High Voltage (HV) technology, a large depletion zone is created which allows improving the charge collection. Front-end electronics contain a charge sensitive amplifier and a novel implementation of analog correlated double sampling (CDS) circuit. Signals are then passed to 128 readout channels at the chip periphery, each channel containing an amplifier and an 8-bit Analog-to-Digital Converter (ADC). The digitalized signals are serialized and output via 8 Low Voltage Differential Signals (LVDS). The frame rate of the sensor is 6.1 kHz. Figure 1 shows the schematic of one channel.

The matrix consists of 64×64 pixels, with two flavors, called current pixels (Figure 2(a)) and voltage pixels (Figure 2(b)). The voltage pixels are the most simple ones, while the current pixels, due to the complexity of their design, have the option to use the CDS mode.

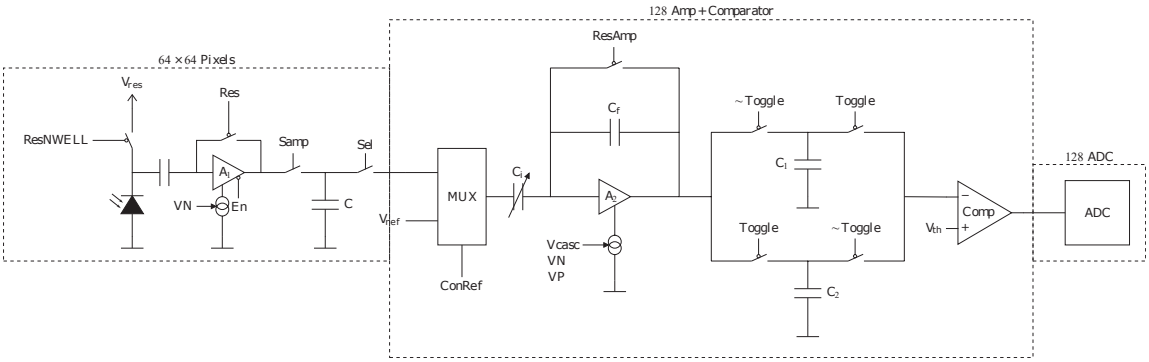
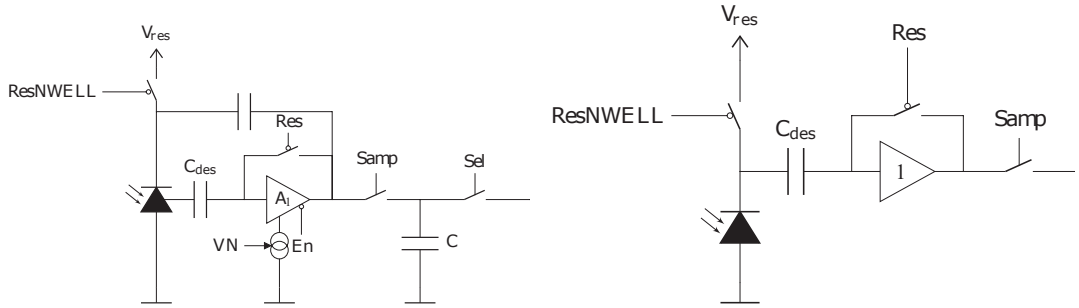


Figure 1. Schematic of one channel with the current pixel.



(a) Schematic of the current pixel.

(b) Schematic of the voltage pixel.

Figure 2. Schematic of the two types of pixels.

As it was before explained, the current pixels has the most complex design, this is due to the fact that this one has the possibility to work on CDS mode. This pixel consists on a Photodiode, a decoupling capacitor -C_{des}-, a charge sensitive amplifier with adjustable bias current through VN voltage (set in the PC software), a storage capacitor -*C*- and a series of switches (Figure 2(a)).

The simplified functioning of the current pixel consist of four phases, controlled by the signals sent by the FPGA:

1. During the first phase switches *ResNWell*, *Res*, and *Samp* close. By doing this, the amplifier is enabled, it is in reset state and the reset voltage is stored in capacitor *C*. (Figure 3).

2. In the second phase all switches are open, and the photodiode collects the signal charge. During this time the amplifier is disabled.

3. During the third phase, reset voltage is readout. The switch *Sel* is closed, allowing the reset voltage stored on the Capacitor *C* to advance to the ADC part of the readoout chain. (Figure 4).

4. Finally, in the fourth phase the switches *Samp* and *Sel* are closed. The charge sensitive amplifier is enabled, allowing the accumulated charge by the pixel to be amplified. (Figure 5).

The output of the pixel column is connected to a multiplexer, which allows readout in CDS mode (signal minus reset level is amplified) or readout in single sampling mode (signal minus reference

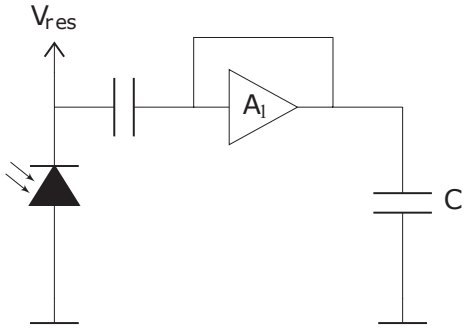


Figure 3. Phase 1 - storage of the reset value on C.

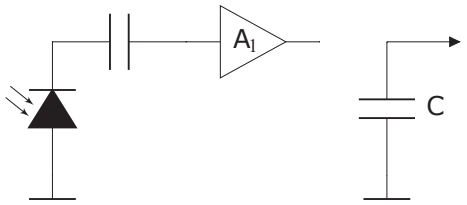


Figure 4. Phase 3 - send the reset voltage on C to the amplifier on the next part of the chain.

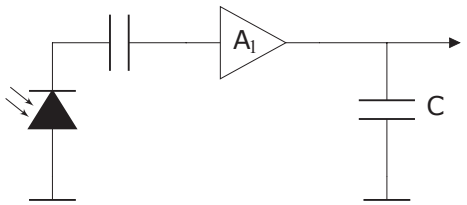


Figure 5. Phase 4 - send the signal voltage to the amplifier on the next part of the chain.

voltage is amplified). After, the signal passes through an differential amplifier with programmable gain. CDS takes part in this place. The voltage at the output of the amplifier is stored at capacitor C_1 or C_2. These capacitors are then discharged by a constant current and a comparator is used to detect a threshold crossing. The discharge time is proportional to the signal amplitude.. The schematic of the system is shown in Figure 6.

Equation 1.1 shows the formula for output voltage of the amplifier A_2.

$$V_0 = (V_{signal+reset} - V_{reset})\frac{C_i}{C_f} = V_{signal}\frac{C_i}{C_f} \tag{1.1}$$

By using the 2 capacitors with 4 switches topology (C_1, C_2, $Toggle$, and $\sim Toggle$) the speed of the system is improved.

2 The System

The hardware system consists of the chip under test, two PCB, one where the chip is bonded and the other to make the physical interface between the FPGA and the chip (Figure 7(a)). The FPGA used is a Nexys Video [5], which creates the link between the PC and the chip. The FPGA receives

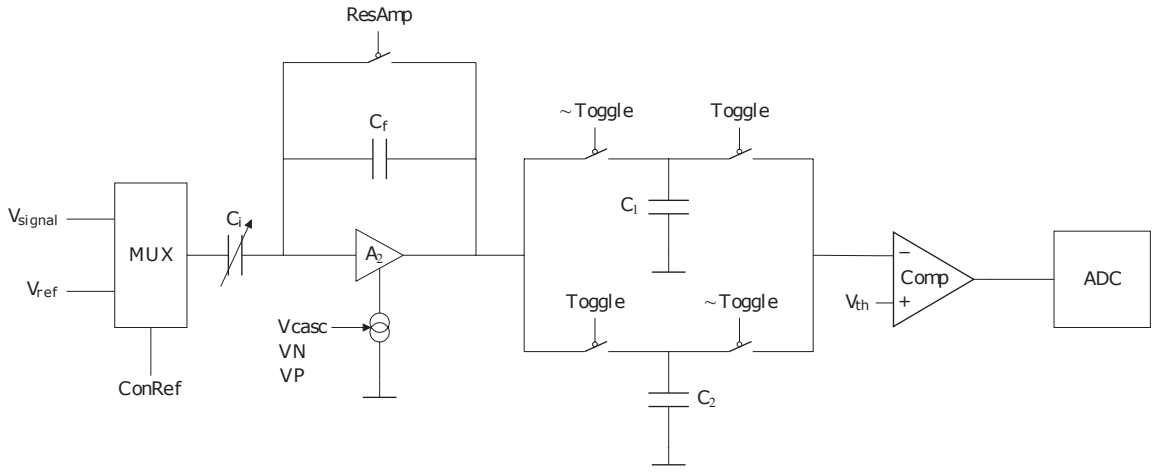
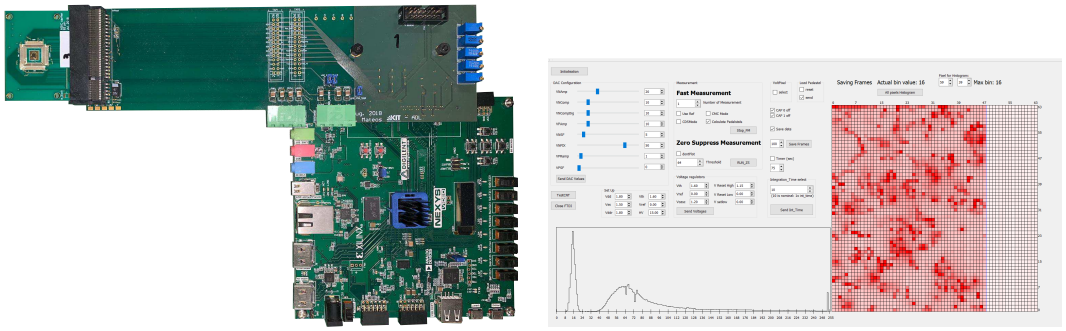


Figure 6. Schematic of the amplifier, comparator, and ADC chain.

the configuration data for the chip, from the PC. Then FPGA generates all the relevant signals to control the chip and it receives the data from the chip and sends it to the PC in the correct form and order. On the PC side, an interface was designed with Qt (Figure 7(b)). Using this interface, it is possible to set the values of the internal DACs of the chip, display in real-time the pixel.



(a) Custom PCB designed. (b) Interface programmed.

Figure 7. Hardware and software of the system.

3 Measurements

The chip has been irradiated with X-Ray tube and electrons. The interaction with silicon for both radiations is different, while X-Ray photons of low energies interact with silicon via photoelectric effect, the electrons losses energy by Coulomb interaction and creates electron-hole pairs in the depletion zone which are collected by the diode [6, 7].

For the X-Rays, it was used a Seyfert ISO-DEBYEFLEX 3003 X-Ray tube with energies from 6.4 keV to 25.3 keV at ITP Institute at Karlsruhe Institute of Technology. The electron measurements were carried out with a TECNAI-F20 Transmission Electron Microscope (TEM) with 200 keV electrons at Thermo Fisher Scientific in the Netherlands.

3.1 X-Ray measurements

The energy range was from 6.4 keV to 25.3 keV. 7 different targets were used to obtain different energies. For every pixel offset was calculated and subtracted, 64 was added. By histogramming the output of the chip (offset corrected ADC counts for every pixel), and then fitting the peak of the histogram with a Gaussian function it is possible to compute the mean output value over each pixel. After the mean values are averaged to obtain the values shown in Table 2.

Table 2. Energy of the targets and chip output ADC count value obtained

Target	Energy [eV]	μ [ADC count]
Fe	6403.13	105
Cu	8048.11	115
Zn	8639.1	118
Mo	17479.1	157
Ag	22162.99	172
In	24209.78	177
Sn	25271.34	180

Figure 8 shows the histograms of all pixels together of each irradiation, and the Gaussian approximation for each peak (red curve). The mean value in ADC counts of the Gaussian is related to the source energy applied and can be used for calibration. A presence of low-energy peak (around 110) on the histograms of the high energies measurements is due to residual Copper on the tube setup.

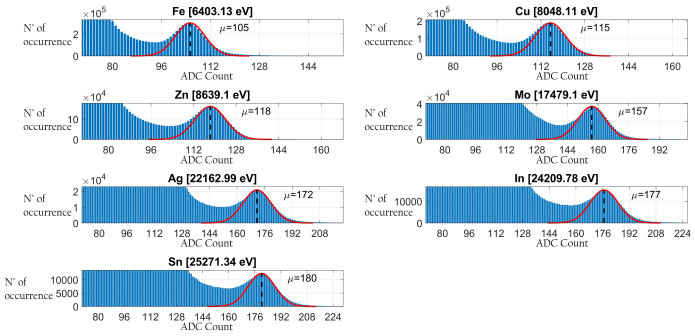


Figure 8. Histograms obtained for the different energies and fitted Gaussians.

To compute the noise of the system, a Gaussian curve is fitted (Figure 9) at the base line of the pixel signal, and the sigma value represents the noise. In this case, the value obtained was 86e^- (average over the whole matrix). The mean value is not 64 because of temperature change.

To obtain the conversion factor between the ADC count output of the chip and the beam energy, the linear fit was used. The conversion factor is the slope of the linear approximation, which was calculated as being 253.37 eV/bit (R^2=0.996) (Figure 10).

After the energy test, a total dose measurement was carried out. The chip was irradiated continuously for 8 hours until it receives 50 Mrad. At the end of the irradiation, the chip was working correctly, with with a noise floor of 201e^- (average over the whole matrix).

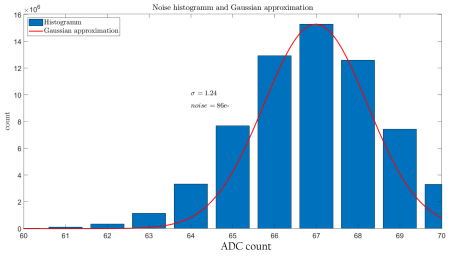


Figure 9. Noise floor and fitted Gaussian.

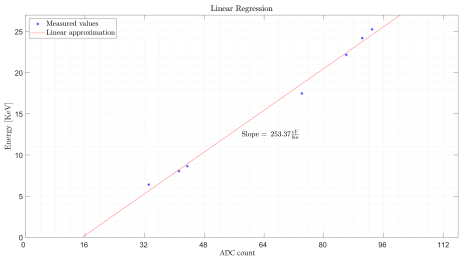


Figure 10. Calibration curve.

By doing an energy test again with the same sources and environmental conditions, it was found that the conversion factor changed to 329.18 eV/bit (R^2=0.997). This proves the correct functioning of the sensor after 50 Mrad of total dose.

The next day, the chip was irradiated for 32 hours to deliver 200 Mrad to the chip, accumulating 250 Mrad of total dose received by the chip. Following, it was tested again with the different sources, however, despite the chip shows response to visible light, due to the high background noise, it was not possible to calculate the factor conversion.

3.2 Electrons measurements

The chip was tested with electrons at Thermo Fisher facilities. The beam was first calibrated with a Faraday Cup, and then the whole silicon sensor was uniformly irradiated. The chip was able to detect single electrons hits (Figure 11).

The measurements were carried out by steps, each of them increasing the current value. Before each measurement, the background noise was acquired. Furthermore, the chip was tested with 0V and 40V of negative biasing HV substrate.

The chip stops to work properly and the pixel gain changed when the total dose was around 78 krad. Because of the pattern at the output, it is suspected that a failure on the ADC is responsible for this, more precisely, an NMOS switch connected to C_1 and C_2 (Figure 6) which will not be radiation tolerant.

The background noise before the irradiation started was 47 ADC counts, and the noise after the last working measurement (61.4 krad of total dose) was 65 ADC counts, which supports the theory that the matrix is radiation tolerant but some part of the surrounding circuitry is not.

Another chip was tested under the same conditions, in this case, the beam was focused only over the matrix sensor, trying to avoid the irradiation of the surrounding circuitry. Figure 12 shows

one of those steps, the hot spot is where the beam was focused.

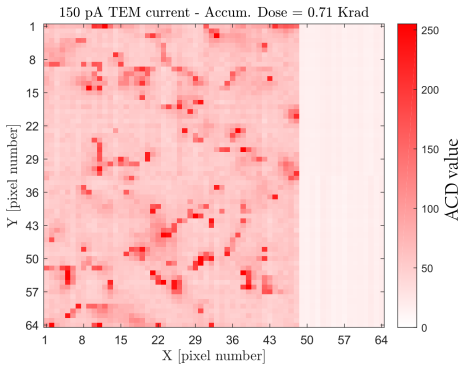


Figure 11. Single electrons measured with current pixels.

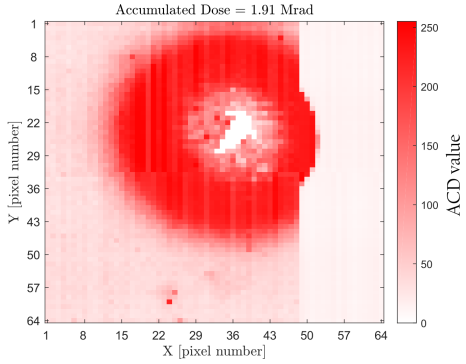


Figure 12. Electron beam focused only over the sensor matrix.

After 3.5 Mrad, the pixels at the center of the spot were saturated without the beam on. Under these circumstances, the chip was able to stand 63 Mrad (due to the set up of the beam, the surrounding received an unknown dose). After this dose, the chip stopped working, showing no output data. This second measurement demonstrated the radiation hardness of the sensor matrix compared to the surrounded circuitry, and the need for improvements on the electronics. The measurement also shows the difference in radiation tolerance of the pixel when a different type of radiation is delivered. With photons, the background noise increased from 44 to 71 at 50 Mrad, while with electrons the noise shows a much higher variation, increased from 39 to 142 at 3.5 Mrad.

This measurement showed that the matrix can stand more radiation, however, the surrounding circuitry could not.

3.3 Conclusions

The chip shows a linear response for the energy range between 6.4 keV ~ 25.3 keV, with a noise level of 86e^-. The chip was also tested for total dose up to 50 Mrad without showing signs of damage but with an increase of noise (from 86e^- to 201e^-), and the charge conversion factor, from 253.37 eV/bit to 329.18 eV/bit. After 250 Mrad, the noise is too high, making impossible to distinguish the energy peaks. Further experiments will be carried out, like the influence of annealing.

It is possible to detect single electrons hits with the system, however, it is necessary to improve the radiation hardness of the design to ionizing dose for the chip to withstand higher levels of electron irradiation. Measurements show that the sensor matrix can stand a high dose, but the surrounding electronics can not.

The higher the substrate voltage the greater the depletion region is. We expect a lower charge spreading with higher voltages due to the increased collection by drift. However, the substrate is currently 200 μm thick and it cannot be fully depleted. The charge spread could be reduced by back thinning the chip.

Further investigation on the ionizing dose tolerance is to be carried out.

Acknowledgments

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