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A Low Noise Signal Read-Out Circuit for Integrated Quantum Diamond Magnetometers

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ABSTRACT A customized low-noise signal read-out circuit, which is designed for the implementation of the integrated low power consumption quantum magnetometers based on nitrogen-vacancy centers in diamond, is reported in this article. As the circuit has a 3.7 $\text{pA/Hz}^{1/2}$ low-input noise which is superior to the latest studies, the integrated quantum diamond magnetometer can achieve a subnanotesla magnetic sensitivity with a low laser power of 70 mW. The circuit is designed with a compact 9.6 × 3.7-cm printed-circuit board, and has been applied to implement the integrated quantum diamond magnetometer. The contributors of the signal noise have been analyzed in this article, and an optimized low noise amplifier circuit design has been obtained. The circuit is featured by the performance in low noise, and the experimental results prove that the circuit has a considerable advantage in signal read out for the magnetometer with a low laser power. This study has a bright future to be applied in the practical application that requires low noise signal read-out functions.

INDEX TERMS Lock-in amplifier, low noise, nitrogen-vacancy (N-V) center, quantum magnetometer.

I. INTRODUCTION

Nitrogen-vacancy (N-V) centers in diamond, have been recognized as a potential candidate to realize quantum sensing at room temperature and atmosphere environment [1], [2]. Due to the long spin coherence time, the optical initialization and read out, the N-V centers can be used to implement quantum sensors for magnetic field [3], [4], electric field [5], [6], strain [7], and temperature [8], [9]. The excellent physical properties of N-V centers allow for high-resolution and noninvasive magnetic field measurement [10] and microscale magnetic imaging [11], [12]. The optically detected magnetic resonance (ODMR) technique has been applied to realize N-V magnetometers [13], and low-noise signal read-out circuits are required to realize the signal detection [14], [15].

In order to deliver practical applications, compact designs must be developed to replace the discrete instruments on the existing N-V magnetometry platforms [16]. Huang et al. [17] reported a portable and integrated magnetometer based on the diamond N-V centers, and laser diode, diamond sensor, microwave (MW) antenna, optical components, optical detector as well as a data acquisition card were integrated. Kim et al. reported an N-V center-based quantum sensor using complementary-metal-oxide semiconductor (CMOS) technology. MW generator, optical filter, and photodetector are integrated with CMOS technology, and a commercial lock-in amplifier (LIA) is used to realize signal readout. An advanced version based on CMOS technology was reported in [19]. A larger sensing area and a better spectral filter design are included in this work, and the noise contribution of the magnetometer is analyzed. Liu et al. [20] and Zhou et al. [21] also reported the implementation of integrated N-V quantum magnetometers with commercial LIAs. The output signals from the N-V samples can be readout with a commercial LIA, whereas such solution is bulky and requires high power consumption, and it cannot achieve a considerable

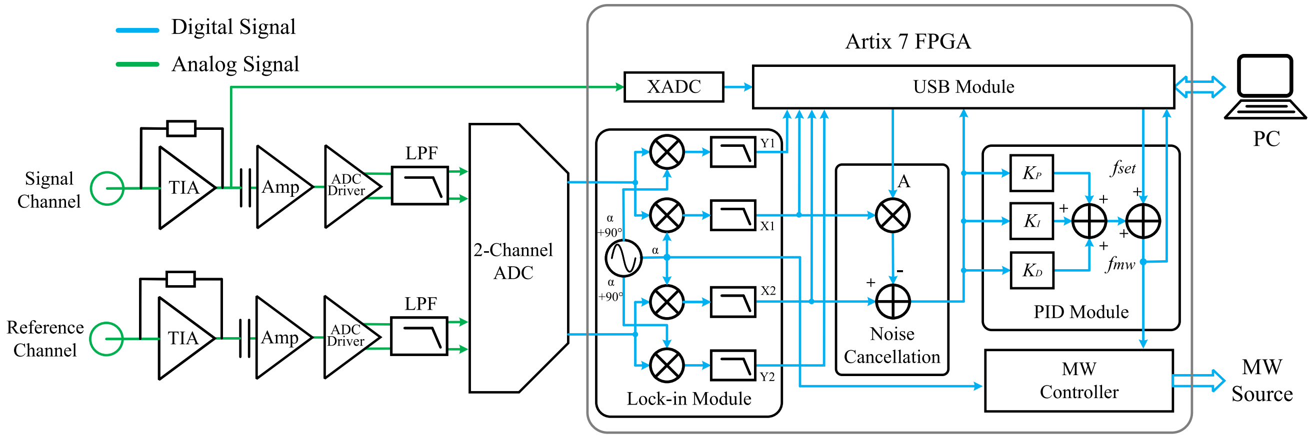

FIGURE 1. Architecture of the low-noise signal read-out circuit.

low input noise. There also exist home-built signal read-out circuits for N-V magnetometers. Wang et al. [22] reported a field-programmable-gate-arrays (FPGA)-based signal readout circuit which can be used to implement board-level N-V magnetometers. Commercial FPGA board [23], [24] and trans-impedance-amplifier (TIA) [25], [26] can also be used to develop the signal readout circuits for N-V magnetometer. However, such commercial circuits lack the capacity to achieve low-input noise and compact size. We report a customized circuit for real-time magnetic field vector measurement with the N-V centers in 2023 [27]. The circuit has a 25-pA/Hz$^{1/2}$ input noise, whereas it is suitable to be applied in large-scale experimental platforms which can integrate high power lasers. Low power consumption laser source should be implemented in the compact and integrated N-V magnetometer [28], [29], and the amplitude of the output optical signals as well as the optical noise is lower than that on the large-scale platforms. The electrical noise of the signal read-out circuit should be lower than the noise contributed by the N-V platform to avoid introducing extra errors in magnetic measurement. Hence, a compact low-noise signal read-out circuit is required to acquire the signals from the low power consumption N-V magnetometer, and such a circuit will be meaningful to push forward the application of the quantum magnetometry based on N-V center.

A customized low noise signal read-out circuit, which can be integrated in compact N-V magnetometers, is reported in this article. The circuit has a 3.7-pA/Hz$^{1/2}$ equivalent input noise which is lower than that reported in the latest studies. The circuit is implemented on a centimeter-scale 12-layer printed-circuit board, and a three-stage low-noise input amplifier, a 16-b analog-to-digital converter (ADC), as well as a Xilinx Artix-7 FPGA [30] is integrated. In order to realize signal read out for the N-V magnetometer, a lock-in module is realized with the reprogrammable digital resources in the FPGA chip. We applied the circuit in a compact N-V magnetometer to verify its performance, and the test results proved that the circuit has a considerable advantage in low-noise signal read out. The reported study is meaningful to the research areas which require low noise signal read out.

II. ARCHITECTURE

The architecture of the low-noise signal read-out circuit is shown in Fig. 1, and a Xilinx XC7A100T FPGA is utilized as the central control and digital data processing unit.

Two three-stage amplifiers are implemented to amplify the input signals, which are driven by photodiodes (PD). The two signal read-out channels are used to acquire the output signal and the reference signal from the N-V magnetometer, respectively, [31], [32], [33]. The output signal is the fluorescence signal from the diamond sensor, and the reference signal is a fraction of the laser beam for laser noise cancellation. The first-stage of the amplifier circuit is the most critical component as it is the major noise contributor of the circuit, and therefore both low-voltage noise and low-current noise are required to design such an amplifier. A 2-kΩ trans-impedance amplifier (TIA) is implemented with low-noise operational amplifier OPA828 [34], which can convert the input current signals from the PD into voltage signals. The amplifier OPA828 has 1.2-fA/Hz$^{1/2}$@8333 Hz low-current noise and 4-nV/Hz$^{1/2}$@8333 Hz low-voltage noise. Although the noise requirements for the second-stage and the third-stage amplifiers are less stringent than those for the first stage, the two amplifiers should have a low 1/f noise corner, which is defined as the frequency at which the spectral density of 1/f noise (also known as flicker noise) transitions to another type of noise, typically thermal or white noise. The second-stage amplifier is ADA4896 [35] which has a 100-Hz 1/f noise corner, and the third-stage amplifier is AD8132 [36] with 8-kHz 1/f noise corner. The chip ADA4896 is used as a noninverting amplifier to further amplify the signal, and the chip AD8132 is a fully differential amplifier which is suitable to be used as the driver for the ADC chip. The output AC signal from the N-V platform has a 10-μA peak-to-peak amplitude, and therefore the gains of the latter two amplification stages are set to be 10 and 6, respectively, to obtain an appropriate input voltage amplitude for signal acquisition.

A 4.7-μF DC block capacitor is located at the output terminal of the TIA to eliminate the DC offset of the N-V signals. With the DC block capacitor, the signal can be further amplified without saturating the following amplifiers, and the amplified signal can match the input range of the ADC. The output signals of the third-stage amplifier are filtered by low-pass-filters (LPF) which have DC-242-kHz pass-band. A 16-b two-channel ADC chip LTC2180 [37], which has 3.3 LSB RMS transition noise and a 25-Msps sampling rate, is used to acquire the amplified signals. A 2-channel digital lock-in module, a noise cancellation module, a proportional–integral–derivative (PID) module, a MW controller, as well as a universal-serial-bus (USB) module are implemented with the re-programmable resources inside the FPGA chip. The utilized FPGA chip XC7A100TCSG324 has 101400 logic cells, 240 DSP48E1 slices, 210 user I/Os, and a 15 × 15-mm compact size. The FPGA chip provides adequate resources to meet the requirements for realizing the function modules to readout the signals for N-V magnetometer. The lock-in module is used to realize the signal extraction for the N-V magnetometer, and both the real part and the imaginary part of the signal are acquired. A digital signal generation unit is implemented in the lock-in module to generate the demodulated signal to perform the lock-in function, and to output the pulse signals for modulating the MW source which is used to control the N-V samples. The demodulated signal and the MW control signal have the same frequency, which is determined by the N-V magnetometer platform [31]. The real parts of the output signals from the lock-in module are further processed by the noise cancellation module, and the outputs of the signal channel are multiplied by a factor A which is contributed by the inconsistency of the two channels, and then subtracted from the outputs from the reference channel [38], [39]. The cancellation coefficient A can be calculated as follows:

$$\mathrm{A} = \frac{\mathrm{cov}(\mathrm{X1}, \mathrm{X2})}{[\sigma(\mathrm{X1})]^2} \tag{1}$$

where cov(X1, X2) is the covariance of X1 and X2, whereas σ (X1) is the standard deviation of X1. The PID module is used to track the shift of the N-V magnetic resonance frequency according to the results of the noise cancellation, and the application of PID can extend the measurement range [27], [40]. The equation used in the PID module is

$$f_{\mathrm{mw}} = K_P \cdot X[n] + K_I \cdot \sum_{i=1}^{n} X[i] + K_D \cdot (X[n] - X[n]) + f_{\mathrm{set}}, \tag{2}$$

where $X[n]$ is the nth sample point of the output from noise cancellation module; K_P, K_I, and K_D are PID control parameters; and f_{set} is the initial MW frequency at the central zero point of ODMR spectrum. Once the N-V magnetic resonance frequency shifts, PID controller will adjust f_{mw} to a new central zero point. According to the output of the PID module, the MW controller can adjust the frequency of the MW source integrated in the N-V magnetometer via SPI in real time [31]. On the other hand, the 12-b XADC hardcore [41] inside the FPGA is used to monitor the amplitude of the TIA output signals. The calculating results of the lock-in module, the noise cancellation module, the PID module, as well as the XADC are transmitted to the host computer via the USB module, which also manages the control command distribution.

TABLE 1. Parameters for the Amplifiers

k	f	V_{noise1}	I_{noise1}	V_{noise2}
1.38×10^{-23} J/K	8333 Hz	4 nV/Hz$^{1/2}$	1.2 fA/Hz$^{1/2}$	1 nV/Hz$^{1/2}$
I_{noise2}	V_{noise3}	I_{noise3}	C_D	R_D
2.8 pA/Hz$^{1/2}$	10 nV/Hz$^{1/2}$	2.6 pA/Hz$^{1/2}$	4 nF	200 GΩ
C_F	C_1	R_T	R_G	R_S
330 pF	4.7 uF	2 kΩ	75 Ω	68 Ω
R_F	R_1	R_2	R_3	R_4
680 Ω	84.5 Ω	511 Ω	84.5 Ω	511 Ω
T				
300K				

III. NOISE ANALYSIS

The system noise of the N-V center based magnetometer can be described as

$$N_{\mathrm{total}} = \sqrt{N_{\mathrm{NV}}^2 + N_{\mathrm{Laser}}^2 + N_{\mathrm{Circuit}}^2}. \tag{3}$$

N_{total} is the overall noise of the magnetometer, N_{NV} is the noise of the N-V sample [14] and is mainly contributed by the shot noise which is defined as the intrinsic noise of photo detector caused by the photo number fluctuation [42], N_{Laser} is the noise contributed by the laser source in the magnetometer [38], [39], and N_{Circuit} is the circuit noise of the signal read-out circuit. As the noise of laser can be suppressed to a nondominant level by applying noise cancellation, the sensitivity of magnetometer is mainly limited by the shot noise and the noise of the read-out circuit. In order to avoid introducing extra noise to the magnetometer, the noise of read-out circuit should be much smaller than the shot noise of the magnetometer.

The noise of the circuit is composed of the noise of the three-stage amplifier, the power noise, and the noise of the ADC chip. In this section, a detailed analysis of noise contributors is presented.

The schematic of the three-stage amplifier is shown in Fig. 2. The input signal of the circuit is the current signal from the photodetector in the N-V magnetometer, and the circuit has a differential output port. The output voltage noise densities of each stage can be described as [43]

$$N1 = \sqrt{\begin{array}{l}(R_T I_{\mathrm{noise1}})^2 + V_{\mathrm{noise1}}^2 + 4kTR_T + 4kTR_D\left(\frac{R_T}{R_D}\right)^2 \\ +[2\pi f\,(C_D + C_F)\,V_{\mathrm{noise1}} R_T]^2\end{array}} \tag{4}$$

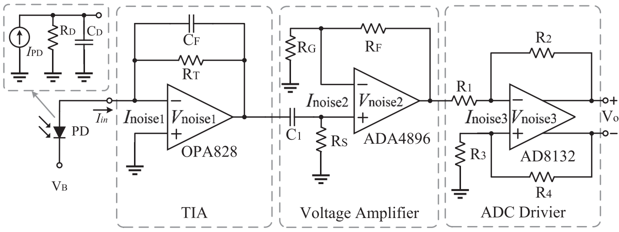

FIGURE 2. Schematic of the three-stage amplifier.

$$N2 = \sqrt{\begin{array}{l}\left[(R_S I_{\text{noise2}})^2 + V_{\text{noise2}}^2 + 4kTR_S\right]\left(1+\frac{R_F}{R_G}\right)^2 \\ +(R_F I_{\text{noise2}})^2 + 4kTR_F + 4kTR_G\left(\frac{R_F}{R_G}\right)^2\end{array}} \tag{5}$$

$$N3 = \sqrt{\begin{array}{l}(R_2 I_{\text{noise3}})^2 + (R_4 I_{\text{noise3}})^2 + 4kTR_1\left(\frac{R_2}{R_1}\right)^2 + 4kTR_2 \\ +4kTR_3\left(\frac{R_4}{R_3}\right)^2 + 4kTR_4 + V_{\text{noise3}}^2\left(1+\frac{R_2}{R_1}\right)^2\end{array}}. \tag{6}$$

N_1, N_2, and N_3 are defined as the output voltage noise density of each amplifier stage separately. The first-stage output noise density N_1 is contributed by the current and voltage noise of the amplifier (I_{noise1} and V_{noise1}), the thermal noise of the trans-impedance R_T, the parasitic resistance R_D and capacitors C_D and C_F. The N-V magnetometer outputs signals with a DC current around 2 mA, and therefore R_T is set as 2 kΩ to convert the signals to voltage signals. C_D and R_D are the parasitic capacitance and resistance of the PD in the N-V magnetometer, C_F is the compensation capacitor for circuit stability, f is the operating frequency 8333 Hz which is determined by the N-V magnetometer, k is the Boltzmann constant, and T is the operating temperature. The noise densities N_2 and N_3 of the second and third stages are also contributed by the current and voltage noise of the amplifiers, as well as by the thermal noise of the resistances.

Table 1 shows the detailed values of the parameters in the amplifier schematic; and the theoretical noise density N_1, N_2, and N_3 can be calculated as 7.1, 14.7, and 73.1 nV/Hz$^{1/2}$, respectively. The gains of the latter two stage amplifiers are 10 and 6, hence the final output noise density of the three-stage amplifier circuit can be calculated as

$$N_{\text{AMP}} = \sqrt{(6\cdot 10\cdot N_1)^2 + (6\cdot N_2)^2 + N_3^2}. \tag{7}$$

The total output voltage noise density of the amplifier circuit is 440 nV/Hz$^{1/2}$, and the contributions of the three stages are 426, 82.2, and 73.1 nV/Hz$^{1/2}$, respectively. Even though the first-stage amplifier has the best noise performance, it is the dominant noise source due to the cascaded architecture, and therefore a low noise amplifier design is required. The OPA828 chip used in the first-stage amplification has both low current noise and low voltage noise. According to (2), the noise contributed by current noise, voltage noise, trans-impedance R_T, parasitic resistance R_D, and capacitors are 2.4 pV/Hz$^{1/2}$, 4.0 nV/Hz$^{1/2}$, 5.8 nV/Hz$^{1/2}$, 0.6 pV/Hz$^{1/2}$, and 1.8 nV/Hz$^{1/2}$, respectively. Hence, the thermal noise from the trans-impedance is the major noise contributor. Considering solely the impact of the TIA noise, the equivalent input current noise is

$$\begin{aligned} N_{\text{IN}} &= \frac{N_{\text{AMP}}}{10\times 6\times R_T} \\ &\approx \sqrt{\begin{array}{l} I_{\text{noise1}}^2 + \left(\frac{V_{\text{noise1}}}{R_T}\right)^2 + \frac{4kT}{R_T} + \frac{4kT}{R_D} \\ +\left[2\pi f\,(C_D+C_F)\,V_{\text{noise1}}\right]^2\end{array}}. \end{aligned} \tag{8}$$

The noise contributed by the power and the ADC chip can also be calculated. The output noise of the power supply chip TPS7A8001 [44] is 0.35 μV/Hz$^{1/2}$ at the operating frequency 8333 Hz, and the power supply rejection ratio of three stage amplifiers are −103, −121, −70 dB, respectively. Hence, the power supply contributes a noise density bellowing 1 nV/Hz$^{1/2}$. The ADC noise is composed of the transition noise and the quantization noise, and can be calculated as follows [45], [46]:

$$N_{\text{ADC}} = \sqrt{N_{\text{trans}}^2 + N_{\text{quant}}^2}\Big/\left(\sqrt{f_s/2}\right). \tag{9}$$

N_{ADC} is the total noise of ADC, and f_s is the sampling rate of ADC. The transition noise N_{trans} equals 3.3 LSB, and the quantization noise N_{quant} is LSB/12$^{1/2}$ [47]. LSB is defined as the least significant bit of the ADC. The ADC chip has a 2-V input voltage range, a 16-b resolution, and a 25-Msps sampling rate. Hence, the value of the ADC noise density is 27.7 nV/Hz$^{1/2}$.

The power noise and the ADC noise are much lower than the noise of the amplifier circuits, and both the current noise and voltage noise of the amplifiers can be suppressed to a secondary contribution level through component selection and circuit design optimization. Hence, the thermal noise of the trans-impedance is the theoretical noise limit of the circuit. In order to approach the thermal noise floor boundary, the circuit design should be aggressively optimized to minimize the effect of other noise sources.

IV. EXPERIMENTAL RESULTS

The reported low-noise signal read-out circuit has been designed and fabricated. Fig. 3 shows the prototype photograph of the circuit and the schematic diagram of the analog circuit. The circuit is implemented on a 9.6- × 3.7-cm 12-layer printed-circuit-board (PCB), and it has a low-power consumption of 3.7 W. The signal detection bandwidth and the equivalent noise of the circuit have been tested to characterize its electrical properties, and the circuit has also been applied in a low power consumption N-V magnetometer to prove its performance in signal read-out.

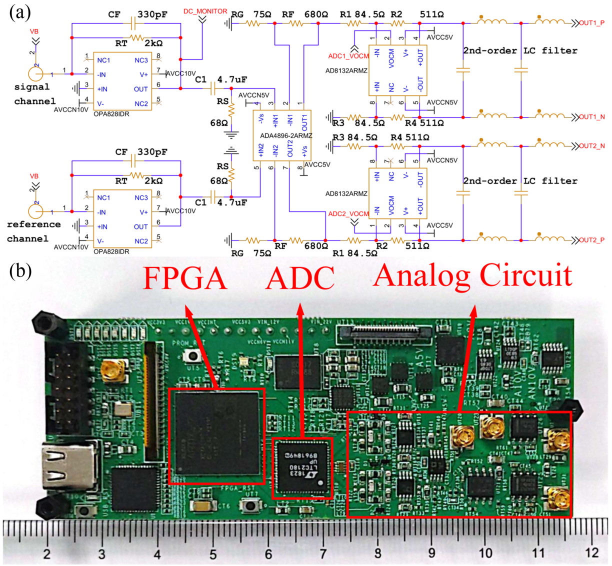

FIGURE 3. **(a) Schematic diagram of the analog circuit. (b) Prototype photograph of the low-noise signal read-out circuit.**

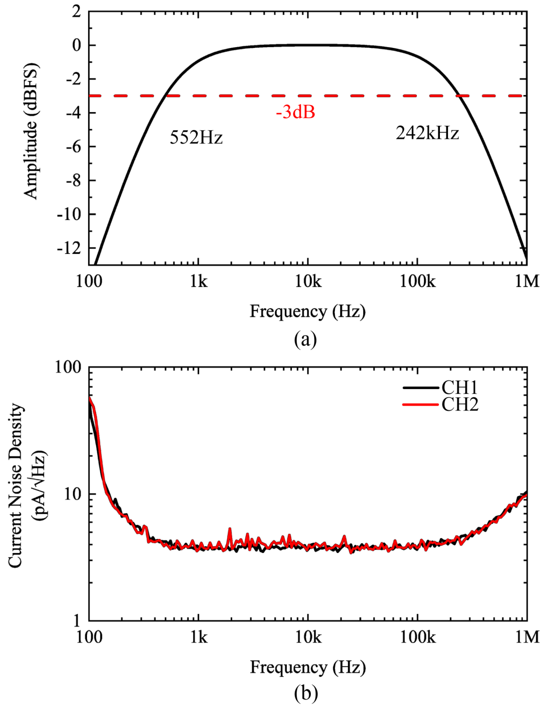

FIGURE 4. **(a) Bandwidth of the low-noise signal read-out circuit. (b) Equivalent input noise of the circuit.**

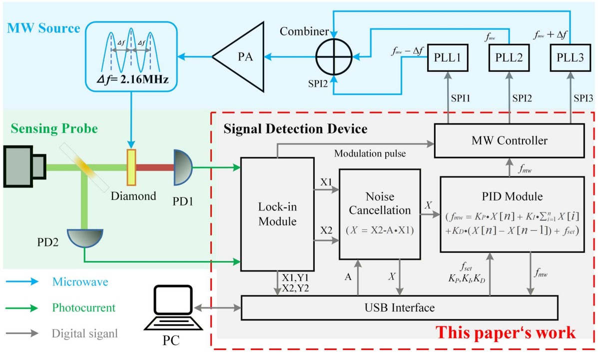

FIGURE 5. **Hardware connection of the low power consumption N-V quantum magnetometer.**

The test result for the bandwidth of the reported circuit is shown in Fig. 4(a). As the input signals from the N-V magnetometer is modulated with kHz frequency signals, the TIA is designed with a −3-dB bandwidth of 522 Hz–242 kHz. The upper limit of the pass-band is determined by the LPF located at the front terminal of the ADC, and the lower limit is contributed by the DC block capacitor located at the output terminal. Fig. 4(b) shows the equivalent input noise of the circuit. The equivalent input noise is measured by collecting the output of the circuit for 10 s, with the input terminal not connected and with sweeping the demodulating signal frequency of the digital signal generation unit inside the FPGA [14], [48]. Both the two input channels are tested and a 3.7 pA/Hz$^{1/2}$ low-equivalent input current noise has been obtained at 8333 Hz. The 3.7-pA/Hz$^{1/2}$ current noise corresponds to a 3.7 pA × 2 kΩ × 60 = 444 nV/Hz$^{1/2}$ output voltage noise, which is consistent with the theoretical analysis in Section III.

As the noise characteristic has been obtained, the circuit has also been applied in a low power consumption N-V quantum magnetometer [31] to verify the capacity of signal read-out, and Fig. 5 shows the hardware connection of the N-V platform. A permanent magnet array made from neodymium iron boron is used to provide the bias field for the sensing probe, and the resonance frequencies of the four N-V axes are separated. The N-V centers in the diamond are excited by a 532-nm green laser, and then generate red fluorescence. The PD converts the fluorescence signals to current signals which are measured by the reported circuit. A beam splitter is implemented to split a fraction of the laser beam for laser noise cancellation. The MW source is used to generate MW signals with three frequency components which are used to control the spin stage of the N-V centers. The three-frequency MW is driven by a power amplifier and has a frequency difference of 2.16 MHz. Such solution can excite all the three hyperfine transitions of N-V simultaneously to enhance ODMR contrast and can further enhance the sensitivity of the magnetometer [31], [49]. The MW controller configures the three phase-locked loops (PLL) to generate the three-frequency MW, and a two-level frequency modulation is applied to the three PLLs. The signal read-out circuit is implemented to measure the output fluorescence current signals from the N-V centers, to realize digital processing for laser noise cancellation, and to achieve the PID control for the MW source.

Fig. 6 shows the experimental results of applying the reported circuit in the low power consumption N-V quantum magnetometer. The continuous wave spectrum in Fig. 6(a) is measured with the ODMR method [50]. The spectrum is obtained by acquiring the demodulated signal from the

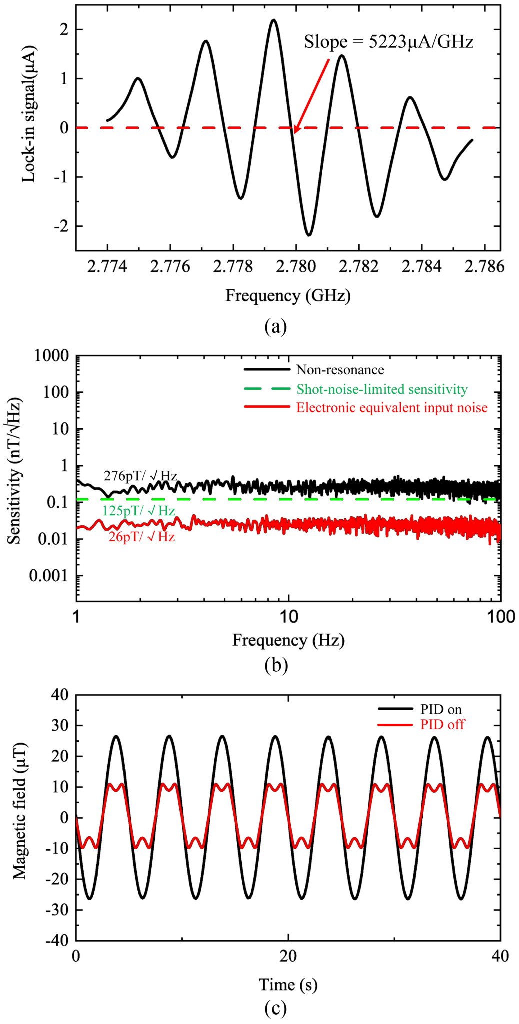

FIGURE 6. **Experimental results of applying the low noise signal read-out circuit in the low power consumption N-V quantum magnetometer. (a) Continuous wave spectrum. (b) Spectrum of sensitivity. (c) Measured magnetic field with and without PID operating.**

lock-in module with sweeping the MW frequency. The slope at the central zero point of the continuous wave spectrum equals 5223 μA/GHz, and it can be used to further calculate the magnetic sensitivity of the N-V magnetometer. Fig. 6(b) shows the magnetic sensitivity spectrum, which is obtained with a low laser power of 70 mW. As the laser has a 7% efficiency, the total power consumption of the applied laser is 1 W, and the low laser power impose minimal heat dissipation requirements on the system. The sensitivity spectrum is obtained by measuring the system noise floor of the N-V magnetometer, and a fast-Fourier-transform (FFT) is applied to transform the time-domain data into frequency-domain data. The FFT results divided by the product of the slope S in Fig. 6(a) and the constant of electron gyromagnetic ratio $\gamma = 28$ Hz/nT [3], can be considered as the magnetic sensitivity [31], [51]. The black line in Fig. 6(b) shows that a 276 pT/Hz$^{1/2}$ magnetic sensitivity can be obtained with a low laser power under nonresonance condition. The green line is the shot-noise-limited sensitivity 125 pT/Hz$^{1/2}$, which is determined by the N-V system and is the theoretical limit of the magnetic sensitivity [42]. The red line is the equivalent noise floor contributed by the reported circuit. A 3.7-pA/Hz$^{1/2}$ input current noise contributes to a 26-pT/Hz$^{1/2}$ low magnetic measurement noise, which is much lower than the N-V system noise. The utilization of low-power laser contributes to the reduction of both the photocurrent signal strength and the noise floor of the N-V platform, and imposes stricter requirements on the noise performance of the signal read-out circuit. Therefore, the low-noise circuit has a negligible contribution to magnetic sensing, and has a considerable advantage in low noise signal read out. To verify the functionality of the PID controller, the magnetometer was used to measure an alternating sinusoidal external magnetic field. With the PID controller disabled, the measured magnetic field can be expressed as

$$B = \frac{X}{\gamma S} \tag{10}$$

where X is the output of the lock-in module after noise cancellation, γ is the electron gyromagnetic ratio, and S is the slope in Fig. 6(a); with the PID controller enabled, the external magnetic field can be expressed as [27]

$$B = \frac{f_{\mathrm{mw}} - f_{\mathrm{set}}}{\gamma} + \frac{X}{\gamma S}. \tag{11}$$

Fig. 6(c) shows the result of the application of PID module when the sensing probe is used to measure a sinusoidal alternating external magnetic field which is generated by a coil. The result shows the application of PID has a significant effect on extending the dynamic range of the N-V magnetometer, and signal distortion can be avoided.

V. DISCUSSION

A. PCB ROUTING AND LAYOUT

The PCB routing and layout for the reported circuit should be optimized for achieving a low-noise design. The amplifiers are routed with short lines to minimize signal loss, and a solid ground plane is located under the analog layer to eliminate the crosstalk as well as the effect of environment noise. The power and ground planes for the analog circuits and the digital circuits are isolated to suppress the digital noise coupling into analog circuits. Capacitors are placed as close as possible to the power supply pin of the chips, and therefore bypass paths to ground can be implemented to eliminate the coupled noise from power sources. Via holes connected with analog ground are mounted nearby the analog signal lines to reduce parasitic capacitance and inductance. In order to reduce crosstalk and parasitic coupling, the length of signal lines is minimized.

B. TRANS-IMPEDANCE AND PARASITIC CAPACITANCE

According to (8), increasing the value of the trans-impedance can reduce the equivalent input current noise, whereas the

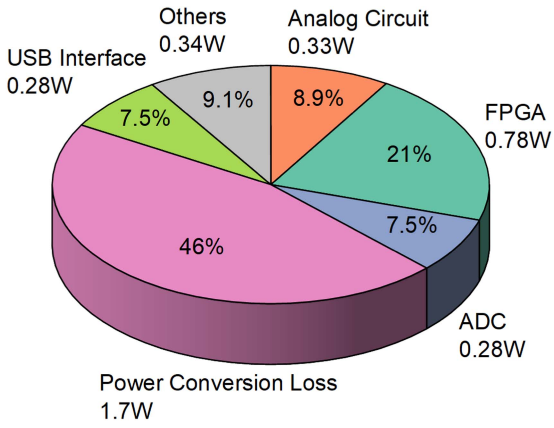

FIGURE 7. Chart of the circuit's power consumption.

TABLE 2. Comparison with Other Studies

Parameter	This work	2023 [22]	2023 [23]	2023 [27]	2024 [24]	2024 [25]	2024 [26]
Power consumption	3.72 W	N/A	N/A	5.7 W	N/A	10.33W	N/A
Input current noise (pA/Hz$^{1/2}$)	3.7 @8.3 kHz (2 kΩ)	N/A	N/A	25 @3 kHz (2 kΩ)	N/A	20 @1 kHz (1 kΩ)	20 @6.2 kHz (10 kΩ)
Input voltage noise of LIA (μV/Hz$^{1/2}$)	0.44 @8.3 kHz	8.77 @30 kHz	7.3 @floor	N/A	205 @1 kHz	N/A	N/A
Magnetic Sensitivity (pT/Hz$^{1/2}$)	276	2800	750	N/A	3000	9520	9.4(^{12}C enriched diamod)
Laser Power	70 mW	0.3 W	0.4 W	N/A	0.39 W	N/A	0.45 W
PID control	Yes	N/A	Yes	Yes	No	Yes	No
Footprint	9.6×3.7 cm	N/A	N/A	18×12 cm	13×26 cm	30×25 cm	N/A

output amplitude of the TIA will also be increased. In order to limit the signal amplitude to avoiding exceeding the circuit operating voltage range, the trans-impedance of the first stage amplifier is set to 2 kΩ considering that the current of the signal from N-V platform is around 2 mA. Decreasing the value of the parasitic capacitance is also helpful to realize a low-noise design, and therefore the implementation of low parasitic capacitance photoelectric conversion circuit is also meaningful.

C. POWER CONSUMPTION

Fig. 7 shows the pie chart of power consumption for the reported circuit. The 0.78-W power consumption for FPGA logics is provided by the developing software. The power consumptions for ADC, USB interface, and analog circuits are obtained from the datasheets. The power module for the circuit has a 1.7-W power conversion loss to generate power supply with required voltages for the chips in the circuit. The other 0.34-W power consumption is contributed by the flash memory, the status indicator, and the other peripheral circuits. The total power consumption is 3.7 W, and a more efficient solution for power supply can be performed to reduce the power conversion loss in the future studies.

D. COMPARISON WITH LATEST STUDIES

Table 2 shows the comparison between this work and the latest studies. The equivalent input current noise is not provided in some of the references, whereas the input voltage noise can be obtained according to the CW-ODMR spectrum and the electric noise floor. The voltage noise equals the product of central slope of the CW spectrum, the gyromagnetic ratio of electron, and the electric floor. The current noise of [25] is provided by the datasheet of the used TIA. Compared with those signal read-out circuits used in other studies, the reported circuit has significant advantages in noise performance, power consumption, and overall size, and demonstrates significant advantages for application in low power consumption N-V magnetometer. The authors in [26] showed the implementation of an N-V magnetometer with ^{12}C enriched diamond N-V samples, and a high sensitivity can be achieved as the sample contributes to a much sharper CW slope. In future studies, the magnetic sensitivity of our compact N-V magnetometer can be further improved by replacing the used diamond with ^{12}C enriched samples. Due to the superior noise performance under low-power operation, this work can advance the N-V quantum magnetic sensing technology toward practical application.

VI. CONCLUSION

In this article, we report a signal read-out circuit, which is featured by its low noise, compact footprint, and low power consumption. The circuit is designed to be applied in the low power consumption N-V center-based quantum magnetometer. According to the experimental results, the superior performance noise of the circuit enables it to introduce negligible measurement errors in weak-signal detection scenarios. In future studies, a chip-scale design can be studied to further integrate and optimize the circuit, and the power consumption can also be reduced.

APPENDIX: DERIVATION OF NOISE IN THE SIGNAL READ-OUT CIRCUIT

The noise of the signal readout circuit is mainly derived from the three-stage amplifier circuit and the ADC.

A. NOISE OF THE THREE-STAGE AMPLIFIER

The noise of the amplifier circuit is mainly composed of the inherent noise of the operational amplifier chip as well as the thermal noise of external resistors, and these noises are added in the form of a sum of squares [43]. The derivation process of the output noise of each stage in the three-stage amplifier circuit is as follows.

1) NOISE OF THE TRANS-IMPEDANCE AMPLIFIER

Fig. 8 shows the noise sources in the TIA. The inherent noise of the amplifier chip can be described by the input current noise I_{noise1} as well as the input voltage noise V_{noise1}, and they are independent noise sources. $\sqrt{4kTR_T}$ and $\sqrt{4kTR_D}$ are the thermal noises of R_T and R_D.

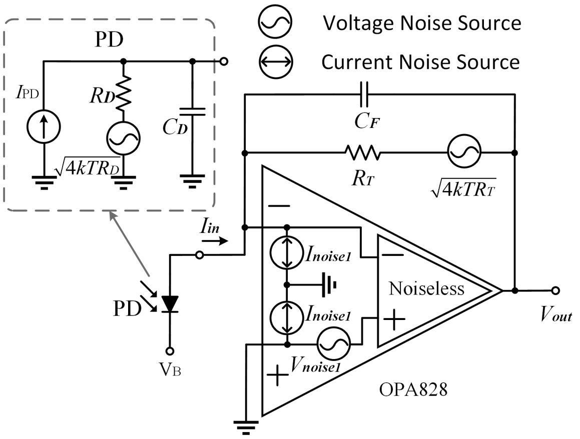

FIGURE 8. Noise sources of the TIA.

To calculate the total noise of an operational amplifier, the output noises contributed by each noise source are calculated separately, and then are summed up together.

For the input voltage noise source V_{noise1}, the circuit is equivalent to a noninverting amplifier with a gain of

$$NG_{11} = \left|1 + \frac{Z_F}{Z_D}\right| = \left|1 + \frac{(1/sC_F)||R_T}{(1/sC_D)||R_D}\right| \tag{12}$$

where $s = j2\pi f$ and j is the imaginary unit. Considering that f is at kHz level, the impedance of R_D is much larger than that of R_T, C_D, and C_F. Hence, R_D can be ignored and the NG_{11} can be simplified

$$\begin{aligned} NG_{11} &\approx \left|1 + \frac{(1/sC_F)||R_T}{(1/sC_D)}\right| \\ &= \left|1 + \frac{sR_TC_D}{1 + sR_TC_F}\right| \\ &= \left|\frac{1 + j2\pi f R_T(C_F + C_D)}{1 + j2\pi f R_T C_F}\right|. \end{aligned} \tag{13}$$

According to the values in Table 1, the approximate condition $2\pi f R_T C_F \ll 1$ can be obtained and (13) can be further simplified as

$$NG_{11} \approx |1 + j2\pi f R_T(C_F + C_D)|. \tag{14}$$

Therefore, the output noise contributed by V_{noise1} is

$$V_{\text{noise1}} \cdot NG_{11} = \sqrt{V_{\text{noise1}}^2 + [2\pi f\,(C_F + C_D)\,V_{\text{noise1}} R_T]^2}. \tag{15}$$

The current noise source I_{noise1} at the noninverting input makes no contribution to the output, since it is directly bypassed to ground. The current noise source I_{noise1} at the inverting input is equivalent to the TIA input signal, giving it a gain of R_T. For the thermal noise source $\sqrt{4kTR_D}$, the circuit is equivalent to an inverting amplifier with a gain of $-R_T/R_D$. The thermal noise source $\sqrt{4kTR_T}$ contributes directly to the output noise.

TABLE 3. Contributions of Noise Sources in the TIA

Noise source	Contribution
Noninverting I_{noise1}	0
Inverting I_{noise1}	$R_T \cdot I_{noise1}$
V_{noise1}	$V_{noise1} \cdot \lvert 1 + j2\pi f R_T(C_F + C_D) \rvert$
$\sqrt{4kTR_D}$	$-\sqrt{4kTR_D} \cdot R_T / R_D$
$\sqrt{4kTR_T}$	$\sqrt{4kTR_T} \cdot 1$

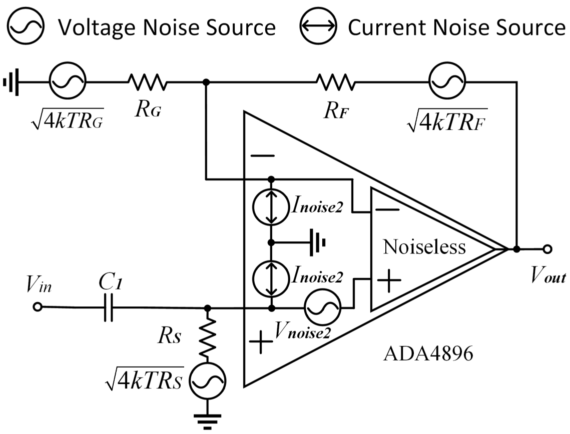

FIGURE 9. Noise sources of the noninverting amplifier.

Table 3 lists the noise contributions of each noise source in the TIA.

By summing up each item, the output noise of the TIA can be obtained as

$$\begin{aligned} N_1 &= \sqrt{\begin{array}{l}\left(\sqrt{4kTR_T}\right)^2 + \left[\sqrt{4kTR_D} \cdot \left(\frac{R_T}{R_D}\right)\right]^2 + (R_T I_{\text{noise1}})^2 \\ + [V_{\text{noise1}} \cdot |1 + j2\pi f\,(C_D + C_F)\,R_T|]^2 + 0^2\end{array}} \\ &= \sqrt{\begin{array}{l}(R_T I_{\text{noise1}})^2 + V_{\text{noise1}}^2 + 4kTR_T + 4kTR_D\left(\frac{R_T}{R_D}\right)^2 \\ + [2\pi f\,(C_D + C_F)\,V_{\text{noise1}} R_T]^2\end{array}}. \end{aligned} \tag{16}$$

2) NOISE OF THE NONINVERTING AMPLIFIER

Fig. 9 shows the noise sources in the noninverting amplifier. I_{noise2} and V_{noise2} are the inherent noise sources of the amplifier chip. $\sqrt{4kTR_S}$,$\sqrt{4kTR_G}$, and $\sqrt{4kTR_F}$ represent the thermal noise of R_S, R_G, and R_F, respectively.

For the voltage noise source V_{noise1} and$\sqrt{4kTR_S}$, the circuit is equivalent to a noninverting amplifier with a gain of $1{+}R_F/R_G$. The current noise source I_{noise2} at the noninverting input will generate a voltage noise via R_S and then be amplified by the equivalent noninverting amplifier. Hence, the gain of the noise source I_{noise2} at the noninverting input is $R_S(1{+}R_F/R_G)$. The current noise source I_{noise2} at the inverting input generates a voltage noise via $R_F||R_G$, and then is amplified by a factor of $1{+}R_F/R_G$. Therefore, the gain of the current noise source I_{noise2} is $(R_F||R_G) \cdot (1 + R_F/R_G) = R_F$. The circuit is equivalent to an inverting amplifier for the noise

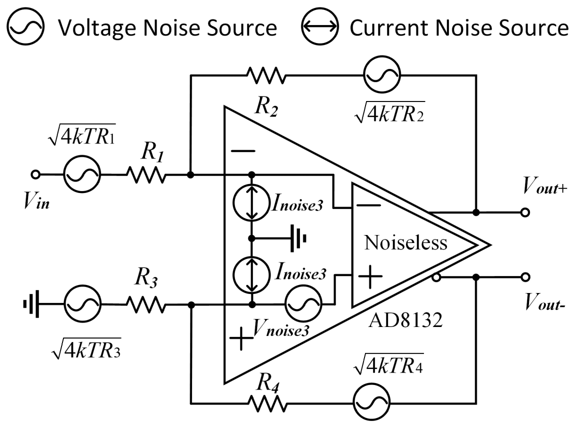

FIGURE 10. Noise sources of the differential amplifier.

TABLE 4. Contributions of Noise Sources in the Noninverting Amplifier

Noise source	Contribution
Noninverting I_{noise2}	$I_{noise2} \cdot R_S(1+R_F/R_G)$
Inverting I_{noise2}	$R_F \cdot I_{noise2}$
V_{noise2}	$V_{noise2} \cdot (1+R_F/R_G)$
$\sqrt{4kTR_S}$	$\sqrt{4kTR_S} \cdot (1+R_F/R_G)$
$\sqrt{4kTR_G}$	$-\sqrt{4kTR_G} \cdot R_F/R_G$
$\sqrt{4kTR_F}$	$\sqrt{4kTR_F}$

source $\sqrt{4kTR_G}$ and the gain is $-R_F/R_G$. The noise source $\sqrt{4kTR_F}$ contributes directly to the output.

Table 4 lists the contributions of each noise source in the noninverting amplifier.

By summing up each item, the output noise of the noninverting amplifier can be obtained as

$$N_2 = \sqrt{\begin{aligned}&\left[R_S I_{\text{noise2}}\left(1+\frac{R_F}{R_G}\right)\right]^2+(R_F I_{\text{noise2}})^2\\&+\left[V_{\text{noise2}}\left(1+\frac{R_F}{R_G}\right)\right]^2+\left[\sqrt{4kTR_S}\left(1+\frac{R_F}{R_G}\right)\right]^2\\&+\left[-\sqrt{4kTR_G}\left(\frac{R_F}{R_G}\right)\right]^2+\left(\sqrt{4kTR_F}\right)^2\end{aligned}}$$

$$= \sqrt{\begin{aligned}&\left[(R_S I_{\text{noise2}})^2+V_{\text{noise2}}^2+4kTR_S\right]\left(1+\frac{R_F}{R_G}\right)^2\\&+(R_F I_{\text{noise2}})^2+4kTR_F+4kTR_G\left(\frac{R_F}{R_G}\right)^2\end{aligned}}. \quad (17)$$

3) NOISE OF THE DIFFERENTIAL AMPLIFIER

Fig. 10 shows the noise sources in the differential amplifier. I_{noise3} and V_{noise3} are the inherent noise sources of the amplifier chip. $\sqrt{4kTR_1}$,$\sqrt{4kTR_2}$,$\sqrt{4kTR_3}$ and $\sqrt{4kTR_4}$ represent the thermal noise of R_1, R_2, R_2 and R_4.

Similar to the current noise source I_{noise2} at the inverting input of the noninverting amplifier, the current noise I_{noise3} at the inverting and noninverting inputs are amplified by the resistors R_2 and R_4. According to the resistive voltage division principle, the voltage noise V_{noise3} is amplified by a gain of $1+R_2/R_1$(or$1+R_4/R_3$, noting that $R_4/R_3 = R_2/R_1$), whereas $\sqrt{4kTR_1}$ and$\sqrt{4kTR_3}$ are amplified with gains of $-R_2/R_1$ and$-R_3/R_4$. The voltage noises $\sqrt{4kTR_1}$ and$\sqrt{4kTR_3}$ contribute to the output directly.

TABLE 5. Contributions of Noise Sources in the Differential Amplifier

Noise source	Contribution
Noninverting I_{noise3}	$R_4 \cdot I_{noise3}$
Inverting I_{noise3}	$R_2 \cdot I_{noise3}$
V_{noise3}	$V_{noise3} \cdot (1+R_2/R_1)$
$\sqrt{4kTR_1}$	$-\sqrt{4kTR_1} \cdot (R_2/R_1)$
$\sqrt{4kTR_2}$	$\sqrt{4kTR_2}$
$\sqrt{4kTR_3}$	$-\sqrt{4kTR_3} \cdot (R_4/R_3)$
$\sqrt{4kTR_4}$	$\sqrt{4kTR_4}$

Table 5 lists the contributions of each noise source in the differential amplifier.

By summing up each item, the output noise of the differential amplifier can be obtained as

$$N3 = \sqrt{\begin{aligned}&(R_2 I_{\text{noise3}})^2+(R_4 I_{\text{noise3}})^2+\left[V_{\text{noise3}}\left(1+\frac{R_2}{R_1}\right)\right]^2\\&+\left[-\sqrt{4kTR_1}\left(\frac{R_2}{R_1}\right)\right]^2+\left(\sqrt{4kTR_2}\right)^2\\&+\left[-\sqrt{4kTR_3}\left(\frac{R_4}{R_3}\right)\right]^2+\left(\sqrt{4kTR_4}\right)^2\end{aligned}}$$

$$= \sqrt{\begin{aligned}&(R_2 I_{\text{noise3}})^2+(R_4 I_{\text{noise3}})^2+4kTR_1\left(\frac{R_2}{R_1}\right)^2+4kTR_2\\&+4kTR_3\left(\frac{R_4}{R_3}\right)^2+4kTR_4+V_{\text{noise3}}^2\left(1+\frac{R_2}{R_1}\right)^2\end{aligned}}. \quad (18)$$

B. NOISE OF THE ANALOG-TO-DIGITAL CONVERTER

The noise of an ADC can be characterized by quantization noise and transition noise. The quantization noise originating from finite resolution is an inherent noise of the ADC. Transition noise is mainly caused by the nonideal characteristics of the internal electronic components of the ADC. The transition noise and quantization noise can be estimated as noise uniformly distributed within the Nyquist bandwidth ($f_s/2$, where f_s is the sampling rate) of the ADC [45], [46], [47].

Given the RMS transition noise N_{trans}, RMS quantization noise N_{quant}, and the average noise density N_{ADC} in the Nyquist bandwidth of ADC, the relationship among the three can be described as follows:

$$N_{\text{trans}}^2 + N_{\text{quant}}^2 = \int_0^{f_s/2} N_{\text{ADC}}^2 df = N_{\text{ADC}}^2 \cdot (fs/2). \quad (19)$$

According to (19), the noise of the ADC can be calculated as

$$N_{\mathrm{ADC}} = \sqrt{N_{\mathrm{trans}}^2} + N_{\mathrm{quant}}^2/\sqrt{f_s/2}. \tag{20}$$

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