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DESIGN AND EXPERIMENTAL RESULTS OF A 1.1KA/800V AC POWER SUPPLY FOR SIRIUS BOOSTER DIPOLES

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Abstract

Sirius is a 4th generation synchrotron light source designed and being built by Brazilian Synchrotron Light Laboratory (LNLS), with first beam scheduled for 2019. Approximately one thousand power supplies (PS) will be needed to feed all the magnets, from which 57 are used to operate the booster injector.

The two booster dipole PS are the most complex, not only due to their higher current (1.1 kA), voltage (800 V) and power (333 kW) output, but also because the current must follow a quasi-triangular waveform, from a value close to zero to almost the maximum in 320 ms and at a repetition rate of 2 Hz.

Due to the high output values, each PS is formed by two sets in parallel of 4 modules in series, totalling 8 modules with 550 A / 200 V output each.

In order to reduce the 2-Hz effect in the grid, each module has two main stages. The input stage has the function to regulate the average voltage in a capacitor bank consuming a constant RMS current from the grid, which value depends on of the PS average output power. The output stage has the function to transfer the energy from the capacitor bank to the load, with the output current following the reference waveform.

This work describes this PS, showing its topology, some aspects of its design and obtained results.

INTRODUCTION

Sirius is a 4th generation synchrotron light source, designed and been built by Brazilian Synchrotron Light Laboratory (LNLS) in Campinas, Brazil. LINAC and booster (BOO) are already installed, and the storage ring (SR) must be ready in the second semester of 2019 [1].

Due to the top-up injection, booster must have the same maximum energy as the storage ring (3 GeV). This means that the output current of booster main power supplies (PS) must follow a 2-Hz quasi-triangular waveform, going approximately from 5% (that corresponds to 150 MeV, the LINAC energy) to 100% of rated current.

This behaviour justified the design of a third family of PS for Sirius, called FAC, used to feed booster dipoles, quadrupoles and sextupoles. Other two families are described in [2].

Despite this family embraces only 6 units, as showed in Table 1, it is the most complex due to its ramping requirements and to prevent the effect of this in the grid, what required multiple stages. Moreover, booster dipole PS operates at the highest current and voltage among all Sirius PS. Figure 1 shows one of these PS.

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Table 1: FAC Maximum Output Values and Quantities

	PS Qt	Io [A]	Vo [V]	Mod/ PS	Max Load R [Ω]	Max Load L [H]
Dip	2	1100	800	8	0.333	0.115
QF	1	120	500	2	2.268	0.457
QD	1	30	45	1	0.652	0.130
Sext	2	150	45	1	0.254	0.002

Figure 1: One of booster dipole PS.

BOOSTER DIPOLE PS DESCRIPTION

Due to the high voltage required to feed all dipoles with a single PS, they were divided in 2 units. Each PS feeds one coil of each dipole in a series association, alternating superior and inferior coils. Moreover, to decrease the rates in power electronic components (semiconductors, capacitors, inductors, etc.) and facilitate replacements, a modular structure was adopted. The last column in Table 1 shows the quantity of modules used in each PS.

The module was designed for a maximum output values of 550 A, 250 V, 45 kW. For dipole PS there are 2 sets in parallel with 4 modules in series each one. The medium point of one series association is earthed, what limits the maximum voltage related to earth in a dipole to half of output voltage. Moreover, this prevents the need to use high voltage cables to connect the magnets.

The current distribution between modules in parallel is controlled, but the voltage among modules was not necessary.

A first prototype (130 A, 18V) using a single module was built in 2014 and used to test some QF quadrupoles [3]. In 2016 a second one (1.1kA, 70V) was built, already using 2 modules in parallel, to measure booster dipoles.

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Two 300 kVA transformers with four secondaries each (300 V) are used to feed all 8 modules independently. The secondary phases are 15 degrees shifted in relation to one each other, to emulate a 24-pulse rectifier.

MODULE DESCRIPTION

This section describes the three stages that constitute a FAC module, which structure is showed in Fig. 2.

Command and Rectifier

The Command Stage (CMD) has the function to connect the triphasic input to the rectifier, when a turn-on signal is received. A pre-charge circuit initially puts resistors in the way to decrease the inrush current.

The rectifier stage (RECT) consists of a triphasic diode bridge with a second order damped filter, and its output is connected to the Input Stage (IS) to feed it. The rectifier bridge heatsink and the inductor are water-cooled.

Input Stage and Capacitor Bank

A Capacitor bank (CB) is used to absorb the load energy variations when ramping. It was specified to operate with a peak-to-peak voltage variation lower than 10%.

The Input Stage (IS) has the double function of keep the average value of CB voltage close to the reference (250V) and attenuate as much as possible the 2-Hz harmonics in the AC input current.

The IS consists basically in a Buck converter with a LC filter, where the CB is the capacitance. Its input current and output voltage are fed back to the control circuit.

The IGBT heatsink and the inductor are water-cooled.

Output Stage

The Output Stage (OS) is responsible to provide current to load, tracking the reference within specifications. It is based on a H-bridge topology with a second order damped filter. Unipolar switching is used to have an output ripple with twice the switching frequency, which is 12 kHz. The PWM signals of the 4 series modules are also shifted among them, what results that the output ripple frequency is 96 kHz.

CONTROL

The controller hardware and firmware used on FAC family is the same of all Sirius PS [2, 4], called Digital Regulation System (DRS), configured with dedicated parameter settings. OS and IS have independent control.

Output Stage Control

A master crate is used to control all the OS, since it has 16 High Resolution PWM (HRPWM). Each OS receives 2 PWM signals, and its driver board generates the other 2 complementary signals.

Output current is measured with 2 high precision DCCTs (ITZ2000, from LEM®), one connected in each side of PS output, and converted to digital by the DRS high-resolution ADC (HRADC, 18 bits, 600 kSPS). The average value of these two measurements is used to calculate the output current error, which is applied to a proportional-integral (PI) compensator.

In order to decrease the tracking error, reference feedforward is applied to PI output. Input feedforward is also necessary, since the CB voltage have a relatively high variation. These voltages are measured with Isoblock transductors from Verivolt® and the 12-bits ADCs of DRS Universal Digital Controller (UDC) board.

Reference is received in 32-bit floating-point representation at 4 kHz sampling rate, which results in 8000 points per ramp cycle.

The current in each arm of PS is measured using medium precision DCCTs and HRADCs and are compared to obtain a compensating signal which decreased the duty cycle of one arm and increases of the other.

The master crate is also responsible for the main communication with the high-level control system, to manage the IHM and to communicate with OS modules diagnostics electronics.

Input Stage Control

Four slave crates are used to control the IS, each one responsible for 2 IS. Two control loops are implemented:

- Output voltage loop: this loop controls the average value of CB voltage, which is feedbacked by Isoblock transductors and HRADCs. The PI compensator is calculated with 0.55 Hz bandwidth and 2 notch filters (2-Hz and 4-Hz) allow the 2-Hz variation in this voltage and provide enough response time.
- Input current loop: the reference for this control loop is the output of the previous one. The IS input current is measured with Hall transductors and HRADCs, and digitally filtered, due to switching frequency harmonics. A PI compensator allows the average value of this current (within a 2-Hz cycle) to follow very close the reference, while 2 resonant controllers (2-Hz and 4-Hz) provide more gain to attenuate 2-Hz harmonics.

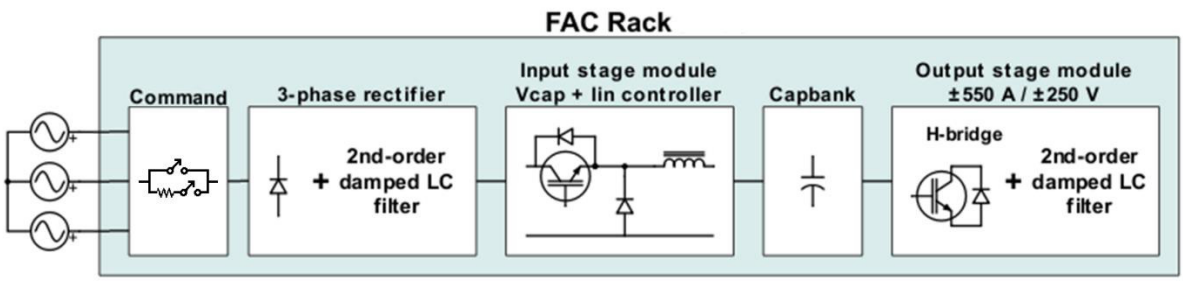

Figure 2: FAC module structure.

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EXPERIMENTAL RESULTS

Both dipole PS were tested before the installation at lower rates, due to load and grid limitations. Figure 3 shows some waveforms for a 0 to 380 A output current ramp. The FFT of the IS current shows the reduction of the 2-Hz and 4-Hz components due to notch filters and resonant controllers.

Tests after installation at Sirius are still in progress, but some results are already available.

Figure 4 shows the load and two arms currents during a 0 to 1.1 kA ramp. Despite of the control of this current distribution can still be improved, the difference between them was lower than 28A, what is only 2.5% of output rated current.

Figure 5 shows the output voltages of the 4 modules of one arm during the same ramp (0 to 1.1 kA). It can be noted that they are close enough, which makes voltage distribution control unnecessary.

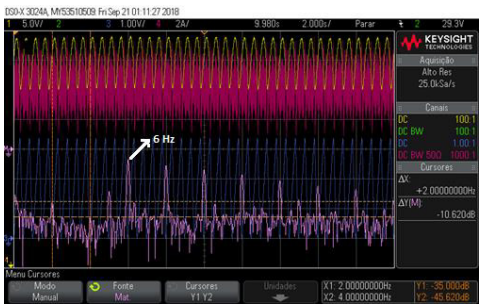

Figure 3: Measurements in laboratory for a 0 to 380 A ramp: Ch1: CB voltage (5V/div), Ch3: Load current (112.5A/div), Ch4: IS input current (5A/div), Math: Ch4 FFT (20dB and 2Hz/div).

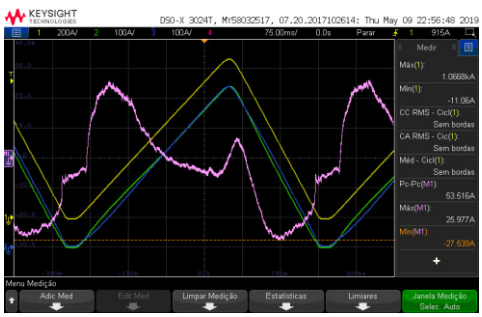

Figure 4: Currents during a 0 to 1.1 kA ramp: Ch1: Load current (200A/div), Ch2 and Ch3: arm currents (110A/div), Math: Ch2-Ch3 (10A/div).

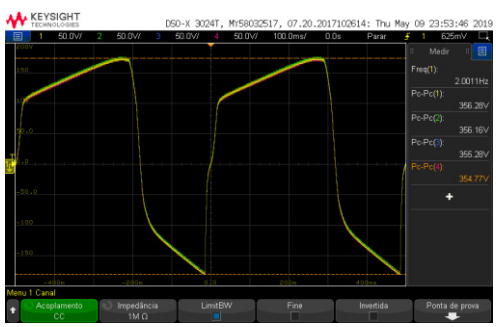

Figure 5: Module output voltages during a ramp (50V/div).

Figure 6 shows the CB voltage and IS input current during a typical demagnetization ramp. It can be observed that the CB voltage has a drop in the beginning of ramp sequence, as well as an increase at the end. This is caused by the slow response of input current control loop. Despite of this, there are no visible deformation in the load current, since the feedforward prevent this.

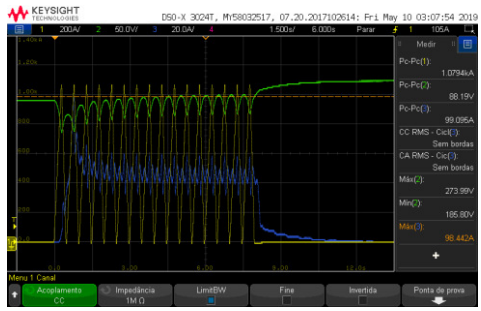

Figure 6: A typical demagnetization ramp: Ch1: load current (200A/div), Ch2: CB voltage (50V/div), Ch3: IS input current (20A/div).

OTHER BOOSTER PS

The QF quadrupole PS is very similar to the dipole PS but using only 2 modules in series. The CB is different because operates with a higher voltage (300V). It is fed by a single 60 kVA transformer with 2 secondaries (380 V) with a 30 degrees displacement, emulating a 12-pulse rectifier.

The sextupoles and QD quadrupoles PS use a single OS each one. They shared the same CB, different from the other PS due to their lower voltage (60V). Instead of an IS, an off-the-shelf PS with current limitation is used.

CONCLUSION

All booster PS were successfully installed, and the measurements already performed showed good results. Other measurements are in progress and soon the PS must be completely characterized.

In this moment they have been used for subsystems commissioning.

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