

ANALYZING SUDDEN BEAM LOSS IN THE SuperKEKB/Belle-II EXPERIMENT WITH RFSoC TECHNOLOGY

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Abstract

In the SuperKEKB/Belle-II experiment, new physics searches are being carried out by colliding 4GeV positrons with 7GeV electrons. The experiment aims to significantly enhance luminosity, targeting an increase to 100 times the current level. However, achieving this goal is challenged by a recurrent issue known as "Sudden Beam Loss" event, where the beam abruptly disappears within tens of microseconds. The cause of this event remains unidentified. To diagnose and debug these sudden beam loss events, a new Bunch Oscillation Recorder (BOR) has been developed, utilizing the Radio Frequency System on Chip from AMD/Xilinx. The BOR measures and records the beam position bunch-by-bunch just before the beam abort and enable detailed analysis of Sudden Beam Loss.

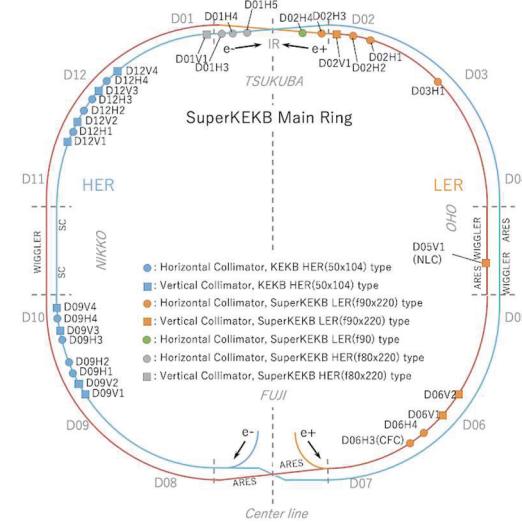
INTRODUCTION

The SuperKEKB accelerator [1] collides electrons and positrons at very high luminosity, providing large quantities of B mesons, tau particles, and other charged particles for the Belle II detector. The accelerator consists of a 7 GeV electron storage ring (HER) and a 4 GeV positron storage ring (LER). By adopting a nanobeam scheme, the beam size at the collision point was narrowed down to a small size, and the world's highest luminosity record, $4.65 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, was achieved in 2022. 31 collimators, equipped in both rings and depicted in Fig. 1, protect the Belle II detector from unwanted beam losses. The accelerator resumed operations in February 2024 after its first long shutdown (LS1) of more than a year. We are operating towards even higher luminosity, but a phenomenon called Sudden Beam Loss is hindering luminosity improvement.

SUDDEN BEAM LOSS

The Sudden Beam Loss (SBL) event is presently the biggest obstacle to increasing luminosity at SuperKEKB [2]. SBL events have caused cracks in accelerator components such as collimators, damage to the Belle II detector, and quenches in the superconducting focusing system. Figure 2 shows how the SBL events have scraped the collimator head. We found, even empirically, that the higher the stored current, the more frequently SBL events occur, followed by severe damage. Thus, we hesitate to increase the stored current as anticipated, hindering the increase in instantaneous luminosity. In addition, once the SBL events occur, leading to beam aborts or the superconducting system quenching, recovery to regular beam operation takes several hours or a day. Therefore, SBL events become a

severe issue in SuperKEKB because they limit the accumulation of integral luminosity and increase instantaneous luminosity. Nevertheless, the cause of the SBL event and the location of its occurrence have yet to be identified.



RF SYSTEM ON CHIP

We proceeded with the new BOR R&D using a novel chip called an RF System on Chip (RFSoC) made by AMD/Xilinx [3]. RFSoC integrates ADC, DAC, FPGA, and CPU. We started the R&D first using the ZCU111 RFSoC evaluation board. The ZCU111 evaluation board, equipped with the XCZU28DR, has eight channels of ADCs up to 4096 Msps. An external clock input allows the RFSoC to be synchronized with the SuperKEKB RF clock. PMOD GPIOs receive SuperKEKB abort signals. On the XM500 RFMC daughter board, SMA ports open for ADC inputs and DAC outputs. Four of the eight ADC inputs are for differential signals, and the other four accept single-ended signals. Two of the four single-ended channels are connected to a balun for 10 MHz to 1 GHz (LF), and the remaining two channels are connected to a balun for 1 to 4 GHz (HF).

DEVELOPMENT OF BOR

Circuit Details

One can obtain a bunch position with the ratio of two voltage signals from the button electrodes. Voltage signals need to be measured with enough timing resolution that is finer than the bunch spacing in SuperKEKB larger than four ns. Figure 3 shows a schematic view of the BOR circuit. Here, we assume the vertical position; we calculate the bunch position by dividing the difference between the signals from the electrodes facing each other by their sum and multiplying it by a pre-defined constant. The waveforms from the two facing electrodes pass through a low-pass filter, eliminating high-frequency noise. They are then input into a 180-degree hybrid circuit to extract their sum " Σ " and difference signals " Δ ". Figure 4 (Left) shows the output signals of the hybrid circuit measured by an oscilloscope. Σ and Δ signals are input into the ZCU111 evaluation board. In our usual cases, we used LF baluns on the XM500 daughter board. Through the LF balun, the signal is input into the RFSoC and is digitized by the RF-ADC. Digital signals are sent to the FPGA, where a ring buffer implemented in the FPGA temporarily holds the waveforms. Figure 4 (Right) shows the waveform measured by RFSoC. Since the amplitude of the Δ signal is small, we interleaved a 14 dB amplifier between a 180-degree hybrid circuit and the ZCU111. We take the peak of the dipolar signal for each Σ and Δ and take their ratio for position calculation. The sampling frequency and phase are correctly synchronized with the RF clock to keep locked to the peak of the dipolar signal of successive bunches. The sampling frequency of 4072 MHz is made with the 8-fold multiplication of the SuperKEKB RF frequency 509 MHz. When the PMOD GPIO receives the SuperKEKB abort trigger signal, it issues a fault trigger to a ring buffer. As of the current design, the ring buffer saves waveforms for 12 turns before the abort.

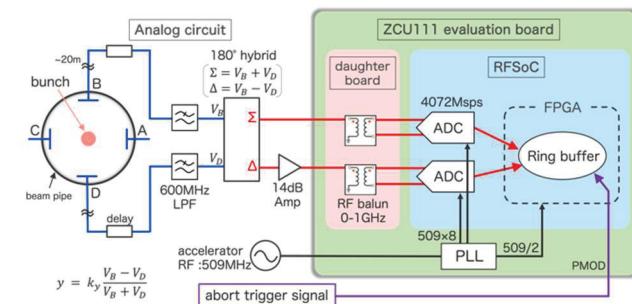


Figure 3: Schematic diagram of the RFSoC-based BOR.



Figure 4: (Left) Hybrid circuit output (yellow is sum and green is difference). (Right) Waveforms measured by RFSoC (blue is sum and orange is difference).

Benchmark

We initially tested the prototype RFSoC-based BOR connecting to two unused button electrodes on the Fuji straight section of the LER. We performed a beam test by making a local beam bump near the Fuji straight section to evaluate the position resolution. In Fig. 5, we see that the calculated positions with RFSoC (vertical axis) agree well with the bump locations (horizontal axis) and an excellent linearity of the overall RFSoC-based system. The standard deviation at each measurement point is about 0.05 mm, which achieves our target performance.

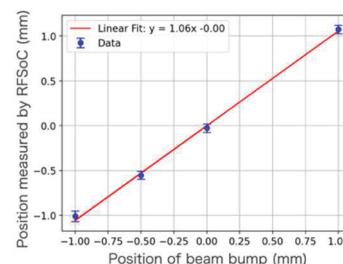


Figure 5: Performance test of position measurement.

SBL OBSERVATION AFTER LS1

An RFSoC-based BOR stayed at the Fuji straight section even after the performance test and has continued the beam abort observation since the end of February 2024. Figure 6 shows the first SBL event recorded using an RFSoC. A 200 ns portion of the beam seems to have been vertically kicked upward about one revolution before the abort. Immediately after the vertical position shift, the beam current starts to be lost. The total current is reduced to about half within one turn. As in Fig. 7, we have observed various types of oscillations and beam losses since the beginning of the data collection process. Our next near-term plan is to install multiple BORs to cover the phase advance widely

and sandwich potential kick source locations. Bunch-by-bunch beam profile measurements, enabled by the currently developing ultrafast monitor, may pinpoint or rule out several SBL mechanism scenarios.

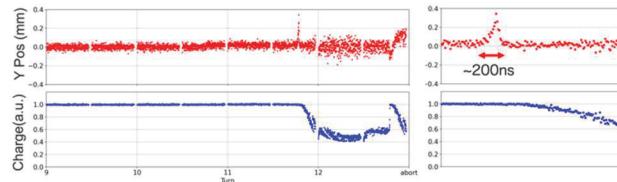


Figure 6: The SBL event recorded with RFSoC (8 March 2024, bunch current~0.33 mA/bunch). Left: Vertical position (upper) and charge (bottom) for the last four turns before the abort. Right: Enlarged view of the spike area.

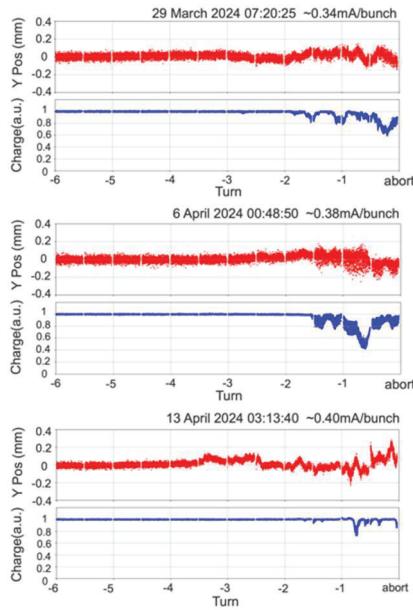


Figure 7: Example of some SBL events.

ANALYSIS

We will introduce two brief analysis results using data of SBL events recorded by the RFSoC-based BOR.

Timing when Oscillation and Charge Loss Start

We analyzed the timing difference between when bunch oscillation and the bunch charge loss start, where the former and latter timing is denoted as " T_{pos} " and " T_{char} ", respectively. The timing analysis proceeds as follows. First, as seen in Fig. 8, we draw a moving average of the vertical position recorded by the BOR (window size is 500 bunches.) The T_{pos} is the bunch index whose moving average line exceeds the ± 0.01 mm threshold. The T_{char} is the bunch index, where the charge decreases by 5%. Figure 9 shows T_{pos} and T_{char} for 65 SBL events; one blue dot corresponds to each event. The area above the red dotted line means bunch oscillations start faster than charge loss. More than 60 SBL events are distributed above the red dotted line. Figure 9 infers that the detection of anomaly bunch oscillation catches early signs of SBL events before the significant charge loss starts.

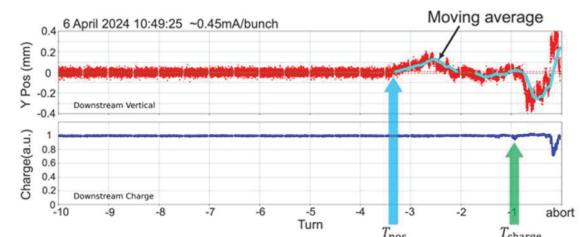


Figure 8: The moving average curve and obtained T_{pos} and T_{char} for the same event in Fig. 6.

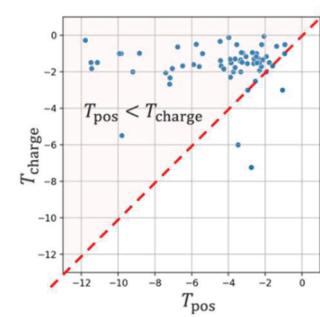


Figure 9: Relation between T_{pos} and T_{charge} for 65 SBL events.

Comparison of the Magnitude of Oscillation at the Two Points

We recorded the bunch oscillations at two points simultaneously using a single RFSoC and compared the magnitude of the oscillation at two locations: point U and point D in the Fuji straight section. At these locations, vertical betatron phases differ by 90 degrees. We introduce the Range value as the magnitude of bunch oscillations, the difference between the maximum and minimum positions of the moving average line seen in Fig. 8. Figure 10 indicates the results of 30 SBL events. SBL events dominantly distribute under the red dotted line, which represents that oscillations at point D are often more significant than at point U. Thus, we expect that some bunch kicks may occur at the location of the betatron phase close to point U. One candidate location is the D06V2 collimator having a narrow vertical aperture. We recently introduced a new RFSoC-based BOR with the evaluation board ZCU208 and installed it downstream of D06V2. We are investigating SBL events further by sandwiching the suspicious collimator section with the two BORs.

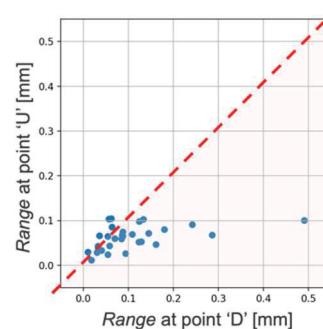


Figure 10: Relation between Range at point U and point D for 30 SBL events.

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- [2] H. Ikeda *et al.*, "Observation of sudden beam loss in SuperKEKB", in *Proc. IPAC'23*, Venice, Italy, May 2023, pp. 716-719. doi:10.18429/JACoW-IPAC2023-MOPL072
- [3] AMD <https://www.xilinx.com/products/silicon-devices/soc/rfsoc.html>