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DEVELOPMENT OF A NEW DIGITAL LLRF SYSTEM FOR HIGH ENERGY PHOTON SOURCE*

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Abstract

A new digital low-level RF (LLRF) system has been developed for the High Energy Photon Source (HEPS), a 6 GeV diffraction-limited synchrotron light source under construction in Beijing. The LLRF system is composed of a digital signal processing board (DSP), two ADC/DAC daughter boards and a RF front-end board. The FPGA of the DSP board has been changed from the original ALTERA Stratix III to Xilinx Zynq-7000 which comes with a versatile Processing System (PS) integrated with a highly flexible and high-performance Programmable Logic (PL) section, all on a single System on Chip (SoC). The control algorithms were implemented in PL section while the EPICS-IOC was running on the embedded Xilinx Linux within the PS. The LLRF system has been tested with a 166.6 MHz mockup cavity in the lab and the RF field inside the cavity can be controlled within +/-0.018% in amplitude error and +/-0.011 degree in phase error (peak to peak). The requirements of HEPS were therefore fulfilled. The hardware design, control algorithms and the test results of the new LLRF system are described in this paper.

INTRODUCTION

High Energy Photon Source (HEPS) is a 6-GeV, 1.3-km, ultralow-emittance storage ring light source currently under construction in Huairou District, northeast suburb of Beijing, China [1,2]. Its main beam parameters are listed in Table 1.

Table 1: Beam Parameters of the HEPS Storage Ring

Parameter	Value	Unit
Circumference	1360.4	m
Beam energy	6	GeV
Beam current	200	mA
ΔE per turn (w/ IDs)	4.14	MeV
Total beam power	850	kW
Main RF frequency	166.6	MHz
Total RF voltage (main)	5.16	MV
3rd har. RF frequency	499.8	MHz
Total RF voltage (HC)	0.91	MV

The layout of the RF system is shown in Fig. 1. Five 166.6 MHz superconducting RF (SRF) cavities will be installed in the storage ring as main accelerating cavities accompanied by two 499.8 MHz SRF cavities as third harmonic cavities. One needs to be noted that the third harmonic system is active rather than passive. Each cavity will be driven by a 260 kW power transmitter adopting solid-state technology. Six 499.8 MHz normal-conducting cavities will be installed in the booster with each driven by a 100 kW solid-state amplifier [3,4]. Its main RF parameters are listed in Table 2.

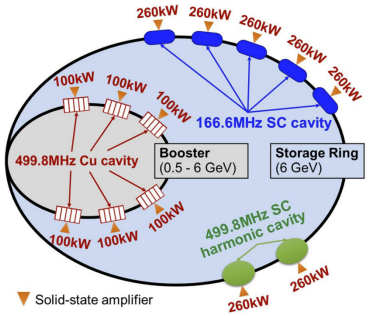

Figure 1: Layout of HEPS RF system.

Table 2: RF Parameters of the HEPS Storage Ring

Parameter	Main RF	Harm. RF
Frequency	166.6MHz	499.8MHz
# of cavities	5	2
Cavity voltage (Vc)	1.2MV	1.75MV
RF power/cavity	180kW	200kW
RF power/SSA	260kW	260kW
Control stability	±0.1% (amp), ±0.1° (phase)	

LLRF system is an important part of the RF system. It is used to maintain the stability of the accelerator cavity field amplitude and phase. We have independently developed the first-generation digital LLRF system based on TCP/IP communication in 2018. It has been successfully applied to the HEPS-TF superconducting cavity horizontal high-power test in 2018 [5] and it has been running steadily for BEPCII RF system since 2019. The hardware of this digital LLRF system mainly includes a digital signal processing board and an RF front-end board. The FPGA of the digital signal processing board adopts Altera's EP3SL150F1152-C2 chip under Stratix III series. At the same time, the board also integrates 6 high-speed ADC input channels and 2 high-speed DAC output channels, clock distribution unit, motor drive isolation circuits, etc. [6]

Since 2021, the second-generation specialized digital LLRF system was developed and successfully debugged in 2022. It was successfully applied to the high-power horizontal tests of 1.3 GHz Dalian superconducting Cryomodule and the high-power conditioning of HEPS Booster normal-conducting copper cavity. The LLRF system mainly includes digital signal processing board, ADC/DAC daughter board, and RF front-end board. Unlike the first-generation digital LLRF system, the FPGA of this digital signal processing board uses XC7Z100-2FFG900 from Xilinx's Zynq-7000 series.

The advantages of the second-generation LLRF system

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compared to the first-generation LLRF system are as follows:

- Adopting an embedded ARM system that can run EPICS IOC.
- Adopting FMC connector, the analog circuits were separated from the digital circuit, and updating and repairing of analog circuits are more convenient.
- The number of channels has been doubled, from the original 6 ADC channels and 2 DAC channels to 12 ADC channels and 4 DAC channels.
- The clock distribution includes two AD9520 chips, which can adopt various clock distribution schemes.
- More FPGA logical cells.

SYSTEM ARCHITECTURE

The RF control adopts a modular design and its layout is shown in Fig. 2. It consists of five main sub-systems: LLRF, interlock, data acquisition, RF local database, and beam trip diagnostics. These systems have been in-house developed and some prototypes are being tested.[7,8]

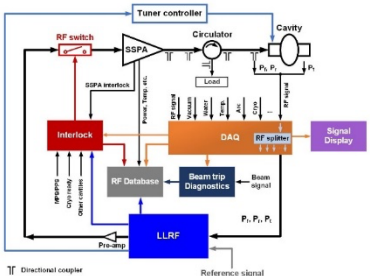

Figure. 2 Layout of the RF control system.

The framework diagram of the HEPS LLRF system is shown in Fig. 3, and it mainly includes a digital signal processing board, an ADC/DAC daughter board, and an RF front-end board. The RF front-end board completes the conversion between RF signal and intermediate frequency (IF) signal, including down conversion of RF signal to IF signal, up conversion of IF signal to RF signal, etc; The ADC/DAC daughter board is used for the analog-to-digital conversion and digital-to-analog conversion of IF signals. The ADC/DAC daughter board connects with the digital signal processing board through the FMC interface. The digital signal processing board can carry up to two ADC/DAC daughter boards simultaneously. The digital signal processing board is the core board of LLRF system, mainly completing feedback control loop algorithms, reference clock distribution, etc. Digital signal processing, control algorithms, and signal communication are mainly achieved by the FPGA inside the board.

Digital Signal Processing Board

The functional diagram of digital signal processing (DSP) board for LLRF system is shown in Fig. 4. It mainly includes FPAG chip, RF reference clock distribution unit, motor drive and Piezo drive circuits, reset and trigger, multi-channel I/O expansion interface, etc. FPGA is the core chip of the board. XC7Z100-2FFG900 chip under Zynq-7000 series produced by Xilinx company is used.

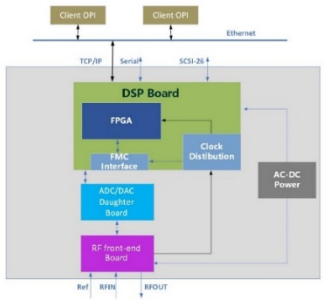

Figure 3: Framework of the 2nd-gen LLRF system.

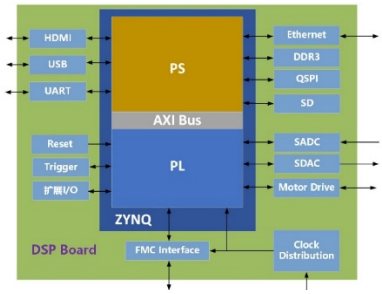

Figure 4: Functional diagram of the digital signal processing board.

The DSP board is composed of two main parts: a processing system (PS) composed of a dual core ARM Cortex-A9, and a programmable logic (PL) part equivalent to one FPGA. The connection between PL and PS adopts the industry standard Advanced Extensible Interface (AXI) connection methods. The PS part integrates two ARM Cortex A9 processor, AMBA interconnection, internal storage, external storage interfaces, and peripherals. These peripherals mainly include USB bus interfaces, Ethernet interfaces, SD/SDIO interfaces, I2C bus interfaces, CAN bus interfaces, UART interfaces, GPIO, etc. The PL part is a logic processing unit, the LLRF control algorithms, digital signal processing, and some other functions are implemented within it. While the EPICS IOC was running on the embedded Xilinx Linux within the PS part.

The clock distribution unit adopts two AD9520s, which has 12 LVPECL outputs (max frequency 1.6 GHz) divided into 4 groups, and each group has a 1-to-32 divider with phase delay. Each LVPECL output can be configured as 2 CMOS outputs (for fout ≤ 250 MHz).

The prototype DSP board is shown in Fig. 5. It consists of 16 layers of printed circuit board, including 2 layers of power supply, 6 layers of GND and 8 layers of signal. The board is mainly divided into power distribution circuits, FPGA and its peripherals, FMC interfaces, clock distribution circuits, motor-driven photoelectric isolation circuit, serial ADC and DAC, CPLD configuration circuits and so on.

ADC/DAC Daughter Board

The ADC/DAC daughter board includes three 16-bit, 125 MSPS, dual-channel high-speed analog-to-digital converters (ADC) AD9268-125, one 16-bit, 800 MSPS, dual-channel high-speed digital-to-analog converter (DAC)

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Figure 5: The prototype DSP board.

AD9788. It is used to meet the requirements of LLRF systems for high-precision and stable control of cavity field amplitude and phase. The ADC/DAC daughter board connects with the digital signal processing board through the FMC high-speed interface. The prototype ADC/DAC daughter board is shown in Fig. 6.

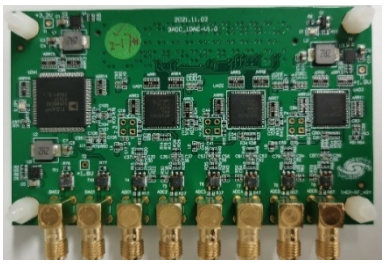

Figure 6: The prototype ADC/DAC daughter board.

RF Front-End Board

The RF front-end board has six down-conversion channels and two up-conversion channels. The RF reference signal has four power divisions, one of which is fed into the DSP board to produce IF signal, which returned to the RF front-end board and mixed with the RF signal to generate local oscillator (LO) signal. The LO signal is then mixed with the RF signal and IF signal, to realize the signal down-conversion and up-conversion. The prototype RF front-end board is shown in Fig. 7.

As mentioned earlier, HEPS includes two different RF frequencies, 499.8 MHz and 166.6 MHz, different RF front-end boards have also been made corresponding to them. Their PCB boards are completely the same, except for the selection of different filters, such as low-pass filters, RF bandpass filters, and LO bandpass filters. In addition, to achieve better electromagnetic shielding, we have designed corresponding aluminum shielding covers over the RF front-end board.

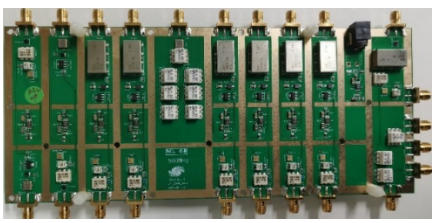

Figure 7: The prototype RF front-end board.

EXPERIMENTAL RESULTS

The HEPS LLRF system was integrated after the debugging of LLRF hardware and software, as shown in Fig. 8. Firstly, the off-line closed loop test of LLRF system was done in which the superconducting cavity was replaced with a 166.6 MHz mockup cavity in the lab and the RF field inside the cavity can be controlled within +/-0.018% in amplitude error and +/-0.011 degree in phase error (peak to peak), respectively. The measurement results are shown in Fig. 9.

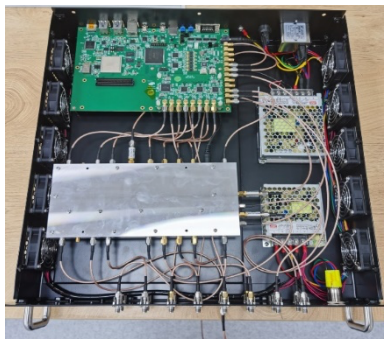

Figure 8: The HEPS LLRF system prototype.

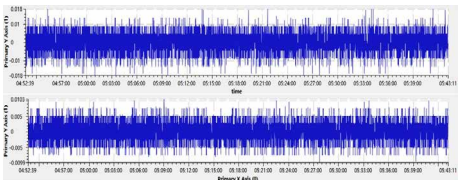

Figure 9: The LLRF measurement results in lab test.

At the beginning, the first generation LLRF system was used in the in the 499.8 MHz normal-conducting cavity high-power conditioning in 2022, max cavity forward power about 120 kW. At last the new LLRF was also demonstrated in it. The LLRF system worked well without problem. and some software bugs found during the operation were fixed. In the cavity high-power conditioning test, the Arc fault detection and protection function has been successfully developed which was used to prevent RF cavities from being damaged by arc, and the Cavity & CPLR auto conditioning program was successfully applied in this experiment which greatly improved the efficiency of the experiment [9]. The functional control of LLRF system is constantly being improved.

SUMMARY

This paper describes the architecture of the new digital LLRF system for HEPS. The FPGA of the DSP board has been changed from the original ALTERA Stratix III to Xilinx Zynq-7000 which comes with a versatile Processing System (PS) integrated with a highly flexible and high-performance Programmable Logic (PL) section. Excellent control stabilities were demonstrated on the mockup cavity in the laboratory. The performance in the lab has been characterized by a residual peak-to-peak noise of ±0.05% in amplitude and ±0.03 degree in phase. The results meet the HEPS specifications

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