INTEGRATION OF THE TIMING SYSTEM FOR TPS

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Abstract

Timing system for the Taiwan Photon Source (TPS) were setup and ready for accelerator system commissioning. Event based timing system was chosen to satisfy various requirements for the machine and experiments. The system consist of event generator and multiple event receivers which installed local control nodes. The timing system is ready in the first quarter of 2014. Performance and functionality are investigated systematically. Parameters like delay, skew, latency, drift due to ambient temperature variation, etc. will be addressed. This report wills summary progress of TPS timing system before system delivery for accelerator commissioning.

INTRODUCTION

The TPS is the latest generation synchrotron light source under construction and commissioning is planned in 2014. Event based timing system will apply for TPS [1-2]. Implement timing system is in proceed. The test system already applied for the TPS 150 MeV linear accelerator (linac) commissioning and acceptance during the second quarter of 2011. Various support for the timing system are in preparation.

The timing system is based on the events coming from event generator (EVG). EVG handles the accelerator synchronization and trigger the injection and the extraction pulse device. In order to provide an efficient management of the sequence RAM in the event generator, the sequencer design of timing system is on going.

TPS EVENT SYSTEM CONFIGURATION

The TPS timing system is an event based system [3]. A central EVG generates events from an internal sequence RAM and external sources. These events are distributed over optic fiber links to multiple event receivers (EVRs). The EVRs, which are located in the control system interface layer, decode the events referred to as hardware triggers or software interrupts. For the linac, the decoded events are further encoded by a gun transmitter and sent over a fiber link to the gun high voltage deck. The event clock is derived from the 499.654 MHz master oscillator so that it is locked to change in the RF frequency. The master oscillator used a GPS disciplined Rubidium 10 MHz clock as external reference. TPS timing modules are 6U CompactPCI form factor modules which include cPCI-EVG-300, cPCI-EVR-300, cPCI-EVRTG-300 and linac gun trigger receiver. Small numbers of PCIe-EVR-300 are used to accompany with fan-less embedded EPICS IOC for beamline timing interface. Configuration tools were developed. Save and restore supports are also

available. Sequencer design is ready for final system integration test.

Configuration of the event system is shown in Fig. 1. Link length between timing master and various equipment areas is compose a 300 m long OM3 fiber. Connect at equipment area to the EVR module is done by another 36 m OM3 fiber. Delay due to fiber is about 1800 nsec.
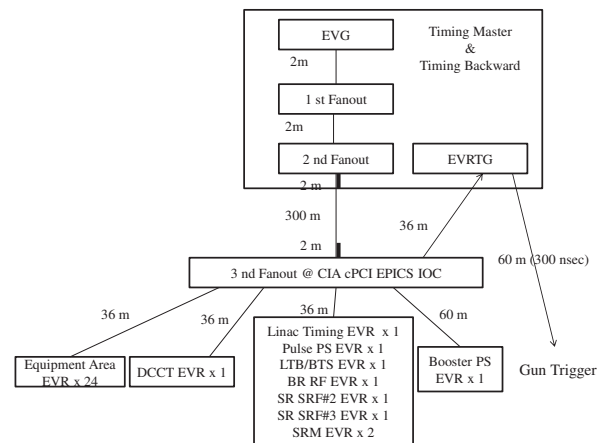

Figure 1: Configuration of event system.

Number of EVG and EVRs installed or will install soon are summary in Table 1. Event modules to support accelerator system are ready for final integration test of accelerator system. Beamline timing will be install when beamline available in 2015 ~ 2016.

Table 1: Event system modules installed around the TPS accelerator system to support commissioning and early phase operation.

Type of event modules	No.	Applications
cPCI-EVG-300	1	Event generator
cPCI-FCT-8	28	Fan-out concentrator
cPCI-EVRTG-300	1	E-gun timing
cPCI-EVR-300	34	Accelerator system timing: 24 CIAs 1 linac 1 BPS 1 LTB/BTS 1 BRF station 2 SRF stations 1 DCCT 2 SRM 1 Pulse PS
PCIe-EVR-300	7	Beamline timing, will installed when beamline available in 2015/2016

INJECTION CONTROL SCHEME

Injection sequence control will be performed by program the content of sequence RAM which all time-stamped trigger events stored in the EVG. The timing sequencer was coded by state notation language (SNL) with the EPICS sequencer. The SNL sequencer script running in timing master IOC to change the sequence RAM contents of EVG which is installed at the same IOC. Timing sequencer communication with client applications via defined PVs. These PVs include e-gun trigger mode, length of multi bunch train, operation mode and bucket address of next cycle … etc. The timing sequencer work efficiently running at the IOC level. The timing sequencer defined several PVs for specific transition among different states to communicate with other IOCs. The sequence RAM will disable by the stop interrupt of the sequence RAM and change sequence RAM contents. Relationship between sequence RAM contents change with the booster cycle is shown in Fig. 2.

Repetition frequency of the booster synchrotron is 3 Hz rate. The sequence RAM is triggered by 3 Hz rate which is synchronize with booster synchrotron clock, storage ring clock and the 60 Hz mains frequency. The sequencer allowed to skip some cycles to reduce repetition rate of specific devices include beam. The booster power supply always running at 1/3 sec basic cycle without change eddy current effect of the booster synchrotron.
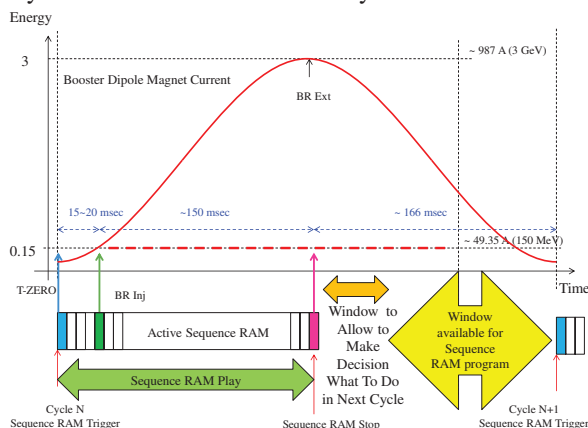

Figure 2: Relationship between booster synchrotron cycle with the operation of sequence RAM.

The sequence is started at T-ZERO which is the trigger time of the sequence RAM and start time of a new accelerator cycle. Energy ramping time of the booster synchrotron is about 150 msec after beam trigger. The sequence RAM will stop after the booster synchrotron finish the ramping cycle. There are about 100 msec time window available for change contents of the sequence RAM. Using EPICS sequencer to program sequence RAM after the sequence RAM stop. The timing sequencer will be running in the timing master EPICS IOC for sequence RAM control in machine operation is satisfy. All parameters for the machine operation modes will be designed as specific EPICS PVs, such as operation mode, e-gun mode (single bunch or multi-bunch), bucket address, repeat cycle, top-up injection, decay mode and etc.

All sequence will store at the sequence RAM. There is a timestamp associated each entry. The event can be activate when load the desired timestamp. The event can be de-activate by replace the event code as NULL event (event code: 0x00), it can activate again when the NULL event replace by original event code. The timestamp value can be change for bucket address requirements. The sequence RAM will program in every cycle. All kind of the operation are fulfilled by these mechanism. The clients can control the timing sequencer to change content in every cycle via pre-defined PVs. The example of sequence RAM management is presented in Fig. 3.

The sequence RAM contents can be updated when current cycle stop. The programming can be done within a few msec. It can program cycle-by-cycle at 3 Hz rate easily.

Injection control is the main theme of the timing system. Timing events related to the operation of all devices will be defined and associate to a timestamp to specify its happened time. To satisfy individual operation of subsystems, coordinate injection process, various trigger events might need enable and/or disable. To provide bucket addressing, the timestamp of some trigger events need to adjust cycle-by-cycle dynamically. The timing sequence will be stored at the sequence RAM in the EVG. The sequence will play every accelerator cycle trigger at 3 Hz rate. The timing sequencer will re-program sequence RAM according to next cycle requirement after current cycle sequence RAM stop.

Software configurable sequence RAM provides a flexibility to change the operation mode. Basic operation support will available at commissioning phase. Sophisticated modes will delivery later after conclude a operation modes will used. A simple configuration tool should be available for sequence RAM management. The possible operation modes will have:

- Accelerator hardware test mode.
- Individual subsystem trigger.
- Single shot, continue injection.
- Repetitive rate reduction by skip one or more cycle for specific trigger.
- Warm up trigger for specific devices.
- Top-up for desired fill pattern without/with feedback.

The bucket addressing will be preformed to change the value of timestamp via timing sequencer at every cycle. Change one count corresponding to 8 nsec which is the period of the event clock ($f_{RF}/4$) use by the TPS event system. Fine delay is supported for the electron gun trigger in and the storage ring injection kicker trigger.

The sequencer provide beam repetition rate reduce functionality by skip one to more accelerator cycles upon request. This can be achieved on the configure page.

Some devices might need operate a few cycles for warm before it reach stable working conditions for beam injection is possible, For example, booster main power supply, injection spectrum of the storage ring might need trigger one or more cycles before it reach to the stable

conditions. The timing sequencer can program the septum and booster main power supply fire one or more cycles before real injection cycle take place. This mechanism can ensure accelerator working properly before beam injection.
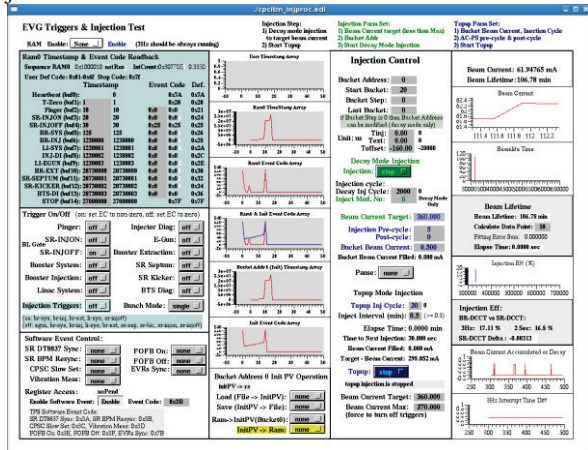

Figure 3: Test scenario for top-up operation.

TIMING SYSTEM READY FOR ACCELERATOR SYSTEM COMMISSIONING

Event based timing system is implemented to support commissioning and operation for the TPS project. The system is ready for final system integration test and beam commissioning. Timing master as well as typical EVR installation is shown in Fig. 4.
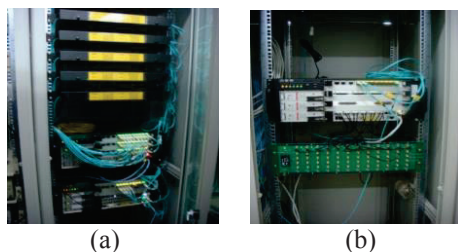

(a)   (b)

Figure 4: (a) Timing master and (b) A typical EVR node.

Total length of the event system fiber links form event generator to the event receiver is 350 m include several short patch cords. Measured skew of EVR outputs have been checked be using oscilloscope with two long equal time delay coaxial cable connect to EVRs in nearest neighbour CIAs is less than 2.5 nsec peak-to-peak for the whole ring corresponding the fiber length variation about +/- 0.5 m. This can be improved later by adjust length of patch fiber cords if necessary.

Jitter of the EVR output is about 20 psec for TTL output and E-Gun trigger jitter is less than 10 psec as shown in Fig. 5. Both kinds of output are used at this moment. Another kind of logic output is available for some special requirements.

Delay of the event links from event generator to event receiver fan-out is about 2.2 μsec.

Drift of timing system due to ambient temperature change major contribute by the fiber links. Contribute due to temperature variation within the cPCI crate which installed event system modules is much less. Timing drift of TPS timing system is around 20 psec for temperature range 25 ± 1 $^{\circ}$C. Further study is needed to investigate when air-conditioning ready soon. If the drift cannot accept by some time-resolved experiments, another temperature compensated sub-picoseconds fiber RF link will used to send RF reference to experiment station as auxiliary support for the event system for such kind applications. Sub-picoseconds clock can re-generate at experimental station for laser and /or instruments synchronization.
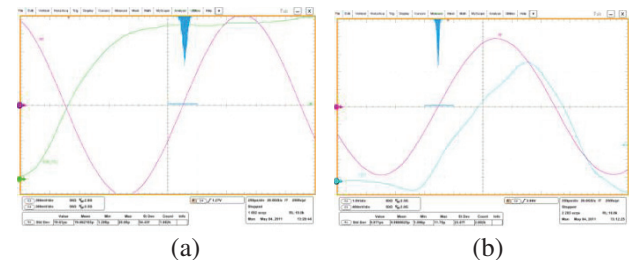

(a)   (b)

Figure 5: (a) Jitter of the cPCI-EVR-300 TTL output relative to the RF clock and (b) Jitter of the beam relative to the RF clock. The beam is triggered by combination of the cPCI-EVRTG-300 and GUN RC-203 trigger module.

SUMMARY

Installation of event system modules and fibre links were done recently. Functionality and performance test and revision are in progress accompany with final integration test which is possible when key subsystem available in July. Preliminary results show that the event system meets requirements for TPS commissioning and operation. Test and modification of timing sequencer are in progress. Various operation scenarios are analysis thoroughly. EPICS sequencer by program using SNL is implemented. Final integration test and revision with injection related devices will be performed start form July 2014 before beam commissioning start. Characterize of the system performance is in on-going. Basic functionality of timing system is achieved. Performance of the system was confirmed to meet requirements of TPS.

REFERENCES

[1] C. Y. Wu, et al., "Preliminary Testing of the TPS Timing System", Proceedings of IPAC2011, MOPO041, San Sebastian, Spain.

[2] C. Y. Wu, et al., "Timing System for the Taiwan Photon Source", Proceedings of ICALEPCS2011, WEPMS013, Grenoble, France.

[3] Micro-Research Finland Oy, website: http://www.mrf.fi.