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Scalable Readout Architecture for Large-Scale Quantum Sensor Arrays in Fundamental Physics

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Modern experiments in particle physics, astroparticle physics, and cosmology increasingly rely on large cryogenic sensor arrays to achieve the sensitivity needed to probe phenomena beyond the Standard Model, including the neutrino-mass scale, dark-matter interactions, neutrinoless double-beta decay, and B-mode polarization of the cosmic microwave background. These efforts require the simultaneous readout of tens to hundreds of thousands of detectors, pushing current data-acquisition technologies and motivating the use of frequency-division multiplexing, particularly microwave SQUID multiplexing (μMUX), to scale to such array sizes. In this work we present the Quantum Interface Controller (QIC), a modular software-defined radio platform for high-fidelity, scalable readout of cryogenic detectors and superconducting qubits. Based on Xilinx Zynq UltraScale+ MPSoC and RFSoC technology, the QIC integrates multi-gigahertz DACs/ADCs, FPGA-based real-time processing, and a unified software stack, supporting both DirectRF generation and super-heterodyne sampling to synthesize and demodulate thousands of microwave tones per unit. A firmware-integrated Cryogenic Detector Emulator (CryoDE) provides a digital detector twin for hardware-in-the-loop validation. This paper presents the QIC architecture, firmware and software environment, it is currently being utilized in the ECHo neutrino-mass experiment, the BULLKID-DM dark-matter search, and for superconducting-qubit readout in quantum-computing applications, demonstrating its suitability as a scalable platform for next-generation quantum-sensor arrays.

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1. Introduction

A central goal of modern particle and astroparticle physics is the search for phenomena beyond the Standard Model [1]. Although the Standard Model successfully describes known particles and interactions, it cannot explain dark matter, neutrino masses, or several features of the early universe [2–4]. Addressing these open questions requires experiments capable of detecting extremely small energy deposits, often a few electronvolts, using cryogenic quantum sensors that operate at temperatures where thermal noise is strongly suppressed.

Many large-scale research efforts rely on such sensors to probe New Physics. Neutrino-mass experiments like ECHo and HOLMES employ high-resolution microcalorimeter arrays to study electron-capture decays [5, 6]. Searches for light dark matter, such as BULLKID-DM, SuperCDMS, and CRESST, use cryogenic detectors to identify faint interactions [7–9]. Cosmology experiments including QUBIC, the Simons Observatory, and CMB-S4 aim to observe the imprint of inflation in the cosmic microwave background, requiring multiplexed readout of large TES or bolometer arrays [10–12].

These experiments face a shared scalability challenge: cryogenic detector arrays now contain tens to hundreds of thousands of channels, far exceeding what traditional wiring can support. Frequency-division multiplexing has therefore become essential. Microwave SQUID multiplexing for TES and MMC detectors [13, 14], and resonator-based multiplexing for KIDs [15], allow large sensor arrays to share only a few microwave feedlines by assigning each channel a distinct resonant frequency. To address the growing need for flexible and scalable readout electronics, we outline recent developments of the Quantum Interface Controller (QIC) architecture.

2. The Quantum Interface Controller

The QIC is a software-defined radio platform developed for the demanding readout requirements of modern cryogenic detector arrays and superconducting quantum technologies. These systems require precise microwave control, wideband signal generation, and low-noise, high-throughput digitization. QIC meets these demands by combining embedded processors, FPGA-based real-time processing, and multi-gigahertz data converters within a single architecture that remains adaptable across diverse experimental environments [16–19].

At its core, QIC employs Xilinx Zynq UltraScale+ MPSoC and RFSoC devices, which integrate ARM processors, programmable logic, and high-speed DACs/ADCs on one chip. This eliminates the need for external data-conversion hardware or complex clock-distribution networks [20]. The close integration of converters and digital logic minimizes latency, improves synchronization, and enables real-time calibration and adaptive control of microwave tones.

A key advantage of the hardware design is its ability to operate directly in high-frequency Nyquist zones, enabling DirectRF synthesis [21]. In this mode, microwave tones are generated without analog upconversion, while high-speed ADCs perform band-pass sampling of the incoming signals. Numerically controlled oscillators place tone clusters across the available bandwidth. Digital downconversion then divides the received spectrum into sub-bands processed by efficient filter-bank structures [17, 19].

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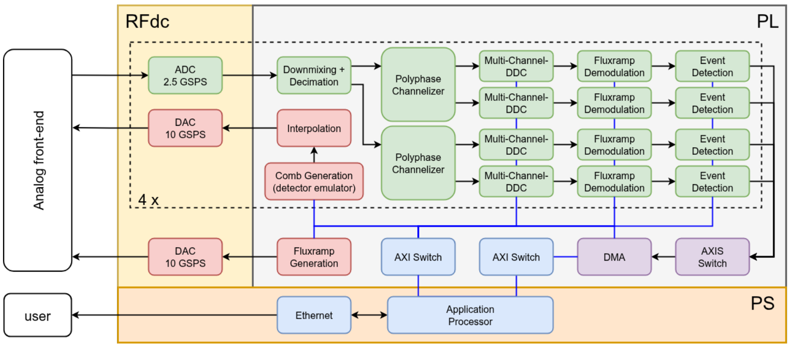

Figure 1: Firmware architecture of the QIC. Modules can be replicated or omitted as required.

The QIC firmware is modular and hierarchical, as seen in Figure 1, supporting build-time configuration and runtime control of tone placement, modulation, flux-ramp parameters, and detector-specific processing. This flexibility enables the same firmware base to be used across MMC, MMB, KID, and superconducting-qubit platforms [17–19, 22].

An important component is the Cryogenic Detector Emulator (CryoDE) [23], a digital detector twin that reproduces realistic pulse shapes and resonator responses. It enables hardware-in-the-loop validation, system-level timing tests, and firmware benchmarking without requiring a cryostat, significantly accelerating development.

The unified software stack runs on embedded Linux and uses gRPC for high-performance communication across distributed nodes [24]. Each board hosts an endpoint driver managed centrally by the ServiceHub [25], which coordinates configuration, device discovery, data routing, and system control. This architecture ensures consistency across deployments and simplifies integration into large experimental infrastructures.

3. Scalable System Integration

As cryogenic detector arrays and quantum-technology platforms grow in scale and complexity, readout electronics must expand from single-module systems to multi-board, multi-crate architectures. The Quantum Interface Controller (QIC) was redesigned with scalability as a core principle, ensuring that the same RFSoC boards, firmware modules, and software interfaces can operate in both small test stands and large distributed installations with tens of thousands of channels.

This scalability is enabled by the Advanced Telecommunications Computing Architecture (ATCA), originally developed for high-availability telecommunications but now widely used in scientific instrumentation [26, 27]. Within the QIC framework, ATCA allows multiple custom RFSoC boards to operate as coordinated nodes through a backplane that provides high-bandwidth networking, synchronized clocks, and low-latency communication [22, 28, 29]. For qubit readout in quantum computing, two dedicated boards (the “RFSoC Hub” and “FLUX-DAC Node”) supply the needed balance between flux-biasing and high-fidelity control, while cryogenic-detector applications typically use only the RFSoC boards.

The architecture scales from a few dozen channels to thousands, as each RFSoC module integrates processing, data conversion, and control logic. Adding boards increases capacity nearly

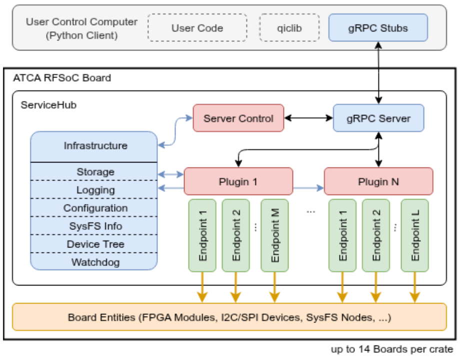

Figure 2: Software infrastructure of the QIC. The user interfaces with the platform through the Python `qiclib` library over gRPC. Dedicated plugins control hardware component in the platform.

linearly. The backplane ensures deterministic timing across all modules, supporting coherent multiplexing schemes such as microwave SQUID readout or multi-qubit control.

Synchronization between boards is maintained through shared reference clocks, deterministic high-speed links, and firmware-level timing routines [22]. These mechanisms guarantee phase coherence across nodes, enabling stable resonator sweeps, flux-ramp demodulation, and calibration procedures without drift, critical as experiments expand to full-scale cryogenic arrays.

The modular software architecture further supports scalability, as seen in Figure 2. The ServiceHub manages system-wide communication, configuration, and firmware coordination, ensuring consistent behavior across all boards. In the host system, the qiclib library is used to treat a multi-crate installation as a single instrument [30], the QIC provides a coherent and extensible platform capable of growing with the demands of next-generation sensor arrays and quantum experiments.

4. Conclusion

The development of the Quantum Interface Controller marks a major advance in scalable, high-performance readout electronics for cryogenic detector arrays and quantum devices. By integrating multi-gigahertz data conversion, real-time digital processing, flexible firmware, and a unified software environment, the QIC offers a versatile platform suited to a wide range of scientific applications. Its use in experiments such as ECHo, BULLKID-DM, and QSolid highlights its effectiveness across different quantum detector and qubit technologies.

A central strength of the system is its ability to scale from small laboratory setups to large multi-crate installations requiring precise synchronization and high channel counts. The ATCA architecture, combined with DirectRF techniques and modular firmware, equips the QIC to meet the growing needs of next-generation particle-physics, cosmology, dark-matter, and quantum-technology experiments. The integrated Cryogenic Detector Emulator further accelerates development by enabling rapid, hardware-level validation without a cryostat.

As experimental programs expand in size and complexity, the demand for flexible and maintainable readout solutions will continue to increase. The QIC provides a unified approach that balances performance, adaptability, and long-term sustainability. The QIC stands as an enabling technology for future discovery efforts within the ECFA DRD5 and DRD7 R&D programmes.

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