# RD53B Wafer Testing for the ATLAS ITk Pixel Detector

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**Abstract.** RD53B/ITkPix-V1 is the most recent hybrid pixel readout chip development for the ATLAS pixel detector at the HL-LHC. It is the first full-scale 65 nm hybrid pixel-readout chip of its kind. ITkPix-V1 consists of more than one billion transistors with a high memory triplication ratio to cope with the high particle density at the heart of ATLAS. Chips will be as close to the interaction point as possible to optimize the resolution of impact parameters. The ITkPix-V1 chip features a 5-Gbit connection, with special data compression to deal with high hit intensities. In addition, a low-power, low-noise analog front-end is used to ensure high readout speeds and low detection thresholds. Failure of chips in ATLAS would be problematic. Therefore, a thorough test is necessary before and during production. For this purpose, the Bonn ATLAS group has developed BDAQ53, a fast and versatile simulation and testing environment that allows small and large-scale testing for ITkPix-V1 and its successor chips. This conference note will give an overview of the testing environment while focusing on large-scale wafer testing to evaluate ITkPix-V1's suitability for its deployment at the HL-LHC.

## 1. Introduction

ITkPix-V1/RD53B (ITkPix-V1) is part of a two-silicon-die combination, a so-called hybrid module (Figure 1). This configuration allows the top die to be specialized in charge collection induced by a large density of traversing ionizing particles, while the other die offers enough space for a chip to house analog amplification circuits and digitization electronics in each pixel. In addition, the bottom chip (ITkPix-V1) offers a standardized interface to forward data from the pixel matrix to the detector readout (Figure 1). Each ITkPix-V1 offers a total of 0.15 megapixels distributed over an area of 2 cm x 2 cm [1]. The ATLAS inner tracker (ITk) will consist of 33 092 ITkPix − V1 with an active area of approximately 12.7 $m^2$ distributed over five barrels and in total 14 disks in forward and backward direction [2], surrounded by an additional four silicon strip detector barrels [3]. This new ITk will succeed parts of the current ATLAS detector [4].

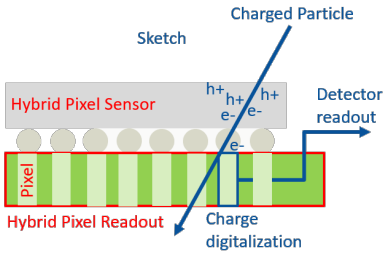


Figure 1: Charge produced by an ionizing particle is guided through a bump bond to the ITkPix-V1 readout chip.

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## 2. ITkPix-V1

ITkPix-V1 has four critical points, which must be tested on every chip before further assembly. All conducted tests are designed to cover as much of the following four test domains as possible:

(i) **Analog Chip Bottom**: The analog chip bottom houses band gaps, power regulators, and sensors to supply the digital logic with different voltages necessary for operation.

(ii) **Digital Chip Bottom**: The digital chip bottom aggregates all the digital information from the pixel matrix and is responsible for chip control. It encodes and decodes data sent from and to the chip while handling logical functions.

(iii) **Analog Pixel**: The analog pixel electronics are responsible for charge integration, amplification, and measurement. This circuit is part of each pixel and therefore needs to be tested more than 150 thousand times per chip.

(iv) **Digital Pixel**: The digital pixel electronics are responsible for digitizing the analog signal, generated by the analog pixel electronics. This circuit is also part of each pixel and therefore needs to be tested more than 150 thousand times per chip.

## 3. ITkPix-V1 - Wafer Probing Setup

In chip production, it is common practice to test each chip at the wafer level. A perfect wafer yields up to 132 ITkPix-V1. To determine the yield, the University of Bonn has developed the following wafer probing setup with the BDAQ53 test system [5] at its heart. Figure 2 shows a

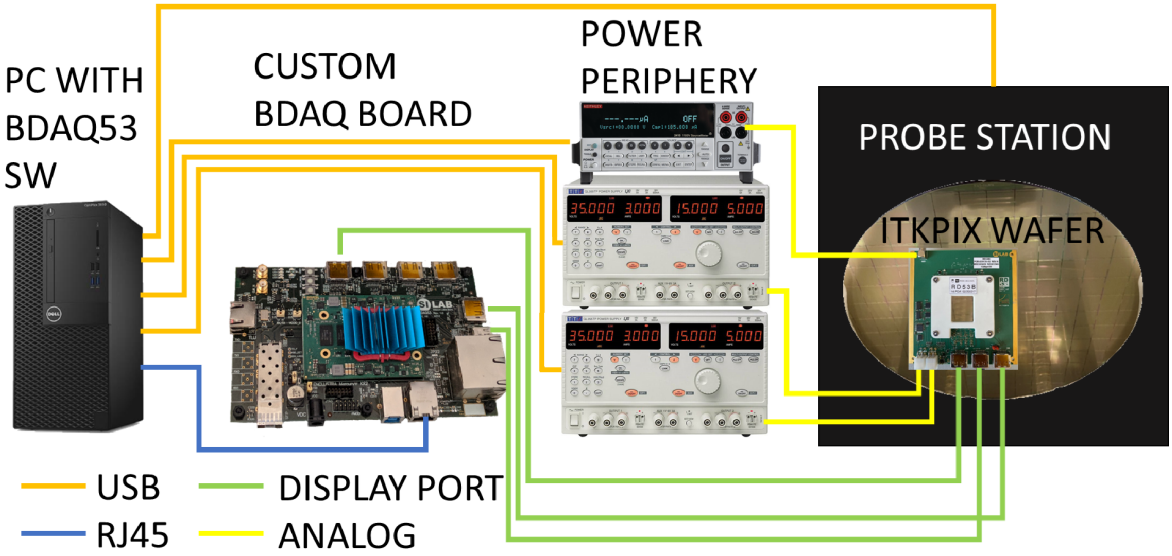



Figure 2: ITkPix-V1 wafer probing setup.

simplified version of its components. From left to right, we find the data acquisition PC, which controls powering, measurement, and probe station periphery via a serial interface. Controls like this allow the setup to automatically turn on and off, while informing the probe station to disconnect from the chip and proceed to the next one. Connection to the chip is established with a probe card, featuring approximately 200 tungsten probes that temporarily touch the wire bond pads on the chip. The chip functionality is then tested using BDAQ53, which connects to the probe card via display port cables, to forward the received chip data to the data acquisition PC via RJ45.

## 4. Test Routines

The functionality tests are oriented along the domains introduced in Section 2. Figure 3 shows the order of the tests with a color reference for the given domain. The order of tests is chosen cover the most likely failure modes first. A chip that draws too much current, e.g. due to an analog power rail shortage, also then by definition does not pass all its following tests. Therefore, if one test fails by a certain margin, the other tests are skipped, and the chip is marked red (non-functioning).

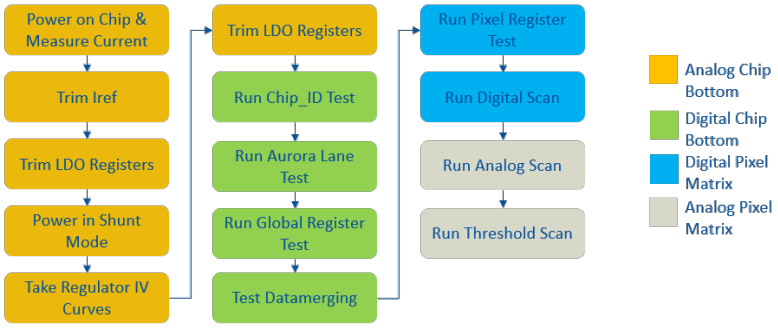
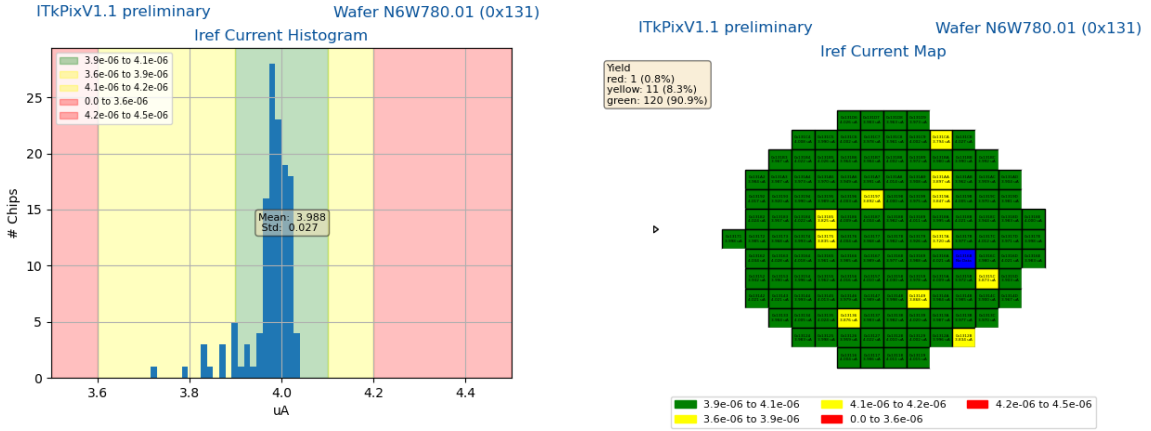



Figure 3: Order of tests conducted per chip.

The yellow domain incorporates four procedures, the first is powering and checking for short circuits by measuring the current after powering. The second is to trim the on-chip reference current to 4 µA "Trim Iref" and the third step is to trim the on-chip digital and analog power rails to 1.2 V. If this is successful, a second powering mode of ITkPix-V1, the so-called shunt mode, is tested. This mode will be used to power multiple ITkPix-V1 in series. For this operating mode, it is crucial that each chip draws the same current, regardless of the chips operating state. The excess current is thermalized in the so-called shunt regulators, which mimic ohmic resistance. [6] The linearity of this ohmic resistance is tested in the step 'Take Regulator IV Curves' (see Figure 3). Subsequently, the supply power rails are again trimmed to 1.2 V. In this powering mode, the chip's digital chip bottom domain is subject to further tests. The general idea behind these tests is that a predefined command pattern is sent to the chip. If the chip responds with the expected and correct pattern, it passes the test. Test patterns include testing if the chip is reachable under the correct chip ID, if the chip can respond on all four data transmission lanes, if all the bits in the chip's configuration registers work, and if a feature called data merging works. Data merging is a feature, where one chip X can forward its data output to another dedicated data merging input of chip Y. Chip Y then integrates the data from chip X into its own data output stream. For this purpose, BDAQ53 simulates a full ITkPix-V1 transmitter in its FPGA and can forward data to the device under test (chip Y) input, while BDAQ53 monitors the chip Y output for the data sent by the simulated chip X. The blue domain tests if the pixel configuration registers work and the digital hit processing of each pixel work. The gray domain focuses on the analog pixel matrix domain. Here the analog front end is checked and whether each of the pixels responds in a certain threshold region.

## 5. Test Routine Output

Each of the test routines mentioned in Section 4 produces a wafer-level histogram and map, to obtain a statistical overview of chip variations over the same wafer and assign the measured properties of each chip to the correct position for future wafer processing. Figure 4a shows an exemplary histogram of the trimmed reference current (Iref). The plot is divided into three performance domains: red, yellow, and green. Chips that have values in the red area, fail the test and the probe-software will immediately go to the next chip. Yellow chips are chips, which do not quite fulfill the detector requirements, but can most likely still be used for bench testing and development. Green chips are chips that pass the criterion of being assembled into modules. On the basis of this histogram, the colors in Figure 4b, are assigned and form a so-called wafer




(a) Reference current histogram after trimming for 132 chips

(b) Wafer map for reference current after trimming

Figure 4: Exemplary wafer probing test histogram and wafer map

map. Blue chips in the wafer map are not represented in the histogram, due to an earlier measurement error (e.g. shorted power rails). In the next step, wafers will be cut and green, yellow, and red chips will be sorted and assigned for their future use.

## 6. Summary

This paper summarizes the automated wafer probing process of the ATLAS ITk Pixel chip RD53B/ITkPix-V1. During production, more than 80000 ITkPix-V1 will be tested in at least three sites by ATLAS groups in Glasgow, Paris, and Bonn, each of which will probe three wafers per week. These sites will all run with hardware and software as presented in this paper, ensuring the readiness of 33092 ITkPix-V1 for integration into the ATLAS Inner Tracker for the HL-LHC upgrade at CERN in 2025.

## References

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