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SDC
SOLENOIDAL DETECTOR NOTES

LEVEL 1 TRIGGER DECISION DESIGN FOR THE SDC

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1 Introduction

The SDC level 1 trigger decision is based on local decisions about the presence of objects such as photons, electrons, muons, and jets, as well as global sums of E_T and missing E_T. It uses the global compilation of this information to decide whether to keep (i.e. trigger on) a particular 16 nsec beam crossing. Each of the objects, such as electrons, muons and jets, are required to pass a series of p_t or E_t thresholds, which are used in making the Level 1 Trigger Decision.

The identification of trigger objects often depends on correlations between different subsystems participating in the trigger decision. The identification of an electron involves correlating information from the tracking and calorimeter systems. Identification of an electron in the calorimeter requires detecting isolated electromagnetic energy. The first step is to find a calorimeter trigger tower with energy in the electromagnetic compartment and little or no energy in its hadronic compartment (i.e. typically $E_{HAC} < 0.1 * E_{EMC}$). Next the towers adjacent to this tower are checked for having little or no energy in both electromagnetic and hadronic compartments. This establishes electromagnetic energy that is transversely and longitudinally isolated. However, since the size of the calorimeter trigger towers (nominally .1 x .1) is coarse, this isolation determination is improved with information from the shower max detector. Since a photon would also deposit the same pattern in the calorimeter, but would not deposit in the tracking system, the tracking system is used to distinguish between a photon and electron.

The Level 1 Electron Trigger starts with .1 x .1 towers with energy in the electromagnetic compartment and little or no energy in the hadronic compartment surrounded by towers with little of no total energy. These isolated electron candidates are reported out on a .2 x .2 grid. In order to distinguish electrons from photons, correlation with the outer tracker is used. The shower max detector provides a local hit in .2 $\eta \times$ .00625 ϕ bins. The outer tracker provides tracks with a p_t on a .00625 ϕ grid. The shower max is first correlated with the tracker to produce a coincidence hit with a p_t in .2 x .2 bins (after making the coincidence on a .00625 ϕ scale) for checking against the calorimeter in η, ϕ, and p_t. The photons are selected without the track match, but with a shower max match and a higher energy threshold.

The Level 1 Trigger finds jets by looking for .4 x .4 calorimeter towers over a series of thresholds. It finds muons by finding muon tracks over a series of muon p_t thresholds. The muon system is not correlated with the tracking system until Level 2. It must have a sharp enough p_t threshold to allow for a few kHz Level 1 rate while satisfying the trigger requirement above.

2 General Overview

Figure 1 shows a diagram of the Level 1 Trigger layout. Front-end crates for the calorimeter, shower max, tracking and muon subsystems are shown inside the border. Above them, off the detector, are shown the the level 1 decision processing crates. These include the Calorimeter Isolation/Summation crates, the Track/Shower Max Match crates, the Isolated Electron Match crates, the Energy Sum/Jet Threshold crate, the Muon Trigger Crates, and Final Decision crate. These crates together form a pipeline structure in which data flows off of the detector on 1 Gbit/sec optical fibers into the Calorimeter Isloation/Summation, Track/Shower Max Match and Muon Trigger crates as shown in the figure. Data is transmitted from these crates to the Isolated Electron Match and Energy Sum/Jet Threshold crates for further correlation before it is sent to the Final Decision crate. In the case of the Muon Trigger crates, their data is sent directly to the Final Decision crate. The trigger decision pipeline ends at the Final Decision crate, where a Level 1 Accept/Reject is generated and transmitted to the Global Clock/Control Crate for subsequent distribution to all DAQ and Level 1 Trigger crates.

Those crates which receive raw data directly from the front end trigger hardware on the detector contain Level 2 Interface Cards. These cards enable copies of the raw data for which Level 1 Accepts were generated to be transmitted to the Level 2 Trigger.

Each crate in the system has a backplane processor interface bus. This VME or similiar-type bus is used by the DAQ Interface/Processor card in each crate to program, control and monitor all of the cards in the system. This bus connection and the interface circuitry required on each card is not shown on the current card block diagrams, but is assumed to be present.

Each crate in the system also has a Level 1 Clock/Control Interface card. This card receives the level 1 clock and trigger control information from the Global Level 1 Processor and distributes it to the cards in the crate. See [3] for a further discussion of this card.

The Calorimeter Isolation/Summation crates find .1 x .1 calorimeter towers where $E_{em} \gg E_{hac}$, surrounded by quiet towers. These isolated electron candidates are reported out on a grid of .2 x .2 towers. These crates also sum up the total E_t in .4 x .4 towers, as well as the total E_t, E_x and E_y in the crate. The total .4 x .4 tower sums are tested against 8 thresholds and the number passing each is calculated.

The Track/Shower Max Match crates correlate the outer tracker hits with the shower max hits on a .00625 ϕ scale. The shower max is used to assign the track an η coordinate on a .2 scale. The p_t from the tracker is used to place the track on a 3-bit p_t scale used to match against the calorimeter E_t.

The Isolated Electron Match crates match up the shower max - outer tracker hits and the calorimeter isolated electron candidates on a .2 x .2 grid. The results are counted up in categories of track (including shower max) and calorimeter agreement on p_t, disagreement on p_t, and shower max match only with the calorimeter (photon). For each category, the total number of matches above each of 6 E_t thresholds is accumulated. Failures to match shower max and calorimeter are also counted.

The Energy Sum/Jet Threshold crate continues the global E_t, E_x, and E_y sums as well as adding up the number of .4 x .4 calorimeter towers above a series of 8 thresholds.

The Muon Trigger Crates count up the number of muon tracks passing each of 4 programmable p_t thresholds. They also store 3 bits of p_t and the track location with a resolution of $\Delta\phi = .01, \Delta\eta = .05$ for use by the second level trigger.

The Final Decision Crate sums up and makes cuts on calorimeter total and missing E_t (the latter from the individual E_x and E_y sums). It sums up the total number of calorimeter .4 x .4 regions over 8 thresholds and makes cuts on this. It sums up the total number of isolated electron (and photon) candidates within the categories and p_t thresholds described above and makes cuts on these. It also sums up the total number of muons over the p_t thresholds and makes cuts on these. The resulting trigger decision is then forwarded to the level 1 clock/control logic. See [3] for a further discussion of this logic.

3 Calorimeter Isolation/Summation Crate

Figure 2 shows a Calorimeter Isolation/Summation crate. There are 24 of these crates, 16 for the barrel and 8 for the intermediate regions of the detector. Each barrel crate covers 1.6 η x 0.8 ϕ. A crate contains 8 Memory Lookup cards (MLU cards), which receive the hadronic and electromagnetic energies from the .1x.1 calorimeter tower sums. The MLU cards convert the the input FADC tower sum values into E_T on a 12-bit linear scale, compute E_T, E_x, and E_y sums on the .4x.4 region of 16 trigger towers that each services, and calculate an Encoded Tower Type (ETT) code for each tower. This type is based on the amount of energy deposited in the hadronic and electromagnetic compartments. The code is 0 for any tower below the electromagnetic threshold (quiet), and 1-6 for an electron exceeding one of six thresholds, and 7 if the tower is hadronic. A further description of the ETT code and the isolated electron detection logic that uses it can be found in [1].

Each crate also contains 2 Pattern Recognition ASIC cards (PRA cards), which receive ETT codes from 4 MLU cards, corresponding to a .8x.8 region. These boards search for isolated electrons at six independent thresholds within the .8x.8 region. The result is a series of 3-bit codes indicating the absence or presence and threshold of an isolated electron. A flag exists for each .2x.2 region which is fully confined within the .8x.8 area, and for each .1x.2 or .2x.1 region which is on the edge, and for each .1x.1 region on the corners of the .8x.8 area. These isolated electron codes are transmitted to the Isolated Electron Match Crates, for further correlation with adjacent regions of the calorimeter and with data from the Tracking and Shower Max subsystems.

Each crate also contains an Energy Summation Card (Energy card). This double-width card covers a 1.6η x .8ϕ region and receives the energy sums for the .4x.4 regions from all 8 MLU cards. It computes the total E_T, E_x and E_y sums for the 1.6x.8 region. It also tests the E_T in each .4x.4 tower against 8 thresholds and calculates the number of .4x.4 towers above each threshold. It delivers 3 bits of number above threshold for 8 thresholds, along with the 3 energy sums to the Energy Sum/Jet Threshold Crates.

Each crate also contains a Level 1 Clock/Control Interface card, a Level 2 Interface card, and a DAQ Interface/Processor card.

3.1 Calorimeter Memory Lookup Card

Figure 3 shows a block diagram of the MLU card. The card operates on a .4x.4 region of the calorimeter. 16 optical fibers enter through the front panel, each carrying 8 bits of raw compressed FADC data for the EMC and HAC sections of a .1x.1 trigger tower. This data is received serially at a 1 Gbit/sec rate, and converted to a 16-bit parallel path operating at a 16ns rate, for each fiber. The output of the fiber optic receiver circuitry is received by 16 identical MLU blocks, one for each tower.

This MLU block consists of 3 separate lookup operations, all performed in parallel over a 16ns window. The first lookup operation combines the 8 bits each of raw EMC and HAC energies as address into a 64Kx3 MLU, to produce a 3-bit ETT code for the tower. This code catagorizes the tower as either quiet, containing an electron at one of six thresholds, or hadronic. The last two MLUs convert the raw EMC and HAC energies to a 12-bit linear scale. The 16 ETT codes from all MLU blocks are transmitted to a PRA card via the crate backplane. The 32 energies from the MLU blocks are summed in a 12-bit adder tree.

The adder tree is a 5-stage binary tree, 12-bits wide at all stages, that produces an E_T energy for the .4x.4 region covered by the card by suming the EMC and HAC energies from each of the 16 trigger towers. The speed at which each stage is calculated has not yet been determined. The E_T sum is converted to E_x and E_y sums in two parallel 4Kx12 MLUs. All three energies are then transmitted to the Energy card via the crate backplane.

The card also buffers the raw EMC and HAC 8-bit energies for all 16 input optical fibers for subsequent transmission to the Level 2 Interface Card after receiving a level 1 accept.

3.2 Calorimeter Pattern Recognition ASIC Card

Figure 4 shows a block diagram of the PRA card. It operates on a .8x.8 region of the calorimeter, receiving ETT data from 4 MLU cards. The 64 total 3-bit ETT codes are received on the card in a 192-bit wide register bank, and then broadcast to 6 Pattern Recognition ASICs and the quiet detect logic via a ETT data bus. Each PRA examines the entire .8x.8 region, looking for isolated electrons at a particular threshold, with each of the six PRAs selecting a different threshold. The output of each PRA is a 25-bit flag word, with a bit for each of 25 regions in the .8x.8 area indicating if that region contained an isolated electron or not at that threshold. The quiet detect logic examines the same 25 regions, and delivers 25 corresponding bits, with each bit indicating if that region was completely quiet or not. A further description of the PRA can be found in [1].

The 7 bits of raw flags, including 1 quiet flag and 6 electron flags per region, for each of the 25 regions (175 bits total) bits are delivered to the electron threshold encoder and self-test logic. This logic examines the 7 bits for each of the 25 regions, and generates a 3-bit code, the isolated electron code. This code indicates whether the region was completely quiet, or if it contained an isolated electron, and at what level, or that neither of the above cases was true. The resulting 25x3 (75) bits of isolated electron codes are delivered to the Isolated Electron Match crates.

In self-test mode, this logic also examines the output of all 6 PRAs, which are set to the same threshold for self-test, and detects an error if the output bits of all 6 PRAs are not in agreement.

3.3 Calorimeter Energy Summation Card

Figure 5 shows the block diagram of an Energy card. This double-width card covers a 1.6η x $.8\phi$ region of the calorimeter. It receives the 8x36 (288) bits of E_T, E_x and E_y .4x.4 energy sums from the 8 MLU cards. With these energies, it performs two functions. The first function is to produce E_T, E_x and E_y energy sums for the 1.6x.8 region using 3 parallel 12-bit, 8-input adder trees. The 36 bits of total energies are then transimitted to the Energy Sum/Jet Threshold crates via the front panel.

The second function is to test the E_T .4x.4 energies against 8 thresholds and to sum the number of .4x.4 towers at each threshold. The first stage in this is to decode each 12-bit energy to none or 1 of 8 thresholds in a 4Kx8 MLU, where each output bit of the MLU corresponds to one of the 8 thresholds. This is performed simultaneously in 8 MLU blocks for each of the 8 .4x.4 E_T energies. The decoded output bits are then driven to 8 parallel 8-input adder trees, with one tree for each threshold. Each tree sums 8 binary inputs to a single 3-bit output. It references one output bit from each MLU block. The resulting 8 histogram bins of 3-bit jet towers over threshold sums (24 bits total) are transmitted to the Energy Sum/Jet Threshold crates via the front panel.

4 Track/Shower Max Match Crate

Figure 6 shows a Track/Shower Max Match crate. There are 12 of these crates: 8 for the barrel, and 4 for the intermediate regions of the detector. Each barrel crate covers 1.6 η x 1.6 ϕ. A crate contains 8 double-width Track/Shower Max Hit cards (TSM cards), which receive the the raw tracker and shower max hit data for a 1.6η x 0.2ϕ region. The TSM cards correlate the track and shower max hits and deliver the results to the Isolated Electron Match Crates for further correlation with the isolated electron hits.

Each crate also contains a Level 1 Clock/Control Interface card, a Level 2 Interface card, and a DAQ Interface/Processor card.

4.1 Track/Shower Max Hit Card

Figure 7 shows a block diagram of the TSM card. The card operates on a 1.6 η x 0.2 ϕ region of the detector. Each card is double-width, and receives 16 optical fibers containing shower max hits and 8 optical fibers containing p_T information from the tracker. Each shower max fiber delivers 16 bits of binary hit information for a .2x.1 region, where each bit corresponds to a hit/no hit in a .2η x 0.00625ϕ region. Each tracker fiber delivers four 4-bit bins of p_T information, where each bin corresponds to 1.6η x 0.00625ϕ, and the area covered by the data on each fiber is 1.6η x 0.025ϕ.

The data is received by the fiber optic reciever circuitry and converted to a parallel data on a 16ns clock basis. The data from both subsystems is brought together in the hit resolution sorting logic. This logic finds the largest p_T with a corresponding shower max hit in .00625 ϕ for each .2x.2 region. This is accomplished using 5-bit 32-input comparator trees.

The comparator tree finds the shower max hit with the largest p_T, or alternately, if there are no shower max hits, simply the largest p_T, as follows. At the .00625 ϕ level, the binary shower max hit/no hit bit is appended as the MSB to the corresponding p_T data, producing a 5-bit word. This is repeated for all p_Ts and shower max hits with the result being 32 5-bit values for .2 in η and .2 in ϕ. These values are delivered as unsigned data to a 32-input magnitude comparator tree, which selects the largest 5-bit value. By assigning the shower max hit bit as the MSB, the result is that all .00625 ϕ regions with shower max hits have larger values than those without, and would be selected above regions without hits. Thus, a region with a shower max hit, and with the the largest p_T will provide the value for the .2x.2 area.

A total of 8 comparator trees are used; one for each .2 in η. Each delivers a 5-bit value, where the MSB indicates if there was a shower max hit in the .2x.2 region, and the 4 other bits are the largest p_T corresponding with a shower max hit found in that region. For each region, the 4-bit p_T value is converted to a 3-bit threshold value in a 16x3 MLU block. This threshold value is selected to properly correspond with the isolated electron threshold codes generated by the Calorimeter Isolation/Summation Crates. For each region, the shower max hit flag and the 3-bit p_T threshold code are transmitted to the Isolated Electron Match Crates via the front panel.

Each TSM card also buffers the raw p_T values and shower max hits received on the fiber-optic cables for subsequent transmission to the Level 2 Interface Card upon recept of a level 1 accept.

5 Isolated Electron Match Crate

Figure 8 shows an Isolated Electron Match Crate. There are 6 of these crates: 4 for the barrel and 2 for the intermediate regions of the detector. Each barrel crate covers 1.6 η x 3.2 ϕ. A crate contains 8 Region Match cards (RMC cards), each of which handles a .8x.8 region. The RMC card receives the isolated electron codes from the PRA cards, performs the last level of isolation checking on the edge/corner partial regions, and then compares the isolated electron codes against the track/shower max hit data from the TSM cards to produce a histogram summary of isolated electron/ track/shower max hit totals on .2x.2 regions in the .8x.8 area. There are 18 histogram bins, with each bin being 3-bits wide. The bins count the number of isolation/shower max hits with no p_T, the number with a good p_T match, and the number with a p_T mismatch, at each of the six electron thresholds. The RMCs also deliver an error flag with indicates the presence of isolated electrons without a matching shower max hit. These errors are stored for later system diagnostics.

Each crate also has 2 or 3 Isolated Electron Hit Summation cards (HSC cards). These are double-width cards which continue the histogram summation from 4 front panel input sources to a single frontpanel output. The first two cards are used to continue the summation from 4 RMC cards apiece. At this level, each HSC card covers a 1.6 η x 1.6 ϕ region. The third HSC is used to perform the next levels of summation using lower level HSC cards as the input source. The third HSC card position will be populated in the crates as necessary to implement the histogram summation tree.

Each crate also contains a Level 1 Clock/Control Interface card and a DAQ Interface/Processor card.

5.1 Region Match Card

Figure 9 shows a block diagram of the RMC card. The card operates on a .8x.8 region of the detector, which is offset .1 in η and .1 in ϕ from the .8x.8 region covered by the PRA cards. This offset is equivalent to one trigger tower in both directions. The card receives 75 bits of isolated electron codes for 25 fully confined and edge/corner partial regions from 4 PRA cards. 45 of those bits represent 9 fully confined .2x.2 regions, 6 edge .1x.2 or .2x.1 regions, and a single .1x.1 corner region from from a single PRA card. 12 bits each from two other PRA cards represent 3 .1x.2 or .2x.1 edge regions and 1 .1x.1 corner region, which will be combined with corresponding edge or corner regions from the first PRA card to form composite .2x.2 regions. The last PRA card contributes 3 bits for a single .1x.1 corner region, and forms a composite .2x.2 region with the corner regions from the other 3 PRA cards.

Isolated electron codes for composite regions are generated in the partial region resolution logic. The code for a composite .2x.2 region is the largest code for any of its partial regions. The logic consists of 6 2-input 3-bit magnitude selectors, which select the larger of the 2 codes for each of the 6 edge regions, and a single 4-input magnitude selector, for the corner region. During this resolution, the codes for the confined regions are propagated along side the magnitude select logic, so that all codes stay in sync with each other in the pipeline. The output of the partial region resolution logic is 16 3-bit isolated electron codes, for each of the .2x.2 regions in the .8x.8 area. These codes are sent to the hit matching logic on the board.

The isolated electron/shower max/tracker hit matching logic compares the isolated electron codes to the hit data from the corresponding track and shower max sections in the detector. The track/shower max data arrives from 4 different TSM cards. Each TSM card delivers a 4-bit code for each of 4 .2x.2 areas, with the total area for each card being .8 η x .2 ϕ. The code consists of a shower max hit/no hit bit, and a 3-bit code corresponding to the p_T threshold. The logic delivers 3x6x3-bit (54) bits of histogram data, indicating the number of isolated electron/shower max hits with no p_T, the number with a good p_T match, and the number with a p_T mismatch at each of the six electron thresholds. It also delivers an error flag which indicates the presence of an isolated electron without a shower max hit. These 55 bits are delivered to the front panel, where they are transmitted to a HSC card.

The matching logic operates as follows. For each .2x.2 region, there is a 3-bit magnitude comparator and some other combinatorial logic which examines the isolated electron and p_T codes to produce 3 signals: GOOD, MISMATCH, and NOPT. GOOD is active if the p_T code is $\geq$ than the isolated electron code. MISMATCH is active if the p_T code is $<$ the electron code but not zero, and NOPT is active if the p_T code is zero. These three mutually-exclusive lines serve as enables to 3 separate 3-to-8 decoders, which all decode the electron code. Output lines 1-6 of each of the three decoders, which correspond to valid isolated electrons, are then sent as binary inputs to 18 separate 16-input adder trees. Output lines 0 and 7 of each decoder are not used. They correspond to electron codes 0 and 7, which do not indicate the presence of isolated electrons. Each tree computes the sum for one histogram bin from the 16 individual .2x.2 regions. For each region, there is also an additional combinatorial block which compares the electron code and the shower max hit bit. If the electron code is in the range 1 to 6 and the shower max hit bit is not active, then an error flag for the .2x.2 region is produced. The error flags for all 16 regions are combined in a OR tree to produce the single error flag for the entire .8x.8 area. These errors are stored on the card for subsequent diagnostic purposes.

5.2 Isolated Electron Hit Summary Card

Figure 10 shows a block diagram of the HSC card. It is the basic building block for the summation tree for the isolated electron hit histograms. At the lowest level, it operates on a 1.6x1.6 area from 4 RMC cards. At higher levels, it operates on data from up to 4 HSC cards. A HSC card is used in the Final Decision Crate to provide the histogram results for the total detector.

The HSC card is a double-width card that recieves 55 bits of electron/shower max/tracker histogram and error flag data from each of 4 sources through the front panel. The logic on the card consists of 18 3-bit adder trees of 4-inputs each to sum the histograms, and a 4-input OR network to combine the error flags. The card delivers 55 bits of output data in the same format to the frontpanel, where it is delivered to the next level HSC card or the final decision logic.

6 Energy Sum/Jet Threshold Crate

Figure 11 shows an Energy Sum/Jet Threshold Crate. There is one of these crates for both the barrel and the intermediate regions of the detector. It contains 4 double-width Energy Summation Cards (ESC cards). Each card covers 1.6 η x 6.4 ϕ in the barrel region, or one end-cap in the intermediate regions of the detector. Each ESC card computes 12-bit E_T,

E_x and E_y energy sums from the lower level sums from 8 Energy cards.

Each crate also contains 4 Jet Threshold Summation Cards (JTSC cards). These cards cover the same area as the ESC cards. They compute the next level 5-bit Jet Threshold histograms from the lower level bins from 8 Energy cards.

Each crate also contains a Level 1 Clock/Control Interface card and a DAQ Interface/Processor card.

6.1 Energy Summation Card

Figure 12 shows a block diagram for the ESC card. This double-width card is used to compute the 12-bit E_T, E_x and E_y energy sums for the detector. At its lowest level, it covers a 1.6x6.4 area, operating on data from 8 Energy cards. A ESC card is used in the Final Decision Crate to sum up the result energies from the 4 cards in the Energy Sum/ Jet Threshold crate, thus providing the total E_T, E_x and E_y energies for the detector.

The ESC card receives 3x12 bits (36 bits) of energy values from each of 8 front panel input sources. This data is driven to three identical 12-bit, 8-input adder trees–one for each energy. The three resulting 12-bit energies are then delivered to the front panel for tranmission to the next level ESC card or the final decision logic.

6.2 Jet Threshold Summation Card

Figure 13 shows a block diagram for the JTSC card. This double-width card is used to compute the jet threshold histograms for the detector. It operates in parallel with and over the same area as an ESC card. A JTSC card is also used in the Final Decision Crate to compute the final jet threshold histograms for the detector.

The JTSC card receives 8x5 bits (40 bits) of jet towers/threshold from each of 8 front panel sources. This data is driven to 8 identical 5-bit, 8-input adder trees–one for each jet threshold. The eight resulting 5-bit sums are then delivered to the front panel for transmission to the next level JTSC card or the final decision logic.

7 Muon Trigger Crate

Figure 14 shows a Muon Trigger Crate. There are 6 of these crates, 4 of which cover all of ϕ and $|\eta| < 2.5$ in four equal sections. In addition, there are two forward muon trigger crates, one for each end. A crate contains 8 Muon Logic Cards (MLC cards). Each MLC card covers 1.2 η x 0.8 ϕ in the barrel region. A MLC card receives 12 optical fibers from the muon regional front end crates. Each of these fibers contains 3 bits of p_t and 5 bits of ϕ for the two highest p_t tracks in a .2 η x .4 ϕ region. The card buffers this raw data for transmission to the Level 2 trigger via the Level 2 Interface Card in the crate. The 24 bins of track p_t information is converted to one of 4 thresholds via memory lookup tables. The resulting threshold values are then summed to produce 4 3-bit histogram bins, indicating the number of muon tracks at each of the 4 p_t thresholds.

Each crate also contains a Muon Summation Card (MSC card). This card receives the 4 3-bit threshold histogram bins from each of the 8 MLC cards. It sums the bins together at each threshold to compute the total number of tracks at each threshold for the entire crate. These histogram bins are transmitted to the Final Decision Crate.

Each crate also contains a Level 1 Clock/Control Interface card, a Level 2 Interface card, and a DAQ Interface/Processor card.

7.1 Muon Logic Card

Figure 15 shows a block diagram of the MLC card. The card operates on a $1.2\eta \times 0.8\phi$ region in the barrel section. 12 optical fibers, each carrying 3-bits p_t and 5-bits ϕ information for the two highest p_t tracks in a $.2\ \eta \times .4\ \phi$, are connected at the front panel. The data is received serially at a 1 Gbit/sec rate, and converted to a 16-bit parallel path operating at a 16ns rate for each fiber. The data for all 12 fibers is delivered from the receiver circuitry to the Level 2 storage buffers and the threshold MLUs. Both the raw p_t and ϕ data is delivered to the Level 2 Interface Card across the backplane, for delivery to the L2 trigger system as necessary.

For each of the 24 tracks processed by a MLC card, the 3-bit p_t code is converted to one of 4 thresholds by 24 programmable 8x4 MLU blocks. Each block delivers the p_t decoded to none or 1 of 4 thresholds on 4 parallel lines. The output of the 24 blocks are then summed by threshold in 4 3-bit result, 24 binary input adder trees. The result is a histogram of the number of muon tracks at each of 4 thresholds. This result is delivered to the MSC card via the front panel.

Each MLC card also buffers the raw muon track data received on the fiber-optic cables for subsequent transmission to the Level 2 Interface Card upon recept of a level 1 accept.

7.2 Muon Summation Card

Figure 16 shows a block diagram of the MSC card. This card is used to compute the muon threshold histograms for the detector. It is used to sum together the histograms from 8 MLC cards, or in the Final Decision Crate, the histograms from each of the 6 Muon Trigger Crates.

The MSC card receives 8x12 bits (96 bits) of muon threshold histograms from each of 8 front panel sources. This data is driven to 4 identical 3-bit, 8-input adder trees–one for each muon threshold. The 4 resulting 3-bit sums are then delivered to the front panel for transmission to the next level MSC card or final decision logic.

8 Final Decision Crate

Figure 17 shows the Final Decision Crate. There is one crate for the Level 1 Trigger for the entire detector. This crate contains a single HSC card, ESC card, JTSC card, and MSC card. These cards perform the final level of computation for each of their respective subsystems. The HSC card computes the final histogram totals for electron/track/ shower max hits. The ESC card computes final the E_T, E_x and E_y energy totals for the calorimeter. The JTSC computes the final histogram totals for jet thresholds, and the MSC card for the muon thresholds.

All four of these cards transmit their results via their front panels to the Final Decision Memory Lookup Card (FDM card). This card uses memory lookup tables and other logic to distill the input data into a trigger "vector" for each subsystem. This vector contains pertinent fields for correlation with other subsystems to produce the final trigger decision. The four vectors are transmitted to the Final Decision Logic Card (FDL card) across the backplane.

The FDL card receives the subsystem trigger vectors from the FDM card and performs the final analysis and correlation necessary to produce a level 1 accept/reject decision. It consists of a number of programmable decision blocks, each of which examines a subset of the trigger vector data to produce its decision. The decisions from all of the blocks are ORed together to produce the overall accept/reject. This decision is transmitted to the Level 1 Global Clock/Control Crate for distribution throughout the detector. A further description of the Clock/Control subsystem for the level 1 trigger can be found in [3].

8.1 Final Decision Memory Lookup Card

Figure 18 shows a block diagram of the FDM card. This double-width card has 4 separate memory lookup (MLU) architectures on it, one each for total and missing transverse energy triggers, jet threshold triggers, electron/track/shower max triggers, and muon triggers. Each of these architectures produces a trigger vector that is sent to the FDL card. The structure of the trigger vectors will be subsystem dependent, and reflect the general types of trigger information needed from each subsystem to serve as the basis for the final decision.

The data from each of the four subsystems enters the card through the front panel. It receives 55 bits from the HSC card, 36 bits from the ESC card, 40 bits from the JTSC card, and 12 bits from the MSC card.

The MLU architectures will have between them as necessary a limited degree of interconnections to provide a coarse correlation capability between the subsystems. This capability will permit the subsystems to tune their vector outputs with some knowledge of the state of the other subsystems, with which they will be correlated on the FDL card. An example of this is to provide the electron/track/shower max subsystem with rough knowledge of the results of the total/missing transverse energy calculations. which it can then factor in when building its own vector.

8.2 Final Decision Logic Card

Figure 19 shows a block diagram of the FDL card. This double-width card receives the four subsystem trigger vectors from the FDM card via the backplane and processes them in multiple programmable trigger decision blocks to produce the accept/reject decision which is sent to the Level 1 Global Clock/Control Crate.

Each programmable decision block has 3 major sections. The first section is the vector field select logic. This logic consists of reprogrammable high-density logic, such as a Field Programmable Gate Array (FPGA). A Xilinx IC is an example of this type of part. It's purpose is to select individual relevant fields from the subsystem vectors and to perform a logical correlation between them. The result of this correlation is an address to a MLU block which generates a preliminary accept signal. This preliminary accept is then passed through a programmable prescaler block. The accept signal from all of the blocks are ORed together for transmission through the front panel to the Level 1 Global Clock/Control Crate.

The decision blocks all operate independently from each other on different subsets of the same vector data from the FDM card. Blocks will be allocated to different general types of triggering through dedicated connections to only certain fields of the subsystem vectors. They are thus programmable for different triggers within the scope of data available to that block. For example, one block may be dedicated to triggering conditions which involve photons and transverse energy, while another is dedicated to electron/ muon conditions, each dedicated by means of the vector fields that it can access.

9 Design Summary

The level 1 decision hardware is comprised of numerous on and off-detector crates which are interconnected both electrically and optically to form multiple pipelined data streams, which come together at the Final Decision crate to generate a Level 1 Accept/Reject for the detector.

There are four major physical subsystems: the calorimeter, shower max detector, the outer tracker, and the muon subsystems. Trigger data from these physical subsystems is processed in the pipeline to form four major triggering subsystems: isolated electron/photon hits, total/missing transverse energy, jet threshold sums, and muon threshold sums.

The isolated electron/photon trigger subsystem correlates data from the calorimeter, shower max detector, and outer tracker. From the calorimeter, the raw EMC and HAC section 8-bit digitized pulseheights for .1x.1 trigger towers are transmitted to the MLU cards in the Calorimeter Isolation/Summation Crates. On these cards, trigger towers are tested for transverse isolation of the energy deposition within the EMC section of the tower, and assigned to an energy threshold in the form of an ETT code. On the PRA cards, in the same crate, the trigger towers are tested for longitudinal isolation at their respective threshold on 8x8 tower regions. The result is a series of isolation codes for 2x2 trigger tower regions which are sent to the Isolated Electron Match Crates.

While this is occuring, the raw shower max and tracker hits for corresponding regions in the detector are received by the Track/Shower Max Hit Cards in the Track/Shower Max Match crates. These cards receive the raw shower max hits for $.2\eta$ x 0.00625ϕ regions, and correlate them with the raw p_t codes for the tracker 1.6η x 0.00625ϕ regions. The result produced by these cards is a 4-bit word for each of the .2x.2 regions corresponding to the 2x2 calorimeter trigger towers. This code contains a shower max hit flag and a threshold code corresponding to the scale of the isolation electron codes. This data is also sent to the Isolated Electron Match Crates.

Within the Isolated Electron Match Crates, the two above data streams converge. Each Region Match Card in the crate compares the results of the isolation logic with the results from the track/shower max comparison for a .8x.8 region. The result is 18 3-bit histogram bins for the area. These bins count (1) the number of isolated electrons with no p_t track (photons), (2) the number with an exact p_t track match, and (3) the number with a p_t track mismatch, at each of the six thresholds. Within these same crates, the histogram results from multiple RMC cards are summed together over increasingly larger areas in the HSC Cards. The output of the HSC cards in the individual Isolated Electron Match Crates are then sent to a final HSC card in the Final Decision Crate, where the histograms are produced for the entire detector.

The total/missing transverse energy trigger uses the same raw calorimeter trigger tower pulseheight data as the isolated electron trigger. For this subsystem, each MLU card calculates the total E_T on a 12-bit linear scale for the 4x4 region of trigger towers. It uses this value as address to two MLUs to calculate the E_x and E_y values for that region of the detector. All three values are then sent to the Energy Card in the same crate. In this card, the E_T, E_x and E_y energy values for the entire crate are calculated and from there transmitted to the Energy Sum/Jet Threshold Crate.

In the Energy Sum/Jet Threshold Crate, the regional energy sums from all of the Energy Cards are summed together in the Energy Summation Cards. Each of these cards can sum the energies from 8 Energy Cards to produce a single E_T, E_x and E_y result for the entire area. The energies from each of the ESC cards are transmitted onto the Final Decision Crate, where a single ESC card makes the final summation to produce the E_T, E_x and E_y values for the entire detector, and delivers them in turn as to the FDM card, where the missing energy is calculated from E_x and E_y.

The jet threshold trigger also uses the calorimeter energy data. This trigger begins on the Energy Card in the Calorimeter Isolation/Summation Crates. It takes the E_T value computed for each .4x.4 area by the MLU cards and compares it to one of 8 thresholds. It then sums the number of the 8 .4x.4 jet towers, one from each MLU card, which are at each threshold. This histogram result is transmitted alongside the with the E_T, E_x and E_y transverse energy calculations to the Energy Sum/Jet Threshold Crate.

In this crate, the histogram summation is continued in the Jet Threshold Summation Cards. Each of these cards can sum the histogram data from 8 Energy Cards to produce a single result consisting of 8 threshold bins, with 5 bits per bin. The histogram results of each of the 4 JTSC cards are transmitted to the Final Decision Crate, where a single JTSC card computes the histogram values for the entire detector.

Finally, there is the muon trigger subsystem. Unlike the three previous trigger subsystems, this trigger subsystem consists of a physical subsystem which stands alone until correlation is performed in the final decision logic. Raw p_t data for the two highest p_t tracks in a $.2\eta$ x $.4\phi$ region is transmitted from the front end in each fiber optic cable to the Muon Logic Cards. Each MLC card then compares 24 p_t tracks from 12 cables with 4 thresholds via programmable MLUs. It then sums the number of tracks at each threshold into 4 3-bit histogram bins. The histogram bins are then transmitted to a Muon Summation Card in the same crate, which produces a single set of 4 3-bit histogram bins for the entire Muon Trigger Crate. These bins are then sent to the Final Decision Crate, where a single MSC card computes the histogram values for the entire detector.

All of the subsystem trigger data pipelines converge in the Final Decision Crate at the Final Decision Memory Lookup card. This card distills the data streams down into individual trigger vectors for each subsystem, with some correlation between subsystems. The trigger vectors are then sent to the Final Decision Logic card, where the individual triggers for the detector and prescale values are programmed in. The FDL card examines the trigger vectors according to the programmed criteria and produces the Level 1 Accept/Reject for the entire detector.

10 Physical Requirements

10.1 Crate Summary

Summary of Crate Usage in the Level 1 Final Decision Logic:

Crate Type	Quantity
Calorimeter Isolation/Summation	24
Track/Shower Max Match	12
Isolated Electron Match	6
Energy Sum/Jet Threshold	1
Muon Trigger	6
Final Decision	1
Total Crates:	50

10.2 Card Summary

Summary of Card Usage in the Level 1 Final Decision Logic:

Card Type	Nominal per Crate Usage	Total Quantity	Comments
Calorimeter MLU	8	192	
Calorimeter PRA	2	48	
Calorimeter Energy	1	24	
Track/Shower Max Match	8	96	
Isolated Electron RMC	8	48	
Isolated Electron HSC	2-3	16	incl. 1 card in Final Dec. Crate
Energy Summation	4	5	incl. 1 card in Final Dec. Crate
Jet Threshold Summation	4	5	incl. 1 card in Final Dec. Crate
Muon Logic	8	48	
Muon Summation	1	7	incl. 1 card in Final Dec. Crate
Final Decision MLU	1	1	
Final Decision Logic	1	1	
L1 Clock/Control Interface	1	50	1 each in all crates
DAQ Interface/Processor	1	50	1 each in all crates
L2 Trigger Interface	1	42	only in crates with L2 connection

10.3 ASIC Requirements

This section provides a preliminary assessment of custom ASICs which may need to be developed to implement the functionality described in this document. The need for an ASIC is determined by identifying those cases on the above defined cards where there is a critical need for density or speed in a functional block that cannot be met by off-the-shelf commercial devices.

The first ASIC candidate is a 12-bit adder block. This would be a fixed-point 12-bit adder node with 2 or 4 inputs. It would be able to perform a summation on 2 inputs in a single 16ns crossing clock, or on 4 inputs over two 16ns clocks in a pipeline fashion. The primary area of need for this ASIC would be on the Calorimeter MLU card and Energy cards, where it would be used to sum the large number of 12-bit E_T, E_x and E_y values present on those cards within the limited board space available to dedicate to that function.

The next ASIC candidate has already been well-defined and named as the Pattern Recognition ASIC (PRA). This ASIC has the function of performing a longitudinal isolation cut on an 8x8 array of trigger towers, at any one of six different energy thresholds. This

ASIC would utilize the high densities available with BiCMOS technology to perform its function in an board area many times smaller than what would be required with general purpose logic. Six of these ASICs will reside on each Calorimeter PRA card. For a total of 6x48, or 288 PRAs, for the detector.

The task of correlating shower max hits with track p_t values also may require an ASIC. This ASIC would be a 5-bit magnitude selector node. This node would have 2 or 4 5-bit inputs, from which it would propagate the largest value to the output. This function is required to find the largest p_t track in $.2\phi$ with a shower max hit from among the 32 tracks in $.00625\phi$. The blocks would be stacked in a tree structure to examine the total $.2\phi$ area. This ASIC would be used on the Track/Shower Max Hit cards.

Thus, there are three candidate ASICs at this time for the level 1 trigger decision logic: a 12-bit adder node, an isolation pattern recognition circuit, and a 5-bit magnitude selector.

11 Fiber Optic Cable Data Formats

This section shows the data formats for the fiber optic cables which transmit data from the front end subsystem crates to the level 1 trigger processing crates off of the detector. There are 4 format types: one each for calorimeter trigger towers, tracker p_t values, shower max hits, and muon p_t/ϕ bin data. A description of the fiber optic data transmission design can be found in [4].

11.1 Calorimeter EMC/HAC Energy Cable

The following table shows the format for the data cable which transmits the EMC and HAC energies from the calorimeter front end to the MLU cards:

Bits(s)	Definition
0 to 7	EMC Energy, compressed format
8 to 15	HAC Energy, compressed format

A fiber is used to transmit the raw EMC and HAC pulsehight energies as 8-bits each of compressed data for each .1x.1 trigger tower. Each MLU card receives 16 fibers, for a total of approximately 3072 such fibers for the entire calorimeter.

11.2 Tracker p_t Cable

The following table shows the format for the data cable which transmits the raw p_t values from the tracker:

Bits(s)	Definition
0 to 3	p_T for ϕ-bin 0
4 to 7	p_T for ϕ-bin 1
8 to 11	p_T for ϕ-bin 2
12 to 15	p_T for ϕ-bin 3

Each fiber transmits four ϕ-bin p_t values. Each ϕ-bin corresponds to a region 1.6η x $.00625\phi$. The total region covered by a fiber is 1.6η x $.025\phi$. Each Track/Shower Max Match card receives 8 of these fibers, for a total of approximatly 760 such fibers for the entire outer tracking subsystem.

11.3 Shower Max Hit Cable

The following table shows the format for the data cable which transmits the raw flags from the shower max detector:

Bits(s)	Definition
0	hit flag for channel 0
1	hit flag for channel 1
2	hit flag for channel 2
3	hit flag for channel 3
4	hit flag for channel 4
5	hit flag for channel 5
6	hit flag for channel 6
7	hit flag for channel 7
8	hit flag for channel 8
9	hit flag for channel 9
10	hit flag for channel 10
11	hit flag for channel 11
12	hit flag for channel 12
13	hit flag for channel 13
14	hit flag for channel 14
15	hit flag for channel 15

Each fiber transmits 16 shower max hit flags. Each flag corresponds to a region $.2\eta$ x $.00625\phi$. An active flag indicates a shower max hit was detected in that region. The total region covered by a fiber is $.2\eta$ x $.2\phi$. Each Track/Shower Max Match card receives 16 of these fibers, for a total of approximately 1520 such fibers for the entire shower max detector.

11.4 Muon Data Cable

The following table shows the format for the data cable which transmits the raw p_t and ϕ data from the muon subsystem:

Bits(s)	Definition
0 to 2	p_t for track 0
3 to 7	ϕ for track 0
8 to 10	p_t for track 1
11 to 15	ϕ for track 1

Each fiber transmits a 3-bit p_t code and 5-bits of ϕ bin information for the two largest tracks in a $.2\eta$ x $.4\phi$ region. The 5-bits of bin information thus provide a granularity of $.00625\phi$. Each Muon Logic card receives 12 of these fibers, for a total of approximately 580 such fibers for the entire muon subsystem.

11.5 Fiber Optic Cable Summary

The following table shows a summary of the four subsystem fiber optic data cable quantities and formats, as described in the previous sections:

System	Quantity	Bits	Definition
Calorimeter	3072	0–7	EMC Energy, compressed
		8–15	HAC Energy, compressed
Tracker	768	0–3	p_T for ϕ-bin 0
		4–7	p_T for ϕ-bin 1
		8–11	p_T for ϕ-bin 2
		12–15	p_T for ϕ-bin 3
Shower Max	1536	0–15	Hit flags for regions 0–15
Muon	576	0–2	p_T for track 0
		3–7	ϕ-bin for track 0
		8–10	p_T for track 1
		11–15	ϕ-bin for track 1
Total:	5952		

References

[1] T. Gorski, J. Lackey, W.H. Smith, W. Temple, *Isolated Electron Pattern Logic Design and Performance at the SSC*, SDC Note SDC-91-00087, 1991.

[2] W. H. Smith, T. Gorski, J. Lackey, *SDC Trigger Preliminary Conceptual Design*, SDC Note SDC-91-00090, 1991.

[3] W. H. Smith, T. Gorski, J. Lackey, *SDC Global Level 1 Processor: Clock & Control*, SDC Note SDC-91-00090, 1991.

[4] M. Thompson, *Fiber Optic Data Transmission for the SDC Detector*, SDC Note SDC-91-00092, 1991.

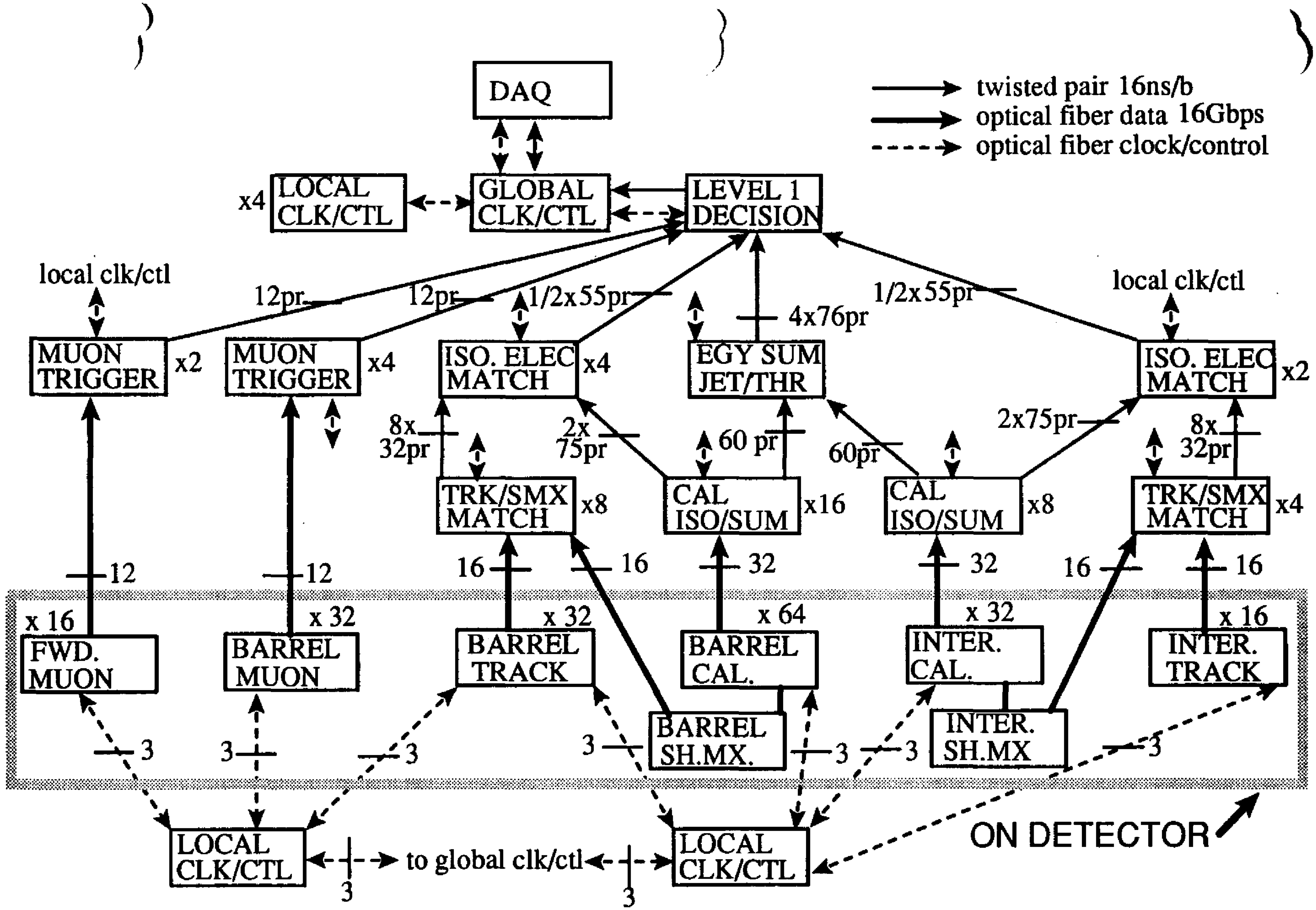


Figure 1. Level 1 Trigger Structure

Calorimeter Isolation/Summation Crate

Number of Crates: 16 barrel, 8 intermediate

Coverage: 1.6 η by 0.8 ϕ

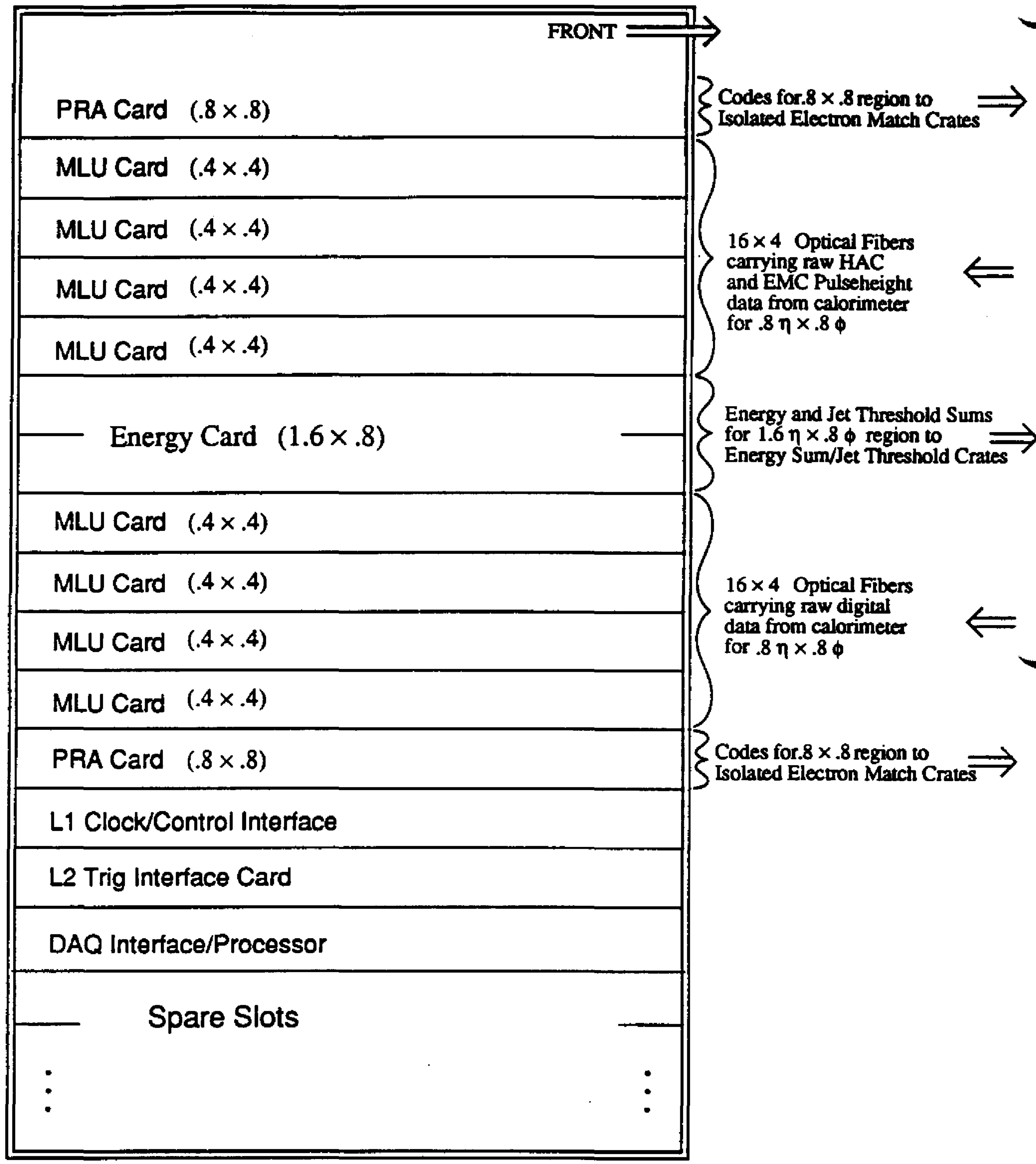


Figure 2

Calorimeter Memory Lookup Card
(MLU Card)

Coverage: $0.4\,\eta \times 0.4\,\phi$

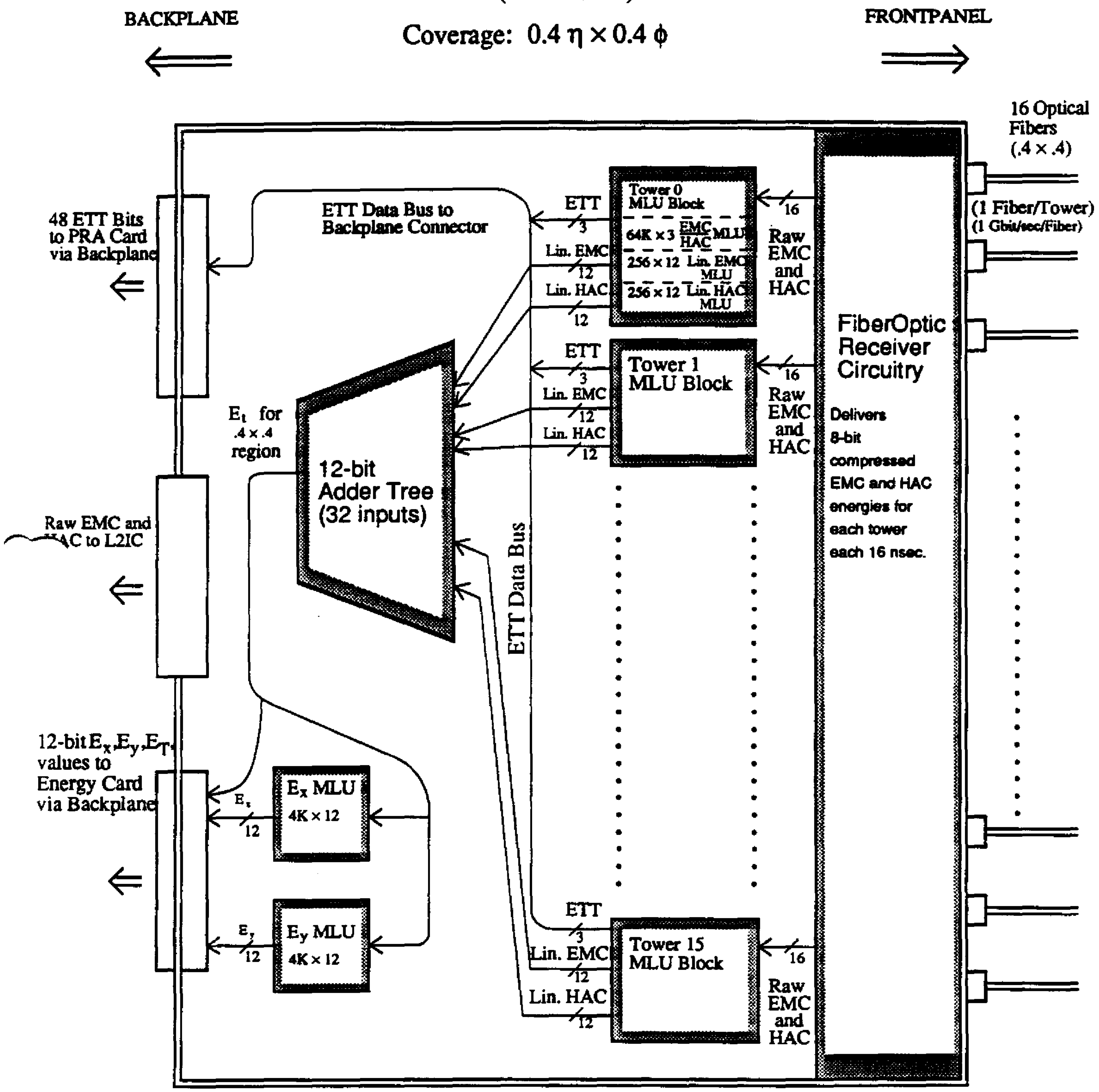
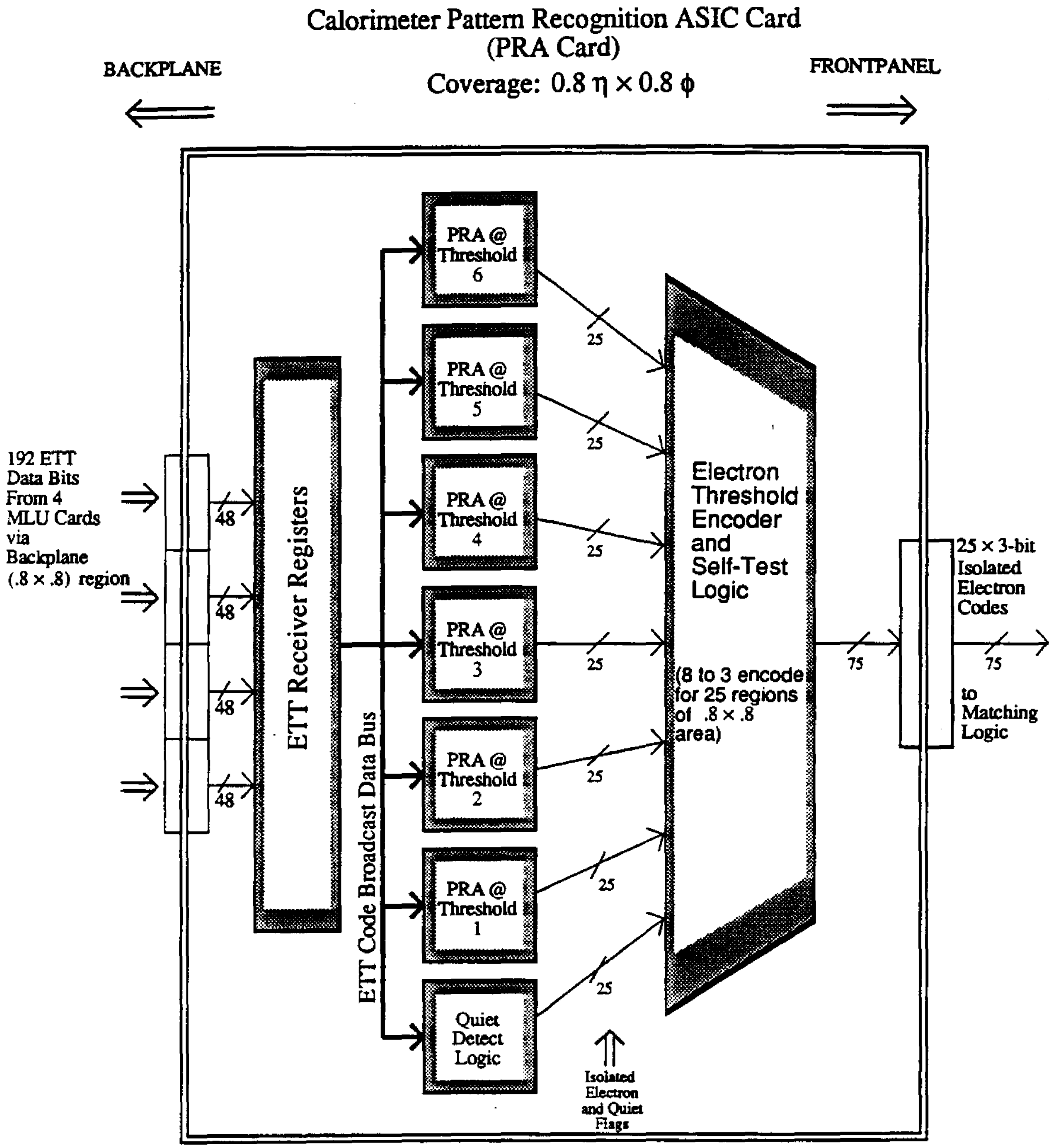
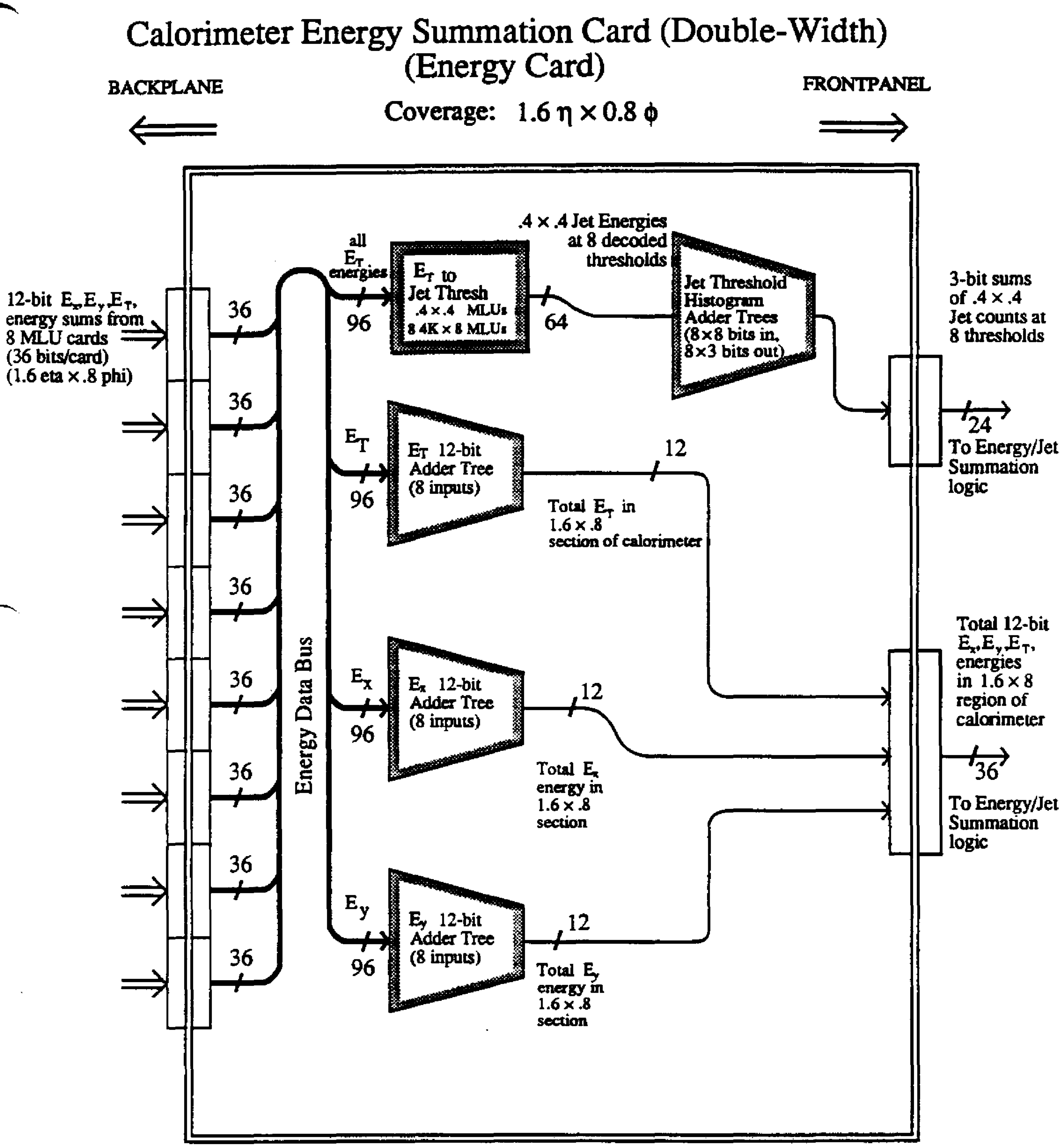


Figure 3



Calorimeter Pattern Recognition ASIC Card
(PRA Card)
Coverage: 0.8 η × 0.8 φ
BACKPLANE
FRONTPANEL
192 ETT Data Bits From 4 MLU Cards via Backplane (.8 × .8) region
48
48
48
48
ETT Receiver Registers
ETT Code Broadcast Data Bus
PRA @ Threshold 6
PRA @ Threshold 5
PRA @ Threshold 4
PRA @ Threshold 3
PRA @ Threshold 2
PRA @ Threshold 1
Quiet Detect Logic
25
25
25
25
25
25
25
Electron Threshold Encoder and Self-Test Logic
(8 to 3 encode for 25 regions of .8 × .8 area)
Isolated Electron and Quiet Flags
75
75
25 × 3-bit Isolated Electron Codes
to Matching Logic

Figure 4



Calorimeter Energy Summation Card (Double-Width)
(Energy Card)
BACKPLANE
FRONTPANEL
Coverage: 1.6 η × 0.8 φ
12-bit Ex,Ey,ET, energy sums from 8 MLU cards (36 bits/card) (1.6 eta × .8 phi)
36
all ET energies
96
ET to Jet Thresh .4×.4 MLUs 8 4K × 8 MLUs
64
.4 × .4 Jet Energies at 8 decoded thresholds
Jet Threshold Histogram Adder Trees (8×8 bits in, 8×3 bits out)
3-bit sums of .4 × .4 Jet counts at 8 thresholds
24
To Energy/Jet Summation logic
ET
ET 12-bit Adder Tree (8 inputs)
12
Total ET in 1.6 × .8 section of calorimeter
Energy Data Bus
Ex
Ex 12-bit Adder Tree (8 inputs)
Total Ex energy in 1.6 × .8 section
Ey
Ey 12-bit Adder Tree (8 inputs)
Total Ey energy in 1.6 × .8 section
Total 12-bit Ex,Ey,ET, energies in 1.6 × 8 region of calorimeter
36
To Energy/Jet Summation logic

Figure 5

Track/Shower Max Match Crate

Number of Crates: 8 barrel, 4 intermediate

Coverage: 1.6 η by 0.8 φ

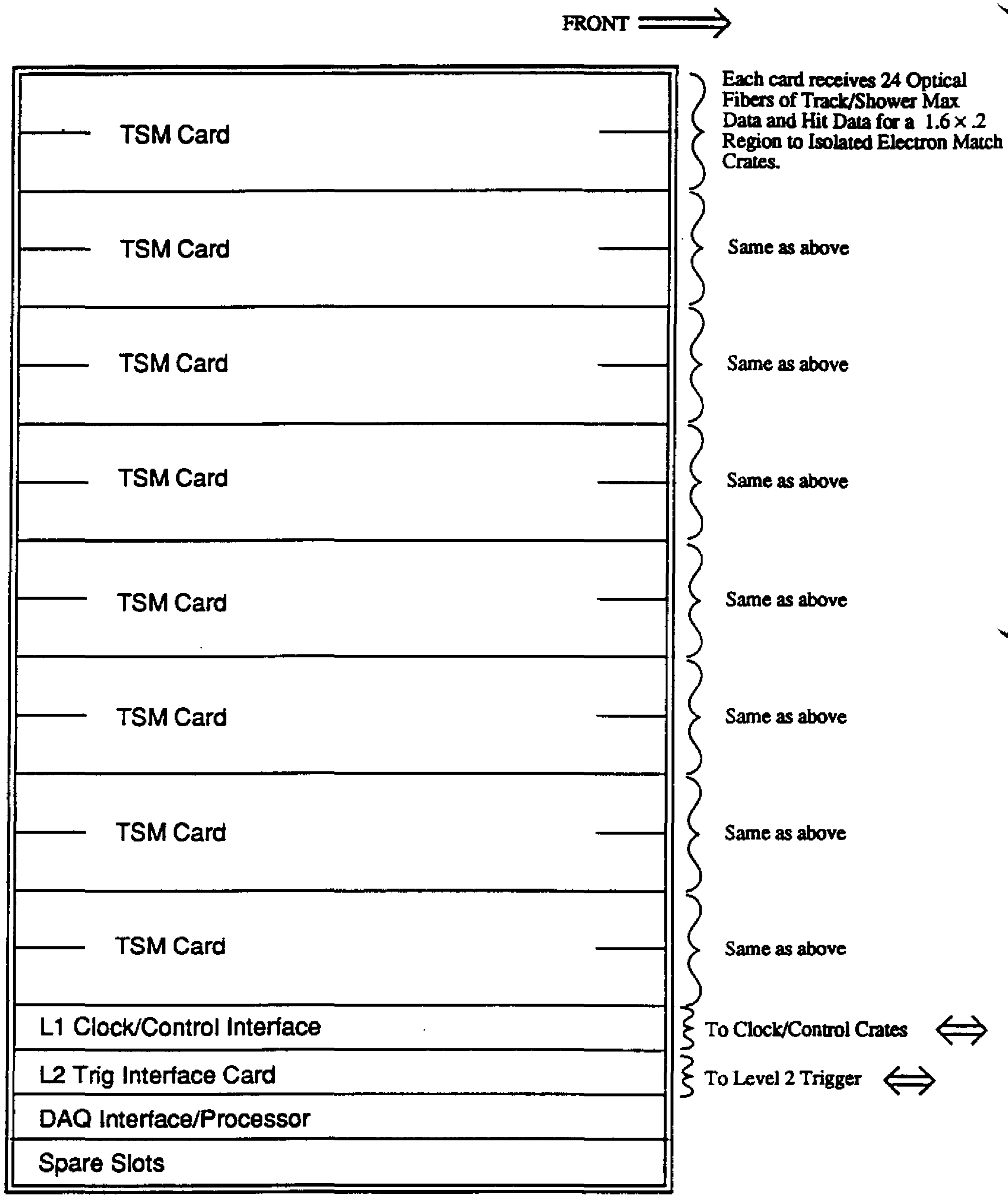


Figure 6

Tracker/Shower Max Hit Card (Double-Width Card)
(TSM Card)

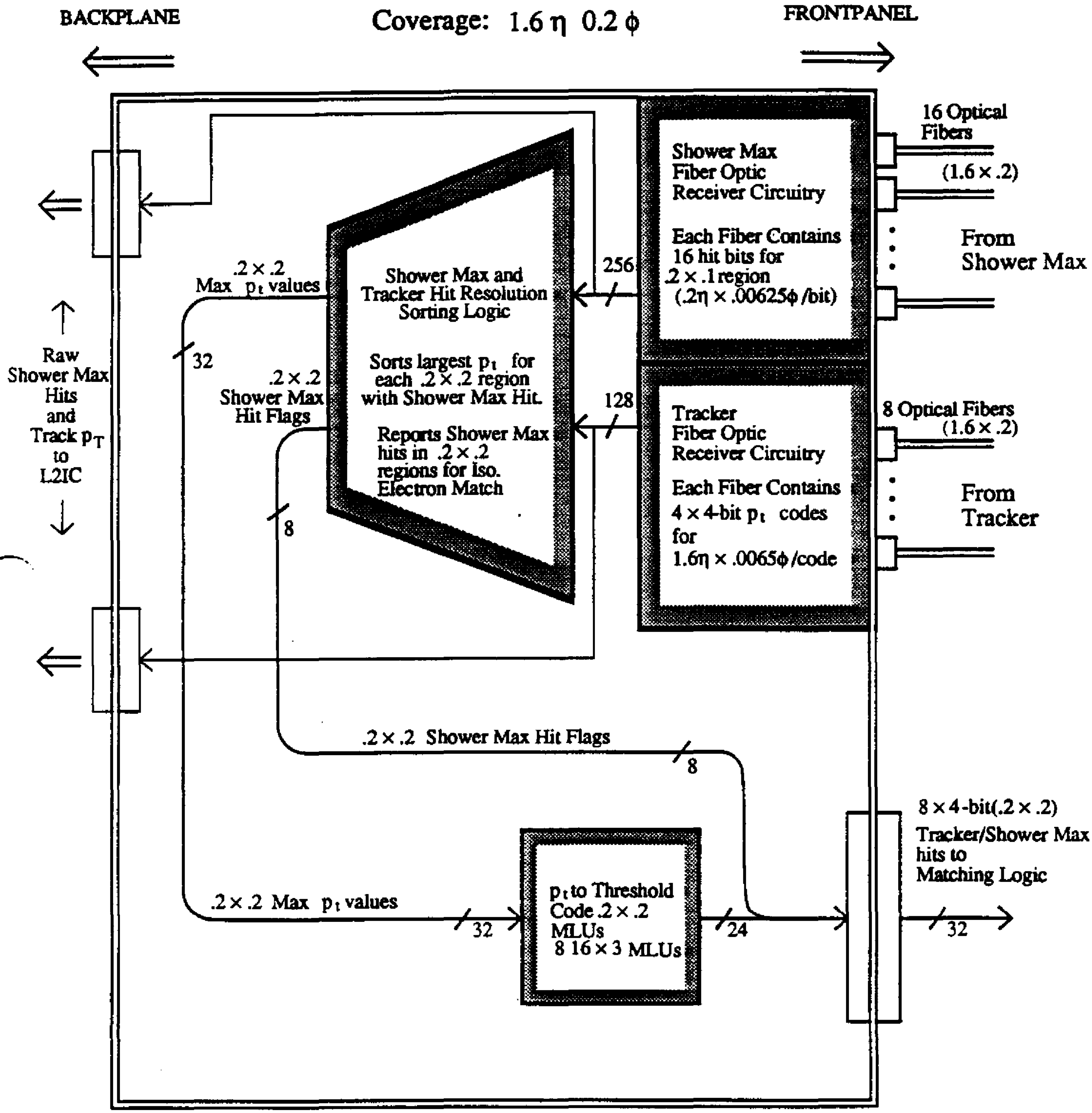


Figure 7

Isolated Electron Match Crate

Number of Crates: 4 barrel, 2 intermediate

Coverage: 1.6 η by 3.2 ϕ

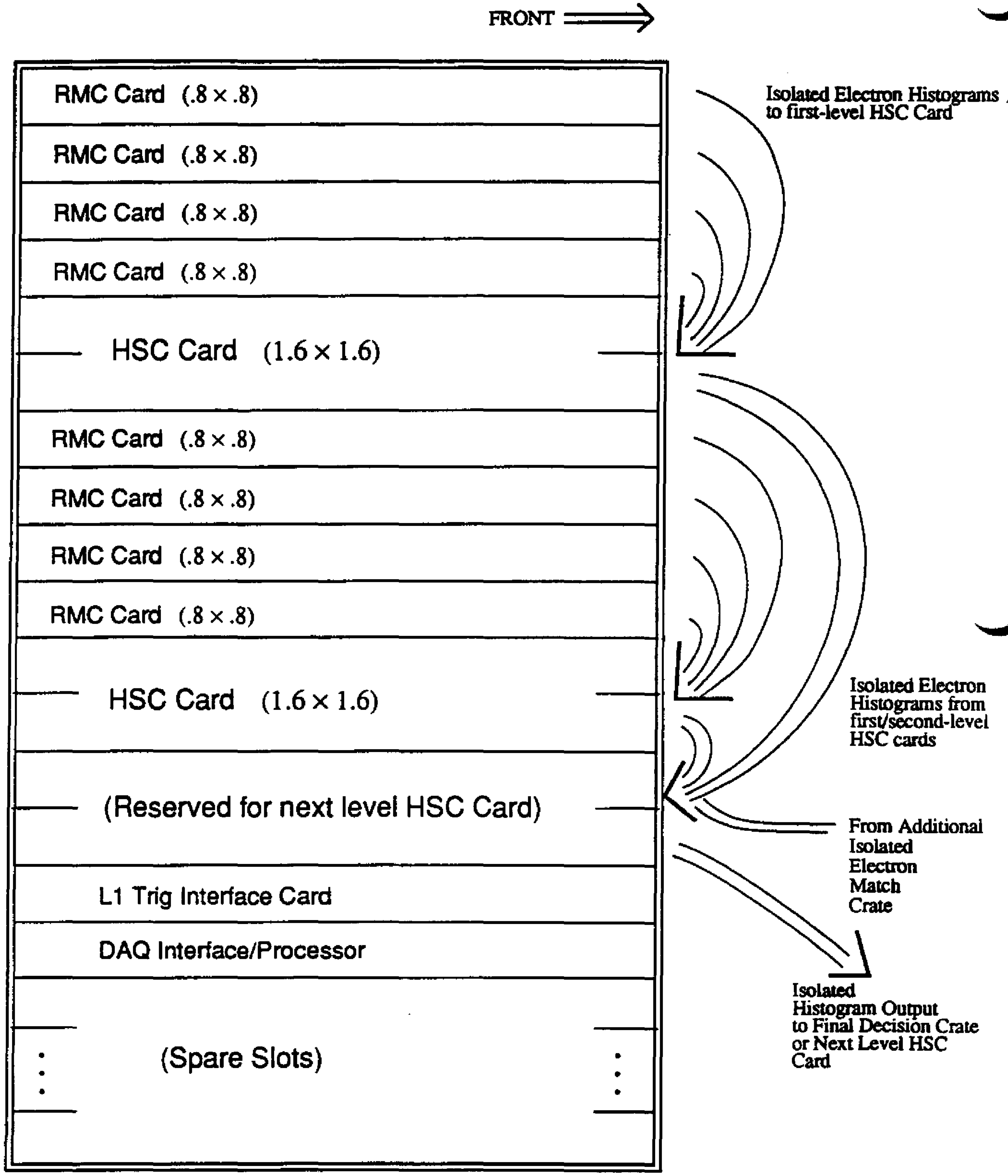


Figure 8

.2 × .2 Region Match Card (RMC Card)

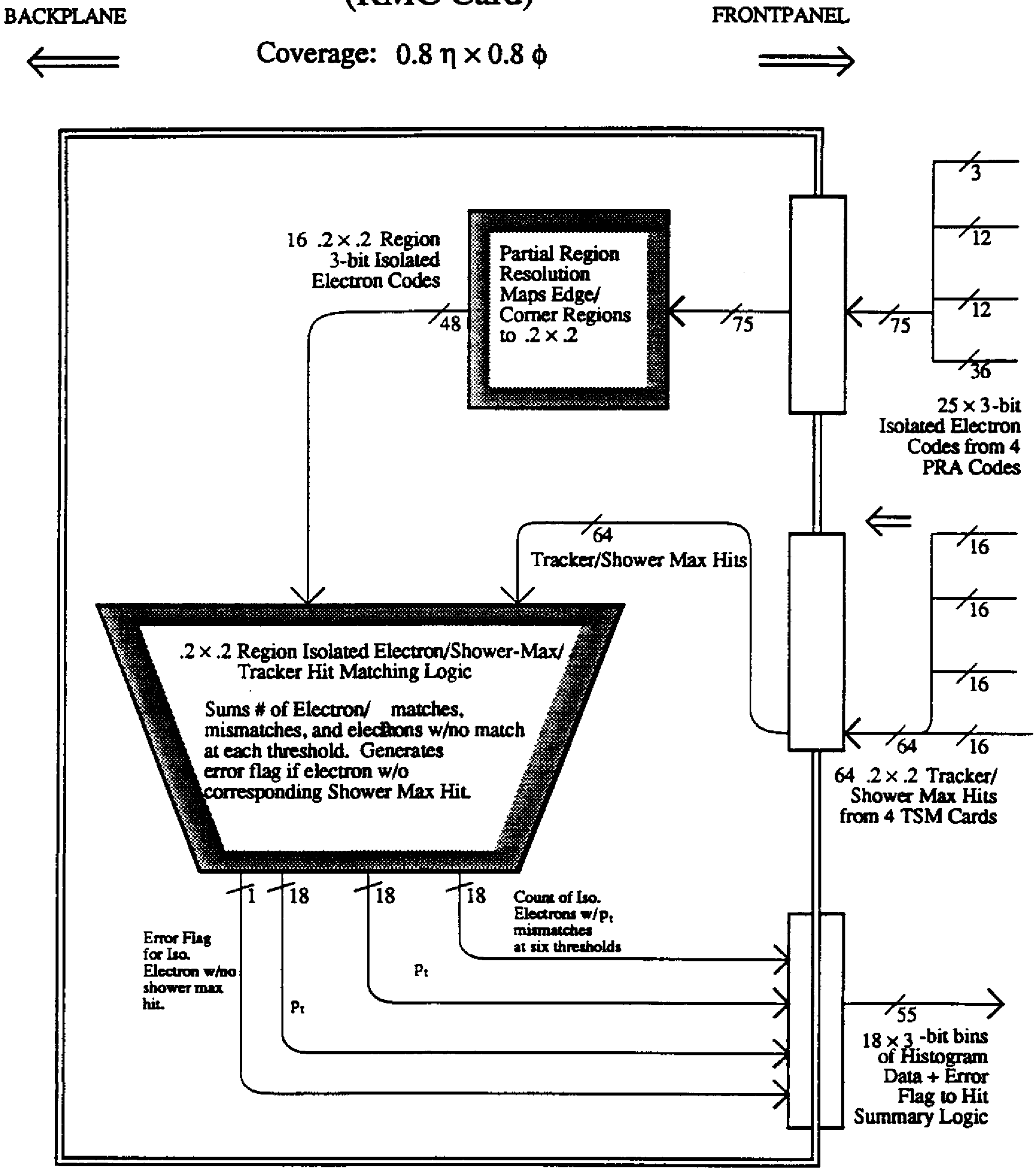


Figure 9

Isolated Electron Hit Summation Card (Double-Width)
(HSC Card)

BACKPLANE ⟸ Coverage: 4 RMC or HSC sources ⟹ FRONTPANEL

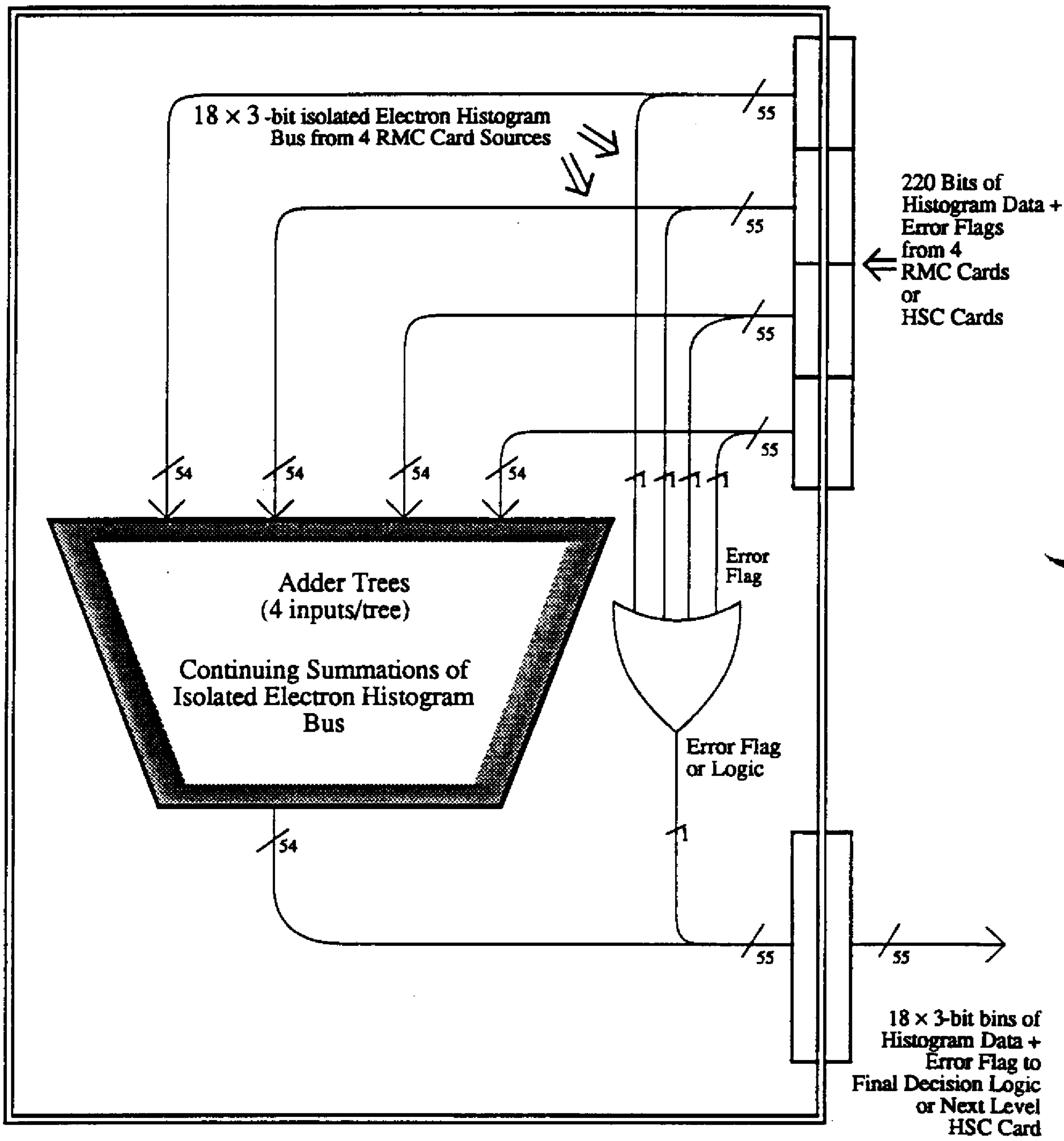


Figure 10

Energy Sum/Jet Threshold Crate

Number of Crates: 1 for both barrel and intermediate

Coverage: entire detector

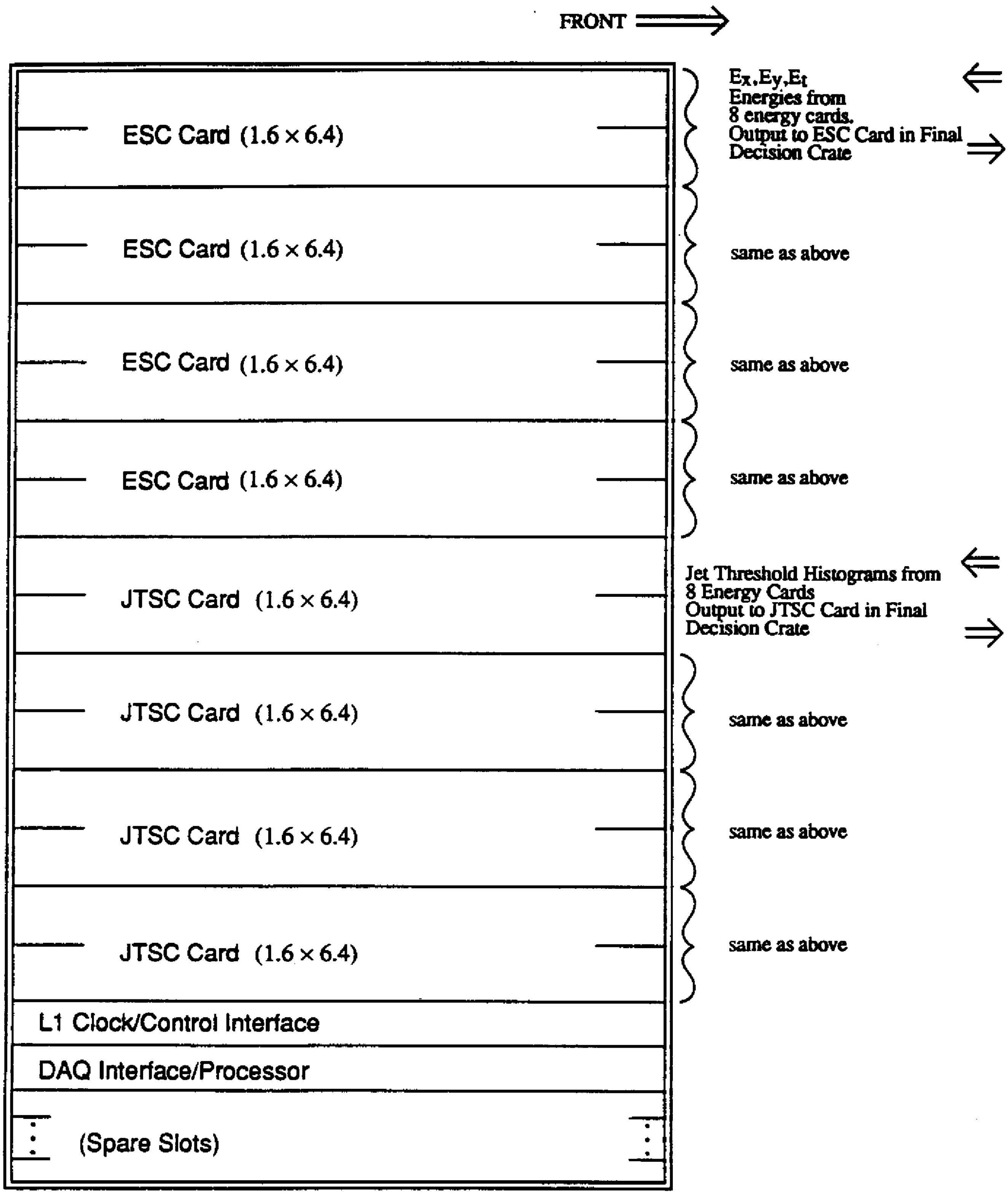


Figure 11

8 to 1 Energy Summation Card (Double-Width) (ESC Card)

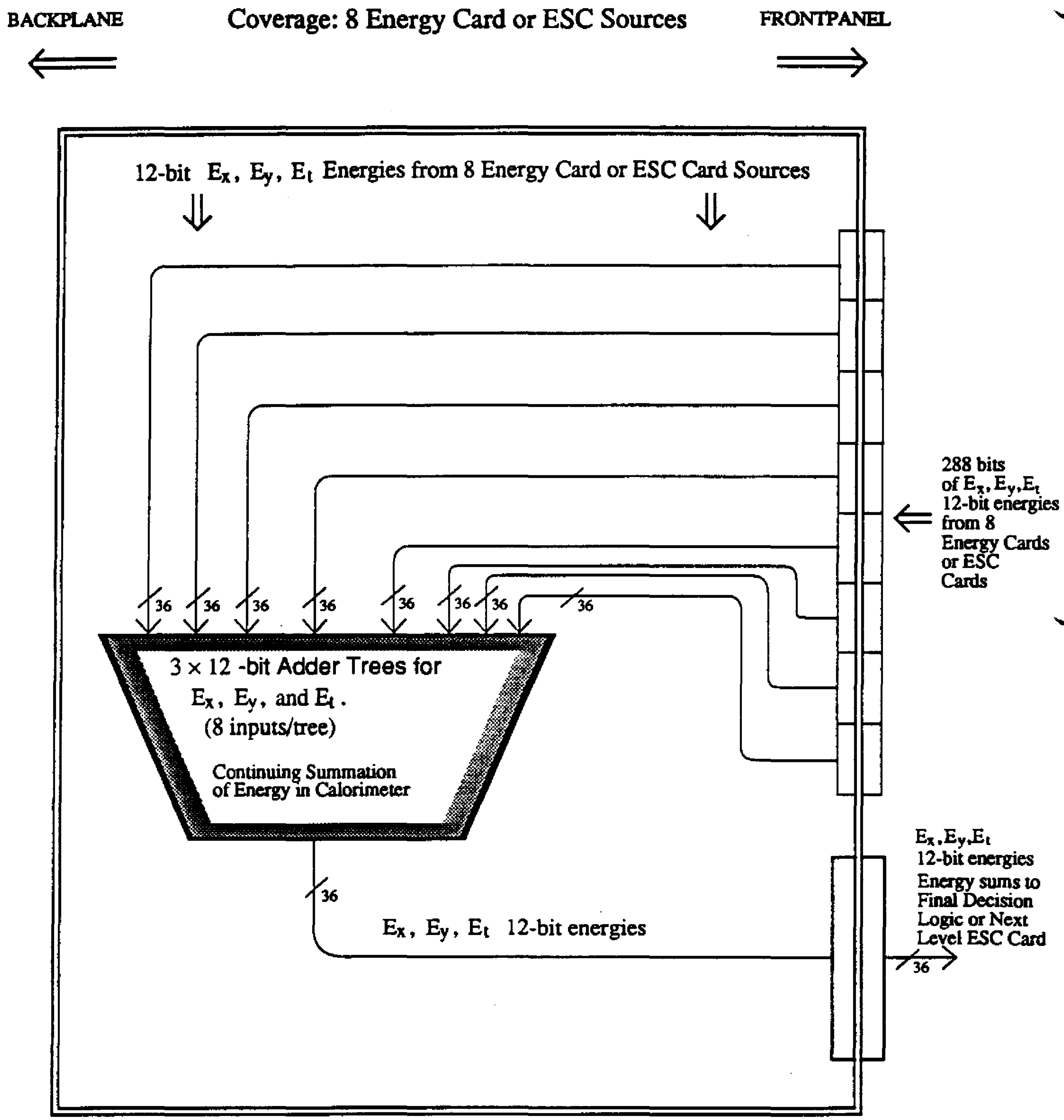


Figure 12

8 to 1 Jet Threshold Summation Card (Double-Width)
(JTSC Card)

BACKPLANE

Coverage: 8 Energy Card or JTSC Sources

FRONTPANEL

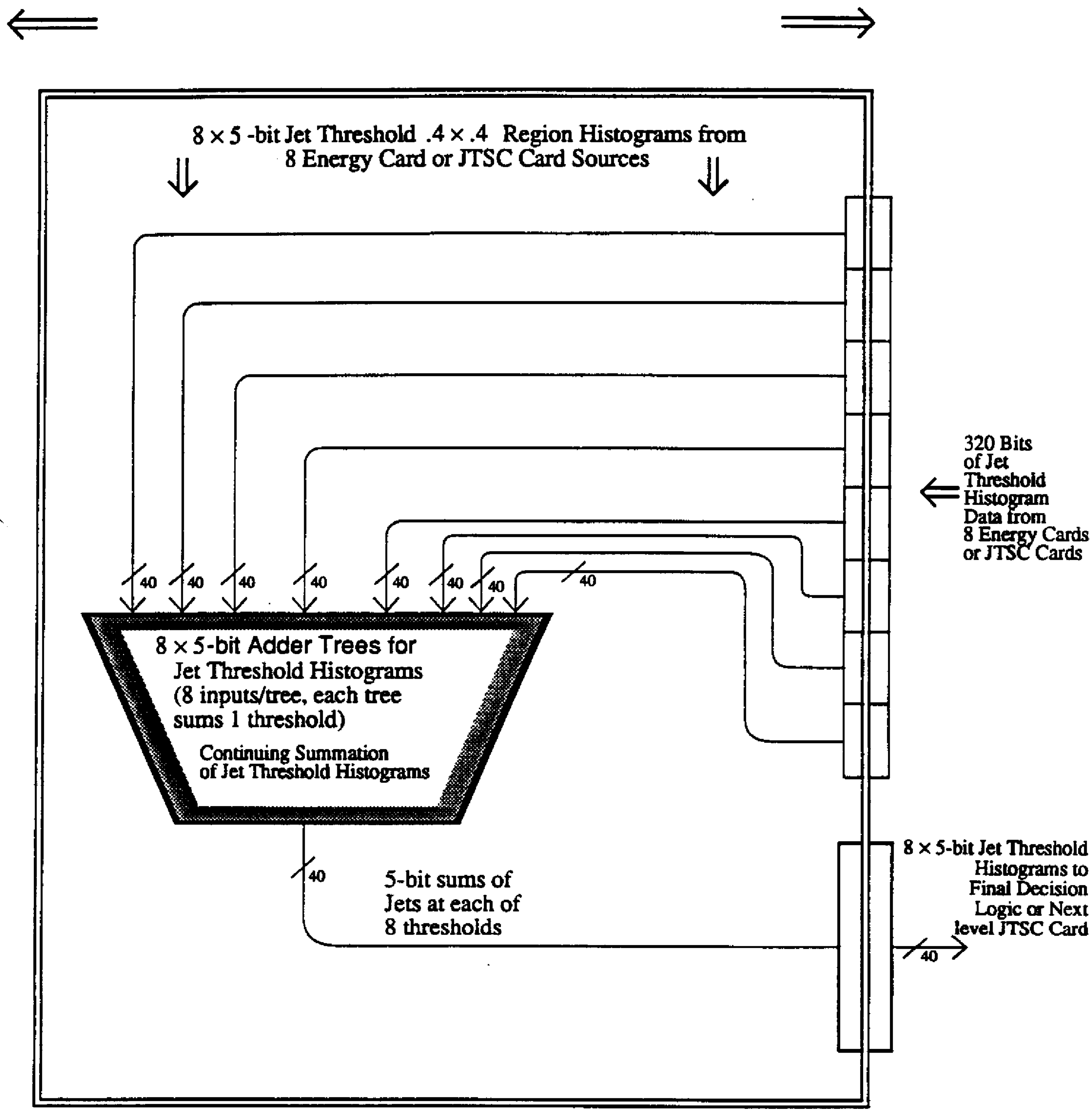


Figure 13

Muon Trigger Crates

Number of Crates: 4 barrel +, 2 intermediate
Coverage: 1.2 $\eta \times 6.4\ \phi$

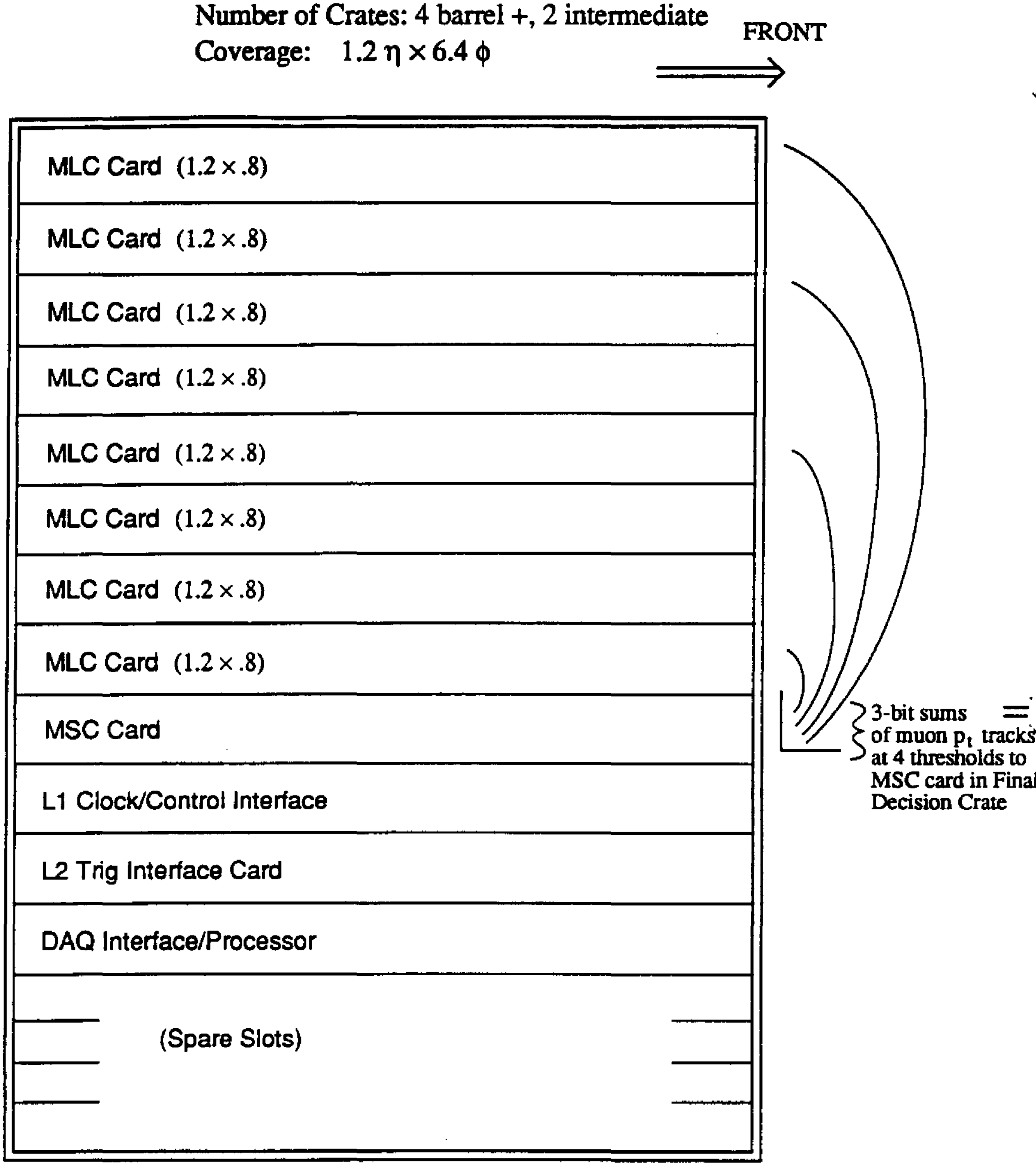


Figure 14

Muon Logic Card
(MLC Card)

Coverage: $1.2\,\eta \times 0.8\,\phi$

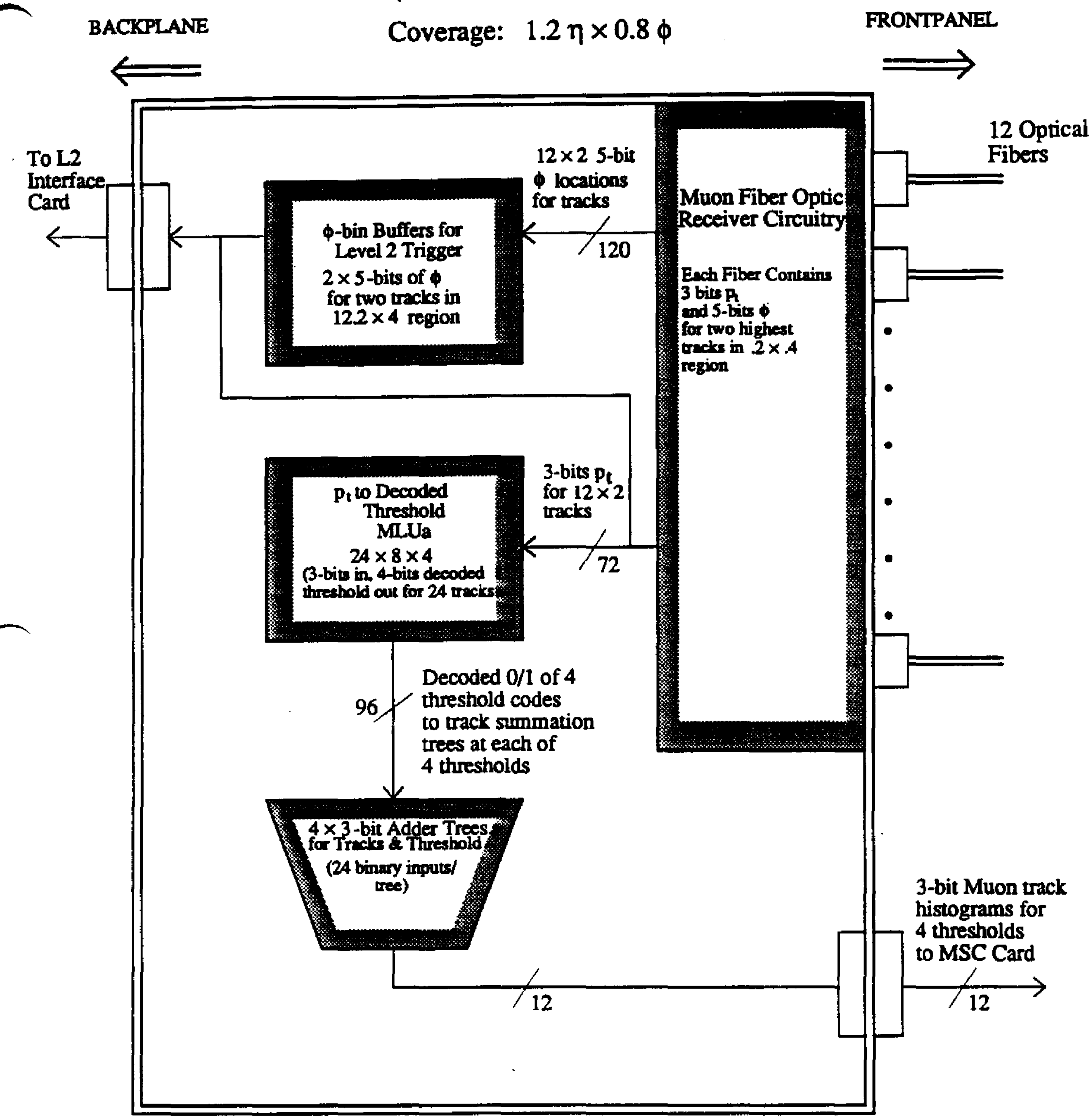


Figure 15

Muon Summation Card
(MSC Card)

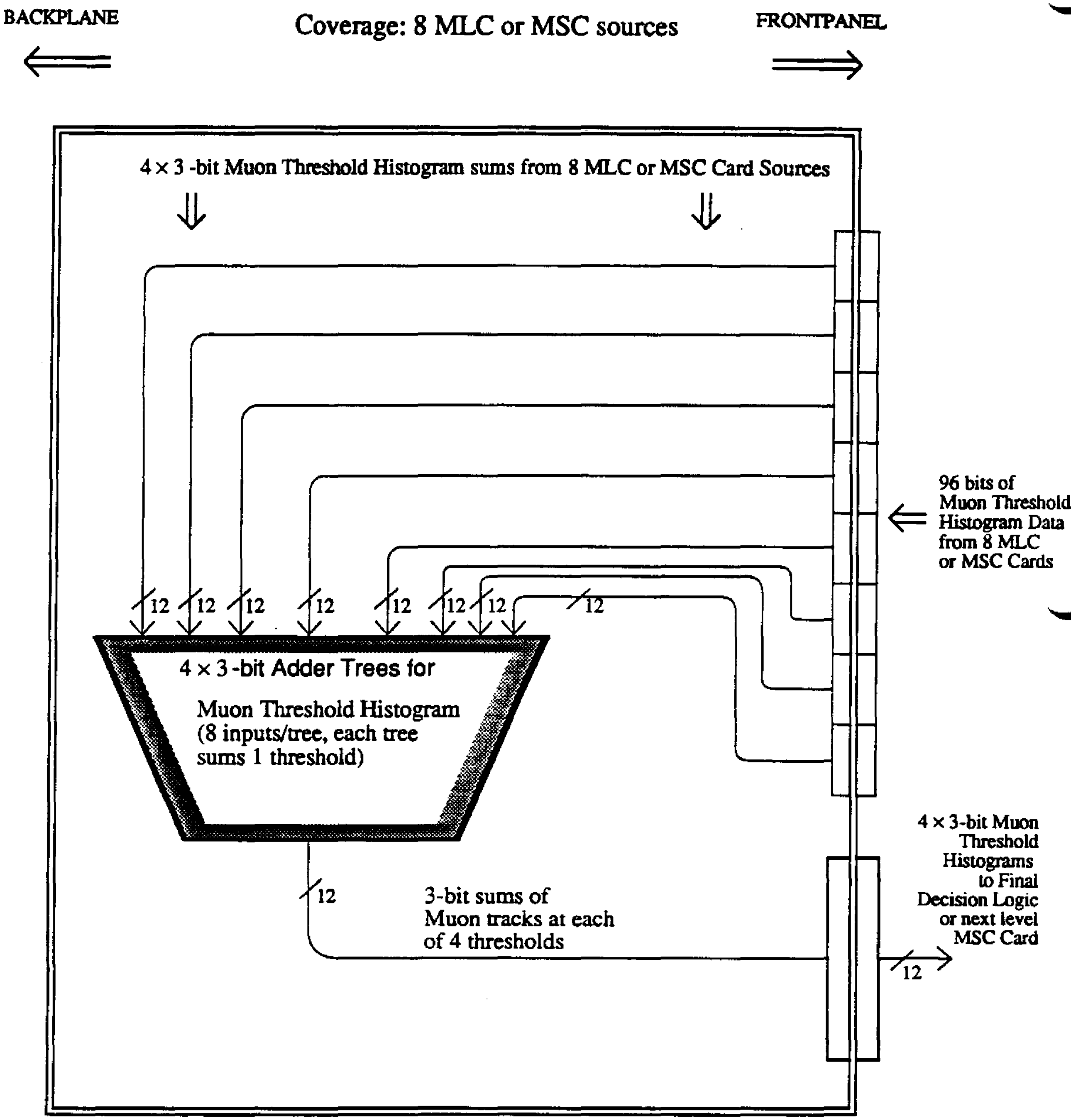


Figure 16

Final Decision Crate

Number of Crates: 1
Coverage: Entire Detector

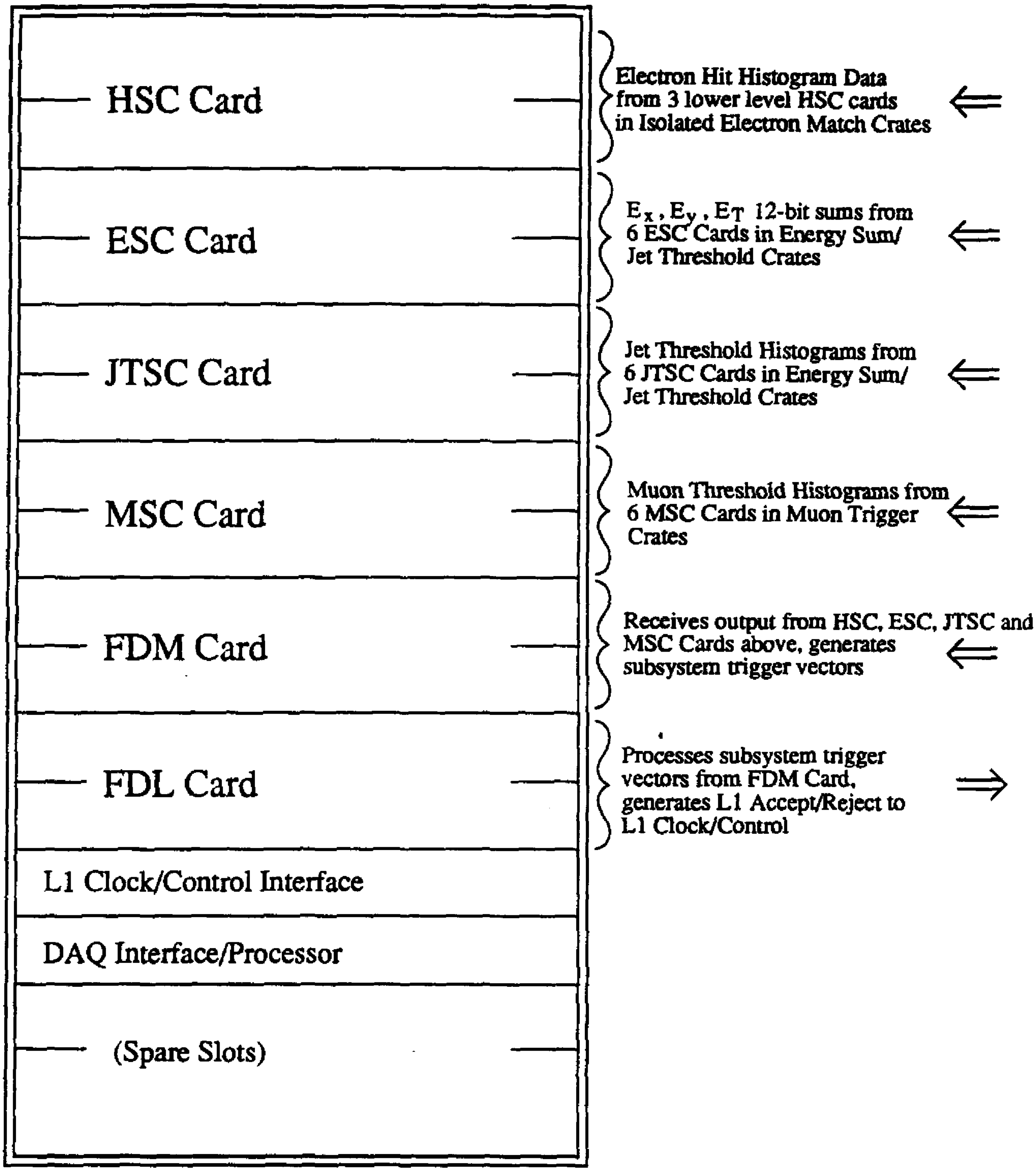


Figure 17

Final Decision Memory Lookup Card (Double-Width) (FDM Card)

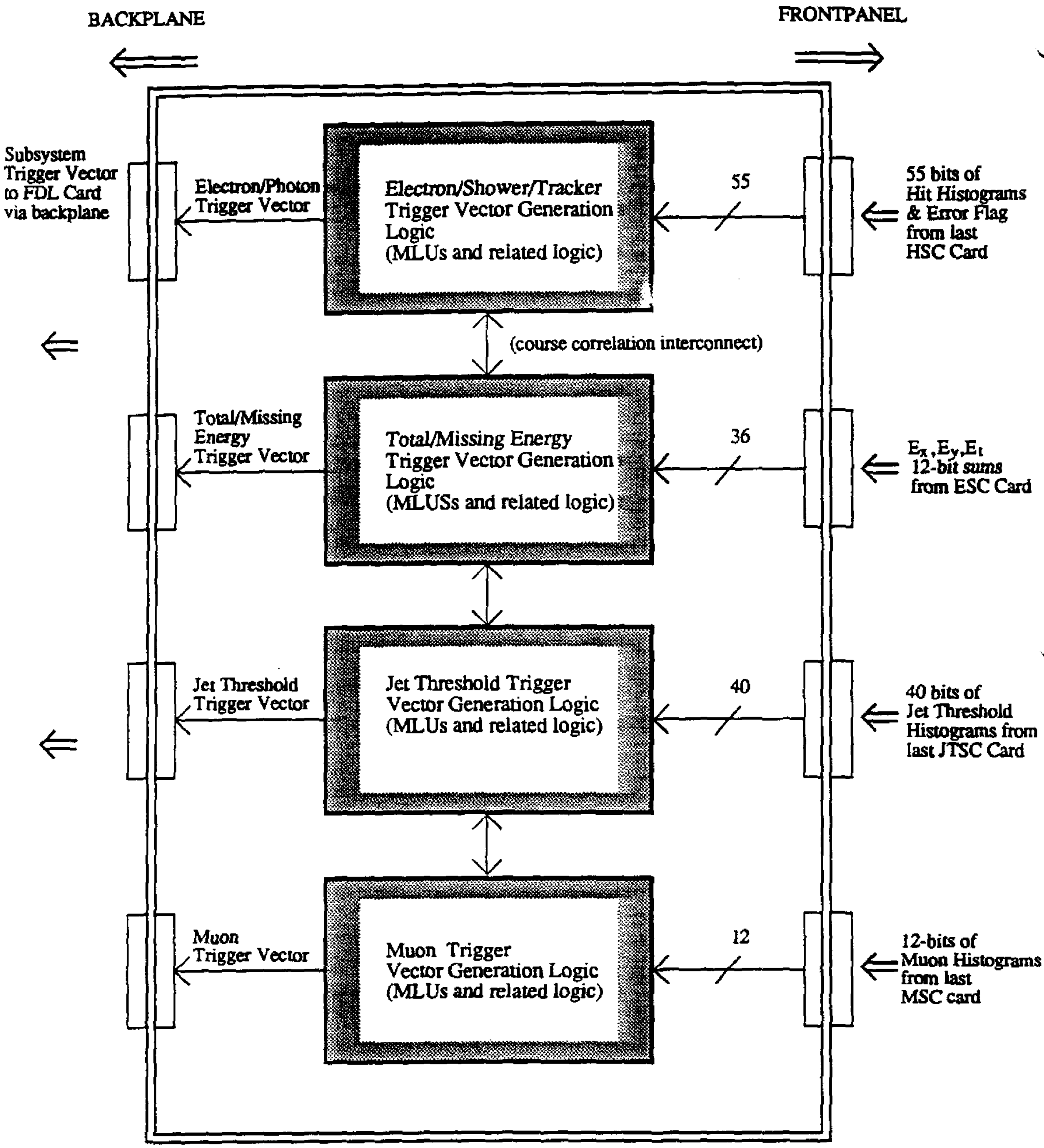


Figure 18

Final Decision Logic Card (Double-Width) (FDL Card)

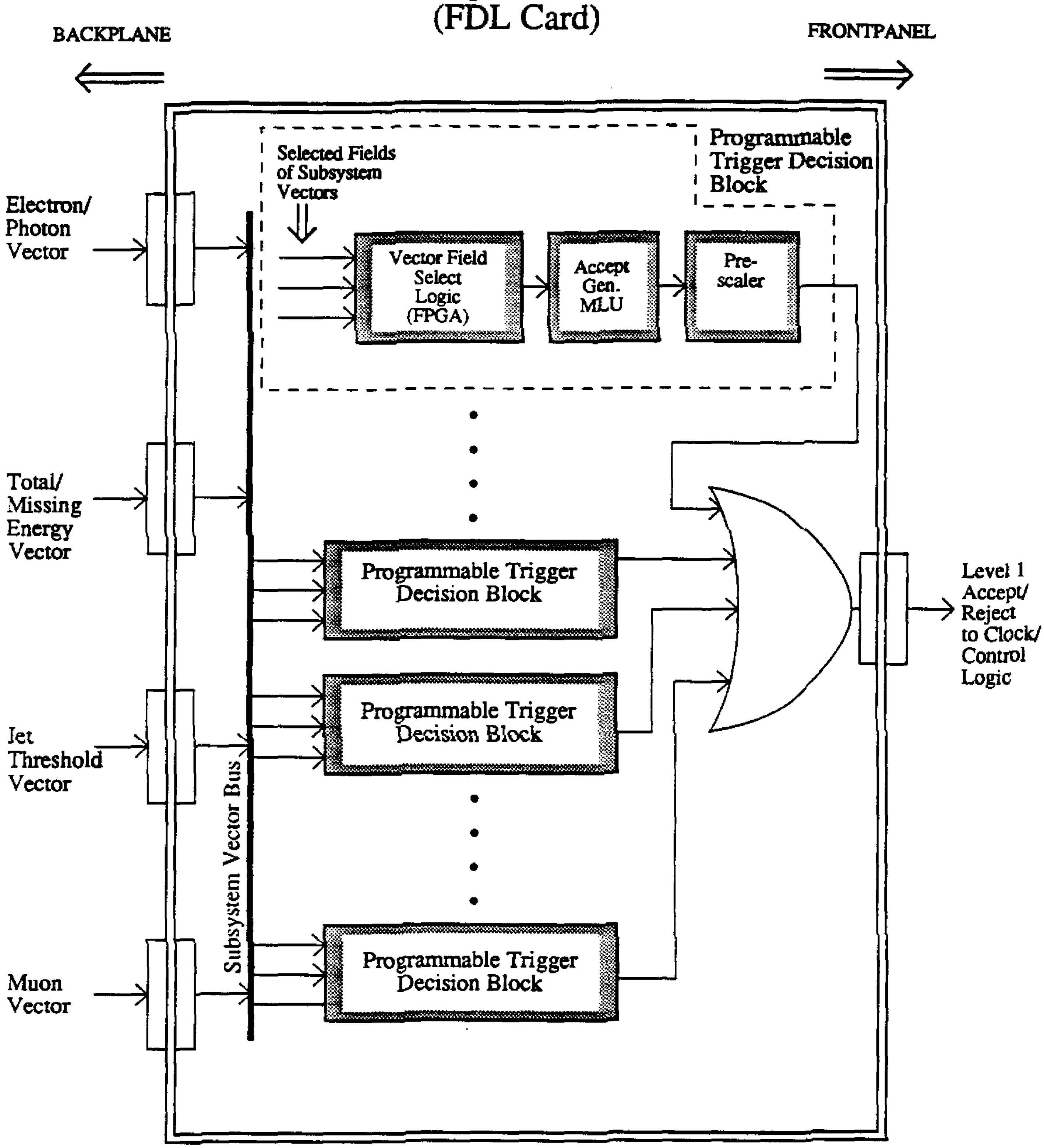


Figure 19