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THE BEAM SWITCHYARD INTERLOCK STATUS SCANNER

INTRODUCTION

One of the main functions performed by the computer is to scan, every 1/360 second, a thousand or more (ON/OFF) interlock status signals inside the Beam Switchyard. The computer under program control scans these signals, detects changes in them, identifies them and prints them out on a typewriter or on a printer. Aside from the time required for printing interlock status changes, the actual time for scanning, detecting, and identifying is rather short compared to 1/360 second (2.8 μsec); consequently plenty of time is left over for the computer to perform other useful tasks in the Beam Switchyard.

Since the SDS 925 computer can only transfer 24 bits of data at a time from its peripheral devices, it is necessary to have some kind of multiplexing system that the computer can control in order to monitor a thousand or more status interlock signals. The ISS (Interlock Status Scanner), shown in Fig. 1, is such a kind of multiplexing system that can transfer 22 bits of data at a time to the computer. The 22 bits of data contain 16 bits of status signal data and 6 bits of address. The ISS can handle up to 1008 signals; that means the computer has to make 63 transfers, at 16 bits per transfer. A special SDS 925 instruction, BPI (Block Parallel Inputs) is used in the program for the interlock status scanner. This BPI instruction, a non-interruptable instruction, allows the computer to make as many transfers as specified by the program.

ISS SYSTEM DESIGN

The hardware of the interlock-status scanner is shown in Fig. 2 and consists of:

(a) Control Logic
(b) 6-bit Binary Up-Counter
(c) Decoder Logic
(d) AND/OR Gate Logic
(e) Level Converter
(f) Parity Generator
(g) 22-bit Register and Lamp Driver
(h) SDS 925 Interface

The control logic is synchronized with the computer under demand and response control, whose timing is achieved by several delay elements connected in series. The delays are set in accordance to how fast data can propagate through various logical hardware. These delays are minimized, so that the total delay through the system is only two computer cycle time (3.5 μsec).

The 6-bit binary up-counter consists of six flip-flops, and it is used as a memory and as a sequence selector.

The decoder logic contains 63 twelve-bit decoders. Each twelve-bit decoder decodes twelve signals from the 6-bit up-counter. Subsequently, the 1008 interlock status signals coming into the ISS can therefore be gated properly to the output by the decoder. Furthermore, the decoder provides a 6-bit address for each 16 bits of data that it has gated to the output.

The AND/OR gate logic contains 63 sets of 16 parallel AND-gate, and the outputs of each set of 16 parallel AND-gate are OR'ed to the next set; hence the output of each AND-gate is OR'ed to the other 62 AND-gates.

One stage of level conversion is required since the ISS voltage level requirements (0v and -3v) and that of the computer (0v and +8v) are different.

The BPI instruction requires the external peripheral device to generate its own odd-parity bit; consequently the ISS contains an odd-parity bit generator.

A 22-bit register is used as a buffer register in order to avoid the possibility of erroneous parity caused by changing input-status signals while the parity generator is in progress generating a parity.

And finally, the SDS 925 interface logic consists of low impedance cable drivers to ensure minimum signal deterioration.

ISS PRINCIPLE OF OPERATION

The operation of the interlock-status scanner can be summarized as follows: The computer under program control sends a test signal, skss, to the ISS to determine if it is ready to send data. If the ISS is not ready, the computer will try again after a few microseconds; if the ISS is ready the computer will proceed to send the next instruction, EOM (Energize Out Mode), to the ISS. A complete timing and synchronization of data transfer is shown in Fig. 3. The ISS, upon receiving the EOM instruction, enables the SDS 925 interface logic and resets the 6-bit counter to OO (Octal). At the rise of EOM signal, the $\overline{R_t}$ (Not Ready)

delay is set and the $\overline{R_t}$ signal becomes high (0v to +8v). During the period when $\overline{R_t}$ signal is high, the computer can neither transfer any data into its memory nor proceed to next instruction. The $\overline{R_t}$ relay is set so the interlock-status signals can have time to propagate through the logic circuit and settle in the interface logic. Also, at the rise of the EOM signal, an ISS propagation delay is set. This delay allows the interlock status signal to settle inside the ISS. At the end of ISS propagation delay, a signal Str (Strobe) is generated to strobe the data from the ISS into the 22-bit register. As soon as the interlock-status signals settle in the register, a correct parity bit is generated. The $\overline{R_t}$ delay time is adjusted to ensure that proper parity gets generated. When $\overline{R_t}$ becomes low (+8v to 0v), the computer transfers the data into its memory and sends the next instruction, BPI. The BPI instruction will generate as many PIN (Parallel Input) signals as specified by the program. Each PIN signal performs the function as the EOM signal. That is, each PIN signal steps up one count in the 6-bit counter, and sets off the $\overline{R_t}$ delay and the ISS propagation delay. The process repeats 63 times to transfer 1008 signals into the computer memory. Once the computer has received all 63 words, it then sends an $\overline{R_{ti}}$ (Acknowledge) signal that resets the 6-bit counter in the ISS. The total time necessary to make 63 transfers is approximately 320 μsec.

COMPUTER FUNCTION

As mentioned earlier, the computer is interrupted every 1/360 sec (2.8 μsec) to scan 1008 interlock and status signals in the Beam Switchyard. The ISS is a multiplexing system that allows the computer to monitor all 1008 signals in 320 μsec. Once the computer has gathered the data, it then proceeds to analyze the data.

First, the computer is programmed to compare the old data (2.8 msec old) with the new data. It compares them word by word. If there is no difference between the two, it then proceeds to compare the next word; however, if there is a difference, then the computer pursues further and compares the two words bit by bit. If there is no difference in the first bit, the computer goes on to the next bit. If there is a difference in the first bit, the computer then records the word number and the bit number in some location in the memory. The computer also detects how the failure occurred, that is, whether the failure went from a normal state to an abnormal state, or vice versa. Once the computer has done the recording, it then proceeds to compare the first bit until it has finished all

16 bits in that word, and then it proceeds to the next word. This process is kept up until the computer has exhaustively compared all 63 words and recorded errors found, if there are any. The analysis of interlock-status data takes approximately 70 to 400 μsec. The former time happens when the computer finds no errors, and the latter time happens when the computer finds a few errors. There is a limit to how many errors the computer can find every 2.8 μsec. This limit is set to 30 errors for the present; however, this number can be increased or decreased, if desired. The limit is necessary, otherwise the computer will spend all its time looking and recording errors. The present limit allows the computer to spend 30 percent of 2.8 msec for interlock-status scanning and to do other useful tasks the remainder of the time.

Once the computer has finished scanning and analyzing interlock-status signals, it will then proceed to do other work; or if there were errors found, it will then start printing data on the typewriter or on the printer. A coded format is adopted for print-out mainly because of economy in core storage and printing speed. The format is illustrated as follows:

GROUP	BIT	STATE	MIN	SEC	BEAM PULSE
07	12	+	15	31	267

The group code is a two-bit octal code ranging from 00 to 76 (0 through 62 in decimal), representing groups of interlocks or status signals. The bit code is also a two-bit octal code ranging from 00 to 17 (0 through 15 in decimal), representing individual interlock or status signals. The state code is indicated by a + sign or by a - sign: +, meaning the change has occurred from fault to normal, and -, meaning the change has occurred from normal to fault. Also along with each interlock or status print-out, a time is given to the closest beam pulse. Time is essential information for analyzing errors. Besides printing out interlock or status code and time, the computer is also programmed to keep track of real-time, so that every hour it can provide the time and date. The format is presented in the following manner:

MONTH	DAY	HOUR	MIN	
XX	XX	XX	XX	---

These three dashed lines at the end indicating month, day, hour, and minutes are printed, and not interlock or status print-out.

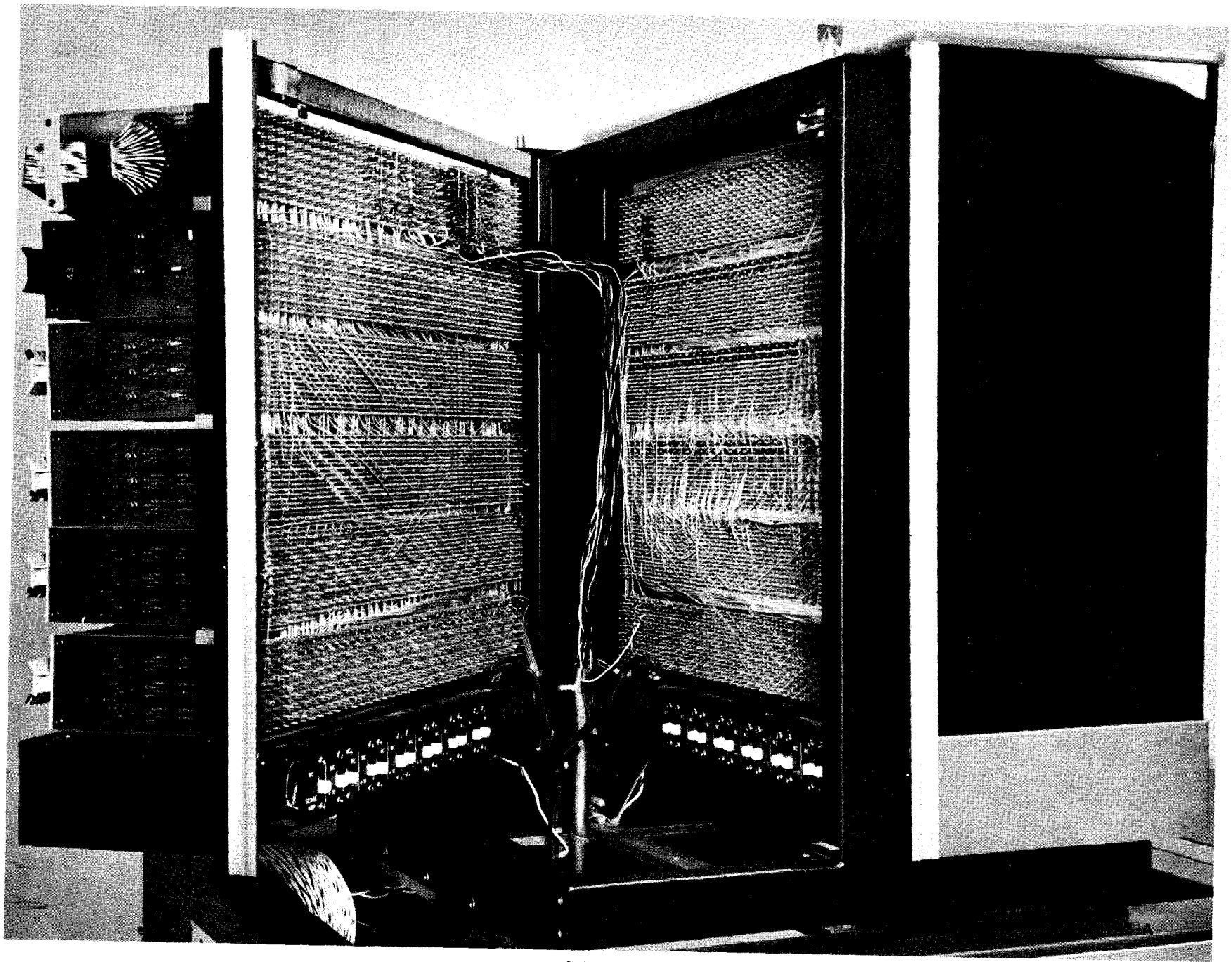

Figure 1

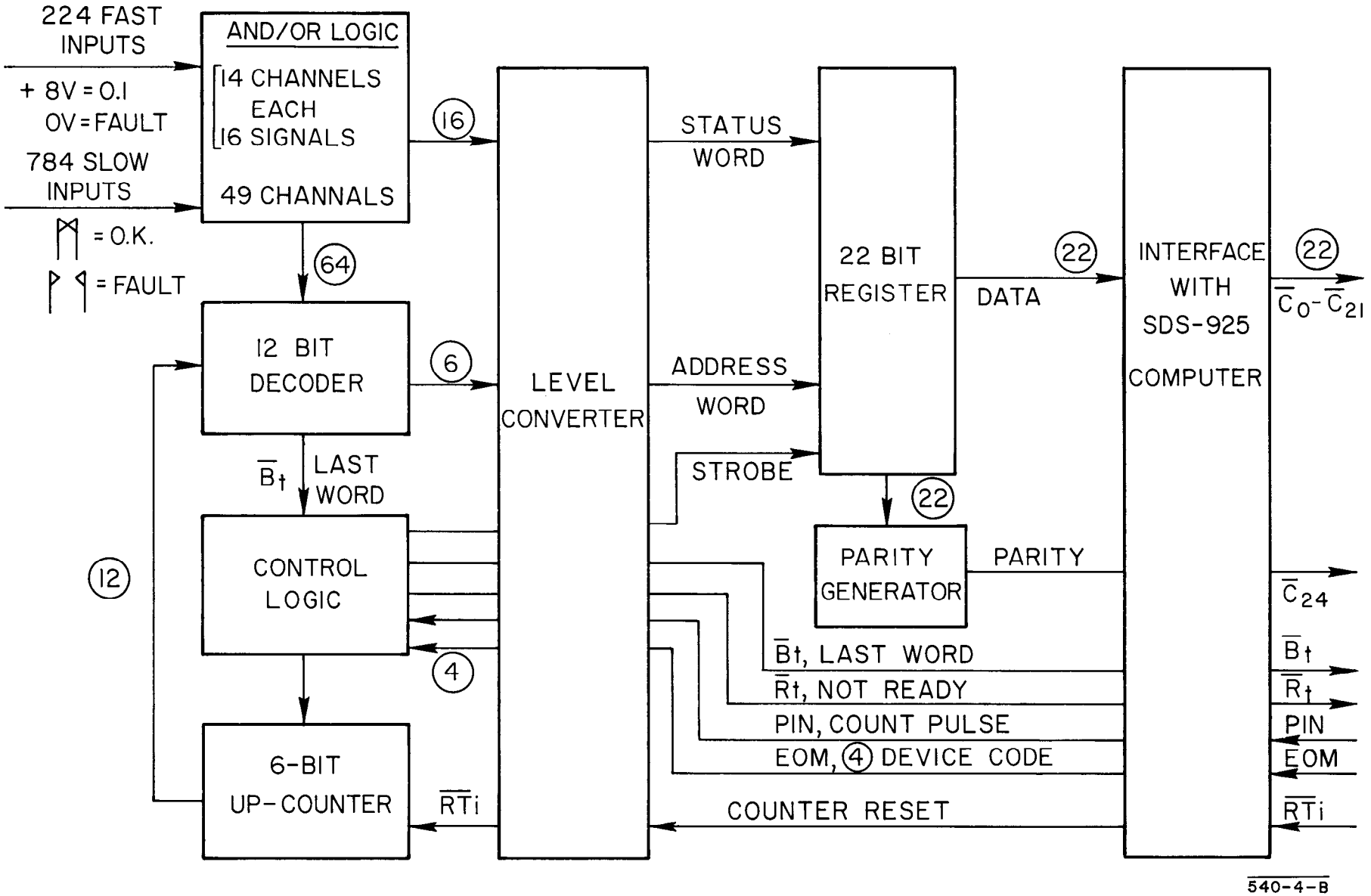
224 FAST INPUTS
+ 8V = 0.1
0V = FAULT
784 SLOW INPUTS
= O.K.
= FAULT
AND/OR LOGIC
14 CHANNELS EACH
16 SIGNALS
49 CHANNALS
16
64
12 BIT DECODER
6
$\overline{B}_t$ LAST WORD
CONTROL LOGIC
12
4
6-BIT UP-COUNTER
$\overline{RT}i$
LEVEL CONVERTER
STATUS WORD
ADDRESS WORD
STROBE
22 BIT REGISTER
22
DATA
22
PARITY GENERATOR
PARITY
$\overline{B}_t$, LAST WORD
$\overline{R}_t$, NOT READY
PIN, COUNT PULSE
EOM, (4) DEVICE CODE
COUNTER RESET
INTERFACE WITH SDS-925 COMPUTER
22
$\overline{C}_0$-$\overline{C}_{21}$
$\overline{C}_{24}$
$\overline{B}_t$
$\overline{R}_t$
PIN
EOM
$\overline{RT}i$
540-4-B

Figure 2

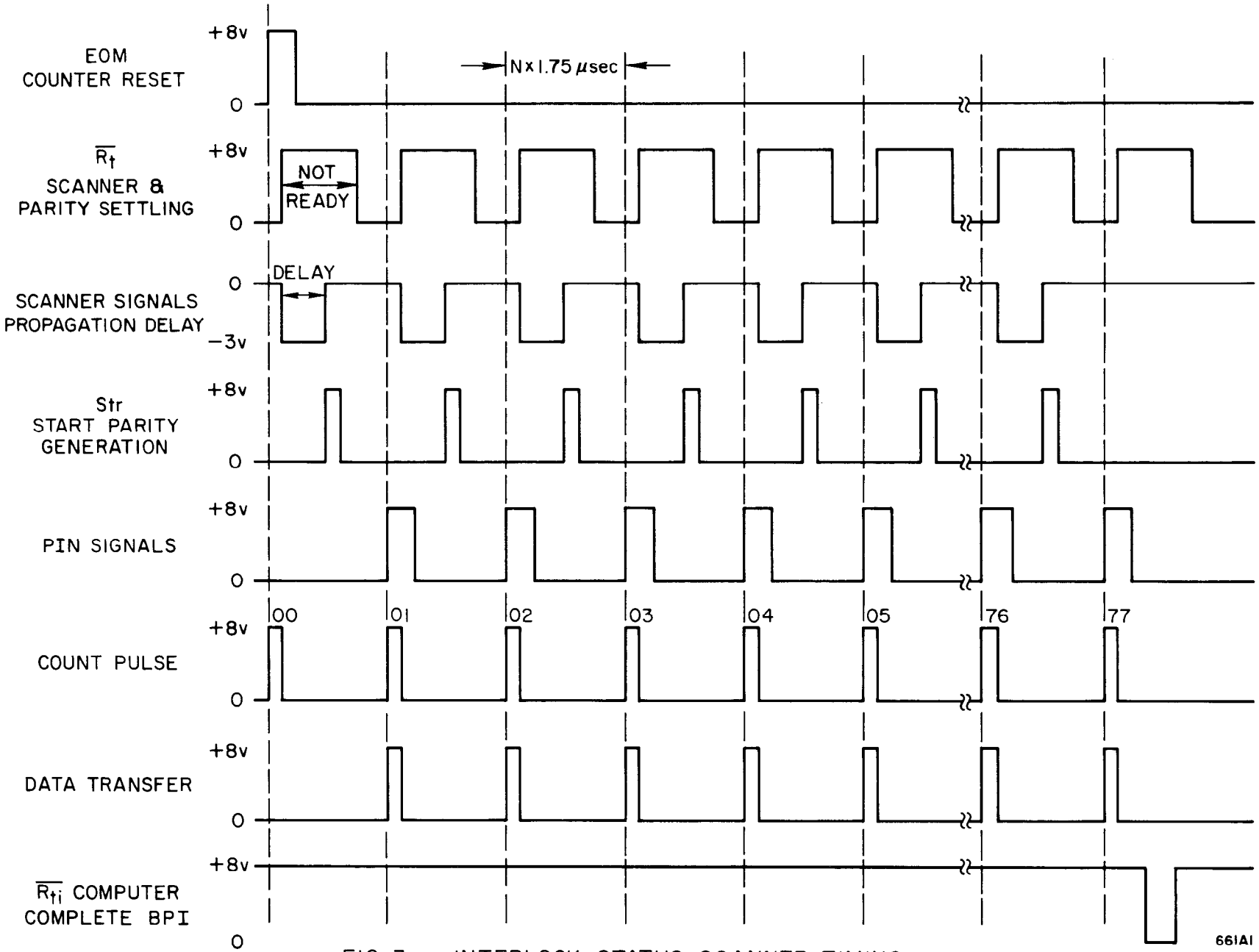

FIG. 3 -- INTERLOCK STATUS SCANNER TIMING