Published by IOP Publishing for Sissa Medialab

Received: *October 24, 2021*
Revised: *December 24, 2021*
Accepted: *February 25, 2022*
Published: *May 30, 2022*

Topical Workshop on Electronics for Particle Physics 2021
20–24 September, 2021
Online

Towards a generic receiver chain for particle detectors

L. Krystofiak,[a,*] F. Rössing,[a] A. Zambanini,[a] C. Grewing[a] and S. van Waasen[a,b]

[a] *Central Institute of Engineering, Electronics and Analytics, ZEA-2: Electronic Systems, Forschungszentrum Jülich GmbH, Wilhelm-Johnen-Straße, 52428 Jülich, Germany*

[b] *Department of Communication Systems, University of Duisburg-Essen, Duisburg, Germany*

E-mail: l.krystofiak@fz-juelich.de, f.roessing@fz-juelich.de

Abstract: A software-adaptable receiver tackles some of the highest challenges in particle detector development. While a generic approach never reaches the same performance as a dedicated development, it covers most application fields and can cut down development time and costs. Prototyping and verification of readout methods prior to the building of the complete systems are also facilitated. An in-depth study of existing particle detectors was conducted to define requirements that such a system will have to fulfill. In parallel, a first investigation of configurability is conducted to assess feasibility using an ADC as the central block in the receiver.

Keywords: CMOS readout of gaseous detectors; Electronic detector readout concepts (gas, liquid); Front-end electronics for detector readout

*Corresponding author.

https://doi.org/10.1088/1748-0221/17/05/C05025

Contents

1 Introduction

Chip design, especially analog and mixed-signal design, is a lengthy process, which comes with high development efforts as well as costs and contains a high risk for the overall success of a project. Moving on to Application Specific Integrated Circuit (ASIC), which are built in more recent process technologies, is therefore a decision that needs to be done carefully. With a generic approach that is designed independently, these risks are shifted to earlier stages, which substantially reduces experiment specific development time and costs. It also opens up possibilities for projects with smaller budgets and enables rapid prototyping, as well as being a potential driver for the community to adapt to new technologies.

2 Concept

2.1 Generic receiver chain

To accomplish a highly generic receiver chain, a direct sampling approach is adopted combining a high-performance Analog to Digital Converter (ADC) with a complex digital signal processing, that extracts relevant features on-chip. Figure 1 contrasts a typical receiver chain with the new concept.

A transimpedance amplifier with adjustable input impedance and gain is used to maximize the signal information coming from the sensor. This not only enhances the interoperability between different experiments, but compensates also signal differences due to process variations of sensors in one experiment.

CRRC filters commonly used to stretch the signal in time and relax the requirements for the subsequent components is omitted in favor of preserving as much information as possible and keeping the area of application of the receiver as wide as possible.

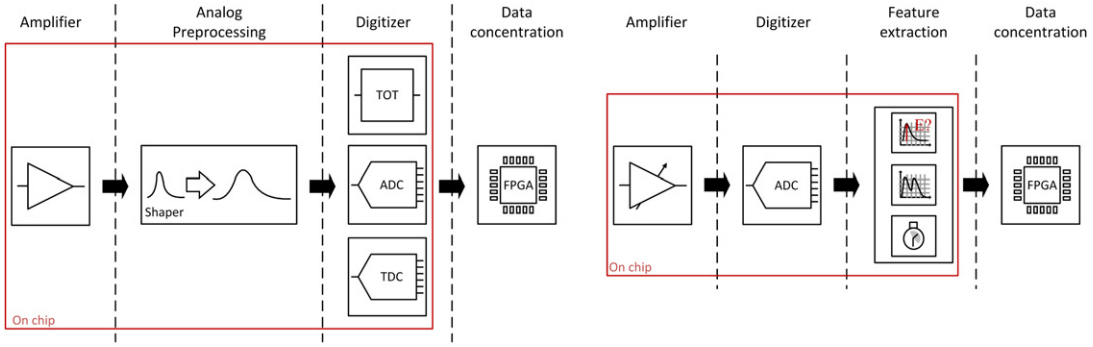


Figure 1. *Left side:* receiver chain as it is typically used in particle detectors. *Right side:* proposed generic receiver chain concept.

As digitizer now a high-performance ADC is at the core of the concept capturing the raw waveform of the signal and replacing all other forms of digitizers in combination with the digital signal processor. The ADC will be configurable in resolution and sample rate for the best trade-off between performance and power consumption for various application scenarios.

The digital processor plays an active role in feature extraction of a pulse and therefore a higher complexity as in usual implementations. It records an event with on-chip memory and then implemented algorithms are applied to extract the energy and the time of arrival, a possible candidate being the algorithm presented in [1], as well as pile-up events. If only some information is needed, the remaining digital signal processing can be switched off to reduce power consumption. There is also a bypass mode sending out raw data.

2.2 Requirement research

An extensive literature research has been done extracting parameters, that have to be covered for a generic receiver. As it is difficult to derive exact specifications for the ADC with feature extraction being done by digital processing, a test bench is currently set up in MatLab and Simulink using real-world data from existing particle detectors to evaluate different feature extraction algorithms and derive requirements for such a generic approach. For now the specifications orientate on the technical feasibility and complexity of the high-performance ADC explained in more detail in section 3.3.

2.3 Process technology as key driver

The key driver for this concept is the use of a bulk CMOS 28 nm process technology. It is considered as a sweet spot of current process technologies in terms of performance, power consumption, integration factor and cost. It allows to incorporate a powerful digital signal processor on-chip, while analog performance and design is not too restricted. As is it still a planar bulk Si technology, layout efforts are not higher than in older technologies keeping costs low. While this has become a very mature node being introduced in 2011 and characterized and updated since then, the operation in particle detectors has not been described yet. There are investigations though, that describe the effects of transistors in a bulk CMOS 28 nm process under radiation showing superior radiation hardness in comparison to older process nodes [2, 3]. Moreover, with old process technologies

2022 JINST 17 C05025

reaching their limits, the search for new results in particle experiments makes it inevitable to move on to more modern process nodes.

3 ADC development

3.1 State of the art ADCs

As the ADC was identified as the most crucial block for the concept, a literature research was done as a first step to see, if a generic approach is viable. Publications of the conferences ISSCC and VLSI, the two conferences for solid-state circuits with the highest impact factor, from 2016 to 2018 were investigated and are plotted with regards to sample rate and resolution in figure 2. Additionally, two off-the-shelf ADCs from analog devices are shown as additional references. With power consumptions in the triple-digit milliwatt range, these ADCs exceed the power budget for a generic approach. Recent developments though show, that even for very high performances of 10.5 bit Bit in resolution and a sample rate of 1.6 GS/s, a moderate power consumption of 37.7 mW, fabricated in 65 nm, is achievable [4].

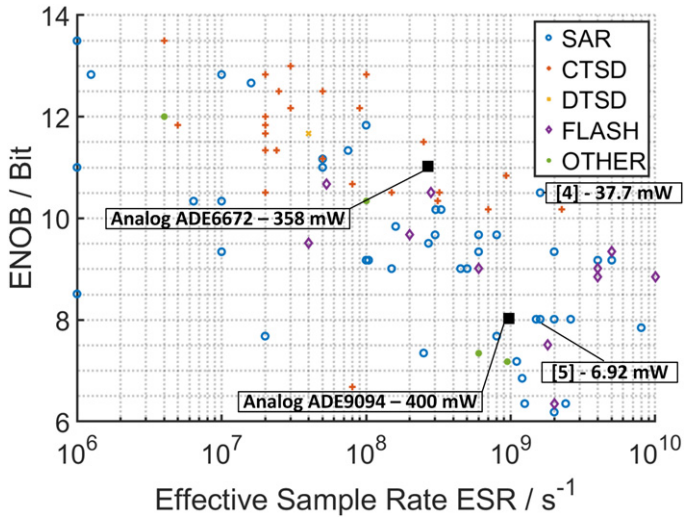


Figure 2. Resolution and sample rate of ADCs presented in ISSCC and VLSI (2016 to 2018).

3.2 Prestudy chip

As a prestudy to the prototype, a test-chip was designed in a 28 nm CMOS process. At its core is a 6 bit differential Successive Approximation Register (SAR) ADC. It was chosen in foresight of its use in the full, software-configurable ADC. The layout of the SAR ADC including input buffer, reference buffer and bootstrapped switches can be seen on the left side of figure 3.

For the switching scheme, merged capacitor switching with a static common-mode is used [6]. It offers the best trade-off between switching logic complexity and thus speed and energy efficiency. It ensures high precision and effective number of bits as it produces no dynamic offset in the comparator.

For this ADC a double-tail latched comparator as seen on the right side in figure 3 is implemented as it offers a good compromise between noise, power and speed. The split in two stages

2022 JINST 17 C05025

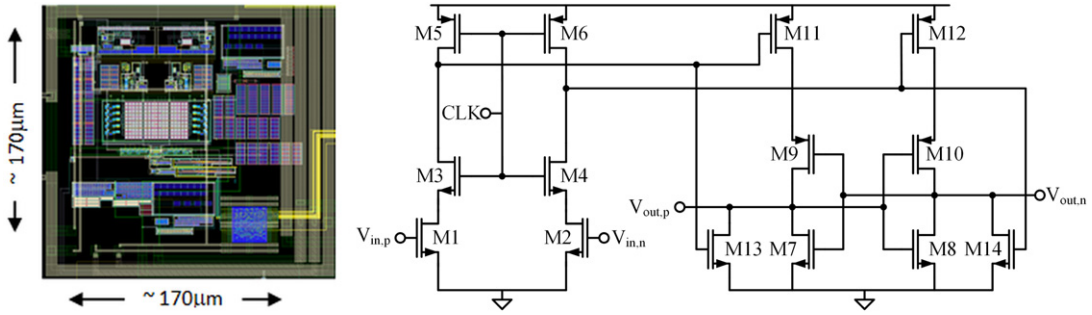


Figure 3. *Left side:* layout of the SAR ADC implemented in the first chip. *Right side:* schematic of the double-tail latched comparator.

allows to focus on speed in the latch and on reduced noise and offset in the dynamic amplifier first stage. The implemented cascoded approach reduces the kickback noise coming from the latch. Additionally, by using the cascode transistors as switches for reset of the comparator and not a transistor below the input pair reduces area and keeps the input transistors M1 and M2 at a stable bias improving resolution further. As it draws no static current, it also brings the benefit of scaling power consumption with sample rate.

The input capacitance is 1.7 pF to meet matching and thermal noise requirements for 12 bit resolution as target of the final ADC based on this concept. The power consumption and area is accordingly higher.

As the chip is still in fabrication, there are no measurement results yet and all presented results rely on post-layout simulations. The area of 0.029 mm^2 includes the bootstrapped switches, input buffer and reference buffer. The power consumption is simulated to be around 7 mW, with 6 mW for the input buffer and 1 mW for the core ADC. The maximum sample rate is 416 MS/s. The resolution was determined by a transient simulation of 1 µs in Cadence Virtuoso with all relevant subcircuits and a full parasitic extraction. The simulated data was then processed in Matlab to obtain the Signal-to-Noise and Distortion Ratio (SNDR) and the Spurious Free Dynamic Range (SFDR) for a sample rate of 400 MS/s. Its results can be seen in figure 4. The SFDR is 43.55 dBc and the maximum SNDR is 32.4 dB for an input frequency of 151 MHz.

3.3 The software-configurable ADC concept

With the results of the literature research and the experience gained from the prestudy test-chip, in a next step a first prototype of the software-configurable ADC is currently built. Its structure can be seen in figure 5. The pipelined ADC is comprised of three sub-ADCs. The first and the second stage each convert 4 bit limited by the gain of the inter-stage amplifiers being one of the biggest bottlenecks in high-performance, pipelined ADCs. The last stage converts 6 bit, totalling a 12 bit resolution subtracting the overlap between stages to enable offset error correction. Going for a high-performance approach in an environment with strict power constraints, power efficiency is one of the key parameters. A software-adaptable concept with adjustable sample rate and resolution produces an area overhead compared to a dedicated solution. Therefore, a small area consumption is another key parameter for the design of the ADC. Due to few analog signal processing steps,

2022 JINST 17 C05025

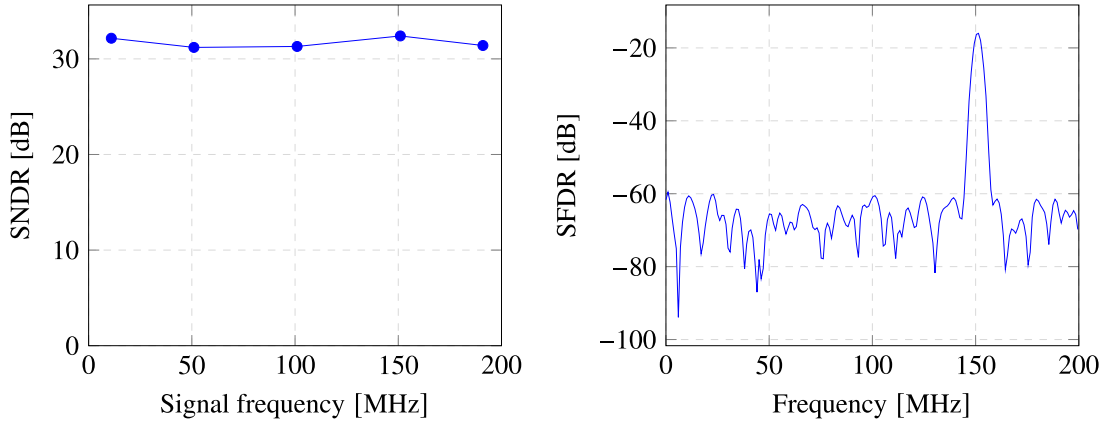
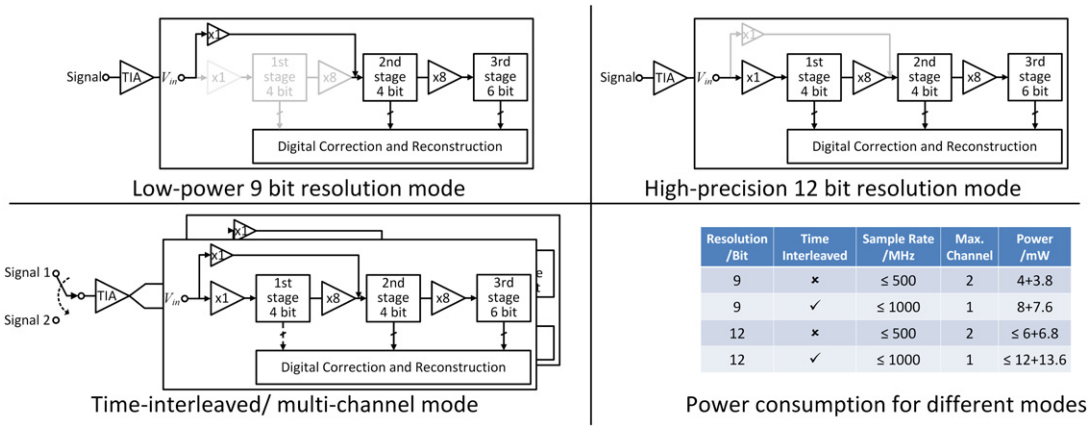


Figure 4. Simulated SNDR of the ADC over signal frequency (*left*) and SFDR at a signal frequency of 151 MHz (*right*) at a sample rate of 400 MS/s with parasitic extraction.

SAR ADCs scale very well with modern technology and have superior power efficiency over other architectures. The literature research showed, that pipelined configurations with SAR sub-ADCs scale favourably compared to flash ADCs in modern technologies. Subsequently, SAR ADCs were chosen as sub-ADCs as the base for this prototype. Since the capacitance value of the first stage has to be highest to meet the overall resolution, it also is most critical for higher sampling rate and uses overall most power of the core ADC. In order to enable a lower ENOB mode with lower power consumption, it is therefore best to bypass the first stage.



Resolution /Bit	Time Interleaved	Sample Rate /MHz	Max. Channel	Power /mW
9	×	≤ 500	2	4+3.8
9	✓	≤ 1000	1	8+7.6
12	×	≤ 500	2	≤ 6+6.8
12	✓	≤ 1000	1	≤ 12+13.6

Figure 5. Different modes of the ADC (*top* and *left*) and its estimated power consumption (*bottom right*).

4 Outlook

Using modern process technologies, the concept of a generic receiver chain for particle detectors becomes viable and offers the possibility for faster developments of prototypes or even full particle detectors. Therefore, a first prototype is currently under development featuring an adjustable transimpedance amplifier, a software-configurable ADC, on-chip capture memory, a digital threshold

2022 JINST 17 C05025

detector and a communication interface on a chip area of 1 mm by 1 mm. Target for the tapeout is end of May and first measurement results are expected towards the end of 2022.

References

[1] L. Jokhovets et al., *Improved rise approximation method for pulse arrival timing,* *IEEE Trans. Nucl. Sci.* **66** (2019) 1942.

[2] C.-M. Zhang et al., *Total ionizing dose effects on analog performance of 28 nm bulk MOSFETs,* in *2017 47th European Solid-State Device Research Conference (ESSDERC)* (2017), pp. 30–3.

[3] A. Pezzotta et al., *Impact of GigaRad ionizing dose on 28 nm bulk MOSFETs for future HL-LHC,* in *2016 46th European Solid-State Device Research Conference (ESSDERC)* (2016), pp. 146–9.

[4] J.-W. Nam, M. Hassanpourghadi, A. Zhang and M.S.-W. Chen, *A 12-bit 1.6 GS/s interleaved SAR ADC with dual reference shifting and interpolation achieving 17.8 fJ/conv-step in 65 nm CMOS,* in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)* (2016), pp. 1–2.

[5] L. Kull et al., *28.5 A 10b 1.5 GS/s pipelined-SAR ADC with background second-stage common-mode regulation and offset calibration in 14 nm CMOS FinFET,* in *2017 IEEE International Solid-State Circuits Conference (ISSCC)* (2017), pp. 474–5.

[6] V. Hariprasath, J. Guerber, S.-H. Lee and U.-K. Moon, *Merged capacitor switching based SAR ADC with highest switching energy-efficiency,* *Electron. Lett.* **46** (2010) 620.

2022 JINST 17 C05025