

# FERMILAB PIP-II BOOSTER LLRF UPGRADE

E. Cullerton†, B. Schupbach, B. Pellico, B. Chase, P. Varghese, D. Klepec, Fermilab, Batavia, USA

## Abstract

A proposed upgrade to the Fermilab Booster synchrotron is presented. A new LLRF system is required for interfacing to the PIP-II Linac that is currently under construction. The present feedback system has legacy analog hardware interleaved with updated digital components for control. A prototype of a new digital system using an FPGA controller is presented along with the RF hardware to handle up and down conversion of RF signals. A prototype FPGA controller is implemented using an Altera Cyclone V System on Chip, with 14-bit ADC’s and DAC’s running at 66 MHz. The controller theory and implementation are described in this paper, along with a description of the RF signal processing scheme.

## INTRODUCTION

The Fermilab Booster is a 15 Hz synchrotron accelerator with a circumference of 474 meters. Beam is injected into the Booster from a transport line which carries the 400 MeV beam output from the current Linac accelerator. The Booster uses a paraphrased RF system to adiabatically capture the multiturn beam into 37 MHz buckets. The Booster then accelerates the proton beam from 400 MeV to 8 GeV in approximately 35 milliseconds. The RF frequency is swept from 37 to 52 MHz during the acceleration period. The LLRF system controls 22 RF cavities split into an ‘A’ group and a ‘B’ group. The phase of each group is controlled to maintain beam position and acceleration phase. For the PIP-II era, some Booster machine parameters will have to change. For instance, the rep rate of the machine will go up to 20 Hz, the injection energy will change to 800 MeV, and the injection will be bucket-to-bucket instead of adiabatic. To ensure a smooth transition to the PIP-II era, the upgrade will have to operate on the current machine parameters and the new PIP-II era parameters. Table 1 lists the main parameter changes of the machine.

Performance Parameter	Present	PIP II Requirement	Units
Input (H <sup>+</sup> Beam Energy (Kinetic))	400	800	MeV
Output Beam Energy (Kinetic)	8.0	8.0	GeV
Protons per Pulse (injected)	5.0×10 <sup>12</sup>	7.0×10 <sup>12</sup>	
Protons per Pulse (extracted)	4.75×10 <sup>12</sup>	6.4×10 <sup>12</sup>	
Beam Pulse Repetition Rate	15	20	Hz
RF Frequency (injection)	37.9	44.7	MHz
RF Frequency (extraction)	52.8	52.8	MHz
Injection Time	.04	0.6	msec
Injection Turns	18	315	Turns
Beam Emittance (6σ, normalized; ε <sub>x</sub> =ε <sub>y</sub> )	<18	<18	π mm-mrad
RF Volts (Max)	1100	1200	V
Delivered Longitudinal Emittance (97%)	.08	0.08	eV-sec
Booster RF Stations	22	22	Count (A&B)

Table 1. Current / PIP-II Booster machine parameters.

## PRESENT LLRF SYSTEM OVERVIEW

The present LLRF system uses analog feedback paths to control phase shifters and Direct Digital Synthesizer’s (DDS’s) to drive the RF system. A block diagram of the system is shown in figure 1. The closed loop transfer function of the system can be easily modeled for analysis. There are many different configurations for synchrotron LLRF systems [1] [2]. The configuration used for the Fermilab booster consist of a phase loop and radial loop outside the PLL. The system model with no electrical delay is shown in figure 2, and the closed loop transfer function is given by:

$$\frac{\omega_{beam}}{\omega_{prog}} = \frac{G_v \cdot \omega_s^2}{s^2 - s \cdot (G_r \cdot \omega_s - G_v) + \omega_s^2 \cdot (1 - G_v \cdot G_r)}$$

The closed loop response is that of a damped oscillator, as expected.

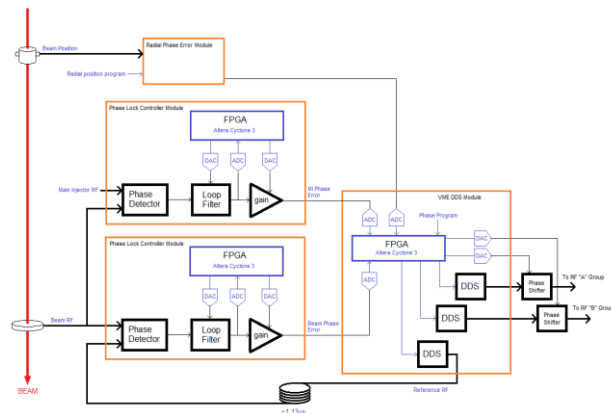


Figure 1. Simplified diagram the current LLRF system.

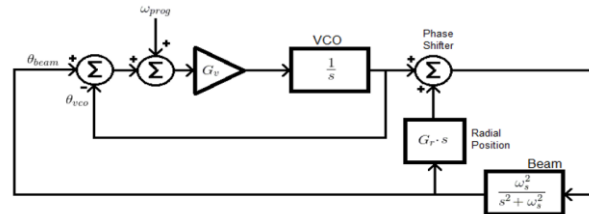


Figure 2. Closed loop model for analysis.

An open loop measurement has been made of the current system as is shown in figure 3. The dotted lines show where feedback loops have been opened. A critical parameter to understand from the open loop measurement is the system group delay, which will impact the system performance. An open model of the system has been created in MATLAB for comparison. The model includes

parameters such as gain, synchrotron frequency, and delay. The tuned model and measured data are plotted against each other in figure 4. The measurement shows a delay of ~4.5 us and this delay was added to the model to match the measured data. This delay will be one focus for improvement in the new design.

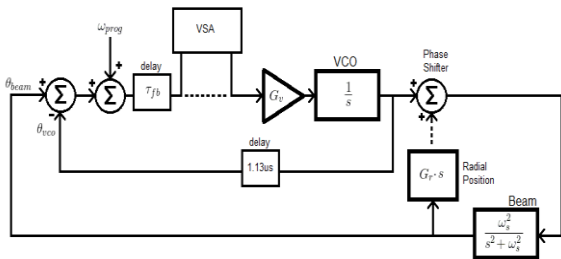


Figure 3. Open loop measurement setup.

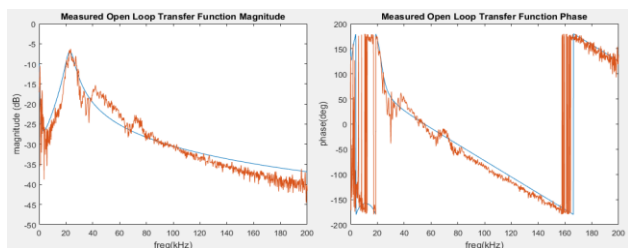


Figure 4. Open loop measurement vs MATLAB model.

## BOOSTER LLRF UPGRADE OVERVIEW

The proposed Booster LLRF upgrade has been partially prototyped using an Intel Cyclone V System on Chip FPGA controller board. A simplified block diagram of the system is shown in figure 5.

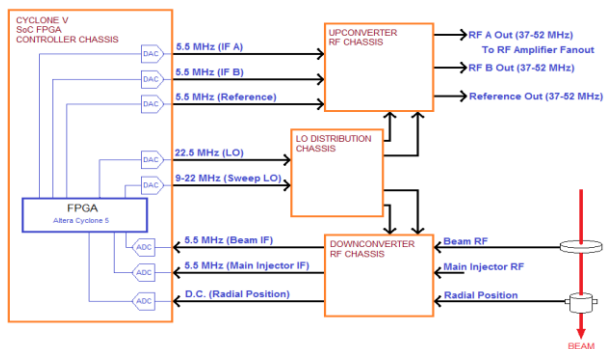


Figure 5. Proposed Booster LLRF upgrade system.

The proposed system uses a single FPGA for the feedback loops of the system. To simplify feedback processing, the RF signals are converted to a constant 5.5 MHz using up and down-conversion. To accomplish frequency sweep control, the FPGA will produce a swept LO used in the up and down conversion process. The estimated delay through the FPGA and ADC/DAC's is about 1200 ns. The electrical delay through the RF up/down conversion portion is neglected for now. This makes for a total loop delay of approximately 1130 ns + 1200 ns = 2.330 us. This is a reduction of delay versus the current system by nearly 2.17

us. There are other unaccounted for delays in the system that will increase the delay, but for now it is an approximation.

A detailed diagram of the FPGA controller is shown in figure 6. There are two NCO's with frequency and phase control to drive the RF A and RF B groups. An on-chip table is used to drive the phase program of the NCO's maintaining phase stability throughout the acceleration cycle. There are two LO signals that are generated with NCO's which are used in a double up-conversion scheme to create the swept RF signals needed for the Booster. An additional NCO is used to generate a reference RF signal. This reference RF output is provided for instrumentation purposes. An internal copy of this reference is used in the phase feedback loop. An electrical delay of ~1.13 us (RF system delay) on the internal reference is created internally using delay blocks and fine phase adjustment at the input of the NCO. Digital down conversion of the 5.5 MHz input signals to baseband is done using I/Q multiplication of the signal with a common receiver NCO. With the ADC's running at 66 MHz, it is easy to implement CIC filters with notches at 11 MHz, which are used to eliminate the upper sidebands of the down converted signals. CORDIC's are used to measure the phase of the down converted I/Q signals and provide amplitude information for gating the feedback systems on or off. There are program tables for feedback elements such as phase loop gain, radial loop gain, radial position program, and Main Injector phase lock gain.

Included in the FPGA is a circuit to measure the open loop response. The circuit drives a 0-200 kHz swept signal into the phase feedback loop and measures the response automatically. This is useful for system verification and measurement of actual delay without having to bring in external measurement equipment.

## RF Signal Processing

The RF signal up-conversion processing converts the 5.5 MHz IF outputs of the FPGA controller to a RF signal. The RF A, RF B, and RF reference signals are upconverted to a swept RF from 37 to 52 MHz. The reference RF is sent to instrumentation. Figure 7 shows a block diagram of the up-conversion process. Signal IF frequencies were selected to optimize both digital and analog filter realization. This process allows for the use of low frequency, low complexity, and low-cost ADC's and DAC's.

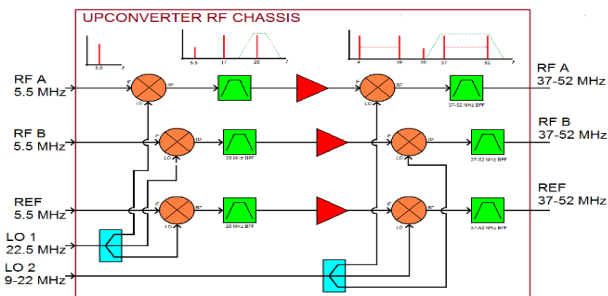


Figure 7. RF signal up-conversion

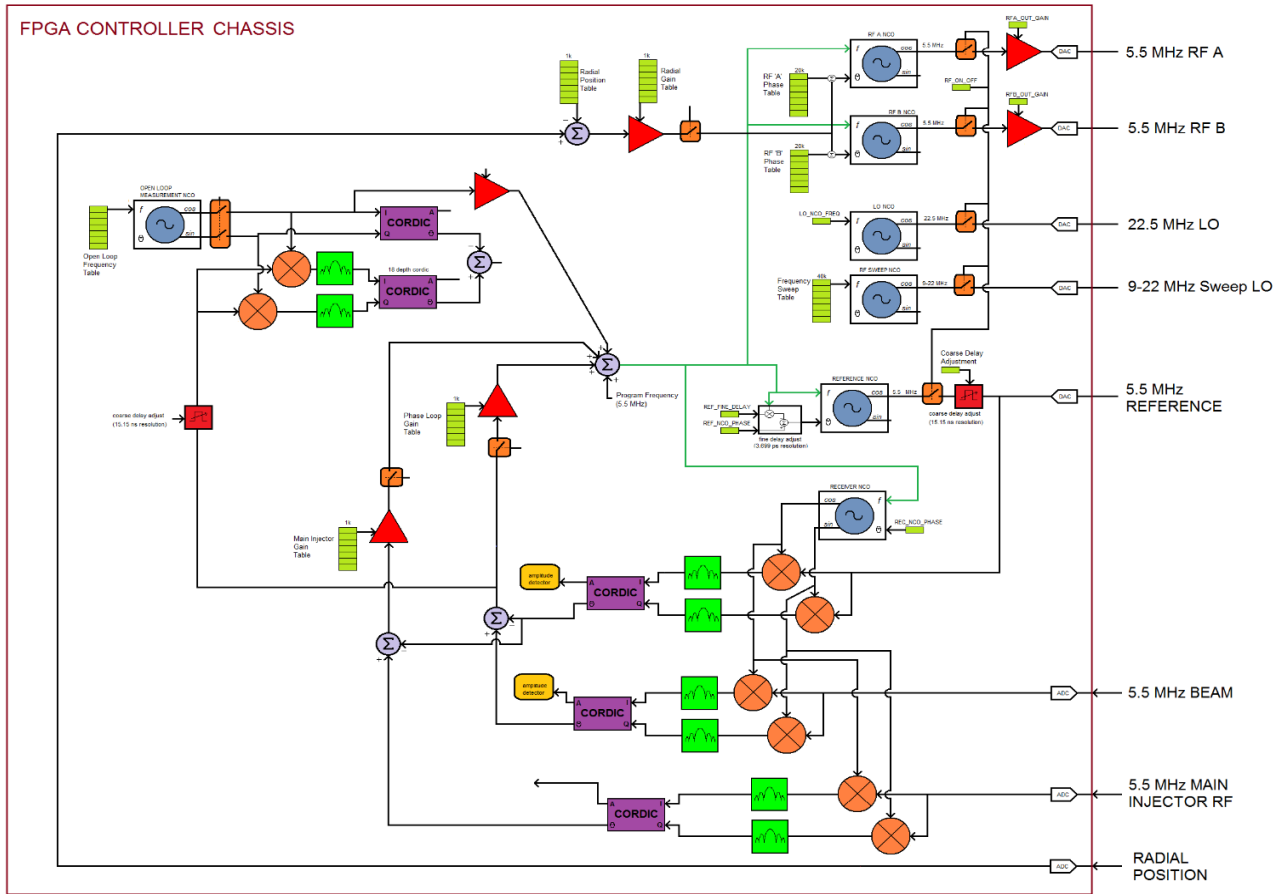


Figure 6. FPGA block diagram.

## SIMULATION

A simulation of the phase loop and the radial loop have been done using a time domain Simulink model. The digital controller, a simple radial position model, and a simple beam model have been incorporated into the model. The open loop measurement circuit has also been included in the model. Three simulations have been done; an open loop measurement, a step input to the frequency program, and a phase loop gain stability at different electrical delays.

### Open Loop Measurement

Results of the open loop simulation are shown in figure 8. These simulation results have been compared to the measured data. A delay of 4.5 us has been added to the Simulink model to match the measured data.

A simulation has been done with a step input to the frequency program. The step to the NCO's is driven to a 20 kHz offset at 0.1 ms, which then returns to 0 at 0.6 ms. An electrical delay of 4.5 us is used for these initial simulations to examine the current stability of the system. The phase error and radial position error due to the step are shown in figure 9.

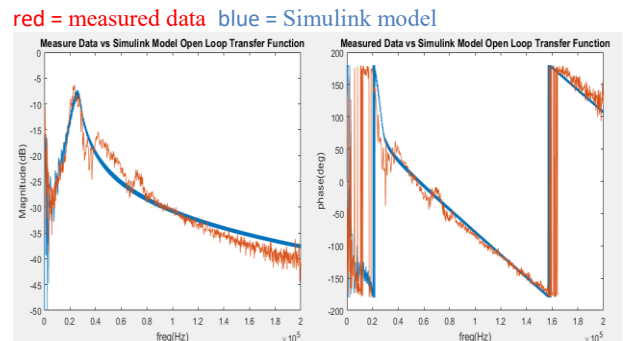


Figure 8. SIMULINK model vs measured data.

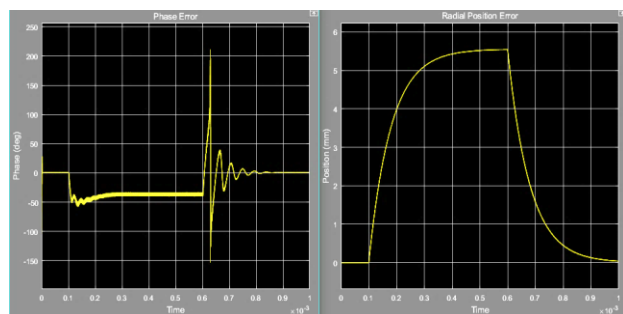


Figure 9. Step response of 20 kHz.

To explore the effect of electrical delay on feedback stability, the radial loop gain is held at a constant value and the phase loop gain is increased until instabilities are observed. Figure 10 shows the step response with a constant radial loop gain, and the phase loop gain at 671 Hz/deg and 839 Hz/deg. Oscillations can be observed when the gain is increased to 839 Hz/deg.

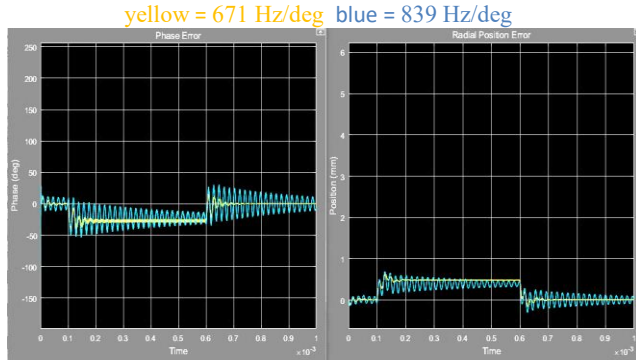


Figure 10. Step response with a phase loop gain of 671 and 839 Hz/deg.

The electrical delay was decreased to 2.8 us and the gain was increased to a point just before and after the system goes unstable. Figure 11 shows the phase loop gain of 1118 Hz/deg and 1230 Hz/deg. The simulation shows that a reduction from 4.5 us to 2.8 us improves the phase disturbance suppression by over 30%.

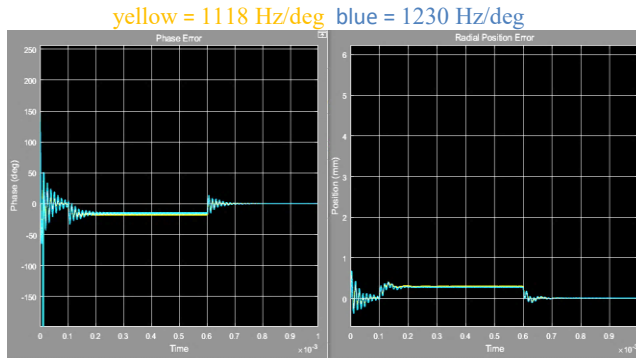


Figure 11. Step response with phase loop gain of 1118 and 1230 Hz/deg.

## HARDWARE PROTOTYPE SYSTEM

The hardware prototype uses a Fermilab designed Altera Cyclone V SoC controller chassis. The firmware for the controller was a replication of the Simulink model as close as possible.

### Prototype Controller Hardware Testing

The prototype hardware includes an external beam simulation circuit and a low pass filter in the radial loop, as modelled the Simulink model. To test the beam circuit, the simulations done in Simulink are repeated.

The open loop measurement, which included the beam hardware circuitry, confirms that the electrical delay has been reduced to 2.8 us. The RF system has not been

included in the measurement. A screen shot of the open loop measurement is shown in figure 12. The delay is higher than estimated earlier and further investigation into the source of these delays is required.

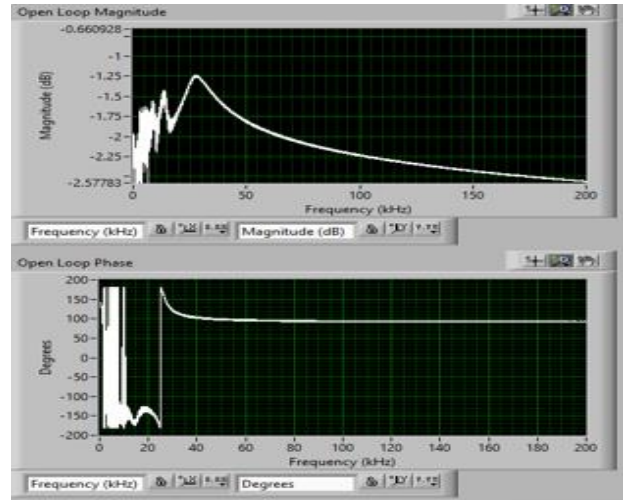


Figure 12. Open loop measurement with prototype hardware (2.8 us of delay added to flatten phase).

The next test is to repeat the open loop step response test. Figure 13 shows the step response to a 20 kHz step input to the NCO, along with the simulated data from Simulink. A good match between the hardware and Simulink simulation is seen. There are oscillations during the pulse due to the imperfections of the hardware beam circuit.

The final test pushed closed the phase loop and increased the gain up to an expected value to see if the system goes unstable. The gain was turned up to 1230 Hz/deg and some small oscillations were observed, as seen in figure 14.

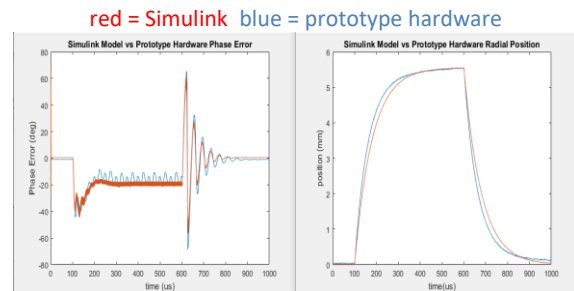


Figure 13. Hardware response vs Simulink simulation.

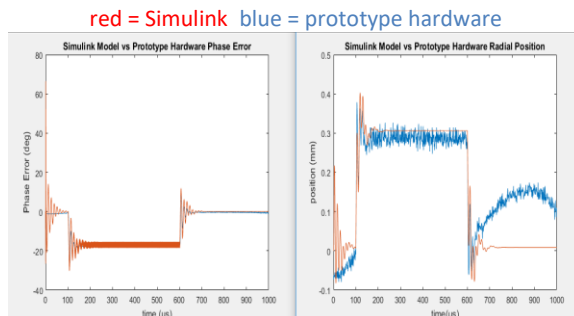


Figure 14. Hardware response as gain is increased vs Simulink.

## **CONCLUSIONS**

A prototype of a proposed hardware FPGA controller for the Fermilab Booster has been developed and completed initial testing. The prototyped controller shows improvement over the current system by reducing the electrical delay through the system by 1.7 us and improving disturbance suppression by over 30%. A MATLAB model and Simulink model have also been developed that show good agreement with the hardware prototype and measured data. The system also provides the required flexibility to meet the requirements of the PIP-II era Booster. System development will continue, and further testing of the system will be done on the current Booster.

## **REFERENCES**

- [1] D. Boussard, "Design of a Ring RF System", CERN 91-04 (1991).
- [2] S. Koscielniak, "RF system aspects of longitudinal beam control", AIP Conference Proceedings 249, 89 (1992).