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AN ADVANCED DIGITAL FEEDBACK CONTROL SYSTEM DESIGN FOR THE MUON LINEAR ACCELERATOR

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Abstract

A unique muon linear accelerator (linac) for the muon g-2/EDM experiment at J-PARC is under development. Digital feedback (DFB) design employed in a low-level radio frequency (LLRF) control system is crucial to fulfilling the required RF amplitude and phase specifications in the RF cavities for a stable and continuous acceleration of the whole bunched particles. To this end, a micro telecommunications computing architecture.4 (MicroTCA.4)-based compact and in-house DFB design, using VadaTech commercial off-the-shelf (COTS) RF system-on-chip (RFSoC) advanced mezzanine card (AMC), is aimed for the muon linac. This feedback control system will employ a direct sampling method that reduces the project cost by requiring less hardware employment for ultra-high frequency (UHF) and L-band accelerating structures. The present status and first results of the project will be reported in this paper.

INTRODUCTION

A new project, namely The J-PARC E34 project at MLF of J-PARC [1, 2], is being developed to measure muon's anomalous magnetic momentum (a_μ) and electric dipole moment (EDM) with extreme precision of 0.1 ppm using a very compact muon linac [3,4]. The muon linac, whose main parameters are summarized in Table 1, has a 40 m length and consists of a radio frequency quadrupole (RFQ), interdigital H-mode drift tube linac (IH-DTL), disk and washer type coupled cavity linac (DAW-CCL), disk-loaded structure (DLS) and Bunchers [5,6]. The accelerating structures of the muon linac are normal conducting standing-wave cavities that operate at 324 MHz (UHF), 1296 MHz (L-band), and traveling-wave (TW) acceleration tube operate 2592 MHz (S-band) frequency (see Fig. 1).

A low-level RF (LLRF) control system employed to control the accelerating field in cavities is critical to obtain high beam quality. The required RF stability is ±1% peak-to-peak (pp) in amplitude and ±1 deg pp in phase for the RF system. Table 2 lists the muon linac's RF parameters. A MicroTCA.4-based in-house LLRF system using a direct sampling method and Vadatech commercial off-the-shelf (COTS) RFSoC AMC (AMC574) [7] is being designed for the muon linac to achieve the amplitude and phase specifications, as shown in Fig. 2. It contains FPGA-based digital feedback and feedforward (DFB&DFF), resonance frequency control by a mechanical tuner or piezo or cooling water temperature control, environmental temperature&humidity control, transmission line adjustments, and interlock systems. A compact and cost-effective LLRF system is considered by separating the RF control and interlock racks. RF control-related rack contains an RF&CLK generator and DFB system-related components and is located in a constant temperature&humidity chamber to eliminate phase drift. The interlock-related rack contains interlock units for the accelerating structures and Bunchers (Fig. 1). However, several tests are necessary to ensure the required performance is achieved.

Table 1: Main Characteristics of the Muon Linac

Parameters	
Beam current	1×10^6 particles/s[†]
Beam energy	212 MeV
Pulse width (beam)	10 ns
Repetition rate	25 Hz
Cavity type	Normal conducting
Length	40 m

[†] A beam-loading compensation system is considered unnecessary because the beam current is small.

Table 2: RF Parameters of the Muon Linac

Parameters	**RFQ/B**[a]	**IH-DTL**	**DAW/B**[a]	**DLS**
Frequency	324 MHz	324 MHz	1296 MHz	2592 MHz
# of RF sources	3	1	7	1[c]
SSA[b]	3	NA	4	NA
Klystron	NA	1	3	1[c]
Max. RF power	5 kW[d]	600 kW	2.5-3 MW (27 kW)[e]	40-60 MW
Pulse width	40 μs	40 μs	40 μs	4 μs
RF stability	±1% (pp) & ±1 deg (pp)			

[a] and [b] denotes Buncher and solid state amplifier, respectively.
[c] Considering employment of the SLED method for the S-band.
[d] and [e] for each 324 MHz and 1296 MHz Bunchers, respectively.

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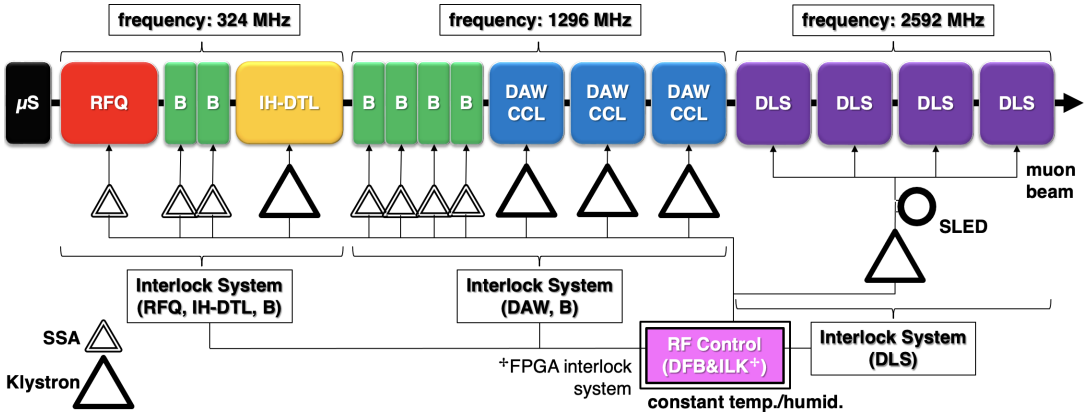

Figure 1: Muon linac LLRF control system overview.

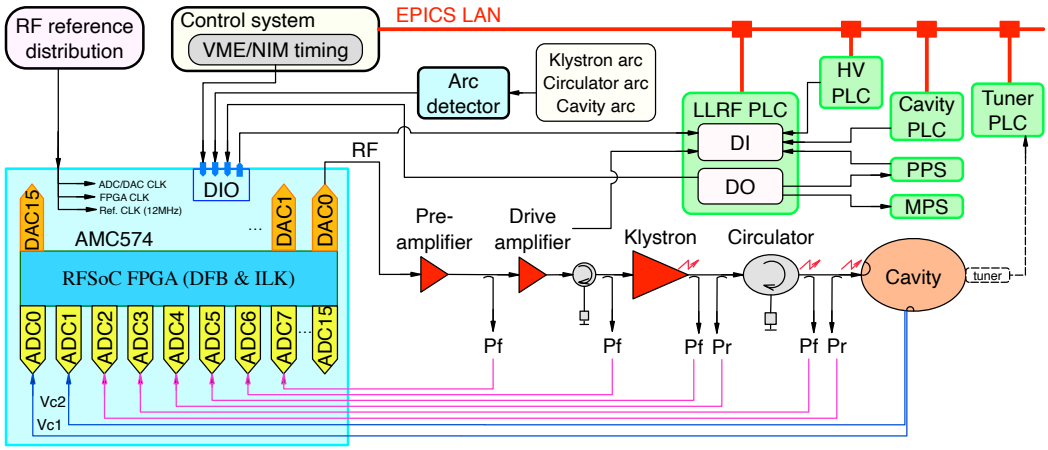

Figure 2: Typical LLRF control system diagram for a single cavity configuration.

DIGITAL FEEDBACK SYSTEM

In particular, the DFB&DFF is a critical component of the LLRF system to achieve the required RF field specifications. An FPGA-based DFB system using AMC574 RFSoC card with direct sampling method employment is planned for UHF and L-band accelerating structures of the muon linac. The AMC574 utilizes the Xilinx XCZU29DR RFSoC. The front panel has 36 high-density (HD) multi-way RF coaxial style connectors by TE Connectivity [8], which bring into the RFSoC the 16 ADC (12-bit @ 2 GSPS) and 16 DAC (14-bit @ 6.4 GSPS). The Xilinx RFSoC [9] offers RF-sampling analog-to-digital (RF-ADC) and RF-sampling digital-to-analog (RF-DAC) data converters, including digital down converters (DDCs), digital up converters (DUCs) that include programmable interpolation and decimation rates (here 8x) a numerically controlled oscillator (NCO), and a complex mixer. Also, there are clock inputs and a dual HD connector for external I/O (64 single-ended or 32 differential) via the front panel of the AMC574. The board is booted from the onboard SD card. A total of 5~6 AMC574 modules are considered for the DFB system, where one module will be used for 2~4 RF sources. In addition, the device manufacturer provides an FPGA reference design (see Fig. 3) and application tool (to exercise all the device features), which runs on the PS CPU of the AMC574.

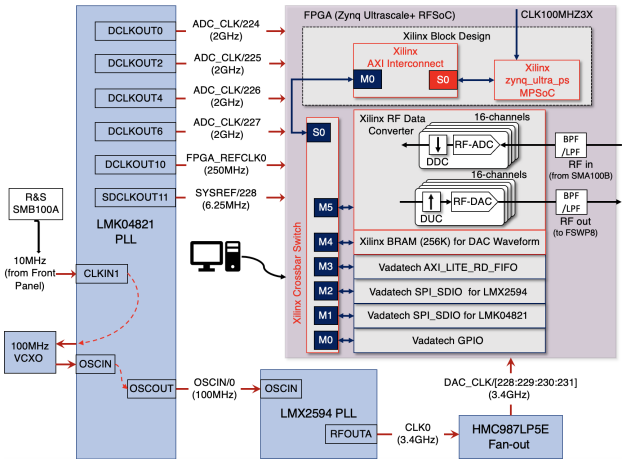

Figure 3: AMC574 FPGA test design block diagram.

PRELIMINARY ON-BENCH MEASUREMENTS

In our R&D efforts, we utilized a variety of essential components from Vadatech, including the UTC002 MicroTCA

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Carrier Hub, AMC725 CPU, power supply, fan modules, and a VT812 chassis. Several tests were performed focusing on device performance in terms of many tones to determine the viability of the AMC574 for the LLRF system in the muon linac. First, we performed measurements willingly on DAC, then ADC, where an RF&Microwave generator was used as a signal source. Additionally, we employed an external reference clock of 10 MHz at 6.5 dBm power.

DAC Measurements

To measure the output performance of the DACs, we utilized a highly sensitive phase noise analyzer (R&S FSWP8) along with a bandpass (BPF) and a low pass filter (LPF, Mini-Circuits SLP-1650+) at the DAC output tuned to the frequency of interest. DAC tone signal data was generated using the Vadatech application tool. Our testing involved measuring the DAC tone frequencies at 324 MHz, 1296 MHz, and 2592 MHz, with the DAC sampling rate running at 3400 MHz. We obtained accurate measurements and compiled the data into a summary table (Table 3). Additionally, a phase noise measurement result of DAC0 at 1296 MHz is displayed in Fig. 4.

Table 3: DAC (DAC0~DAC15) Performance Summary

Test tone (MHz)	**324**	**1296**	**2592**
Harmonics†			
2nd	< −60 dBc	< −56 dBc	–
3rd	< −66 dBc	–	–
Image of tone	−79.6 dBm*	−30.0 dBm*	–
RMS jitter			
BW=10 Hz-1 MHz	~314 fs	~331 fs	~328 fs
BW=10 Hz-10 MHz	~304 fs	~321 fs	~334 fs
Phase modulation			
BW=10 Hz-1 MHz	0.036 deg	0.155 deg	0.312 deg
BW=10 Hz-10 MHz	0.035 deg	0.150 deg	0.306 deg

† Power levels of tones at f=324 MHz and f=1296 MHz are 0 dBm and −4.6 dBm, respectively.

* With BPF&LPF; the images of 324 MHz and 1296 MHz tones are at 3076 MHz and 2104 MHz, respectively.

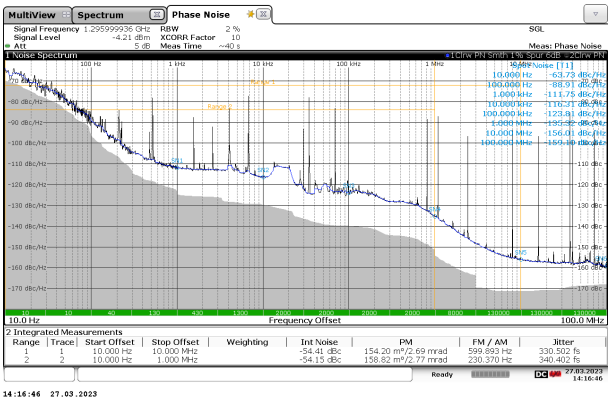

Figure 4: Measured phase noise of DAC0 at f=1296 MHz.

ADC Measurements

The ADC was tested using a signal generator (R&*S* SMA100B), which produced signals with very low jitter. NCO frequencies were set to 0.324 GHz and 1.296 GHz to measure 324 MHz and 1296 MHz RF, respectively, at Real to I/Q Mixer mode in the Xilinx RF Data Converter. The ADC data was acquired using the Vadatech application tool with a sampling rate of 2 GHz. Due to the FIFO length chosen in the reference firmware design, 65536 ADC samples containing I/Q data from RF-ADC channels were captured.

Figure 5 shows ADC phase for 324 MHz and 1296 MHz frequencies. RF stabilities of ±0.31% pp in amplitude and ±0.24 deg pp in phase were achieved in ADC0 at 324 MHz. For 1296 MHz, amplitude stability of ±0.53% pp and phase stability of ±0.65 deg pp were obtained. Here, we applied an 8-point moving average filter (MAF) for 1296 MHz.

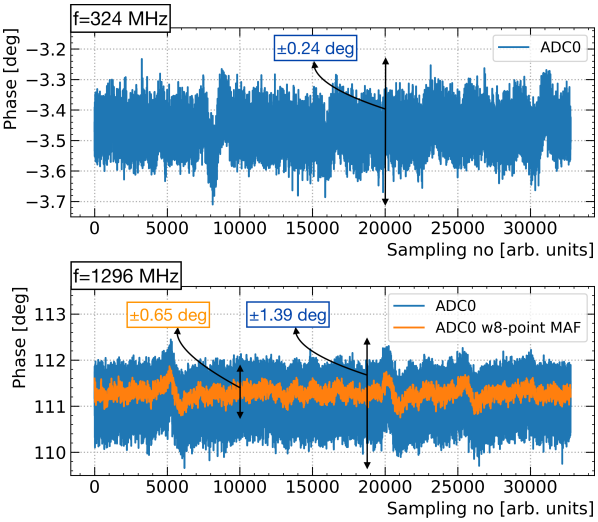

Figure 5: Short-term ADC phase stability at CW mode.

SUMMARY AND OUTLOOK

After evaluating the RFSoC performance, we have decided to develop a compact in-house LLRF control system using direct sampling and a COTS AMC574 for the muon linac. The AMC574 is a good choice for DAC performance, including spectrum and phase noise for the UHF and L-band. However, we will need to implement filters at the DAC output of the AMC574 for both UHF and L-band RF signals to suppress harmonics, spurious and image components. We also noticed that the AMC574, which can directly generate 2592 MHz RF, may not be suitable for the S-band DLS tubes due to poor phase noise performance. Additionally, we plan to implement decimation filters in RF-DAC of RFSoC to improve DAC performance and special IIR/FIR filters within the FPGA (if needed) to achieve better ADC stability results.

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