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THE PIP-II DEDICATED RADIO FREQUENCY PROTECTION INTERLOCK SYSTEM FULL SCALE PROTOTYPE DESIGN AND INTEGRATION*

W. Cichalewski†, P. Amrozik, G. Jablonski, W. Jalmuzna, R. Kielbik, K. Klys, R. Kotas, P. Marciniak, B. Pekoslawski, W. Tylman, Technical University of Łódź, Department of Microelectronics and Computer Science (DMCS), Łódź, Poland
J. Holzbauer, N. Patel, P. Varghese, Fermi National Accelerator Laboratory, Batavia IL, USA

Abstract

The Radio Frequency Protection Interlock (RFPI) system watches over fifty signals near the superconducting cavities cryomodule. Its major role is to recognize faulty situations instantly and drop permits for the Low-Level Radio Frequency control system (LLRF) and solid-state amplifier (SSA) operation. The full-scale prototype RFPI is a recent version of the PIP-II dedicated system capable of fulfilling the requirements of this newly constructed Linac project. Its hardware structure is compact but still modular. It provides enough capability to protect four superconducting resonators and their close environment at the same time. This work summarizes the production phase and the integration process of this designed RFPI system. The work introduces also the hardware and software structures of this system. Moreover, we also summarize the on-the-bench testing experiences from the individual hardware module verification and integrated RFPI studies.

INTRODUCTION

The newly designed and under construction linac named Proton Improvement Plan II (PIP-II) is located in Fermilab [1]. This significant upgrade to the existing accelerator infrastructure will allow for new scientific studies within such projects as, for instance, Deep Underground Neutrino Experiment (DUNE) [2].

This design and construction triggered the need for the development of existing and new accelerator systems. An example of such a system is the RFPI. Its main role is to protect the RF system in case of faulty cavities and cryomodule behavior or state. This goal can be achieved by instantaneous operation permits dropping while monitored signals begin to deviate from predefined safety limits. The PIP-II version of the RFPI system must provide enough channels to protect four cavities from a single cryomodule independently.

The first phase of the system design has resulted in the proof of concept prototype preparation [3]. That device provided valid information on the correctness and performance of each input/output signal. The second prototype covers a full list of input and output signals. Its structure changed internally on the hardware and software level. Still, protection functionality for 4 cavities remained unchanged.

This design consists of one central HW unit (carrier module) that hosts the system-on-chip module responsible for main protection logic realization and the other SOM responsible for the overall RFPI management. Additionally, it carries 7 FMC (FPGA Mezzanine Card) slots to be used for modules dedicated to different input/output signals. Such modularity provides possibility of different system configuration depending on the individual implementation requirements.

MAIN LOGIC UNIT AND MANAGEMENT SUBSYSTEM CARRIER MODULE (KC)

Main logic unit is a FPGA based hardware module that collects all the input signals (in digital representation) and compare their levels against safety limits. It is also responsible for managing output (permit) signals. Moreover, via the FMC connectors it allows individual inputs management and configuration (see Fig. 1).

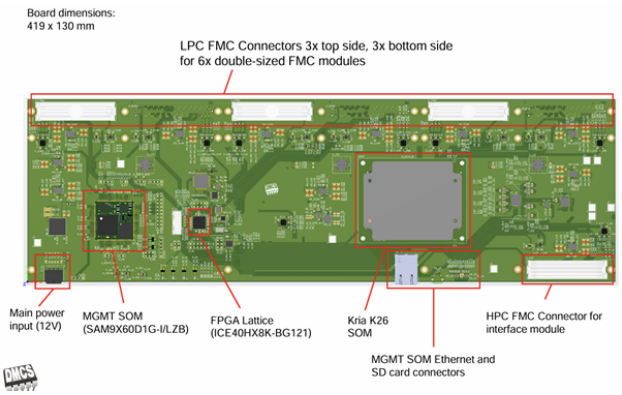

Figure 1: FMC/KRIA carrier module.

The management processor is responsible for: individual system modules power management, voltages and currents monitoring, resetting KRIA SOM, providing UART interface to the main (KRIA carrier) logic, and providing the JTAG access to KRIA chip.

FMC MODULES

The list of input and output signals required for the full-scale design RFPI system includes more than 60 elements (based on the current specification). To cover all

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† wcichal@dmcs.pl

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requirements 5 different FMC designs needs to be integrated into single RFPI system. This modules are: contact switches, field emission probe and non-ionizing RF protection (FEP/NIRP), resistance temperature detector (RTD) and coupler bias HV power supply current and voltage (HV), interface board, and RFPI permits outputs (LLRF and SSA).

Contact Switches Type Input Signals FMC Module

The contact switch module collects input signals that report a faulty situation by opening the PLC contact switch. In the current design such signals are: the coupler Window Cooling Airflow, the coupler vacuum, Personal Safety Permit, module He pressure and Level, beam line vacuum. The protection system must provide an appropriate voltage (12V or 24V) for these switches and instantly detect their status change (from close to open).

The required configuration can be done on the hardware level in the module assembly process. The module not only detects the switch status on the other side but also supports diagnostics that is capable to identify cable open or short faults and overwrite the signal status.

To provide a scalable solution and modularity, each signal is a single independent cell in the design. This means that the quantity of channels can be adjusted depending on the particular implementation requirements.

FEP/NIRP Signals FMC Module

The main role of the FEP signal module is fast and precise detection of the current induced in the system (which corresponds to field emissions). In addition, it needs to provide the required bias voltage for the antenna. The concept has been verified in the PoC design and now has been extended to four FEP channels (one per cavity) to cover final specification (see Fig. 2).

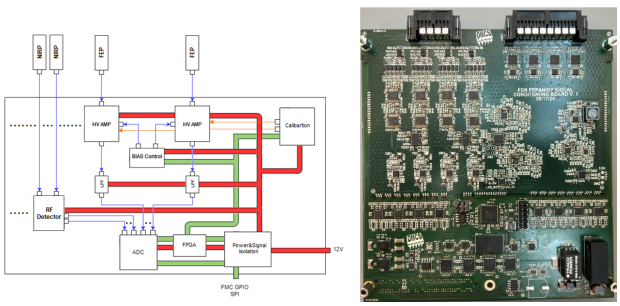

Figure 2: FEP module structure diagram (left side) and produced module top view (right side).

For each channel the bias voltage (up to 40V) can be generated and managed by the SPI interface from outside. The FEP input s connected to the high voltage, transimpedance amplifier that is used as a current detector. After the low-pass filtering of the signal it is delivered to the ADC inputs.

The module not only provides current detection and bias generation capabilities, but also consists of the subcircuit that incorporates a low-tolerance resistor for precise signal calibration.

The other part of this FMC module has been dedicated to the Non-ionising RF Probe signal detection. The RF detectors used in the design are ready to measure 6 to 8 RF inputs between -60 and 0 dBm for all the PIP-II frequencies.

Resistance Temperature Detection (RTD) and Coupler Bias High Voltage Power Supply Signals FMC

The PIP-II design specifies that the RFPI hosts two temperature probe RTDs (based on the PT-103) that collect data from the vicinity of each resonator (8 in total).

The four wire configuration incorporated in this solution can provide reliable temperature diagnostics in the expected range (around 270 to 300K). Moreover, this design includes the overcurrent protection, under and overvoltage monitoring. Additionally, an integrated calibration circuit provides on the fly system verification and diagnostics if needed (see Fig. 3).

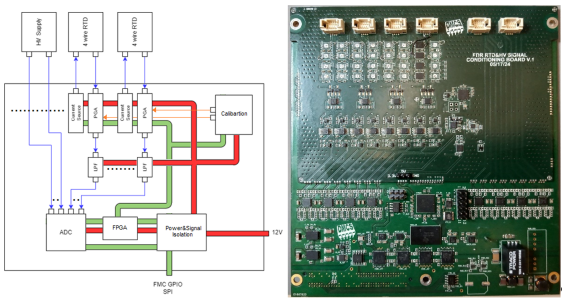

Figure 3: RTD module structure diagram (left side) and produced module top view (right side).

The second half of the module focuses on the coupler-biased high-voltage power supply voltage (V) and current (I) signals. This preconditioned analog signals are adjusted to the range from 0 to 10 V. The ADC chip of the FMC module determines these values, and the main logic immediately detects violations of the safe limits.

Interfaces and LLRF Communication FMC Module

The FMC interface module incorporates functions from different domains of the system. On one side, it contains the SFP interfaces that are dedicated to collect input signal from the LLRF (via the fast communication links) and in the future the HV PS communication. On the other hand, it carries ethernet interfaces as well as external clock input, SD card connector for main logic, debug UART interface for management, status LEDs and others.

Output Permits Signals for LLRF and SSA Module

As specified in the requirements of the PIP-II RFPI system: each cavity that is protected by the system should have 4 different permits. They are: LLRF permit, Solid State Amplifier (SSA) permit, SSA DC voltage permit, and machine protection system (MPS) permit. Additionally, two input signals (TTL like) are provided for each cavity by this module. One is already used as a SSA ready input signal (see Fig. 4).

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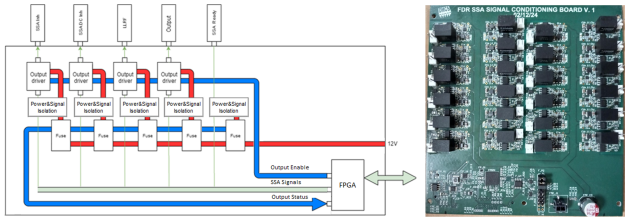

Figure 4: Module structure diagram (left side) and produced module top view (right side).

Each output permit is 5V digital signal. The single output is an independent cell to provide signal isolation and design modularity. To prevent from outputs damage during short circuity situation the thermal fuses are used. Moreover, the output enable signal can disable the output operation regardless of the protection function state in case of system health issues.

FIRMWARE AND SOFTWARE STRUCTURE

Both management unit and the main logic unit have similar layers of firmware and software. This starts from the bottom with firmware up to the operator GUIs necessary for system monitoring and configuration. These layers are: Firmware (VHDL) for the Xilinx SOMs, Operating system driver, User system library, Control system process (EPICS IOC), operators/expert OPIs.

Management Unit Software Structure

The management processor controls various signals via GPIO (digital) interface. Additionally it incorporates several I2C to communicate with current/voltage monitors and JTAG multiplexer and boot mode selector available via dedicated Lattice FPGA). The GPIO and I2C interfaces are the main channels for the user library to provide a middle layer between the hardware and the control system (EPICS IOC).

The EPICS has been chosen as a control system that is more and more widely used among the PIP-II systems. The IOC for the management is based on the Asyn driver that communicates with the FMC slots using the user library. The library manages individual slot power and reports about theirs current and voltage levels and system health. This information is available in the PVs and is exposed to the user via a dedicated OPI (see Fig. 5).

Main Logic Unit Firmware Software Structure

The main logic unit firmware has to not only realize the protection function. Its goal is also to establish and maintain communication with other, smaller Lattice FPGA chips placed on the FMC modules (SSA, RTD/HV and FEP/NIRP).The protocol used for communication between the two is simple register-based solution.

The same as for the management part, here the user library serves as an interface between the lower firmware layer and the EPICS layer (see Fig. 6).

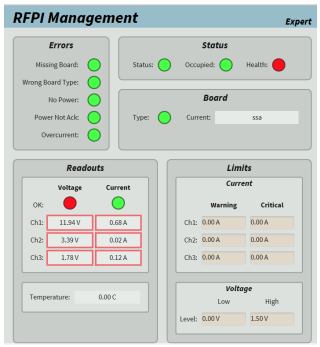

Figure 5: Management subsystem expert GUI.

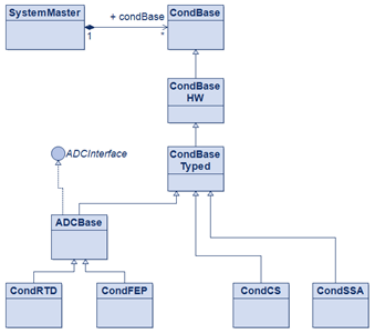

Figure 6: Main logic unit library structure.

Here also the EPICS IOC incorporates the Asyn Driver approach to provide communication with lower parts (Fig. 7).

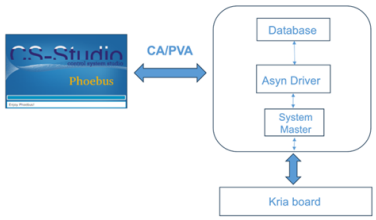

Figure 7: Main logic unit EPICS IOC structure.

CONCLUSION

All hardware and software parts of the full-scale RFPI prototype have been designed and produced. The system integration has been completed successfully. Individual modules were evaluated prior to integration to confirm the performance levels. Post-integration unit verification and evaluation was possible thanks input signals introduction from artificial, external sources. The individual modules tested confirmed the parameters of the signal detection precision level achieved during PoC studies. Additionally, the new system accommodates many more input and output signals, and degradation in the system reaction has not been observed, still satisfying the fully specified reaction time limits.

To prove its readiness for PIP-II implementation, we now have placed this RFPI system version in the CMTF facility where in-situ tests with PIP-II dedicated cryomodules are planned.

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