The ETROC2 prototype for CMS MTD Endcap Timing Layer (ETL) upgrade

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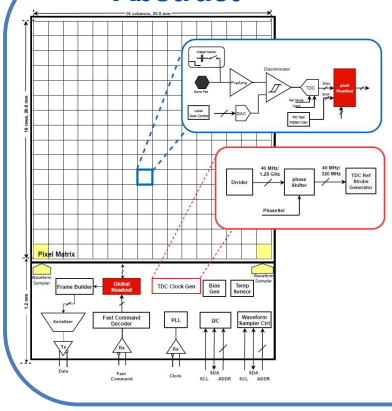
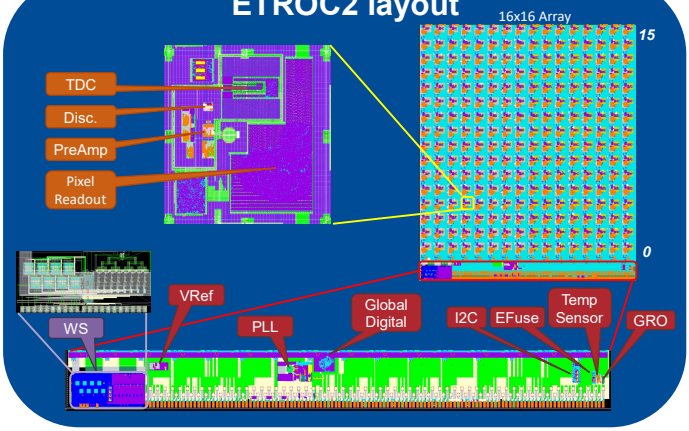
Abstract



The ETROC (Endcap Timing Readout Chip), implemented in commercial 65nm CMOS process, is being developed for the LGAD-based CMS Endcap Timing Layer (ETL) at HL-LHC to deliver timing measurements down to 35 ps resolution. It is designed to handle a 16^2 pixel (1.3^2 mm^2) cell matrix; Each channel consists of a preamplifier, a discriminator, a TDC used for TOA (Time Of Arrival) and TOT (Time Over Threshold) measurements, and a memory for data storage and readout. An in-pixel auto threshold calibration is included, along with a self-testing pattern generator. The TOT is used for time-walk correction of the TOA measurement. The clock distribution is based on a 16x16 H-tree design with shielding structures to alleviate interference. The global peripheral circuits include a PLL, a phase shifter, an I^{2}C controller, a fast-control block, a global readout, a data driver along with an e-fuse, and a temperature sensor. ETROC builds data frames for each L1A selected event and can provide L1 trigger information for user-defined delayed hits.

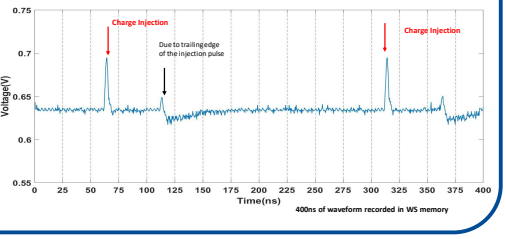
The ETROC2 is the first full size (16x16) and full functionality prototype for ETROC. At 21mm x 23mm, it is one of the largest chips in High Energy Physics.

ETROC2 layout

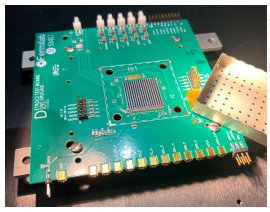


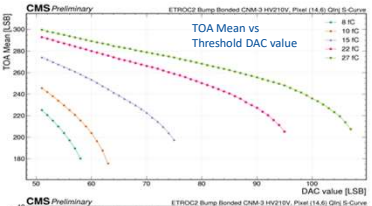
Waveform Sampler (2.56 GS/s) (Recorded w/ Charge Injection)

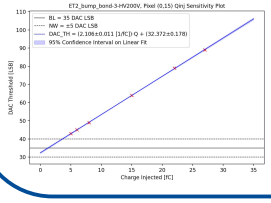
Important to monitor signal waveforms to detect variations from the increasing radiation dose. Recorded waveforms can be used to optimize thresholds and bias voltages to maintain the target performance.

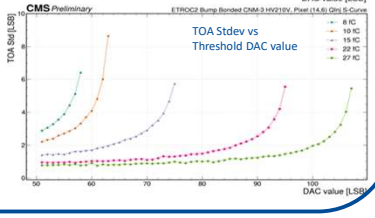


Bump bonded ETROC2 performance using Charge Injection



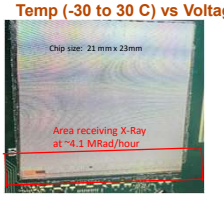


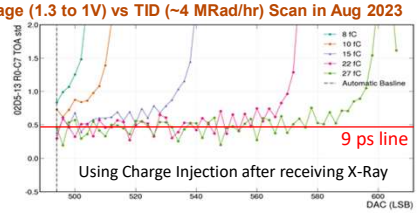




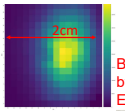
Initial ETROC2 Radiation & Beam test at CERN

Temp (-30 to 30 C) vs Voltage (1.3 to 1V) vs TID (~4 MRad/hr) Scan in Aug 2023

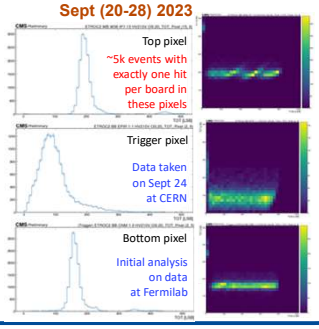




Beam Testing with 120 GeV Proton (67%) & Pion (33%) beam in Sept (20-28) 2023



Beam profile seen by bump bonded ETROC2+LGAD



Track Trajectory

Design blocks (I^{2}C, ESD-pad, eRx, phase-shifter) developed through common projects at CERN and the CERN ELT library were used in the ETROC1 development. We thank the designers of these design blocks, especially Syzmon Kulis and Paulo Moreira (CERN) for the support, and Jeffrey Prinzie and Stefan Biereigel (KU Leuven) for their PLL design. We thanks the Torino group for LGAD sensor support, especially Nicolo Cartiglia, Valentina Sola and Marco Ferrero, and the CNM and Barcelona group and EPIR company for bump bonding, especially Sebastian Grinstein and Sushant Sonde. We thank CERN ASIC Support and CERN CHIPs for their support with the ETROC2 design and testing, especially Kostas Kloukinas and Xavier Llopart. Special thanks to Humberto Gonzalez, Michelle Jonas, Paula Kippert and Albert Dyer at Fermilab for their technical support, and to Alessandro Caratelli, Giulio Borghello, Gennaro Termo, Jerome Alexandre Alozy, and Maxence Marc Ledoux, at CERN for their support for the TID, Climatic chamber and wafer probe testing. This poster has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics.