Cryogenic Front-End ASICs for Low-Noise Readout of Charge Signals

Prashansa Mukim, *Member, IEEE*, Gabriella A. Carini, *Member, IEEE*, Hucheng Chen, *Senior Member, IEEE*, Grzegorz W. Deptuch, *Senior Member, IEEE*, Shanshan Gao, Gianluigi De Geronimo, *Member, IEEE*, Soumyajit Mandal, *Senior Member, IEEE*, Venkata Narasimha Manyam, Veljko Radeka, *Life Fellow, IEEE*, and Sergio Rescia, *Member, IEEE*

***Abstract*— This paper presents design details and measurement results of LArASIC, a front-end application specific integrated circuit (ASIC) designed for low-noise readout of charge signals generated in neutrino study experiments within liquid argon time projection chambers. LArASIC comprises of 16-channels of programmable charge amplification and pulse shaping stages that provide a voltage readout proportional to the input charge and was optimized for operation at liquid argon temperature, i.e., 89 K. The chip was fabricated in a 180 nm CMOS process. Measurements at liquid nitrogen temperature, i.e., 77 K, indicate that the channel outputs have high linearity (INL < 0.1%) within the operating range, an equivalent noise charge of 534 electrons for a peaking time of 1 μs and a detector capacitance of 150 pF, and a worst-case inter-channel cross-talk of 0.35%. The paper also presents design choices made in the process of migrating LArASIC to CHARMS, an ASIC to be fabricated in a 65 nm process that includes all features provided by LArASIC, along with additional digital programmability for improved robustness and flexibility. CHARMS is intended for use in future high-energy physics experiments that require high-resolution charge or light readout with shorter pulse peaking times.**

***Index Terms*— Charge amplifier, front-end electronics, low-noise electronics, single-ended-to-differential converter, shaping filter, cryogenic CMOS.**

I. Introduction

PARTICLE detection experiments carried out in noble liquid time projection chambers (TPCs) [1] aim to reconstruct the three-dimensional trajectories of particles or the energy distributed among the particles, with high spatial, temporal and energy resolution. For this purpose, front-end ASICs are utilized to read out the signals resulting from conversions of energy of the particles, including photons, into charge, as voltage pulses. While placing the front-end electronics inside the TPC reduces the parasitic capacitance originating from long cables and thus enables low-noise, high-resolution readout of the signals generated due to ionization [2], [3], [4], it also necessitates reliable operation of the electronics at cryogenic temperatures.

The history of development of cold front-end electronics for high-energy physics experiments dates back to the 1980s, when a pre-amplifier based on a junction field-effect transistor (JFET) was first designed for the NA34-HELIOS liquid argon (LAr) calorimeter [5], [6]. The developments that followed include design of JFET based pre-amplifers for the MicroBooNE experiment [3] and the liquid krypton (LKr) calorimeter for the NA48/NA62 experiment [7], followed by design of pre-ampliers in 1 μm GaAs technology for the ATLAS LAr Hadronic Endcap Calorimeter (HEC) [8].

The need for low-noise and low-power readout electronics with long lifetime and scalability for the Deep Underground Neutrino Experiment (DUNE) [9], motivated research and development efforts involving the use of complimentary metal-oxide semiconductor (CMOS) based electronics. DUNE is a major scientific experiment currently under construction that aims to study the properties of neutrinos. The DUNE far detector, located 1.5 km underground at the Sanford Underground Research Laboratory in South Dakota, will operate with an intense neutrino beam generated at the Fermi National Accelerator Laboratory in Illinois after it has traveled 1,300 km through the Earth. For this purpose, the far detector will utilize four 17 kTon liquid argon (LAr) TPCs that detect both the ionization charge and the scintillation light generated when incident neutrinos occasionally interact with argon atoms.

After over a decade of development focused on the design of CMOS-based cryogenic readout electronics, the solution shown in Fig. 1, comprising of three ASICs, has been chosen for the readout of charge in the DUNE far detector TPCs. LArASIC, which is the first ASIC in the readout chain and is implemented in a 180 nm CMOS process with a 1.8 V power supply, provides amplified and filtered voltage pulses with an amplitude proportional to the ionization charge generated by the traversing particles, with programmable gain and pulse peaking time. These pulses are digitized with 12-bit resolution

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Prashansa Mukim, Gabriella A. Carini, Grzegorz W. Deptuch, Soumyajit Mandal, Veljko Radeka, and Sergio Rescia are with the Instrumentation Department, Brookhaven National Laboratory, Upton, NY 11973 USA (e-mail: pmukim@bnl.gov).

Hucheng Chen and Shanshan Gao are with the Physics Department, Brookhaven National Laboratory, Upton, NY 11973 USA.

Gianluigi De Geronimo was with the Instrumentation Department, Brookhaven National Laboratory, Upton NY 11973 USA. He is now with the Nuclear Engineering and Radiological Sciences Department, University of Michigan, Ann Arbor MI 48109 USA.

Venkata Narasimha Manyam was with the Instrumentation Department, Brookhaven National Laboratory, Upton NY 11973 USA. He is now with the Connectivity and Sensors Group, Qorvo US Inc., Greensboro NC 27409 USA.

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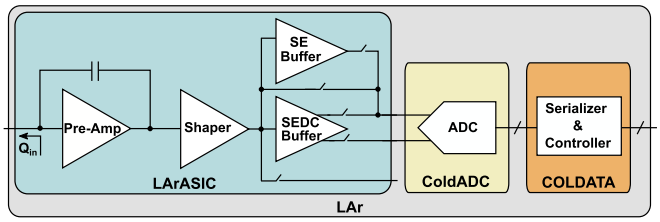

Fig. 1. Three-ASIC (LArASIC-ColdADC-COLDATA) charge readout solution adopted by the DUNE far detector.

by the ColdADC ASIC [10], implemented in a 65 nm CMOS process with a 1.2 V power supply. Finally, the digitized outputs are serialized at 1.28 Gb/s and transmitted out by the COLDATA ASIC [11], also implemented in a 65 nm CMOS process. For using in the experiment, all three ASICs are integrated on a single PCB that is designed to operate at LAr temperature (LArT), i.e., 89 K, to ultimately meet the requirements for the DUNE far detector electronics. The latter include readout of charges up to 500,000 electrons with high linearity, channel gain of $\approx$ 10 mV/fC, input-referred equivalent noise charge (ENC) less than 1,000 electrons for 100-200 pF input capacitance, peaking time for the front-end adjustable between 1-3 μs, digitization at 2 MS/s, channel-to-channel crosstalk < 1 %, and total power consumption of less than 50 mW for each channel.

Other ongoing work on CMOS-based cryogenic front-ends for charge or light readout includes single-channel ASICs for high purity germanium (HPGe) detectors [12], as well as multi-channel ASICs such as LArPix [13] and CRYO [14], [15]. While both LArPix and CRYO include analog-to-digital converters (ADCs) integrated with the front-end circuits, LArASIC provides dedicated low-noise analog front-end functionality, and its output is processed by the independently optimized ColdADC and COLDATA ASICs.

Characterization of transistors in various technologies, and shift in transistor properties at cryogenic temperatures, such as increased threshold voltage, steeper sub-threshold slope, increased transconductance and lower white noise have been reported in the literatures [16], [17], and [18]. Although the overall architecture of LArASIC and characterization of the devices used in the chip at cryogenic temperatures have also been summarized in previously published work [2], [4], [19], design details of the core channel circuits have not been discussed. This paper presents the detailed circuit design of LArASIC and measurement results for the latest production version.[1] It also discusses design choices and additional features that will be included in a next generation version of LArASIC currently being designed in a 65 nm process that comprises of CHARge aMplifiers and Shaping filter circuits, and is named CHARMS.

The organization of this paper is as follows. The architecture and design of circuit networks that form each channel of LArASIC and CHARMS are described in Section II. Simulation results of the channel circuits in LArASIC using cryogenic transistor model parameters are presented in Section III. Measurement results at liquid nitrogen temperature (LNT, i.e., 77 K[2] for the latest production version of LArASIC are presented in Section IV. Finally, conclusions are drawn and details about intended use of CHARMS for future applications are summarized in Section V.

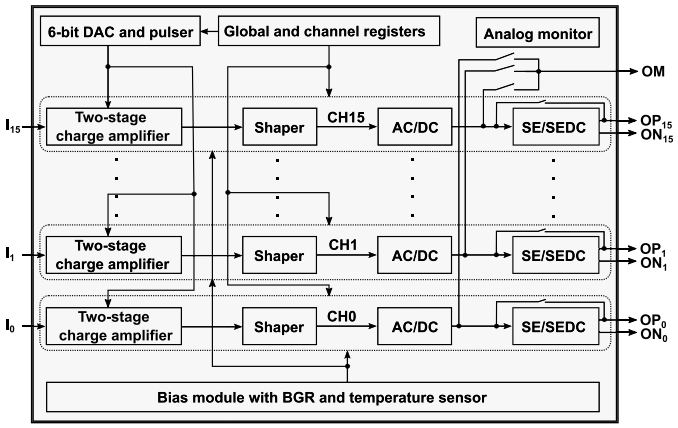

Fig. 2. Top-level block diagram of the LArASIC architecture.

II. Front-End Architecture and Design

The overall architecture of LArASIC is shown in Fig. 2. It comprises of 16 independent channels that include two stages of charge amplifiers [20] designed for achieving low-noise with a detector capacitance of 100-200 pF. The first stage provides a fixed charge gain of 20, and the second stage provides a programmable charge gain of 3, 5, 9 or 16, resulting in a total charge gain of 60, 100, 180 or 320 for readout of charges up to 300 fC, 180 fC, 100 fC and 56 fC, respectively.

The charge amplifiers are followed by a shaping filter [21] to produce semi-Gaussian voltage pulses with programmable peaking time, T_p, of 0.5 μs, 1.0 μs, 2.0 μs, or 3.0 μs. The shaping filter converts the amplified current signals to voltage pulses with channel gain of 4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, or 25 mV/fC, for programmable charge gain of 60, 100, 180 or 320, respectively. It also provides anti-aliasing before digitization. As an example, the channel response of LArASIC in time domain as well as in frequency domain for different peaking times is shown in Fig. 3. For an ADC sampling frequency f_s of $2/T_p$, the -3 dB frequency for each value of T_p is almost a decade lower than f_s, where the channel gain is reduced by $\approx$70-80 dB, thus providing Nyquist-rate sampling without aliasing.

Different pulse peaking times provide flexibility in accommodating different speeds at which the charge flow forms an input signal. They also present a trade-off between contributions from series voltage and parallel current noise sources [22]. The series voltage noise represents noise form the amplifier and is proportional to the total capacitance at the input of the front-end, including the detector capacitance. On the other hand, the parallel current noise represents noise originating from current flow in parallel with the signal source,

[1]During the latest production run of LArASIC, 250 wafers were fabricated with a total of 150,000 dies, achieving 99% yield.

[2]LArASIC was tested at LNT, which is close to LArT, due to lower cost and ease of availability of liquid nitrogen.

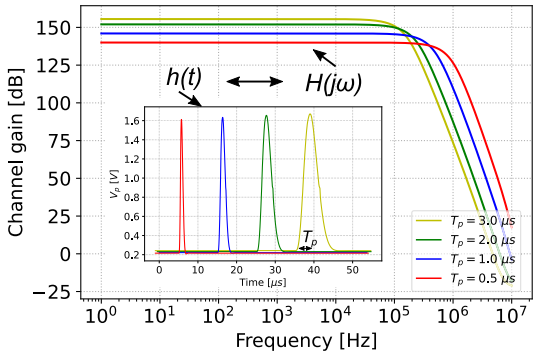

Fig. 3. LArASIC channel response in time and frequency domains for different values of peaking time, T_p.

such as due to the detector leakage current or the parallel resistance present in the charge amplifier feedback path.

The shaping filter output can be either AC- or DC-coupled to the output of LArASIC, and read out either directly, through a single-ended (SE) buffer, or through a single-ended-to-differential converter (SEDC) buffer. The SE and SEDC buffers are suitable for driving larger capacitive loads. Additionally, the direct outputs of the 16 shaping filters can be multiplexed and probed on a single wire for testing purposes. The output baseline voltage, i.e., the DC value of the output voltage, with respect to which pulse amplitudes are measured, can be set to either 200 mV or 900 mV for collecting and non-collecting modes respectively. The 200 mV baseline allows processing of input charges of only one polarity, i.e., negative, but with ample headroom for a maximum swing of 1.4 V to provide a dynamic range (DR) $\geq$ 10-bits. On the other hand, the 900 mV baseline allows processing of either both positive and negative input charges, or bipolar signals, but has a reduced one-sided DR.

Global and channel registers, programmed through a three-wire serial peripheral interface (SPI), are used to set operational conditions of LArASIC, such as the charge gain, peaking time, baseline voltage level, buffering mode, and other settings for each channel. A 6-bit digital-to-analog converter (DAC) and test-charge pulser are also included on the chip to provide test inputs to the charge amplifiers and calibrate the channels. All biasing circuits utilize a bandgap voltage reference (BGR) for ensuring desired operation of the channels with constant current at temperatures ranging between room temperature (RT) and LNT. The output of the BGR can be monitored externally, along with a temperature-sense voltage. It should be noted that the design details and results presented in this paper mainly pertain to the core channel circuits, and description of auxiliary circuits such as the BGR, bias networks, SPI interface, DAC, and test pulser are out of the scope of the current paper.

The overall architecture and design specifications of CHARMS are similar to LArASIC. However, the higher f_T of the 65 nm process is exploited to achieve a minimum shaping filter peaking time of 0.25 μs, as opposed to LArASIC's 0.5 μs, for the same power consumption, thus supporting faster processing and increased timing resolution. Additionally, digital programmability in CHARMS is provided by a 2-wire I^2C interface that is enhanced to prevent drift of the baseline voltage, as described in the next section.

A. Charge Amplifiers

Each channel of LArASIC contains two cascaded charge-amplification stages CA_1 and CA_2, as shown in Fig. 4. Each stage integrates the current delivered to its input through the feedback capacitors C_{f1}, equal to 950 fF, and C_{f2}, equal to 8 pF, around the single-ended, high open-loop-gain voltage amplifiers A_1 and A_2, respectively. The value of these capacitors is chosen so as to prevent saturation at the amplifier outputs within the range of expected input charges. The pre-bias reset quiescent current, I_{RQI}, flowing through M_{n1} can be chosen from four different values, i.e., 100 pA, 500 pA, 1 nA, or 5 nA through digital control of the voltage V_{leak} and sets the DC-level at the output of amplifier A_1. Stabilization of the DC-operating point of CA_1 and a continuous adaptive reset mechanism [23] for the output of A_1, V_{out1}, are provided by M_{n2} and the current mirror formed by M_{p2} and M_{p1}.

In response to a current pulse at the input of A_1, a voltage step is produced at V_{out1}, that shows a non-linear and input-current-dependent return to the baseline as a function of time [24]. Multiplication and coupling of charge to the next charge amplification stage with compensation of this non-linearity is performed by the transistor M_{p3} and capacitor C_{m1}, implemented using multiple copies of identically sized transistor and metal-insulator-metal (MiM) capacitor segments that are used to implement M_{p1} and C_{f1}, respectively. By precise sizing of these components, along with nearly equal DC potentials achieved at nodes V_x and V_y by ensuring equal density of current flows through the input transistors of A_1 and A_2, precise multiplication of the total input charge by a factor equal to the ratio of C_{m1} and C_{f1}, which is also equal to the ratio of widths of M_{p3} and M_{p1}, is performed. Thus, the output current of CA_1, I_1, follows the narrow, pulse-like shape of the input current, I_{in}, as a result of pole-zero cancellation [25] between feedback and coupling elements of CA_1. However, it is broadened in time due to the finite bandwidth of CA_1.

The second charge amplification stage, CA_2, operates similarly. For precise charge multiplication to be performed by CA_2, nearly equal DC-potentials at nodes V_y and V_z would also be preferred. However, the voltage at V_z is set by the differential amplifier in the shaping filter stage that follows CA_2 to either 300 mV or 900 mV depending on the output baseline setting. Thus, M_{n6} is included in a cascode configuration to reduce the channel-length modulation effect on M_{n5} that would impact the output current I_2 of CA_2. CA_1 is designed to provide a fixed charge-gain of 20 as the ratio of C_{m1} and C_{f1} is 20, and the ratio of widths of M_{p3} and M_{p1} is also 20. CA_2 is designed to provide a programmable charge gain of 3, 5, 9 or 16 by selectively switching 'on' parallel, adequately defined portions of C_{m2}, M_{n5}, and M_{n6}.

As a consequence of the charge multiplication performed by CA_1, the pre-bias current of CA_2 flowing through M_{p3} is also multiplied, causing a greater drift in the baseline voltage at the output of the amplifier A_2 and reducing the headroom for handling the signal swing. Thus, the CHARMS chip, which is currently in development, targets reduction of this drift by subtracting the pre-bias current of CA_2 through the transistor $M_{n3\text{-}sub}$, as shown in Fig. 5. In the absence of layout-induced

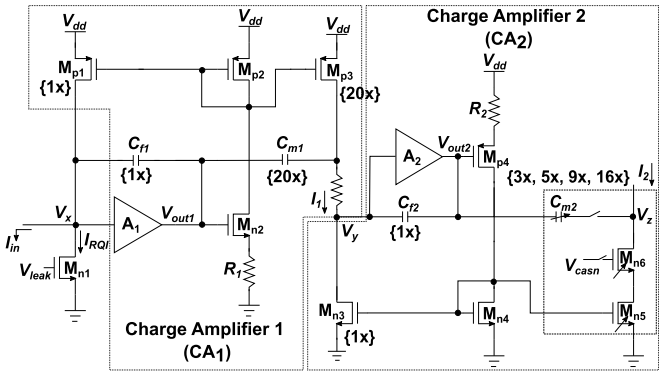

Fig. 4. Schematic diagram of the charge amplifiers CA_1 and CA_2.

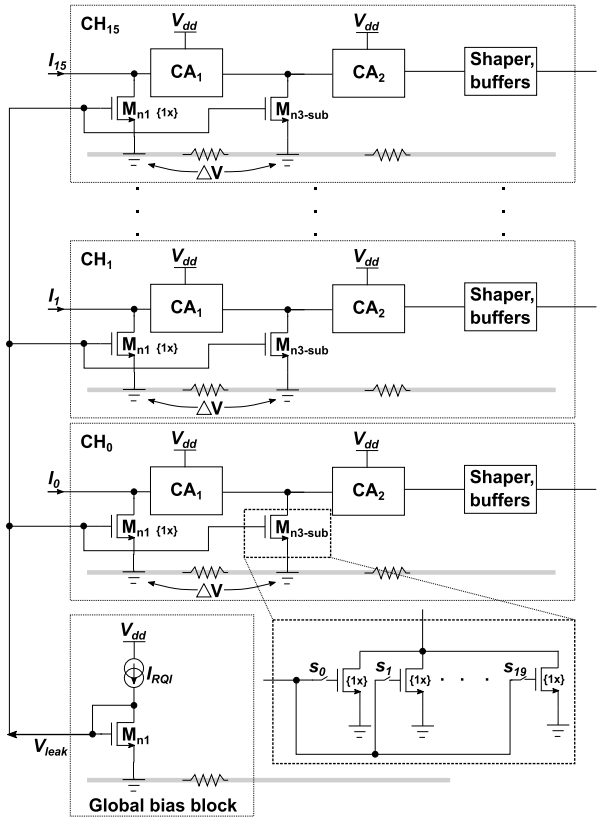

Fig. 5. Digitally-assisted implementation of I_{RQI} subtraction at the output of the amplifier CA_1 in CHARMS.

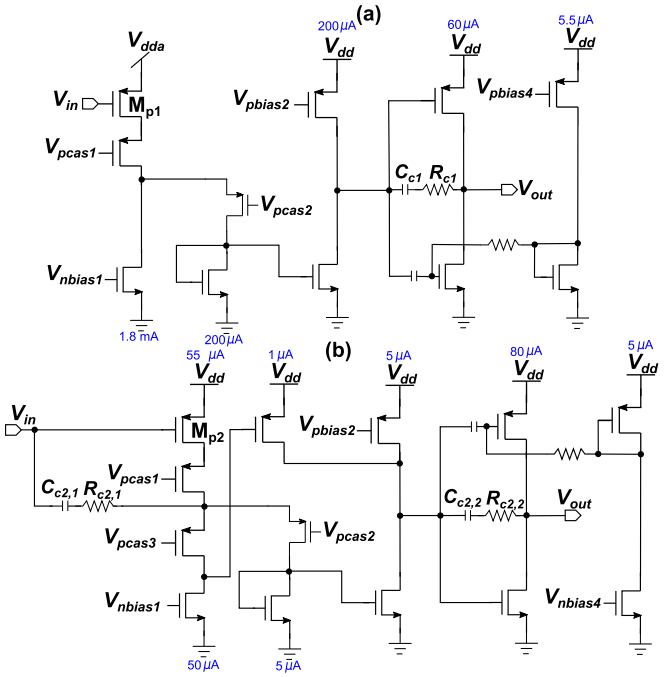

Fig. 6. Schematic diagrams of the high open-loop-gain amplifiers (a) A_1 and (b) A_2 used in the amplifiers CA_1 and CA_2.

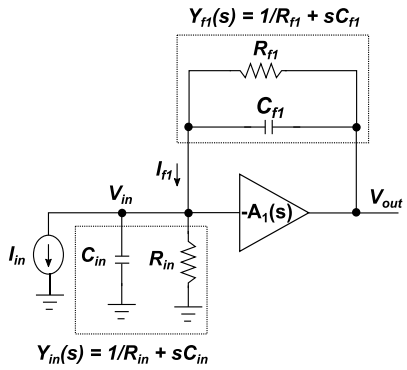

Fig. 7. Representation of the CA_1 input and feedback paths as a simplified equivalent circuit.

non-idealities, Monte Carlo simulations at RT indicate a 16× I_{RQI} subtraction to be optimal [26]. However, the measurements showed that the voltage V_{leak}, which is generated by the global bias block and distributed to transistors M_{n1} and $M_{n3\text{-}sub}$ in the two charge amplification stages in each channel, is not identical between the two charge amplifiers due to IR drops introduced by the series resistance of the ground interconnect. Thus, the gate-source voltage, V_{gs}, seen by these transistors, is also mismatched. Furthermore, these transistors operate in deep subthreshold, where the dependence of the drain current on V_{gs} is proportional to $e^{(V_{gs}-V_{th})(q/\eta kT)}$, and increases at LNT compared to RT. During measurements, the variability in the subtracted I_{RQI} was observed to be almost 10× higher at LNT than at RT, and even a few mV of V_{gs} mismatch was sufficient to cause the effective subtraction to become greater than 20× and make the continuous reset mechanism of CA_2 inactive. Therefore, instead of fixing the subtraction factor to a constant value equal to the ratio of the widths of $M_{n3\text{-}sub}$ and M_{n1}, the I_{RQI} subtraction in CHARMS can be programmed by 20 thermometer-coded switches, as shown in Fig. 5. The inclusion of 5-bits of programmability for the I_{RQI} subtraction is expected to make the revised design more robust to increased variability at LNT and layout-induced non-idealities.

The amplifiers A_1 and A_2, which are shown in Fig. 6, use three-stage designs with a folded-cascode first stage, a high-gain common-source second stage, and a push-pull output stage. The charge amplifier CA_1 uses both nulling-resistor-based Miller compensation, provided by C_{c1} and R_{c1} between the second and third stages of A_1, and reduced gain compensation, provided by the feedback path, to ensure closed-loop stability. A simplified circuit representation of the elements in CA_1 that contribute to its loop gain and closed-loop stability is shown in Fig. 7, where C_{in} and R_{in} represent the equivalent total capacitance and resistance seen at the input of CA_1, $A_1(s)$ represents the frequency response

of the amplifier A_1, C_{f1} is the feedback capacitance of CA_1, and R_{f1} is a resistor modeling the reset current provided by the M_{p1}, M_{p2} current mirror in Fig. 4. Although the feedback current of the charge amplifiers is input signal-dependent and time-variant, it has been modeled here as a linear resistance to simplify the analysis. The loop gain, $L(s)$, of CA_1 is

$$L(s) = -\frac{Y_{f1}(s)}{Y_{in}(s)} \times A_1(s) = -\frac{1 + sC_{f1}R_{f1}}{R_{f1}} \times \frac{R_{in}}{1 + sC_{in}R_{in}} \times A_1(s). \quad (1)$$

At high frequencies, $|L(s)|$ is given by

$$|L(s)| = \frac{C_{f1}}{C_{in}} \times |A_1(s)|. \quad (2)$$

For CA_1, $C_{f1} = 950\,\text{fF}$ and $C_{in} = 190\,\text{pF}$; the latter comprising of the gate-capacitance of transistor M_{p1} in Fig. 6, which is $\approx 40\,\text{pF}$, and the detector capacitance, which is 150 pF. Thus, at high frequencies, the magnitude of the loop gain $L(s)$ is scaled by a ratio of $C_{f1}/C_{in} \approx -46$ dB, which acts as reduced gain compensation. Similarly, CA_2 is compensated using both Miller compensation via $C_{c2,2}$ and $R_{c2,2}$, and reduced gain compensation via $C_{c2,1}$ and $R_{c2,1}$.

The input transistor of A_1, M_{p1}, which plays a crucial role in determining the total ENC [27] of the channel, utilizes an independent power supply, V_{dda}, to prevent coupling of power-supply interference from other circuits in the channel. Based on earlier noise-characterization measurements at cryogenic temperatures [19], implementing M_{p1} as a p-channel transistor is preferable for reducing $1/f$ noise. The device is biased at 2 mA, operated in moderate inversion and sized to have a gate capacitance of $\approx 40\,\text{pF}$ to ensure comparable contributions from thermal and low frequency noise and, thus minimizing the ENC for a detector capacitance of 150 pF. Specifically, M_{p1} has a length of $L = 270\,\text{nm}$ to avoid the increase of $1/f$ noise in minimal length transistors [28], [29] and a total width of 20 mm, split into 400 fingers, resulting in a gate capacitance of $\approx 40\,\text{pF}$. The design of the charge amplifiers CA_1 and CA_2 for CHARMS is similar to that of LArASIC, but both thin-oxide 1.2 V transistors and thick-oxide 2.5 V transistors are used. To support a DR $\geq$ 10-bits, circuits in CHARMS utilize a 1.8 V power supply, and thick-oxide transistors are used where voltage swings larger than the core voltage of 1.2 V are expected. Thick oxide transistors are also utilized for elements where minimizing gate leakage current is essential. For example, the input transistor, M_{p1}, of the amplifier A_1 in CHARMS is a thick-oxide transistor with a length of $L = 400\,\text{nm}$ and a total width of $W = 24\,\text{mm}$ to achieve the optimal gate capacitance of 40 pF. Using a thin-oxide device with the same dimensions would result in a gate leakage current I_L of $\approx 20\,\text{nA}$. Its contribution to the ENC, assuming a triangular weighting function, would be $(q_e I_L T_p/3)^{1/2}$ [22], which for a peaking time T_p of 1 μs, is equal to 3.27×10^{-17} C or a charge given by 204 electrons. Whereas, for the thick-oxide device used to implement the input transistor M_{p1} of the amplifier A_1 in CHARMS, the gate leakage current is negligibly small, thus making its contribution to the parallel noise component of the ENC close to zero.

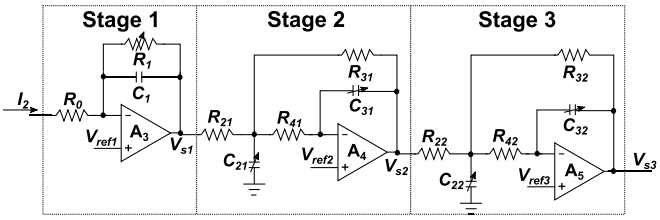

Fig. 8. Schematic diagram of the 5th order shaping filter.

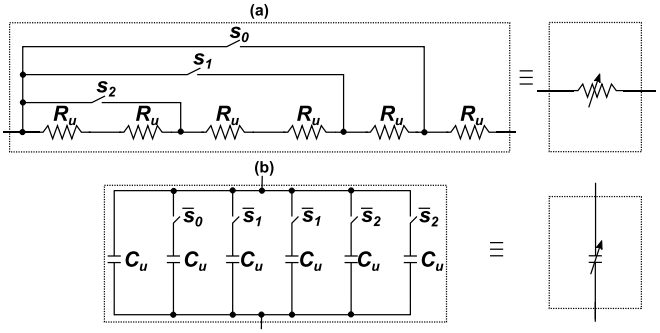

Fig. 9. Configuration for making (a) R_1 programmable, and (b) $C_{21}, C_{31}, C_{22}, C_{32}$ programmable.

B. Pulse Shaping Filter

The charge amplification stages are followed by a fifth-order semi-Gaussian pulse-shaping filter, shown in Fig. 8, that converts amplified current pulses to symmetric voltage pulses exhibiting nearly equal rise and fall times. Making the pulse rise and fall times nearly equal ensures that the weighting function performed by the channel best matches the $\delta(t)$ distribution of the input charge signal [22]. Additionally, the semi-Gaussian pulse shape leads to both a faster pulse drop-off and considerably lower RMS noise voltage than an exponential decay constructed using a CR differentiator and a cascade of RC integrators [30].

The shaping filter comprises of three stages. The first stage is a first-order low-pass filter, with a resistor and a capacitor in parallel in the feedback path of a high open-loop gain differential amplifier, that converts the amplified current signal to a voltage. The value of the resistor is chosen so that its parallel noise contribution is insignificant. The first stage is followed by a cascade of two second-order low-pass filter stages with complex conjugate poles. The filter coefficients are selected so as to approximate the filter transfer function to that of a Gaussian with the desired peaking time [31]. The transfer functions of the first two shaping filter stages are

$$\frac{V_{s1}(s)}{I_2(s)} = -\frac{k_1\omega_1}{s + \omega_1} \quad \text{and} \quad \frac{V_{s2}(s)}{V_{s1}(s)} = -\frac{k_2\omega_2^2}{s^2 + 2\zeta\omega_2 s + \omega_2^2}, \quad (3)$$

where $k_1 = R_1$, $\omega_1 = \frac{1}{R_1 C_1}$, $k_2 = \frac{R_{31}}{R_{21}}$, $2\zeta\omega_2 = \frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}}$, and $\omega_2^2 = \frac{1}{R_{31}R_{41}C_{21}C_{31}}$. The transfer function of the third stage is similar to that of the second stage, but with appropriate resistor and capacitor values (R_{21} replaced by R_{22}, etc.).

The shaping times can be programmed by setting R_1, C_{21}, C_{31}, C_{22} and C_{32} using digitally controlled switches, as shown

TABLE I
SWITCH SETTINGS FOR PROGRAMMABLE PEAKING TIMES

Peaking Time (T_p)	s_0	s_1	s_2
0.5 µs	1	1	1
1.0 µs	0	1	1
2.0 µs	0	0	1
3.0 µs	0	0	0

TABLE II
SHAPING FILTER COMPONENT VALUES

Resistor	Value (kΩ)	Capacitor	Value (pF)
R_0	0.3		
R_u (R_1)	15	C_1	11.9
R_{21}, R_{41}, R_{42}	18	C_u (C_{21})	11.9
R_{31}	60	C_u (C_{31})	2.3
R_{22}	36	C_u (C_{22})	11.9
R_{32}	39	C_u (C_{32})	2.6

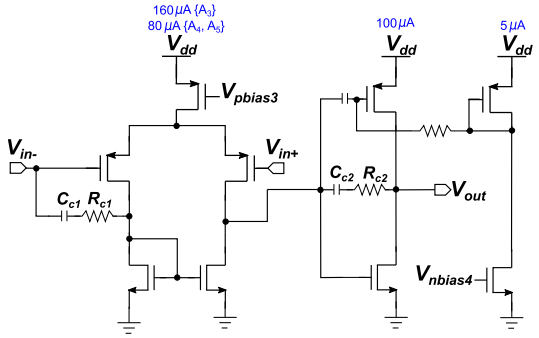

Fig. 10. Schematic diagrams of the amplifiers A_3, A_4, and A_5.

in Fig. 9 and Table I. Scaling the values of R_1, C_{21}, C_{31}, C_{22} and C_{32} simultaneously by a constant factor retains the semi-Gaussian pulse shape, but scales the peaking time by the same factor. Resistors are implemented as poly-resistors and capacitors as MiM capacitors to minimize distortion of the processed signals, which swing almost rail-to-rail. Among the several available solutions that approximate the filter transfer function to that of a Gaussian, the resistance and capacitance values here are chosen so as to allow an on-chip realization that is practical in terms of area usage, and at the same time provides tolerance against mismatch. The values of these components for LArASIC are listed in Table II. For CHARMS, the shortest peaking time of 0.25 μs is realized by scaling the values of the variable components by a factor of 0.5, and using a switch configuration similar to the one shown in Fig. 9 to obtain additional shaping times of 0.5 μs, 1.0 μs, and 2.0 μs.

The amplifiers A_3, A_4, and A_5 in the shaping filter are implemented as two-stage amplifiers with a differential input stage and push-pull output stage, as shown in Fig. 10. The reference voltages V_{ref1}, V_{ref2}, V_{ref3} shown in Fig. 8 are equal to 900 mV for the 900 mV baseline setting, whereas V_{ref1} is set to 300 mV, V_{ref2} to 600 mV and V_{ref3} to 900 mV for the 200 mV baseline setting. All the reference voltages are derived from the BGR. As the amplified input charge is converted to a voltage signal by the shaping filter, the channel overall provides a gain that is the ratio of the voltage amplitude of the output pulse and the input charge. The total gain of the channel is 4.7 mV/fC, 7.8 mV/fC, 14 mV/fC and 25 mV/fC for charge gains of 60, 100, 180, and 320, respectively, provided by the charge amplification stages.

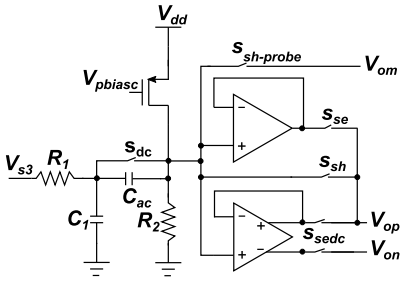

Fig. 11. Output driver with selectable configurations: AC or DC-coupling of the channel and selection between direct, SE, or SEDC driving.

C. Output Drivers

The shaping filter output for each channel, as shown in Fig. 11, can internally be either AC- or DC-coupled to the output using the switch s_{dc}. The output can be read out either directly by turning on the switch s_{sh}, through a SE buffer when driving large capacitive loads by turning on the switch s_{se}, or through an SEDC buffer to additionally provide better inter-channel crosstalk immunity by turning on the switch s_{sedc}. The SE buffer circuit is shown in Fig. 12. It is based on a folded-cascode current-mirror-based operational transconductance amplifier [32], comprising of parallel NMOS and PMOS input pairs implemented by the transistors M_{n1}, M_{n2} and M_{p1}, M_{p2} to support rail-to-rail input operation. Current mirrors formed by the transistors M_7, M_{p9}, M_{p13}, M_{15} and M_{p8}, M_{p10}, M_{p14}, M_{p16} sum the signals provided by the two sides of the rail-to-rail input stages, and mirroring by the transistors M_{n15}-M_{n18} converts the output to a single ended-signal. Transistors M_{n13} and M_{p18} act as the pre-drivers for biasing the Monticelli class-AB output stage formed by M_{n19} and M_{p19} [33], [34], which is Miller compensated using C_c and R_c.

The SEDC buffer circuit generates a differential representation of the signal via the connection of its non-inverting output, V_{op}, to its inverting input, V_{in} [35], as shown in Fig. 13. Since the buffer's inputs are virtually shorted, V_{op} follows V_{ip}. The common-mode input voltage, V_{cm}, is compared with the average of V_{op} and V_{on}, i.e., $V_{o,avg}$, so V_{on} is given by

$$V_{on} = 2V_{cm} - V_{ip}. \tag{4}$$

The differential output, V_{od}, produced by the SEDC is

$$V_{od} = V_{op} - V_{on} = 2V_{ip} - 2V_{cm}, \tag{5}$$

thus achieving a conversion gain of 6 dB.

Compared to the resistor based [36] or three-operational-amplifier-based [37] SEDC designs, the proposed design is simpler and has a smaller footprint and power consumption. However, it also transfers noise from the common-mode input, V_{cm}, to the output with a gain of 6 dB. Therefore, it is necessary to have very good filtering of this common-mode signal. The global BGR-generated reference voltage, $V_{cm} \approx V_{DD}/2$, is accordingly low-pass filtered on-chip as shown in Fig. 14, first globally using R_0 and C_0, and then locally within

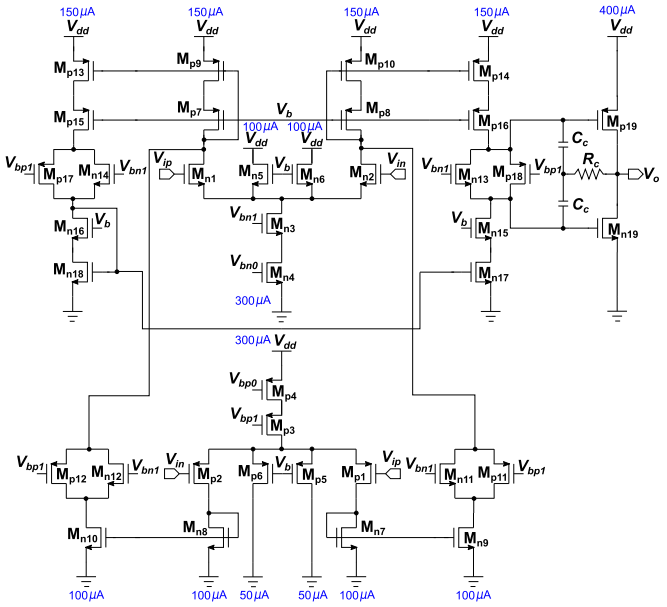

Fig. 12. Schematic diagram of the SE buffer with complementary PMOS and NMOS differential input stages and push-pull, class A-B output stage.

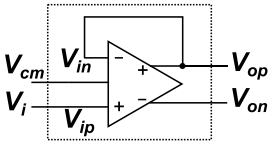

Fig. 13. Architecture of the SEDC buffer with only one operational amplifier.

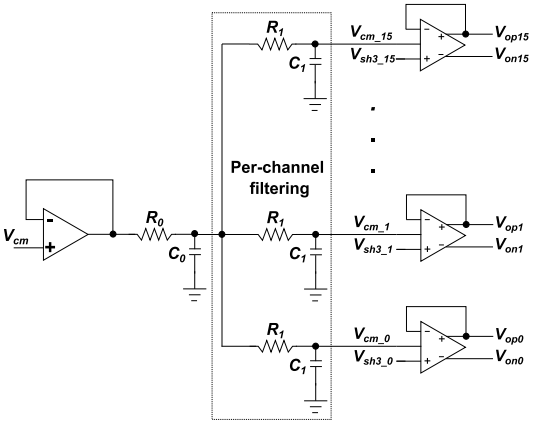

Fig. 14. Per-channel filtering of the SEDC common-mode input signal, V_{cm}.

each channel using R_1 and C_1. Two-stage filtering ensures excellent inter-channel crosstalk, as discussed in Section IV.

In the chosen configuration, V_{op} follows V_{ip} with high-accuracy if the open-loop gain of the differential path is high. Whereas, for V_{on} to change in the opposite direction to accurately create a differential signal, the open-loop gain of the common-mode path should also be high. Thus, both paths should have high open-loop gains and comparable bandwidths to achieve a high fidelity differential signal.

The SEDC buffer circuit [38] is similar to the SE buffer, but comprises of a fully-differential core, including differential-inputs and differential-outputs provided by M_{n19}, M_{p19} and M_{n20}, M_{p20}, as shown in Fig. 15. The common-mode feedback (CMFB) circuit is also designed for operation with rail-to-rail swings. It comprises of an error amplifier that senses the common-mode output voltage $V_{o,avg}$, i.e., the

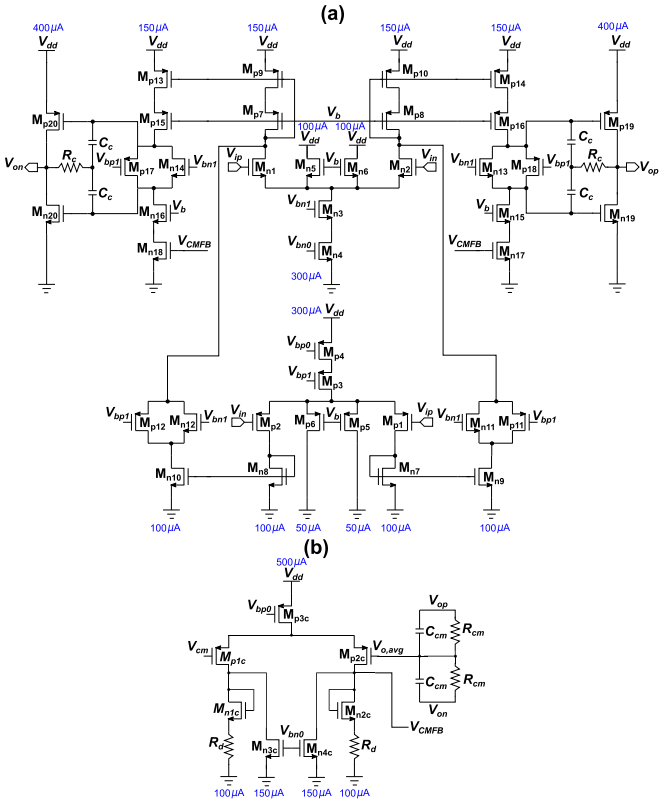

Fig. 15. (a) Schematic diagram of the main SEDC buffer with complementary PMOS and NMOS differential input stages and push-pull, class A-B output stages, and (b) schematic diagram of the CMFB path used in the SEDC buffer.

average of V_{op} and V_{on} via 10 kΩ R_{cm} resistors, compares it against V_{cm} and produces V_{CMFB}, which is fed back to the transistors M_{n17} and M_{n18} in the main amplifier. The gain of the CMFB differential pair is boosted using current subtraction transistors M_{n3c}, M_{n4c} and R_D resistors. The resistors are connected to the source of the diode-connected loads and provide g_m degeneration. Here, the sense resistors are un-buffered to minimize the power consumption. The capacitors C_{cm} provide a zero in the left-half s-plane to improve CFMB stability.

III. Simulation Results

As the BSIM4 [39] foundry models for the 180 nm and 65 nm processes are accurate only for temperatures between 235 K and 400 K, PSP [40] [41] models extracted from I-V and C-V characteristics of MOS test structures operating at LArT were used for simulations of the circuits in LArASIC and CHARMS at cryogenic temperatures. For non-MOS components such as resistors and capacitors, simulations at LArT were carried out by extrapolating the foundry models available in the process design kit. The simulation results presented in section III-A are for pre-layout schematics in LArASIC; they closely match the measured results presented in Section IV. Section III-B presents some simulation results for CHARMS.

A. Results for LArASIC

The AC simulation results of the response of the charge amplifiers CA_1 and CA_2 at both RT and LArT are shown in Fig. 16. The amplifiers A_1 and A_2 utilized in CA_1 and CA_2 achieve open-loop DC voltage gains greater than 90 dB at

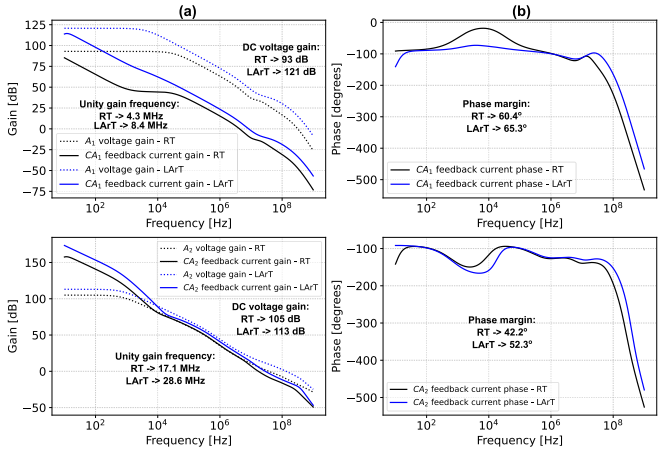

Fig. 16. AC (a) magnitude and, (b) phase responses for the charge amplifiers CA_1 (top) and CA_2 (bottom) in LArASIC at RT and LArT.

both RT and LArT, which helps with achieving precise charge multiplication. Both the DC gain and bandwidth increase at LArT compared to RT are due to the larger transconductance at cryogenic temperatures [16], [17], [18], [19]. The charge amplifier CA_1 achieves a unity gain frequency of 4.3 MHz at RT and 8.4 MHz at LArT, which sets the pulse width of the output current I_1 to approximately 200 ns-300 ns. This ensures minimal degradation of linearity in the output pulse response of the shaping filter for peaking times $\geq 0.5\,\mu$s due to reduction of the peak pulse amplitude because of long transients in I_{in} and I_1, a phenomenon known as ballistic deficit in nuclear electronics [42]. The phase margin (PM) of 60.4° for CA_1 at RT ensures that the amplifier is stable for detector capacitance values between 0 and 150 pF with an optimal transient settling time; the PM increases to 65.3° at LArT. The unity gain frequency of CA_2 at both RT and LArT is sufficiently high to process the output of CA_1 with good fidelity and high linearity. The PM of 52.3° for CA_2 at LArT ensures stability and a fast-settling transient response, and a slightly lower PM of 42.2° at RT avoids over-design at RT.

The transient response of the charge amplifiers for different gain settings was simulated at LArT by modeling the input source as a current pulse in parallel with a 150 pF capacitor representing the detector capacitance. The amplitude and pulse width for these current pulses, as shown in Fig. 17(a), were chosen to be 50 μA and 1 ns, respectively, so as to model an input charge injection of 50 fC, which lies within the operational range of the front-end for even the largest gain setting of 320. These pulses were injected at an interval of 200 μs, which is slow enough to ensure that the circuits are able to respond to the periodic input charge injections without saturating. The input current pulses are integrated by the amplifier A_1 to produce voltage steps at V_{out1} that decay to the baseline, as shown in Fig. 17(b). The voltage step return to the baseline is as a result of the reset current provided by the current mirror formed by M_{p1} and M_{p2} in Fig. 4. Due to the 20-× charge multiplication and pole-zero cancellation provided by CA_1, sharp, amplified I_1 current pulses are produced at the output of CA_1 as shown in Fig. 17(c). The amplified I_1 current pulses produced by CA_1 are once again integrated by the amplifier A_2 to produce negative voltage steps at V_{out2}, as shown in

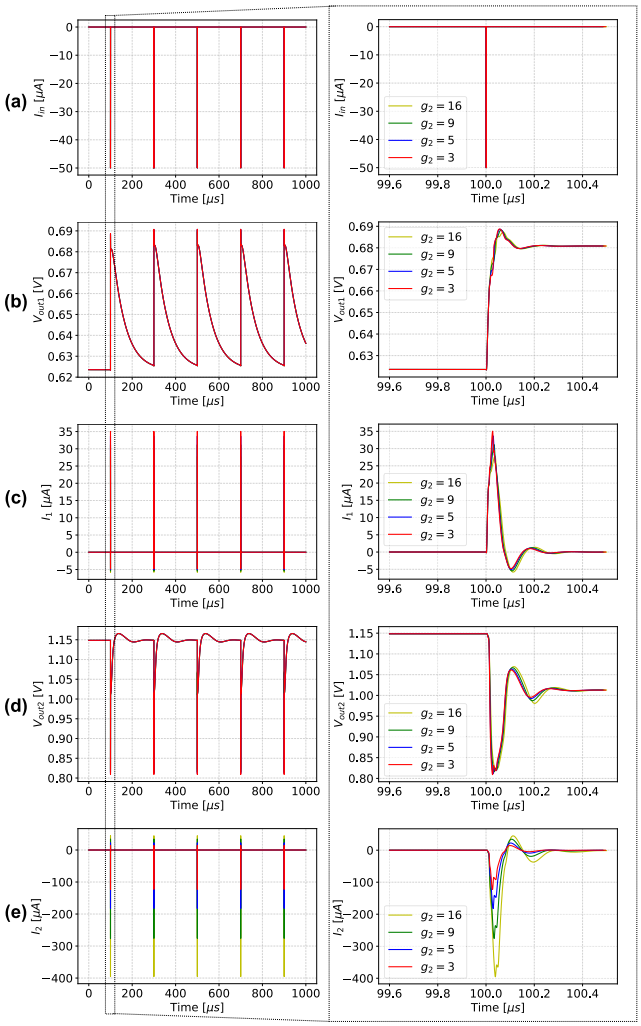

Fig. 17. Simulated charge amplifier responses for LArASIC at LArT for different values of the second stage charge gain (g_2) for the input charge injections of 50 fC and I_{RQI} equal to 500 pA. The plots in the right-hand column show zoomed-in sections of the x-axis, highlighting the response to a single input pulse.

Fig.17(d). The voltage steps at V_{out2} also decay as a result of the reset current provided by the current mirror formed by M_{n3} and M_{n4} in Fig. 4. However, the return of V_{out2} to the baseline voltage is faster than that of V_{out1} since the reset quiescent current injected into CA_2 is multiplied by 20 by CA_1. Finally, in response to the pole-zero cancellation and programmable charge gain (g_2) provided by CA_2, sharp I_2 current pulses of different amplitudes are produced at the output of CA_2, and are shown in Fig. 17(e). The right panels in Fig. 17 show the zoomed-in responses for I_{in}, V_{out1}, I_1, V_{out2}, and I_2 and their corresponding settling characteristics for a single input pulse. All signals settle within approximately 300 ns, and thus do not cause degradation of linearity for the shaping filter peaking times implemented in LArASIC.

To verify that the charge multiplication factors of CA_1 and CA_2 comply with design requirements, the output currents I_1 and I_2 in Fig. 17 were integrated, normalized, and plotted alongside the integrated input current I_{in}. The resulting curves for the case when CA_2 gain (g_2) is 16 are shown in Fig. 18, where I_1 was normalized by the gain of CA_1, i.e., 20, I_2 was

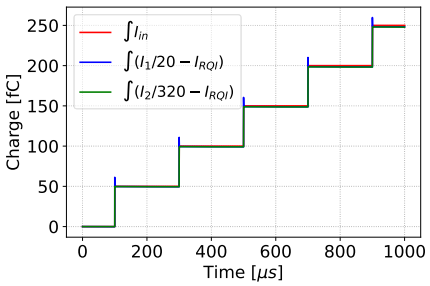

Fig. 18. Normalized integrated output currents, I_1 and I_2, compared to the integrated input current, I_{in}, for the results shown in Fig. 17, given $g_2 = 16$.

TABLE III
AMPLIFIER A_3 AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	61 dB	74.2 MHz	78.7°
LArT	69 dB	197.7 MHz	79.5°

TABLE IV
AMPLIFIER A_4 AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	60 dB	23.4 MHz	96.7°
LArT	63 dB	63.9 MHz	94.9°

TABLE V
AMPLIFIER A_5 AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	60 dB	16.6 MHz	96.8°
LArT	74 dB	74.3 MHz	89.6°

normalized by the product of gains of CA_1 and CA_2, i.e., 20×16, or 320, and the pre-bias current I_{RQI} was subtracted from both, so as to compare the output currents of CA_1 and CA_2 only in response to the input charge injections. The overlapping 50 fC steps in each of these curves for every new input pulse shows that the charge amplifiers perform multiplication by the desired gain factors with high accuracy.

The two-stage Miller compensated amplifiers A_3, A_4, and A_5, used in the shaping filter and shown in Fig. 10, were designed to provide DC open-loop voltage gains > 60 dB and a unity gain frequency sufficiently larger than the expected input signal bandwidth at both RT and LArT. The differential input-stage of the amplifier A_3 is biased with a current that is $2\times$ larger than the first-stage bias currents for the amplifiers A_4 and A_5, as A_3 outputs signals with the highest slew-rate. The simulated AC parameters of amplifiers A_3, A_4 and A_5 at RT and LArT are summarized in Tables III, IV and V. The amplifiers are compensated to obtain a PM close to 90° at both RT and LArT.

The transient response of the shaping filter at LArT was simulated by feeding the output current of the charge amplification stages into its input. The output voltages V_{s1}, V_{s2}, and V_{s3} of the three shaping filter stages are shown in Fig. 19(a) for peaking times of 0.5 μs, 1.0 μs, 2.0 μs and 3.0 μs, and 50 fC input injection with CA_2 gain (g_2) of 3, in the collecting mode, when input charges of only negative polarity can be processed.

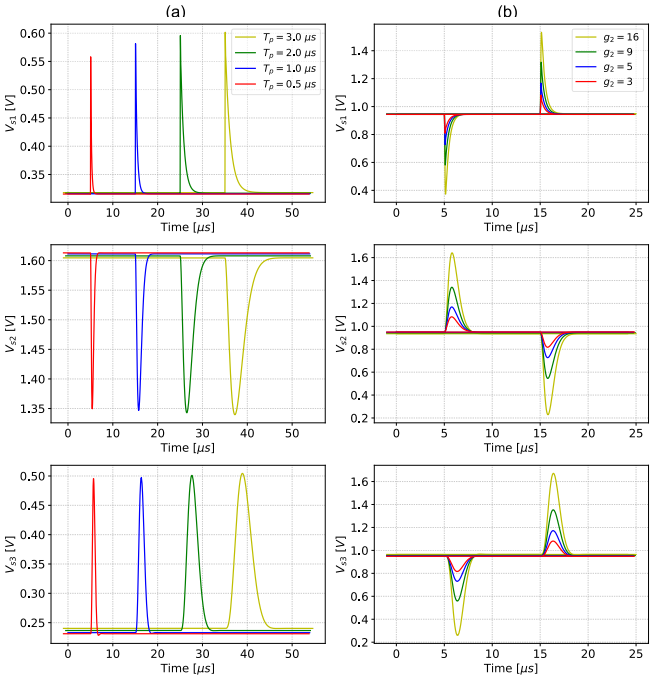

Fig. 19. Simulated responses of the shaping filter stages in LArASIC at LArT for (a) different values of the peaking time T_p in the collecting mode with an input charge of 50 fC and $g_2 = 3$, (b) different values of g_2 in the non-collecting mode with an input charge of 25 fC and $T_p = 1\ \mu$s.

TABLE VI
SE BUFFER AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	86 dB	40.4 MHz	42.8°
LArT	118 dB	104.2 MHz	39.2°

TABLE VII
SEDC BUFFER MAIN LOOP AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	99 dB	32.0 MHz	60.5°
LArT	113 dB	117.2 MHz	57.3°

The rise and fall times become progressively more symmetric as the signal propagates through the three stages. Simulation of the shaping filter stages in the non-collecting mode, when either both negative and positive input charges, or charges that are bipolar, can be processed, are shown in Fig. 19(b). Here, the response of the three stages is shown for a fixed peaking time of 1.0 μs and variable charge gain settings. In the non-collecting mode, the one-sided DR of the front-end is reduced by half. Therefore, the input injection was chosen to be 25 fC to prevent saturation for the largest gain setting.

To ensure stable operation of the SE and SEDC buffers, AC simulations were carried out with a typically expected load, comprising of a 10 pF capacitor in parallel with a 40 kΩ resistance, modeling the trace between LArASIC and the ColdADC chip [10] that digitizes its output, and the input impedance of the sample and hold amplifier in ColdADC, respectively. The simulated AC parameters of the buffers at RT and LArT are summarized in Tables VI, VII and VIII. The high open-loop DC gains for the SE buffer, main loop

TABLE VIII
SEDC BUFFER CMFB LOOP AC PARAMETERS

Temperature	DC gain	Unity gain frequency	Phase margin
RT	112.8 dB	34.9 MHz	49.5°
LArT	127.5 dB	104 MHz	74.6°

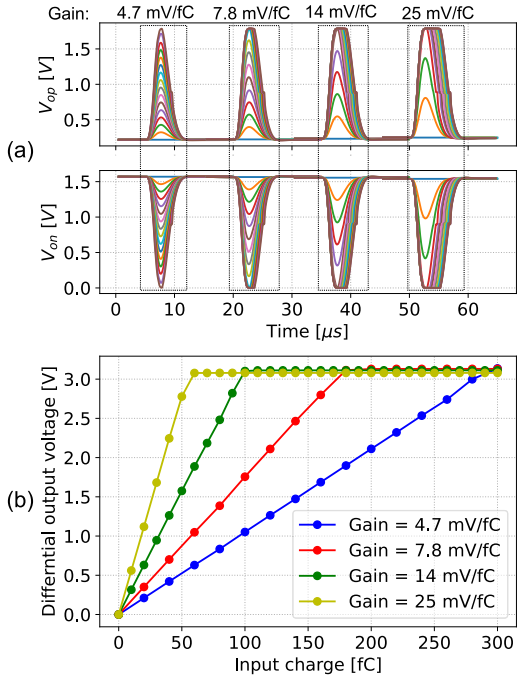

Fig. 20. Simulated SEDC output for LArASIC in the collecting mode at LArT for different gain settings as input charge is swept from 0 to 300 fC showing (a) transient response (b) output voltage amplitude versus input charge.

and CMFB loops of the SEDC buffer at both RT and LArT ensure that they introduce minimal non-linearity to the output signal. Additionally, comparable bandwidths of the main loop and CMFB loop of the SEDC buffer ensure that the differential output signal produced by the SEDC buffer exhibits minimal distortion. The transient response of the SEDC buffer in the collecting mode was simulated at LArT for different gain settings and variable input injections between 0 fC and 300 fC. Fig. 20(a) shows the waveforms produced at the output of the SEDC buffer. The differential output signal has a maximum amplitude of 3.2 V, and starts approaching saturation at about 56 fC, 90 fC, 180 fC, and 260 fC for the second-stage charge gain settings of 3, 5, 9, and 16, resulting in voltage gains of 4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, and 25 mV/fC, respectively. The output amplitude of the SEDC buffer as a function of the input charge is shown in Fig. 20(b). The high degree of linearity within the valid DR for each gain setting is visible.

B. Results for CHARMS

The CHARMS ASIC, which is the successor of LArASIC, is currently being designed in a 65 nm process. Simulations of CHARMS at LArT indicate that this process allows for improvements due to the higher cutoff frequency (f_T) of transistors, and the possibility of using both thin and thick gate oxide transistors, depending on the need to maximize

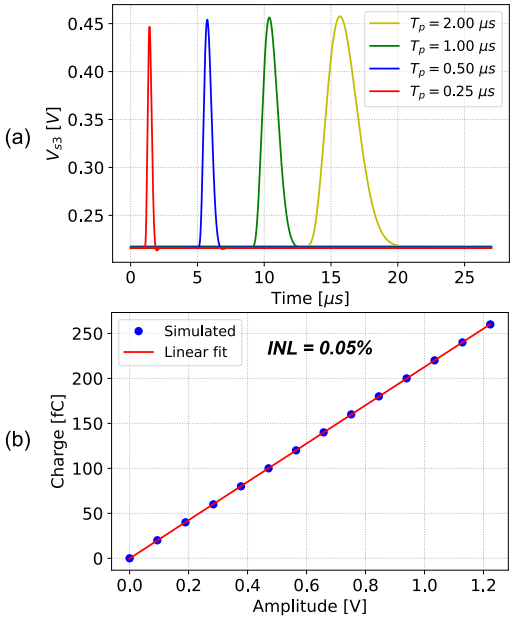

Fig. 21. (a) Simulated shaping filter output for CHARMS at LArT for different peaking times, T_p, and 50 fC of input charge. (b) Simulated V_{s3} output amplitude versus input charge for CHARMS for $T_p = 0.25\,\mu$s.

transconductance, minimize gate leakge current, or minimize output conductance.

The simulated response of CHARMS to a 50 fC input charge injection via a 1 ns wide pulse for different values of the peaking time, T_p, is shown in Fig. 21(a). For the shortest peaking time of 0.25 μs, the input charge vs. the amplitude of the shaping filter was plotted, and the resulting waveform is shown in Fig. 21(b). A linear fit was performed on the simulation data and the integral non-linearity (INL), given by

$$\text{INL} = \frac{\epsilon_{max} - \epsilon_{min}}{Q_{max} - Q_{min}} \times 100\%, \tag{6}$$

where ϵ_{max} and ϵ_{min} are the maximum and minimum deviations from the straight-line fit, and Q_{max} and Q_{min} are the maximum and minimum values of the input charge, was found to be only 0.05%. Thus, CHARMS can provide 2× shorter minimum peaking time than LArASIC while maintaining more than 10-bits of linearity for the same power consumption. Redesign of LArASIC in the 65 nm node therefore presents an opportunity to realize front-end ASICs for readout of charge signals with improved timing resolution.

IV. MEASUREMENT RESULTS

Fig. 22 shows the mask layout of LArASIC and a die micrograph from the latest production run. Experimentally, LArASIC achieved almost 100% yield. The test results are presented in this section, starting with the measurement setup shown in Fig. 23. Test pulse charge inputs with controllable amplitudes for each channel can be provided either through an on-chip DAC or an external signal source. An on-chip MiM capacitor, calibrated to a value of 186 fF with less than 1% channel-to-channel dispersion on the same chip at RT and LNT, is included in the test input path. On applying a voltage pulse either by the on-chip DAC or by an external source, the capacitor injects a known charge signal into the input of the

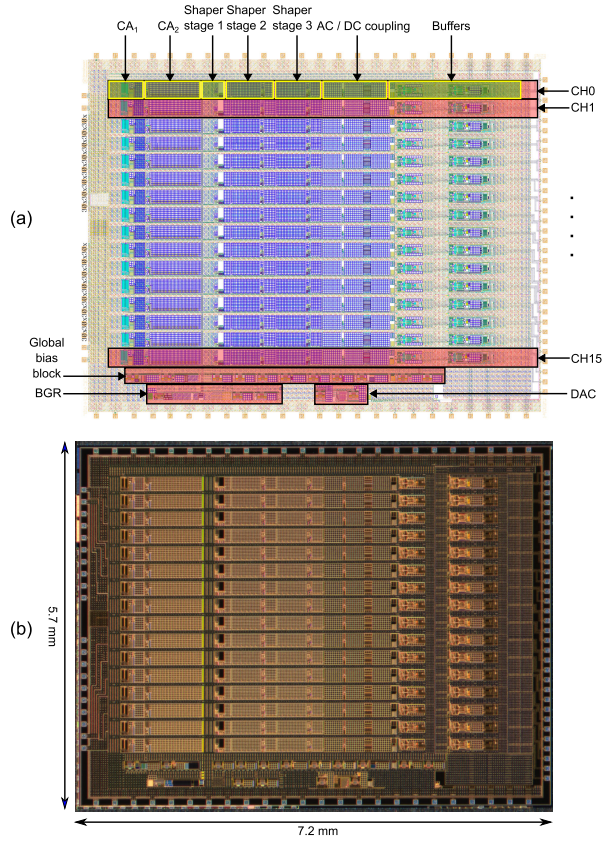

Fig. 22. (a) LArASIC mask layout, (b) LArASIC die micrograph.

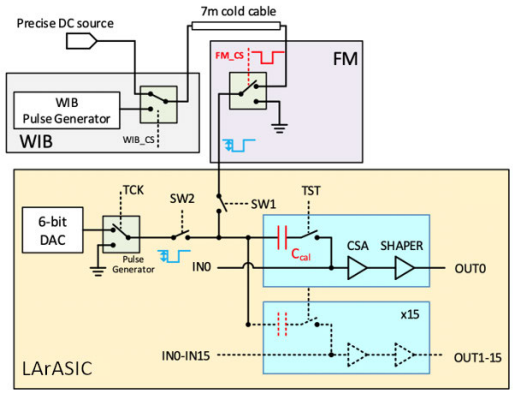

Fig. 23. Cryogenic measurement setup for LArASIC. Test pulses are triggered by a pulse generator within a warm interface board (WIB) at RT and transferred to a front-end module (FM) at LNT via 7 m of cable. The latter triggers the test pulse generator within LArASIC.

amplifier CA_1. An on-chip 6-bit current DAC provides test inputs that span a programmable full-scale charge range of 238 fC, 180 fC, 100 fC or 56 fC for channel gain settings of 4.7 mV/fC, 7.8 mV/fC, 14 mV/fC and 25 mV/fC, respectively.

Measurements of LArASIC's performance were carried out at LNT. Fig. 24 shows typical measured output waveforms for different gain, peaking time, and collection mode settings. The waveforms closely match the simulation waveforms presented in Section III. The peaking time calculated from the output waveforms as the time between 5% and 100% of the amplitude, shows very slight deviations between RT and LNT, as shown in Fig. 25. The variations in the output gain magnitudes at LNT compared to RT were found to be $< 2\%$.

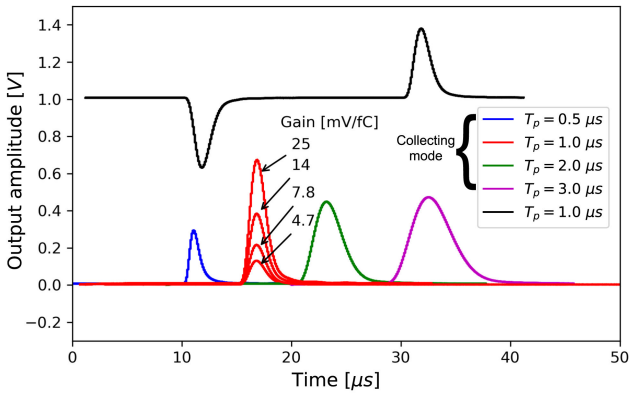

Fig. 24. Measured oscilloscope outputs of LArASIC at 77 K for different gain, peaking time, and collection mode settings.

TABLE IX
MEASURED POWER CONSUMPTION OF LARASIC

Temperature (K)	Baseline (mV)	Power consumption (mW)		
		Buffers off	SE on	SEDC on
300	200	5.6	9.0	10.7
77	200	5.3	8.8	10.8
300	900	5.8	9.5	10.6
77	900	5.5	9.1	10.5

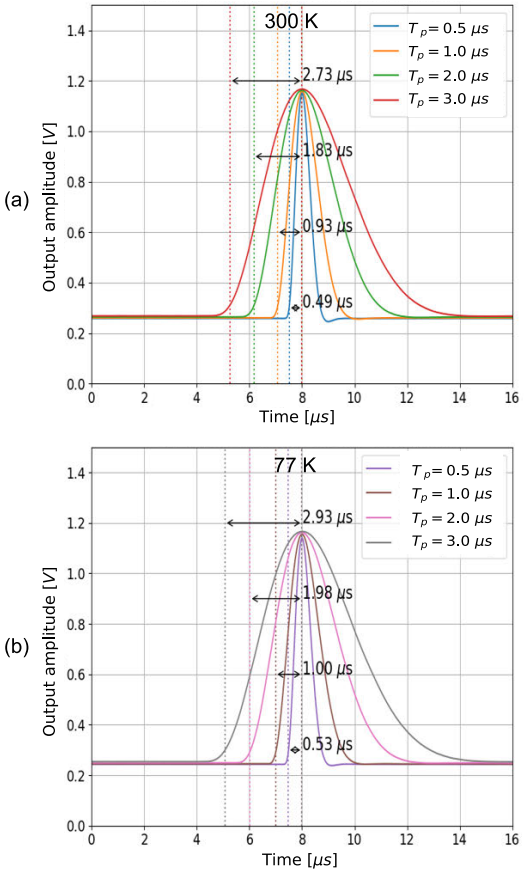

Fig. 25. Measured peaking times of LArASIC at (a) 300 K and, (b) 77 K.

Although the description and characterization of auxiliary circuits such as the bandgap reference are out of the scope

TABLE X
SPECIFICATIONS OF VARIOUS CRYOGENIC FRONT-END ASICs

	LArASIC (this work)	CHARMS (this work)	CRYO [15]	LArPix [13]
Process (nm)	180	65	130	180
Supply voltage (V)	1.8	1.8	2.5	1.8
# of channels	16	16	64	32
Gain (mV/fC)	4.7, 7.8, 14, 25	4.7, 7.8, 14, 25	9.6, 14.3, 28.6, 57.2	25
Input charge range (fC)	300, 180, 100, 56	300, 180, 100, 56	150, 100, 50, 25	50
Peaking time (µs)	0.5, 1.0, 2.0, 3.0	0.25, 0.5, 1.0, 2.0	0.6, 1.2, 2.4 3.2	N/A
Detector capacitance (pF)	150	150	40	5
ENC[1](e-)	534 (T_p = 1 µs)	-	≈250 (T_p = 1.2 µs)	275
Power per channel (mW)	6-11	6-11	19.8	0.3
Operating temperature (K)	89	89	165	89
Measured	Yes	No	Yes	Yes

[1] The ENC for LArASIC and LArPix corresponds to measurements at 77 K; the ENC for CRYO corresponds to measurements at 165 K; ENC for CHARMS in not included as measurement data is not yet available.

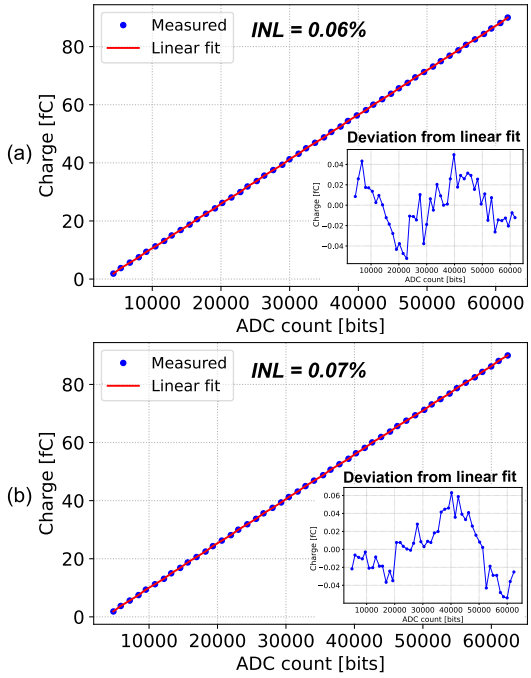

Fig. 26. Measured output linearity of LArASIC at 77 K for a gain of 14 mV/fC and peaking time, T_p equal to (a) 1.0 μs and, (b) 2.0 μs.

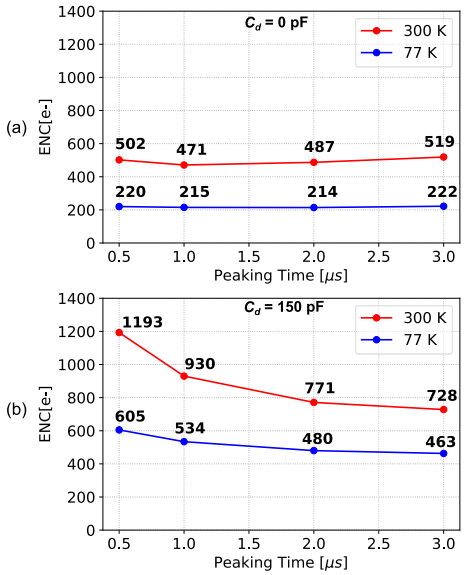

Fig. 27. Measured output noise of LArASIC referred to the input of the channel, expressed in ENC, as a function of peaking time for RT and LNT for detector capacitance, C_d equal to (a) 0 pF and, (b) 150 pF.

of this paper, it should be noted that the measured deviation of the baseline voltage for both baselines was ≈ ± 7 mV at LNT, indicating stable operation of the bandgap down to LNT. The measured output linearity at the point at which the pulse amplitude reaches its maximum for peaking times of 1.0 μs and 2.0 μs and channel gain setting of 14 mV/fC, with the output read out through the ColdADC chip, is shown in Fig. 26. A linear fit is performed on the measured data and the integrated non-linearity (INL) calculated using equation (6) is found to be less than 0.1%.

The output noise of the channel was measured at both RT and LNT in two cases: 1) with no capacitance connected at the input, and 2) with a capacitance equal to the expected detector capacitance of 150 pF at the input. The measured noise versus peaking time referred to the input of the channel and expressed as ENC, for a channel gain setting of 14 mV/fC and output baseline of 200 mV, is shown in Fig. 27. With no external capacitance connected to the input of the channel, ENC increases with T_p due to the higher contribution from parallel noise sources. However, with 150 pF detector capacitance, ENC decreases with T_p due to the reduced contribution from high-frequency series white noise sources [22]. The reduced noise at LNT compared to RT is due to lower thermal noise as well as higher transconductance at lower temperatures. Thus, the measurements demonstrate that LArASIC achieves an ENC of ≈ 500-600 electrons for a detector capacitance of 150 pF at LNT for peaking times ≥ 0.5 μs.

Inter-channel crosstalk measurements for the full readout chain were carried out when the output is read out through the ColdADC chip, driven by the SE and SEDC buffers in LArASIC. The results are shown in Fig. 28 for the case when the SEDC buffer is used. The mean crosstalk is approximately 0.04%, and the peak crosstalk is 0.35%, which is halved

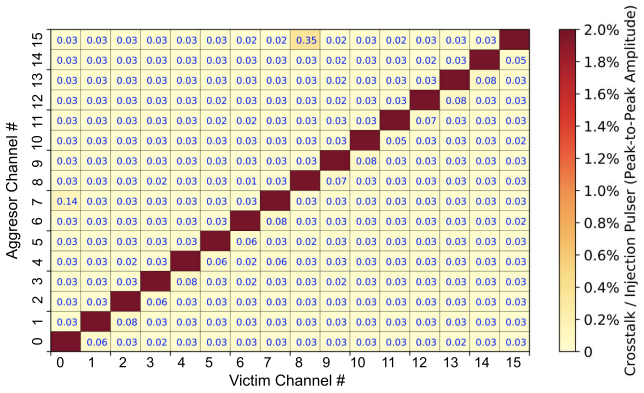

Fig. 28. Measured inter-channel crosstalk for the case when the SEDC buffer in LArASIC was used for driving the ADC.

compared to the case when the output is read out through the SE buffer. The measured per-channel power consumption for both the collecting and non-collecting modes is summarized in Table IX for different output driver configurations.

Table X compares the performance of LArASIC and CHARMS to other cryogenic front-end readout ASICs. Both CRYO [15] and LArPix [13] have more channels but were designed for smaller detector capacitance. The ENC values in Table X correspond to measurements with the expected detector capacitance connected to the input of each ASIC.

V. Conclusion and Future Work

This work has presented the design and measurement results for LArASIC, confirming the performance of this front-end ASIC designed for operation at RT and LArT and fabricated in the 180 nm CMOS process for charge readout in noble liquid TPCs. The design optimization was carried out through simulations using both standard foundry-supplied device models to ensure correct operation at RT, as well as extracted transistor model parameters at LArT to ensure correct operation inside LAr TPCs. The cryogenic-compatible integrated readout electronics enabled by LArASIC drive several high-energy physics experiments. MicroBooNE [3] and ProtoDUNE-SP [43] demonstrated the necessity of integrating cryogenic CMOS ASICs with TPC electrodes to minimize the input capacitance and achieve low noise readout. Now, the large-scale DUNE experiment, using kilotonnes of liquid argon, relies entirely on a three-ASIC readout chain for the front-end, digitization, and data transmission, all operating immersed in the noble liquid. The results of measurements for the latest production run of LArASIC indicate that the chip provides readout of charge signals with high linearity, low inter-channel crosstalk, and an ENC of approximately 500 electrons for a detector capacitance of 150 pF and peaking time of 1 μs at 77 K. The per-channel power consumption is approximately 10 mW when operated at LNT with the SEDC buffer driving board-level interconnects to the input of the ADC.

The work on developing readout ASICs suitable for cryogenic operation is continued in the 65 nm process node, targeted for upgrades of DUNE as well as other physics experiments that require high-resolution charge or light readout with shorter pulse peaking times. The first front-end ASIC planned to be fabricated in the 65 nm node is CHARMS, which will provide a shortest peaking time of 0.25 μs while consuming the same power per channel as LArASIC and also providing additional digital programmability via a standardized I^2C interface for features such as subtraction of the reset quiescent current to prevent baseline drift. The successors of CHARMS will be designed for even shorter peaking times, on the order of 20 ns, so as to provide high-resolution readout of charge signals for experiments such as PIONEER [44] and the future circular lepton collider (FCC-ee) [45].

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