Vertex Detector Electronics: ODE Pre-Prototype

User Manual

Issue: 2
Revision: 1

Reference: IPHE 2000-008, LHCb 2001-057 VELO
Created: 28 February 2000
Last modified: 4 May 2001

Prepared By: Yuri Ermoline

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
Abstract

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2 Revision: 1*
Date: *4 May 2001*

Abstract

This document is a user manual for the ODE pre-prototype module (ODEPP, also frequently referred as Read-out Board number 2, RB2). The module is under development and new features are implemented in every new version.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Vertex Detector Electronics: ODE Pre-Prototype			
2. Document Reference Number: IPHE 2000-008, LHCb 2001-057 VELO			
3. Issue	**4. Revision**	**5. Date**	**6. Implemented features**
1	0	2 Mar 2000	VME slave interface A24/D32, CSR0, CSR1, FIFO, VME trigger, PDU control, FADC data capture mode
1	1	22 Mar 2000	VME reset, TTC trigger, added 24-bit trigger counter
1	2	31 Mar 2000	Changed CSR1 format, added 12-bit FIFO counter, trigger counter reduced to 12 bits
1	3	6 Jun 2000	Added IPHE reference number CSR1(3..1)="001" (module status) Added Appendix A (Useful TTCvi commands) Added Appendix B (FADC card dimensions)
2	0	10 Aug 2000	VME reset VRST(0) and VME TTCrx reset VRST(1) Version & Revision, pseudo digital bit limits (CSR0) TTCrx status CSR1(1), FADC card connector update, FADC data processing (event header finder)
2	1	2 May 2001	VME TTCrx reset modified, new MODE="10" implemented (readout without trigger), OSI card description added

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
Table of Contents

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* **Revision: 1**
Date: *4 May 2001*

Table of Contents

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
Glossary

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* **Revision:** *1*
Date: *4 May 2001*

Glossary

FADC	Flash Analog to Digital Converter
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
ODE	Off-Detector Electronics
TTC	Timing, Trigger and Control

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
1 General description

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

1 General description

Vertex detector ODE pre-prototype (ODEPP, also frequently referred as Read-out Board number 2, RB2) module is designed for the read-out of up to 4 analog multiplexed signals from the vertex detector front-end chip(s) at 40 MHz. ODEPP is a 6U VME module, 2-unit wide. It consists of a main VME board and 3 daughter cards as shown on the Figure 1.
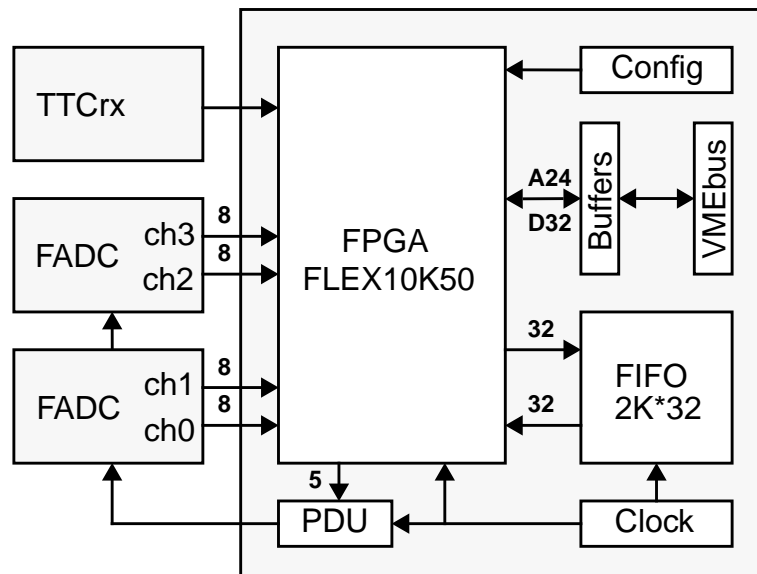

Figure 1

The main VME board provides (see also Figure 2):

- Altera FLEX PFGA EPF10K50RC240-3 (2880 logic elements and 10 embedded array blocks of RAM, 2K bit each [1]), connector for FPGA configuration via down-load cable and socket for the configuration EPROM (EPC1PC8).

- Data buffers, address comparators and Base address rotary switches for the VMEbus slave interface (A24/D32) which is used as a control and monitoring interface to the module.

- 2K*32 bit of FIFO (4 SyncFIFO chips Cypress CY7C4231, 15 ns access time [2]).

- 40 MHz internal clock oscillator, programmable delay unit for FADC clock phase adjustment (PDU15F-1 from Data Delay Devices [3]), LEMO connector for the BUSY output signal (TTL open collector, active low), the Reset button and the green LED.

- Connectors to a TTCrx board carrying a TTCrx chip [4] - the receiver chip of the Timing, Trigger and Control (TTC) system, CERN microelectronics group design.

- 2 connectors for FADC cards (2-channels, 8-bit, 40 MHz, based on AD9059 from Analog Devices [5]) and voltage regulators for FADC cards analog power.

One of the FADC cards can be replaced by the ECS interface prototype or the trigger pre-processor interface prototype.
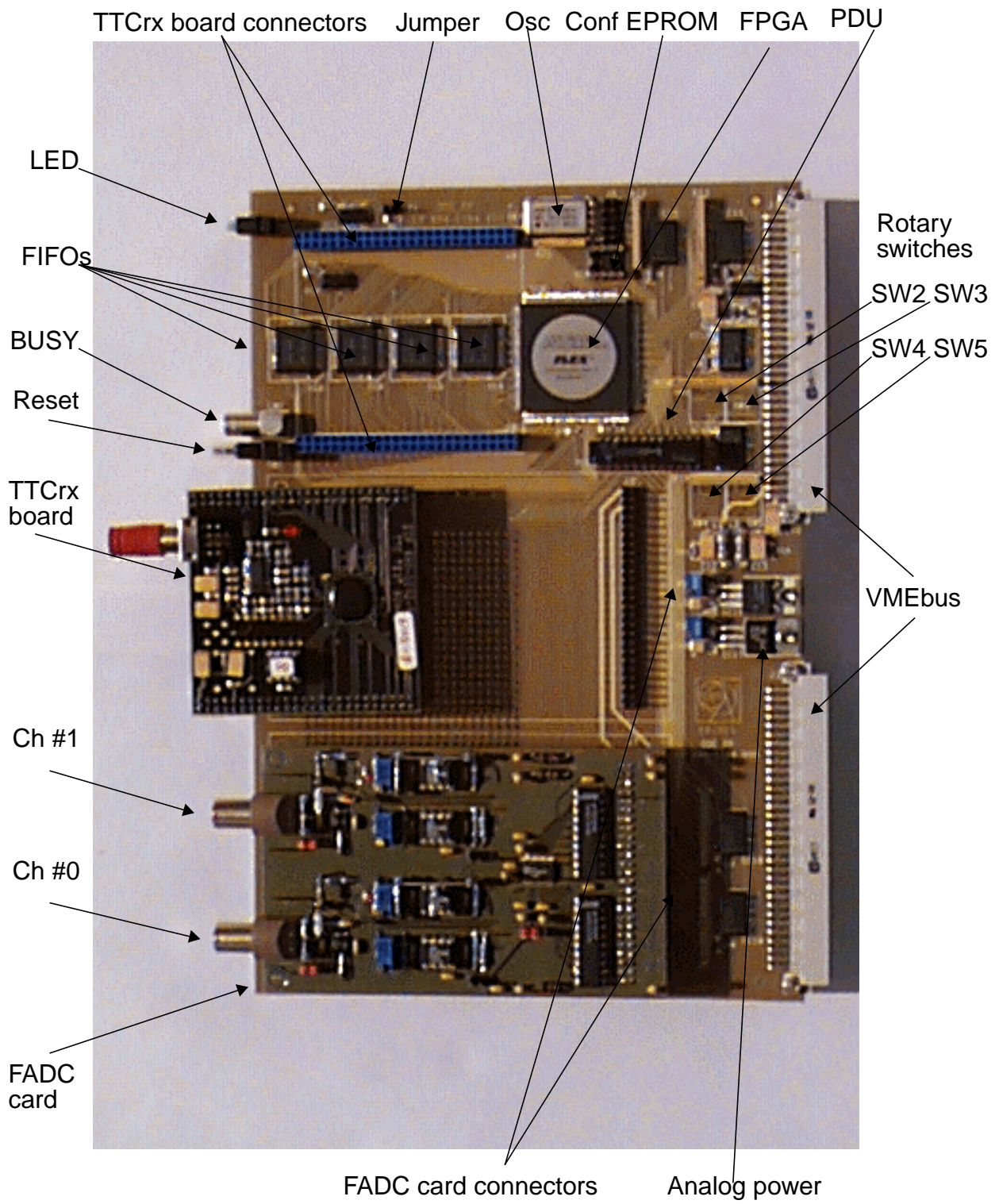
Vertex Detector Electronics: ODE Pre-Prototype
User Manual
1 General description

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2 Revision: 1*
Date: *4 May 2001*

Figure 2

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
1 General description

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

1.1 Module clock

The ODEPP main board can be driven by internal clock from the 40 MHz clock oscillator or by the clock, delivered by the TTCrx chip (40 MHz). The clock source can be chosen by the jumper on the ODEPP main board (see Figure 2):

- Jumper inserted - internal 40 MHz clock.

- Jumper removed - external TTCrx 40 MHz clock.

Clock for the FADC card connectors are provided by the programmable delay unit (see 1.6).

1.2 Module resets

The ODEPP main board are reset on power-on and can be reset by:

- Pressing push-button "Reset" on the front panel or writing '1' into VMERESET register VRST(0) from the VMEbus (see 1.4) sets to zero the module registers, counters and FIFO read/write pointers.

- Writing '1' and then '0' into VMERESET register VRST(1) from the VMEbus (see 1.4) generates reset signal for the TTCrx receiver chip (see 1.5).

1.3 Module triggering

PDE-PP module can be triggered:

- from the VMEbus by writing '1' into CSR1(0).

- from the TTCrx chip (using TTC system) or OSI card, using external trigger (see 1.5).

The triggers are counted by the 12-bit TRIGGER Counter, which can be read from CSR1(15..4).

1.4 VME slave interface

The module uses the P1 and P2 VME connectors and works in A24/D32 mode. Block Transfer mode is not implemented. The recognized Address Modifier codes are 3E, 3D, 3A, 39 (standard access).

The modules's 16-bit Base Address (VME address bits A24..A08) can be selected by 4 internal rotary switches (see Figure 2) in the range (0000-FFFF) hex:

- SW2: VME address bits A23..A20

- SW3:VME address bits A19..A16

- SW4:VME address bits A15..A12

- SW5:VME address bits A11..A08

Vertex Detector Electronics: ODE Pre-Prototype
Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
User Manual
Issue: *2* **Revision:** *1*
1 General description
Date: *4 May 2001*

The address map of the ODEPP module is shown below:

VME address bits A07..A00	Register
"00" hex	CSR0
"04" hex	CSR1
"08" hex	VRST
"10" hex	FIFO

Control/Status Register 0 (CSR0) - $00

Data Bit(s)	Write	Read	Comments
D4..D0	PDU control	PDU status	FADC clock phase adjustment
D7..D5	No action	"000"	
D9..D8	MODE control	MODE status	Operation modes
D11..D10	No action	"00"	
D13..D12	No action	REVISION	Design revision
D15..D14	No action	VERSION	Design version
D23..D16	PDBLL control	PDBLL status	Pseudo-Digital Bit Low Limit
D31..D24	PDBHL control	PDBHLstatus	Pseudo-Digital Bit High Limit

CSR0 provides storage for the static parameters - programmable delay line control value for the FADC clock phase adjustment (see 1.6), the module operation mode (see 2) and the FADC data processing parameters (see 2.1).

Control/Status Register 1 (CSR1) - $04

Data Bit(s)	Write	Read	Comments
D0	VMETRIG	MODBUSY	Start data acquisition from VMEbus
D1	No action	TTCREADY	TTCrx receiver chip ready
D3..D2	No action	"00"	
D15..D4	No action	TRIGCNTR	12-bit TRIGGER up counter
D16	No action	FIFO Full	if '1' - FIFO is full
D17	No action	FIFO Empty	if '1' - FIFO is empty
D19..D18	No action	"00"	
D31..D20	No action	FIFOCNTR	12-bit FIFO up counter

CSR1 is used to start data acquisition (see 2) and to read the status of the module, status of the TTCrx receiver chip, FIFO status and content of TRIGGER and FIFO counters (see 2).

VMERESET Register (VRST) - $08

Data Bit(s)	Write	Read	Comments
D0	VMERESET	'0'	Reset from VMEbus
D1	TTCRESET	TTCRESET	Writing '1' and then '0' resets TTCrx
D31..D2	No action	"00..00"	

Writing to this register generates ODEPP module resets (see 1.2).

FIFO (VME read/write access) - $10

FIFO can be accessed from VMEbus for test purposes.

Data Bit(s)	Write	Read	Comments
D31..D0	VME data	FIFO data	FIFO test

FIFO (FADC data capture / VME data read)

After data acquisition FADC data can be read from the FIFO via VMEbus.

Data Bit(s)	Write	Read	Comments
D7..D0	FADC ch 0	FIFO data	FADC data after data acquisition
D15..D8	FADC ch 1	FIFO data	-"-
D23..D16	FADC ch 2	FIFO data	-"-
D31..D24	FADC ch 3	FIFO data	-"-

1.5 TTCrx board and OSI card

The TTCrx board contains the TTCrx chip (non radhard ES2 version [4]), the optical connector with an integrated detector/preamplifier and some other components. The input optical signal from the TTC transmitter crate carries 40 MHz clock and trigger (TTCTRIG) signals. TTCrx receiver chip can be reset by writing '1' and then '0' into VMERESET register VRST(1) from the VMEbus. The TTCrx status (TTCREADY) can be read from CSR1(1).

In order to operate the TTCrx board the TTC transmitter (TTCvx [6]) and the TTC control module (TTCvi [7]) are necessary, as shown on the Figure 3. The 40.00 MHz clock signal (ECL levels) and the Trigger signal (NIM or ECL levels) are provided by the external logic (e.g. SEQSI module).

The OSI (ODE to SEQSI Interface) card is a simple electrical replacement of the TTCrx board. Card has two LEMO00C connectors for Clock and Trigger input NIM signals and can be driven directly by the external logic (e.g. SEQSI module) without need for the TTCvi and TTCvx modules. OSI card provides clock and trigger signals to the ODEPP main board and doesn't need a reset.
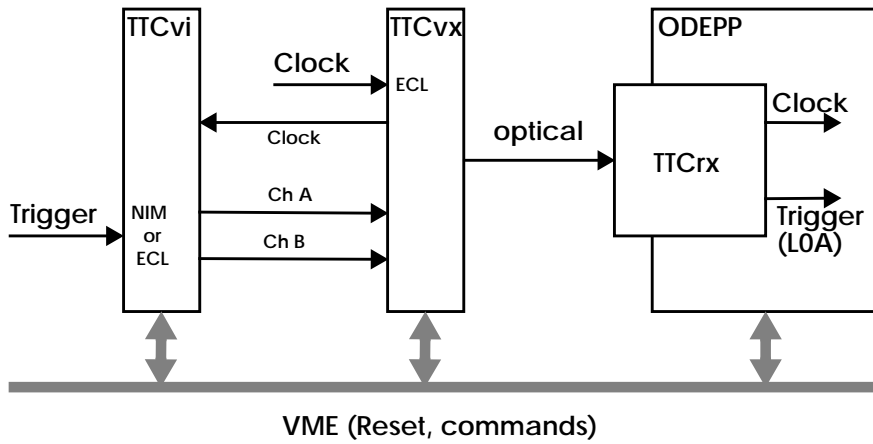
Vertex Detector Electronics: ODE Pre-Prototype
User Manual
1 General description

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

Figure 3

1.6 FADC clock phase adjustment

The clock phase for both FADC cards can be adjusted using programmable delay unit (PDU15F-1, 5-bit digitally programmable delay line) on the ODEPP main board. The delay from the input clock to the PDU (clock on the ODEPP main board) to the output clock to the FADC cards depends on the PDU control code - CSR0(4-0):

$$\text{Delay} = \text{Inherent Delay} + \text{Increment Delay} * \text{Control Code}$$

where Inherent Delay = 9 ns, Increment Delay = 1 ns. The codes for different delay values are given in the table below:

Delay(ns)	Code	Delay(ns)	Code	Delay(ns)	Code
0	10	9	00	18	09
1	11	10	01	19	0A
2	12	11	02	20	0B
3	13	12	03	21	0C
4	14	13	04	22	0D
5	15	14	05	23	0E
6	16	15	06	24	0F
7	17	16	07	25	10
8	18	17	08		

The PDU control code is set to zero after power on and reset.

1.7 FADC card

The 2 channels FADC card (drawing in Appendix B) contain input link receivers, amplifiers, analog-to-digital converter AD9059 (dual 8-bit, 60 MSPS A/D converter) and output buffers.

The input signals from the LEMO connectors (EPG.0B.302.HLN) are differential in the range from 0 to 1 Volts. The upper LEMO connector on the upper FADC card corresponds to FADC channel #3 and the lower LEMO connector on the lower FADC card - to FADC channel #0.

The 50-pin DIN 41651 connector provides the digital and analog power, PDU clock and data enable signals for the FADC card from the ODEPP main board and the 2*8-bit output data from the FADC card output buffers to the ODEPP main board. The connector layout is shown below:

Signal	Pin #	Pin #	Signal
-5V_ANALOG	1	2	-5V_ANALOG
CND_ANALOG	3	4	GND_ANALOG
+5V_ANALOG	5	6	+5V_ANALOG
PDU_CLOCK	7	8	-
ENABLE_B	9	10	FADC_B(7)
FADC_B(6)	11	12	FADC_B(5)
FADC_B(4)	13	14	FADC_B(3)
FADC_B(2)	15	16	FADC_B(1)
FADC1_B0)	17	18	-
SDA(I2C_1)*	19	20	SCL(I2C_1)*
SDA(I2S_2)*	21	22	SCL(I2C_2)*
-	23	24	-
-	25	26	-
POWER_DOWN	27	28	TDI*
TCKO*	29	30	TMS*
TDO*	31	32	TRST*
ENABLE_A	33	34	FADC_A(0)
FADC_A(1)	35	36	FADC_A(2)
FADC_A(3)	37	38	FADC_A(4)
FADC_A(5)	39	40	FADC_A(6)
FADC0_A7)	41	42	-
-	43	44	-
GND_DIGITAL	45	46	GND_DIGITAL
-	47	48	-
+5V_DIGITAL	49	50	+5V_DIGITAL

(*) - reserved for the ECS interface prototype card.

2 Module operation

Module FIFO can be tested by writing and reading from VME. Number of written words are counted by the FIFO up counter, during read from the FIFO, the counter remains unchanged.

Before starting data acquisition cycle, the module has to be reset and the following parameters have to be set:

- PDU control code - CSR0(4..0) - defines the FADC card connector clock delay relatively to the main board clock.

- ODEPP operation mode - CSR0(9..8). The following modes are valid:

  - MODE = "00" - continuous data capture, starting on trigger,

  - MODE = "01" - event data capture, starting on trigger and event header

  - MODE = "10" - event data capture, starting on event header

The module can be triggered from VME or external logic (see 1.3) while in modes "00" or "01". The triggers are counted by the 12-bit TRIGGER Counter, which can be read from CSR1(15..4). The trigger signal also resets the 12-bit FIFO counter.

During the data acquisition, namely during the data writing into the FIFO:

- The VME write to CSR0, CSR1 and FIFO and VME read from FIFO is disabled (however module responds to these VME cycles). VME read from CSR0 and CSR1 is allowed.

  - CSR0: write - disabled, read - allowed.

  - CSR1: write - disabled, read - allowed.

  - FIFO: write - disabled, read - disabled.

  - VRST: write - allowed.

- MODBUSY is asserted and can be checked by reading CSR1(0).

- BUSY output signal (TTL open collector, active low) on the front panel LEMO connector is asserted.

- 12-bit FIFO counter counts a number of data words, written into FIFO and can be read via CSR1(31..20).

The status of the ODEPP module (MODBUSY) and the FIFO (FIFO full, FIFO empty and FIFO counter) can be checked via CSR1 during and after data acquisition. The FADC data can be read from the FIFO via the VMEbus interface after data acquisition.

2.1 MODE = "00" - continuous data capture, starting on trigger

During this mode, after receiving the trigger, the output data from the FADC cards are written into the FIFO every clock cycle until the FIFO is full (after 2K clock cycles or 51.2 µs). The FIFO counter is reset by the trigger and then is incremented by every write into the FIFO.

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
2 Module operation

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

2.2 MODE = "01" - event data capture, starting on trigger and event header

During this mode, after receiving the trigger, the synchronization logic in the module starts to search for the event data header - pseudo digital "0101" in the analog signal package from the SCTA128 chip [8].

The upper limit for the pseudo digital bit low level (PDBLL) and the lower limit for the pseudo digital bit high level (PDBLL) are stored in the CSR0 (see 1.4). They are used by the synchronization logic to define the windows for the digitized SCTA128 data during the header search.

Upon detecting the header, the 12-bit TRIGGER Counter value is written into the FIFO followed by the SCTA128 event data (144 8-bit words, see 1.4, FIFO data format). Up to 14 events can be stored in the FIFO until the FIFO is full (last event may not be completely written into the FIFO if there is no enough space left).

The FIFO counter is incremented by every write into the FIFO. It is reset by every new trigger and therefore contains the number of word written into the FIFO for the last event.

2.3 MODE = "10" - event data capture, starting on event header

Module operation in this mode is similar to the previous one with the exception that the synchronization logic in the module starts to search for the event data header without waiting for the trigger.

The FIFO counter is incremented by every write into the FIFO and contains the total number of word written into the FIFO for all events.

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
3 References

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

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Vertex Detector Electronics: ODE Pre-Prototype
User Manual
Appendix A. Useful TTCvi commands (from [7])

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2* Revision: *1*
Date: *4 May 2001*

Appendix A. Useful TTCvi commands (from [7])

The TTCvi module is A24, A16 / D32, D16 and responds to the following Address Modifiers: 39, 3A, 3D, 3E (standard), 29, 2D (short), 0F, 0B, 3B, 3F (block), 09, 0A, 0D, 0E (extended).

Four rotary switches are used to set the base address (A23 to A8).

The TTCvi module is normally driven by a clock from the TTC transmitter (e.g. TTCvx).

TTCvi provides four trigger inputs on the front panel (0 - ECL, 1,2,3 - NIM), trigger by a VMEbus command and internal random trigger generator. The trigger source is selected by setting CSR1(2..0). The selected trigger is made available as two front panel NIM outputs. An internal 24-bit trigger counter (which can be read and written through VMEbus) counts the number of triggers sent.

$84 - VMEbus module reset generation (Write, A24/D16)

Write access to this address generates module reset.

$80 - CSR1 - Input selection and timing (Read/Write, A24/D16) - trigger selection

CSR(2..0) = 0 (ECL front panel), 1, 2, 3 (NIM front panel), 4 (VMEbus command), 5 (random).

$86 - VMEbus trigger generation (Write, A24/D16)

Write access to this address generates trigger if CSR(2..0) = 4.

$88 / $8A - Trigger counter (Read/Write, A24/D16)

$88(7..0) = Trigger Counter (23..16), $8A(15..0) = Trigger Counter (15..0)

Vertex Detector Electronics: ODE Pre-Prototype
User Manual
Appendix B. FADC card dimensions

Ref: *IPHE 2000-008, LHCb 2001-057 VELO*
Issue: *2 Revision: 1*
Date: *4 May 2001*

Appendix B. FADC card dimensions