Published by IOP Publishing for Sissa Medialab

Received: *October 30, 2024*
Revised: *December 17, 2024*
Accepted: *January 10, 2025*
Published: *February 5, 2025*

Topical Workshop on Electronics for Particle Physics
University of Glasgow, Scotland, U.K.
30 September–4 October 2024

Rad-hard readout system for Timepix3 Hybrid Pixel Detectors

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Abstract: The Beam Gas Ionisation (BGI) profile monitor, located in the Proton Synchrotron (PS) and Super Proton Synchrotron (SPS) at CERN, requires a radiation-tolerant readout system to transfer data from the challenging accelerator surroundings to the back-end for processing. The system needs to control and acquire data from four Timepix3 Hybrid Pixel Detectors (HPDs) located directly inside the beam pipe, a highly radioactive environment. It must ensure reliability given limited hardware access and preserve signal integrity for the high-speed data (32 channels at 320 MHz). However, due to the unavailability of a suitable rad-hard Timepix3 readout, the Beam Instrumentation PiXeL (BIPXL) readout system was designed to meet these requirements. This system employs radiation-hardened components such as the GBTx and the FEASTMP, both developed at CERN. It will be compatible with forthcoming hybrid pixel detector initiatives in similarly harsh radiation conditions.

Keywords: Beam-line instrumentation (beam position and profile monitors, beam-intensity monitors, bunch length monitors); Data acquisition circuits; Front-end electronics for detector readout; Radiation damage to electronic components

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https://doi.org/10.1088/1748-0221/20/02/C02009

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1 Introduction

The Beam Instrumentation PiXeL (BIPXL) readout system allows the data acquisition and slow control of Timepix3 hybrid pixel detectors in high radiation environments. Currently, it is employed in the Beam Gas Ionisation (BGI) profile monitors at CERN. The BGI provides non-invasive, continuous measurement of the beam profile during the acceleration. Two of these instruments were installed in 2021 in the PS, followed by the installation of one SPS-BGI in January 2024.

These monitors are integrated into the accelerator, with four Timepix3 detectors inside the beam pipe, each generating events used for reconstructing the beam profile. Due to the high radiation levels near the beam pipe, the data processing system must be placed outside the tunnel, as the chosen standard off-the-shelf equipment cannot withstand such conditions. This requires the transmission of the 32 Timepix3 channels at 320 Mbit/s (10.24 Gbit/s in total). However, these signals cannot be transmitted over long distances via electrical cables because they would suffer degradation from noise and attenuation. To overcome this, the signals are converted to optical form before transmission. To manage radiation exposure effectively, the readout electronics are divided into "front-end" and "back-end" systems. The front-end system, situated within the radiation zone (about one meter beneath the beam pipe), prepares the signals for optical transmission using radiation-hardened components. Conversely, the back-end system, located outside the radiation area (typically on the surface, hundreds of meters from the tunnel), processes the received optical signals using standard, non-radiation-hardened components. The design and development of a reliable front-end capable of operating within the accelerator complex has been a key priority for this project. For this purpose, components developed at CERN, such as the GBTx (Gigabit Transceiver) [1, 2], VTRx (Versatile Link Transceiver) [3], and FEASTMP DC/DC modules [4], have been selected.

Further details about this design will be presented in this paper, along with future modifications to the BIPXL readout to ensure compatibility with new projects, such as the HL-LHC BGI based on Timepix4.

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1.1 Beam Gas Ionisation profile monitor overview

Leveraging the ionisation of residual gas in the pipe caused by the passing beam, the BGI provides non-destructive measurements of the transverse beam profile [5]. As seen in figure 1, electrons and ions in the center of the instrument are accelerated towards the detector by an electric field. A magnetic field then confines the electrons in a helical motion towards the detector, reducing the transverse spatial drift caused by the electric charges. When the electron hits the detector, the position and time are recorded, and an event is created for later processing by the readout to reconstruct the beam.

The BGI is a unique Ionisation Profile Monitor (IPM) because it uses Hybrid Pixel Detectors, specifically the Timepix3 detector. It consists of a matrix of 256×256 pixels with a pitch of 55 µm, a time resolution of 1.56 ns and 8 output data channels, each with a maximum data rate of 640 Mbit/s. The four Timepix3 detectors used per instrument are mounted on a ceramic chip carrier board, which connects the power and data signals to flexible cables.

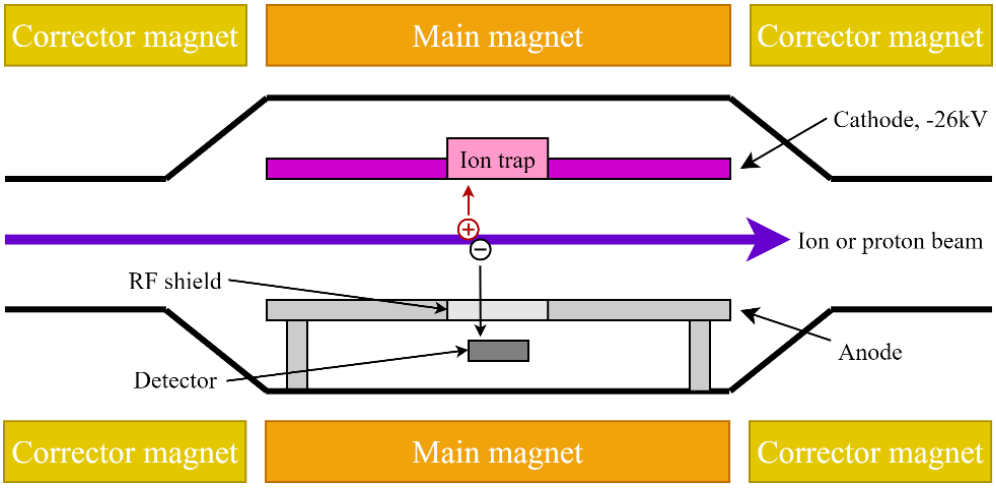

Figure 1. BGI cross section diagram.

1.2 BIPXL readout overview

The BIPXL readout system is responsible for controlling the four detectors and handling the acquisition and processing of the data. The system consists of three main components [6]: the detectors, the front-end, and the back-end, as illustrated in figure 2. The front-end is located approximately one meter below the beam pipe and connects to the detectors using Cat6A cables with RJ45 terminations. The electrical signals are then converted to optical form and transmitted to the back-end via single-mode (SM) optical fibre cables, ensuring signal integrity.

The back-end in based on a ZCU102 Xilinx MPSoC development board (Zynq Ultrascale+, XCZU9EG) and is tasked with generating control signals for the detectors, reading the detectors' configurations, checking synchronisation, creating the timing and Timepix3 events and generating the beam profiles. For this, the two main blocks of the MPSoC are used: the Programmable Logic (PL) for the more time-critical and data-intensive tasks, such as bit manipulation and trigger handling; and the Processing System (PS), which runs the Petalinux operating system and applications for processing incoming data. The generated profiles are then sent to the Front-End Computer (FEC) for publication in the CERNs controls infrastructure. From here, the operators in the control room have access to the beam profile information.

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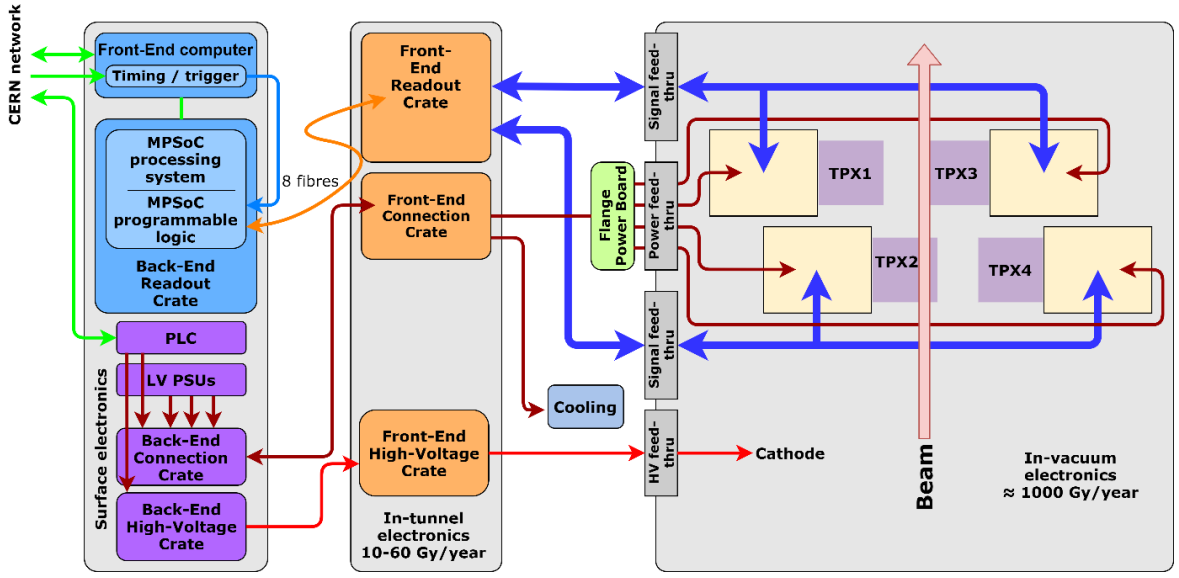

Figure 2. BIPXL readout overview.

2 BIPXL front-end

2.1 Front-end constraints

The front-end electronics must meet several specific requirements. First, the design must ensure operation for over 10 years in a radiation environment due to its proximity to the beam pipe. Measurements taken in 2023 at the two PS-BGI locations (Horizontal and Vertical) indicate that the radiation dose at the front-end board can reach up to 53 Gy/year (table 1). Additionally, the HEH-eq fluence in the PS environment can reach 7.54×10^{11} cm^{-2}, as noted in reference [7].

Second, the design must emphasize reliability and incorporate diagnostics, as system access is limited to technical stops due to its location in the accelerator tunnel.

Finally, preserving the integrity of high-speed signals is essential to maintaining optimal system performance.

Table 1. 4 RPL Dosimeters (CR-136545) measured on March 2023 after a year in the PS-BGI locations.

Device	Dose (Gy)
PS-BGIH flange electronics	696
PS-BGIH front-end electronics	10,5
PS-BGIV flange electronics	427
PS-BGIV front-end electronics	53

2.2 First front-end prototypes

At the start of the PS-BGI project in 2016, no radiation-tolerant electronics board met the data rate requirements for the four Timepix3 detectors. Due to time constraints, an initial compromise was made by using a board called the GEFE (GBT-based Expandable Front-End), developed at CERN [8]. The main limitation of this board was that it only had one GBTx transceiver chip, which restricted the total

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data rate to 3.2 Gbit/s (10 e-links at 320 Mbit/s) [1, 2]. The GEFE had a flash-based FPGA (ProASIC3E) that had been qualified for a total ionisation dose of up to 750 Gy. Despite its data rate limitations, the GEFE board facilitated early tests of the Timepix3 detectors in the first PS-BGI prototype.

To achieve the maximum data rate of 20.48 Gbit/s (from the eight outputs of the four Timepix3 detectors at their maximum speed of 640 Mbit/s), a custom front-end board was developed in early 2018. This new board incorporated additional GBTx chips and utilised a similar FPGA to the one used in GEFE (to reuse the HDL design) for detector control. Additionally, it included a Kintex-7 SRAM-based FPGA for synchronising and packaging the serial data from the detectors. However, due to time and financial constraints, these FPGAs were not explicitly qualified for this application and radiation levels. After a couple of years of installation, this oversight resulted in the FPGAs malfunctioning and failing to recover even after reprogramming.

The solution was to remove the two FPGAs and to reduce the maximum speed of the Timepix3 detectors from 640 Mbit/s per output to 320 Mbit/s, which was sufficient for the project's requirements. It was then possible to connect the Timepix3 signals directly to the GBTx e-links. Consequently, the MPSoC gateware had to be modified to incorporate the logic previously handled by the ProASIC3 and Kintex-7 components. This decision, along with the chosen components, resulted in a design better suited to operate reliably in the intense radiation environment near the beam pipe.

2.3 Current front-end design

A 2U crate has been designed to hold all the components that are part of the BIPXL front-end. The current design consists of two boards connected via an FMC HPC connector. The first board, known as the Front-end baseboard, features 24 RJ45 connectors that facilitate connections with the four Timepix3 detectors and four SMA connectors as ADC inputs. Power is supplied using two FEASTMP DC/DC modules, which are radiation-hardened point-of-load (POL) converters developed at CERN [4].

The second board is the Quad GBTx Mezzanine with four GBTx chips for data serialization/deserialization, one of them designated as the main chip. A GBT-SCA (Slow Control Adapter) chip [9] is then used for digitising and tuning the analog bias current within the Timepix. Each GBTx is connected to a VTRx pluggable transceiver for the optical transmission. The GBTx are configured to each feature 8 uplinks at 320 Mbit/s. Then, the main GBTx handles the 24 downlinks at 80 Mbit/s.

The described design meets the requirements outlined in subsection 2.1. To ensure reliability in a radiation-intense environment, the front-end design avoids components that are not radiation-hardened; for instance, no local oscillator is used. All components selected are designed for use in LHC experiments, withstanding HEH-equivalent fluences up to $10^{16}\,\mathrm{cm}^{-2}$ [10, page 11]. As shown in table 2, these components are capable of tolerating radiation levels significantly higher than those measured at the front-end location (table 1).

The integrity of the high-speed signals is maintained by careful impedance control and precise length matching within each of the differential pairs. The GBTx eLink receivers include adjustable phase aligners, which eliminate the need for precise length matching between the TPX3 data output signals. However, achieving close length matching can still enhance overall performance. With respect to the control signals, the Shutter signal and the T0_Sync signal should have uniform lengths across all Timepix3 devices to ensure consistent operation. Specifically, the T0_Sync signal is responsible for clearing the Time of Arrival (ToA) counters within the Timepix3 devices. To ensure synchronised time stamping across the four Timepix3 devices, it is crucial that these signals maintain the same length.

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Table 2. Maximum ionizing radiation tolerances measured in the selected components.

Component	Maximum ionizing radiation tolerances
GBTx	Up to 100 Mrad (1 MGy)
VTRx (SM)	Up to 50 Mrad (0.5 MGy)
FEASTMP	150–200 Mrad (1.5–2 MGy)
GBT-SCA	Up to 100 Mrad (1 MGy)

3 Results

The updated front-end design required modifications to the back-end MPSoC gateware, where the GBTx FPGA IP core handles decoding optical signals and preparing them for profile generation. These updated hardware and gateware versions were installed and deployed in the PS and SPS systems in January 2024. Throughout the operational year, the team has not observed any adverse effects on the front-end caused by radiation. This is attributed to the selected components having radiation-tolerance limits that exceed the levels encountered.

An example of the result of the profile reconstruction can be seen in figure 3. This shows 11 profiles captured on the LHC beam by the horizontal BGI installed in SPS. These profiles were obtained using 1 ms integration windows, with each window spaced 1 second apart. They represent the distribution of events (counts) per column, which indicates how the particle beam profile evolves over time.

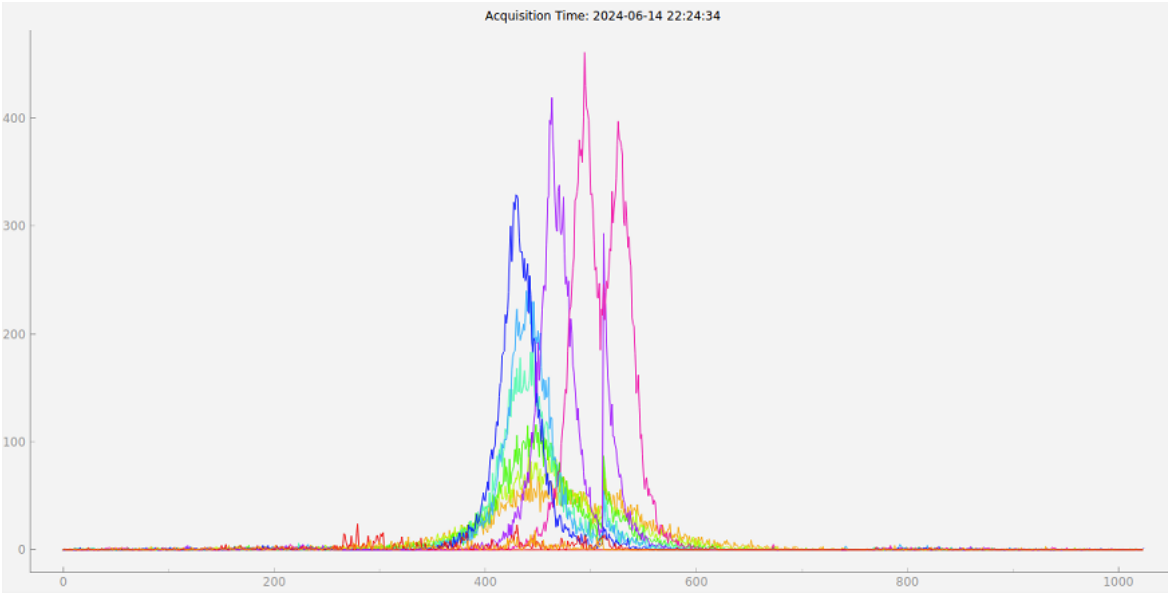

Figure 3. LHC beam profile reconstruction (SPS-BGIH).

4 Future projects and conclusions

The modularity and readout characteristics of the BIPXL make it suitable for future applications based on Timepix detectors for beam instrumentation, such us the BGI profile monitor for HL-LHC [6], the North Area telescope for bent crystals characterization and the beam loss monitors (BLM) for rapid

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deployment in the LHC. These designs may require an upgrade to support Timepix4, in particular to handle its 16 output data signals at 10.24 Gbit/s. Handling this data rate will involve the use of high-speed PCB materials, as well as the update of the rad-hard components version: the low power version of the GBT, the lpGBT and the VTRx+ (SM) transceiver to convert the Timepix4 data output electrical signals to opticalfibres (5.12–10.24 Gbit/s of uplink and 2.56 Gbit/s of downlink) [11]. The DC/DC converters would also be upgraded to the bPOL12V version [12].

To simplify the readout design, the front-end board may be directly connected to the instrument vacuum electrical feedthrough,utilising a new design that is being developed for the HL-LHC BGI based on the 4DPhoton project [13]. This would eliminate the need for RJ45 cables between the BGI and the front-end.

Acknowledgments

The development of the BGI and the BIPXL readout system is the result of the combined effort of a large team. We would like to acknowledge the contributions of W. Andreazza, J. Braach, W. Devauchelle, C. Fleisig, G. Khatri, S. Levasseur, C. Pasquino and M. Teresa Ramos.

References

[1] P. Leitao et al., *Test bench development for the radiation Hard GBTX ASIC*, 2015 *JINST* **10** C01038.

[2] P. Moreira, A. Marchioro and K. Kloukinas, *The GBT: A proposed architecture for multi-Gb/s data transmission in high energy physics*, in the proceedings of the *Topical Workshop on Electronics for Particle Physics (TWEPP-07)*, Prague, Czech Republic, 3–7 September 2007, p. 332–336 [DOI:10.5170/CERN-2007-007.332].

[3] C. Soós et al., *The Versatile transceiver: Towards production readiness*, 2013 *JINST* **8** C03004.

[4] F. Faccio et al., *FEAST2: A Radiation and Magnetic Field Tolerant Point-of-Load Buck DC/DC Converter*, in the proceedings of the *Radiation Effects Data Workshop*, Paris, France (2014), p. 1–7 [DOI:10.1109/REDW.2014.7004569].

[5] C. Fleisig et al., *Detection of Ionisation Electrons with Hybrid Pixel Detectors for Non-Destructive Beam Profile Measurements*, submitted for publication.

[6] M. McLean et al., *Non-destructive beam profile measurements with an Ionisation Profile Monitor (IPM) based on Timepix3&4 Hybrid Pixel Detectors (HPDs)*, *JACoW I* **BIC2024** (2024) WEP15.

[7] A. Canesse et al., *Overview of the radiation levels in the CERN accelerator complex after LS2*, *JACoW I* **PAC2023** (2023) THPA046.

[8] M. Barros Marin et al., *The Giga Bit Transceiver based Expandable Front-End (GEFE)—a new radiation tolerant acquisition system for beam instrumentation*, 2016 *JINST* **11** C02062.

[9] A. Caratelli et al., *The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments*, 2015 *JINST* **10** C03034.

[10] GBTx Manual, https://cds.cern.ch/record/2809057.

[11] J. Troska et al., *The VTRx+, an optical link module for data transmission at HL-LHC*, *PoS* **TWEPP-17** (2017) 048.

[12] F. Faccio et al., *The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness*, *PoS* **TWEPP2019** (2020) 070.

[13] J.A. Alozy et al., *Development of a single-photon imaging detector with pixelated anode and integrated digital read-out*, 2022 *JINST* **17** C06007 [arXiv:2112.10636].

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