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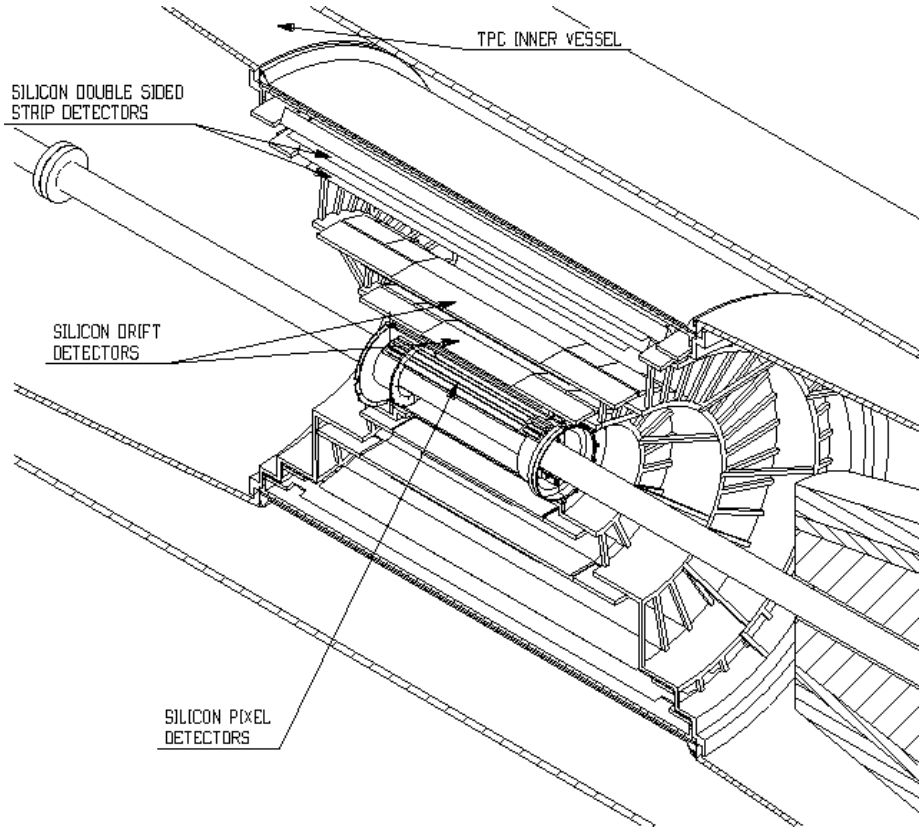

A possible SDD readout scheme for the Inner Tracking System of the ALICE experiment

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Chapter 1

System requirements

The ALICE Inner Tracking System (ITS) is made of 6 silicon detector layers, as summarized in table 1.1. This document refers to the layers 3 and 4, that consist of Silicon Drift Detectors (SDD).

The layers have cylindrical shape and are formed of linear structures called ladders. The SDD ladder organization is shown in table 1.2. The total number of anodes is 61440 (or 69120) for layer 3 and 147456 for layer 4. The maximum power dissipation allowed by constraints on the amount of material for the cooling system is around a total of 0.7 kW for the two layers.

The SDD structure is shown in fig. 1.1. When a particle crosses the detector a charge cloud is generated. Due to the electric field, the cloud drifts toward the anodes. At the collection anodes the cloud has a gaussian-like shape; during the drift the cloud becomes larger, due to charge carrier diffusion, but maintains its shape.
For particle tracking and identification it is necessary to know :

- The cloud position projected along the anodes

Layer	Type	r(cm)	$\pm$z(cm)	Area(m^2)
1	pixel	3.9	12.25	0.06
2	pixel	7.6	16.3	0.17
3	drift	14	21.1	0.37
4	drift	24	29.6	0.89
5	strip	40	45.1	2.27
6	strip	45	50.4	2.85

Table 1.1: Inner Tracking System dimensions

Layer	Ladders	Detectors/ ladder	Anodes/ detector	Anodes/ ladder
3	16-18	5	2x384	3840
4	24	8	2x384	6144

Table 1.2: ALICE SDD layers organization

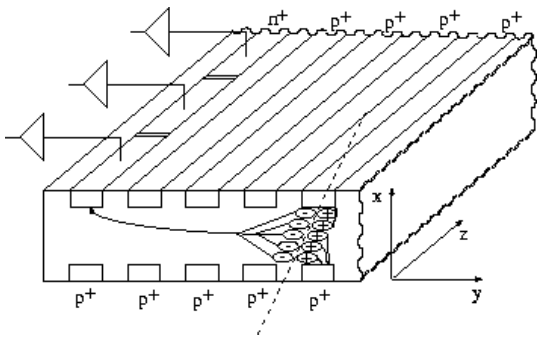

Figure 1.1: Silicon Drift Detector structure

- The charge cloud arrival time (related to the distance from the particle crossing point to the anodes)
- The amount of charge collected by the anode(s)

In order to measure these values a two-dimensional cluster reconstruction has to be performed. Due to the spread of the charge during the drift path, each anode will collect only a fraction of the deposited charge. This effect increases the constraints in terms of noise requirements for the preamplifier. Monte Carlo simulations suggest that 500 e^- ENC could be an acceptable value.
In the experiment the detector will be biased by an electric field of around 480 V/cm, which gives a drift velocity of 6.5 $\mu m/ns$. The detector will be butterfly-shaped, with a maximum drift lenght of 32.5 mm. This gives a maximum drift time of 5 μs. At the anode the gaussian output signal will have σ between $\sim$10 and $\sim$30 ns (depending on the length of the drift path), maximum peak current of 1.6 μA and maximum charge of 40 fC. Signals up to 160 fC are also possible but are rare and not interesting for the particle identification; nevertheless they need to be considered when evaluating the saturation condition of the preamplifier.

Chapter 2

Proposed Architecture

A general scheme of the proposed architecture for the SDD readout is shown in fig. 2.1. The readout chain is divided in two major units :

- Signal amplification and A/D conversion
- Data compression and transmission

The first unit is distributed on the ladder near the detectors, whereas the second unit is concentrated at both ends of the ladder itself.
Key points of the proposed architecture are :

- To convert the analog data into a digital representation as soon as possible, in order to avoid signal degradation during data transmission
- To avoid any on-line data analysis. In a detector like ALICE an early failure detection is very important and it is safer if raw data are sent to the acquisition system. Moreover, data analysis requirements can change during the experiment and a system with hardwired analysis would be less flexible
- To minimize the power consumption near the detector, in order to decrease the amount of material needed to implement the cooling system

2.1 Signal amplification and A/D conversion unit

The basic idea is to amplify the detector output current, sampling it and performing an A/D conversion. As a good tradeoff between power consumption and time resolution a sampling frequency of 40 MHz has been chosen. Such sampling rate allows to obtain at least 3 samples of the signal shape from an anode, even at minimum drift time.However, it is not possible to design an A/D converter

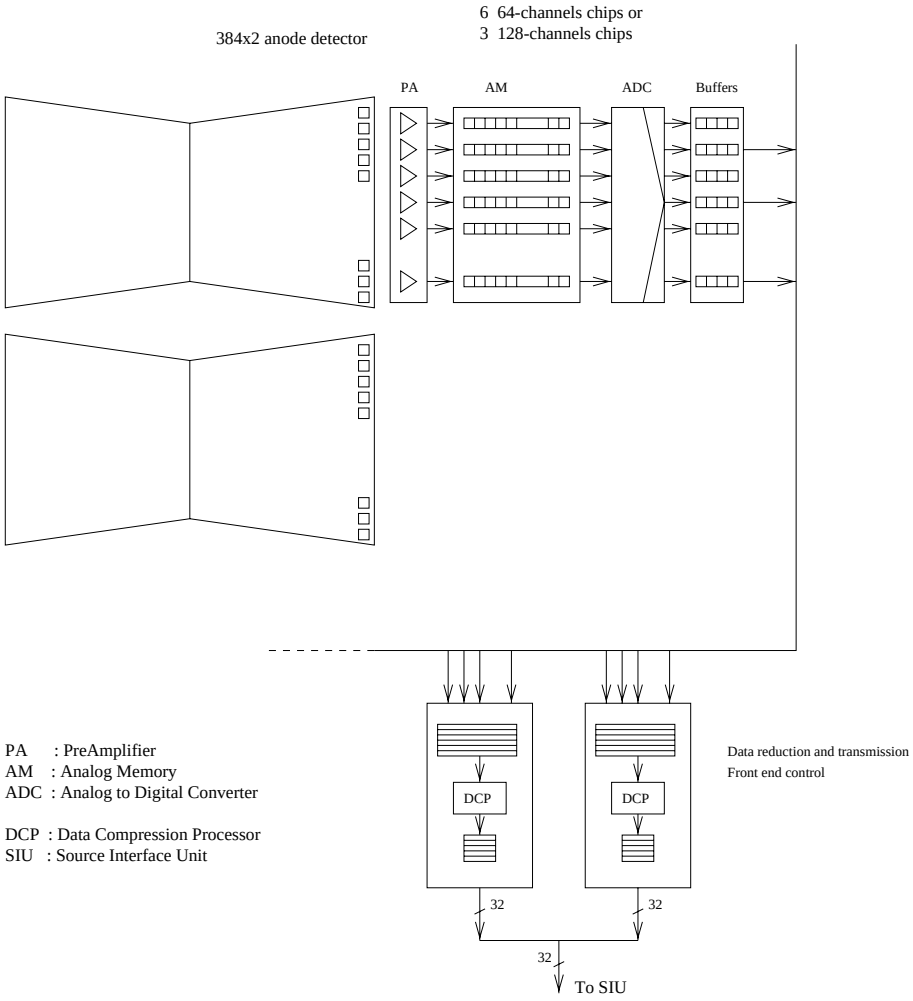

Figure 2.1: A possible SDD readout scheme

at this conversion frequency that satisfies the space and power requirements (the power limits mentioned above allow a maximum power consumption of $\sim$3 $mW/channel$); it is then necessary to implement a temporary analog memory to allow the A/D converter to work only when the external trigger is received. This indeed allows the conversion frequency to be reduced by more than one order of magnitude.
Each half detector (384 anodes) will be connected with 3 chips of 128 channels or 6 chips of 64, depending on chip yield and final chip geometry. Each channel consists of a preamplifier, a 256 cell analog memory, an 8-bit A/D converter and a set of digital buffers and drivers for data transmission.
The circuit works as follows : the SDD output is continuously amplified and sampled at 40 MHz. Samples are stored in the analog memory while waiting for a trigger signal. ALICE detector will produce three useful triggers, namely the first level trigger ($L0$) with a fixed latency of 1.2 μs, the second level trigger ($L1$) with a fixed latency of 2.4 μs and the third level trigger ($L2$) with a variable latency ($\leq$ 100 μs). The chosen trigger signal freezes the analog memory (after an additional delay related to the drift time) and starts the A/D conversion phase, dealt in parallel with the data transmission to the end of the ladder. During the conversion time any signal from the detector is ignored.
The preamplifier is a transimpedance amplifier with an input range of a couple of μA and an output range of about 1 V. The bandwidth has to be around 10-12 MHz, that is a reasonable bandwidth at the chosen sampling frequency. In order to decrease the A/D resolution from 10 to 8 bit without affecting the SNR, a non linear transfer function is required. The upper limit for power consumption is 1 $mW/channel$.
The analog memory needs 256 cells, to cope with the maximum drift time, a write frequency of 40 MHz and a read frequency of 3 MHz. It must dissipate less than 2 $mW/channel$ during writing phase at 40 MHz. Its power consumption during the readout phase, when also the ADC works, has to be lower than 500 $\mu W/channel$.
The A/D converter requirements are : 8-bit resolution and power consumption below 10 $mW/channel$ during conversion. Since the ADC is triggered, it works only around 10% of the time, then the average power dissipation satisfies the overall requirements for one channel. The conversion time depends on the dead time that is tollerable : around 3.5 $\mu s/channel$ for 1 ms dead time and 400 $ns/channel$ for 200 μs dead time.

2.2 Data compression and transmission unit (DCTU)

At the end of the ladder power and size requirement are less stringent, so it is possible to reorganize the data in order to reduce the output bandwidth.
More than 90% of data are baseline samples, so a strong data reduction is possible. Two solutions are under study :

- Zero suppression : nonzero data cluster, corresponding to a charge cloud, are recognized and sent out along with a time-stamp. This solution is efficient but needs careful on-line data analysis in order to efficently recognize variable size data clusters. Furthermore, the analysis of two overlapping clusters can be complex.

- Data compression : this approach intends to obtain data reduction avoiding cluster analysis and loss of information. The principle is to calculate the differences between consecutive samples and to apply a Huffman coding to the values; this algorithm is able to get compression using the spread in result probability. This solution makes the on-line processing very simple, but produces a smaller reduction compared with the previous one.

After the reduction, the data are sent to the transmission unit that is connected with the SIU board (see [2]).

2.3 Transmission between the two units

The amount of data that has to be transmitted between the two units is very large : in the worst case (layer 4) there are 6144 anodes with 256 8-bit samples each. The DCTU chips can be placed on both sides of the ladder; anyway for each side 768 $Kbytes$ have to be trasmitted. Two possible scenarios are under study :

- After the ADC only a 2 *bytes/channel* buffer is used. In this case the transmission time must be equal to the conversion time; this means a bus bandwidth of around 768 $Mbytes/s$ in the case of 1 ms transmission time and 3840 $Mbytes/s$ for 200 μs transmission time. Supposing to transmit at 40 MHz (the same frequency of the analog memory clock) the number of 8-bit buses will be 20 for the first case and 96 for the second one. A more practical number for the first case is 24 buses (one every 128 channels), while 96 buses is exactly one bus for every 32 channels. This leads to a number of cables that is very difficult to manage, especially if the case of 200 μs transmission time has to be chosen.

- After the ADC one or more 256 *bytes/channel* digital buffers are implemented. In this case the conversion result is stored locally and then transmitted at lower speed. An analysis made for the ALICE TPC detector (see [3]) shows that with 2 buffers and a readout time of 2 ms the dead time due to buffer saturation is only 0.1%; the dead time increases to 9.1% with a 10 ms readout time. Supposing to have an 8-bit bus for each 384 channels (half detector) the readout time required is around 2.5 ms, with only 8 buses for each ladder side.

The second solution greatly simplifies the cabling between the two units; unfortunately analog and digital memory cannot effectively be integrated on the same chip (for size and noise reasons) and two chips have to be accomodated on the ladders, where the space and power consumption requirements are more strict. The impact of the second solution in the design is currently under investigation, anyway a resonable figure for power consumption is 5-6 mW for each 256 byte buffer at 1 MHz write time.

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