Reconfiguring Quantum Error-correcting Codes for Real-life Errors

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Abstract.

High error-rates preclude the preparation of fully error-corrected logical qubit state on Noisy Intermediate Scale Quantum (NISQ) computers. When operand logical qubits inherit large state-preparation noise, it is difficult to show that subsequent logical gate fails less frequently than its physical (unprotected) version. We articulate a scheme of decoupling transversal logical gate errors from state-preparation noise and experimentally validate its use-case for IBMQ quantum processors. We find that in the absence of state preparation noise, the IBMQ processors significantly raise the likelihood of certain two-qubit errors in the operand(s) of [[7, 1, 3]] transversal gates. Yet, encoding can still be shown to improve the gate fidelity provided that the gate operands are strategically decoded/corrected for the likely two-qubit errors in lieu of their less likely single-qubit counterparts. This trade-off enables quantum CSS code to principally correct longer strings of errors without increasing the codeword size and paves new avenues of investigating fault-tolerance in NISQ computers.

1. Introduction

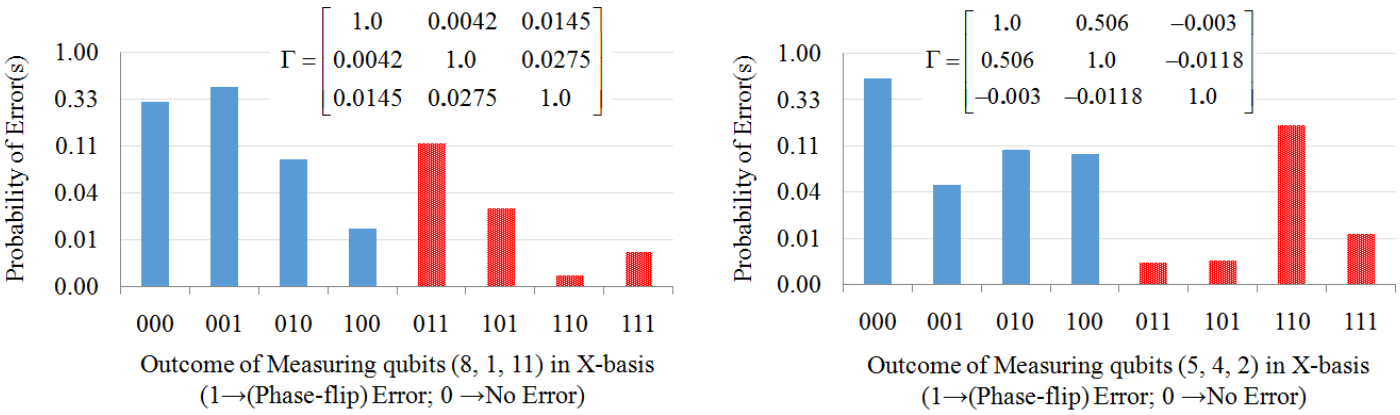
Accurate characterization of noise in the encoded gates is a challenging yet promising avenue of research experiments [43, 50, 27, 47, 35] on real quantum processors. The challenge lies in distinguishing errors on the logical (encoded) gate from those in the faulty preparation of operands initial logical state. Encoding physical qubits into high fidelity logical state remains at odds with hardware limitations including (i) limited number of ancillary qubits and (ii) sparse qubit-qubit connectivity [16, 38, 53]. These

constraints realize unreliable non-local CNOT gates on the encoding qubits, leading to the preparation of noisy encoded state, particularly in case of universal quantum error-correcting code. Recently, a pioneering attempt [20] of preparing $[[5, 1, 3]]$ encoded basis state has reported state-preparation fidelity no higher than 0.57 on 5-qubits superconductor quantum processor. When operands are pre-loaded with large state preparation noise, how can we efficiently uncover logical gate intrinsic errors and show that it can achieve higher fidelity than the same physical (un-encoded) gate?

A two-fold contribution of this work is follows. First, it provides efficient experimental means of indirectly estimating probability distribution of errors (pde) of the transversal logical gate. The scheme does not require encoded state preparation, instead, it suffices to transversally initialize the encoding qubits in the equal superposition state. Therefore, noisy logical gate ε is directly applied to the superposition state and pde is computed by transversally measuring encoding qubits in X-basis. This pde is obtained from experimental statistics and is transformed into the pde of noisy encoded operand by using codespace projector P. The validity of proposed scheme is conditioned upon $[P, \varepsilon] = 0$ whereby ε commutes back to act on the qubits equal superposition state. A remarkable feature of this method is that it offloads the noisiest and the most complicated section of logical state preparation—the projective transformations of superposition state and its pde—onto classical post-processing, leaving quantum device tasked with only transversal gates execution.

Secondly, we analyze the error probability distribution and show that Steane [45] logical gate significantly elevates the likelihood of certain two-qubit errors in the operand. These are degenerate errors and can be easily corrected when converted into non-trivial (other than Identity) codespace Stabilizers. Appendix A provides proof-of-principle examples of distance-3 CSS codes [8] capable of correcting weight-2 bit-flips/phase-flips or both. All two-qubit errors in case of Steane code can be corrected, although, at the expense of their corresponding co-syndrome single-qubit counterparts transform into logical errors. We find that the gate can achieve higher fidelity by virtue of encoding if, instead of dogmatically decoding its operand for single-qubit errors—as occurs in conventional fault-tolerant schemes—a given syndrome is decoded into more likely two-qubit errors instead of less probable single-qubit error. In comparison to the strict single-qubit decoding schemes, our proposed strategy achieves 2-3 fold reduction in the logical failure probability of the operand. It is the probability that decoding and correction of errors in classical post-processing reveals the incorrect qubit logical state. Most importantly, this multi-fold reduction provides critical leverage to demonstrate that Steane code can practically improve the gate fidelity, although only modestly.

This idea is prefaced in Fig-1; it shows example pde of an encoded qubit protected by phase-flip code: $|\bar{+}\rangle \longrightarrow |++\!+\!+\rangle$ (where $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$). The pde was obtained from the results of two experimental circuits: (a) shows transversal logical operation: CNOT $|\bar{+}\rangle$,$|\bar{+}\rangle \longrightarrow |\bar{+}\rangle$,$|\bar{+}\rangle$ gate executed on ibmq_16_melbourne (b) shows $|\bar{+}\rangle$ state undergoing identity gate on ibmqx4_tenerife. The probability distribution of phase-flip errors, obtained by decoding the operand logical qubits, clearly shows that the



(a) Transversal CNOT gate in ibmq_16_melbourne

(b) Memory (Identity) gate in ibmqx4_tenerife

Figure 1. (Color online) The probability distribution (shown using logarithmic ordinates) over the phase-flipped qubits in an IBM Superconductor quantum computers. Both circuits prepared their qubits in equal superposition state (i.e. $|+\rangle^{\otimes 3}$) and Measured these in X-basis after their respective gates. Two or more qubit errors are shown by red textured bars while fewer than two errors are represented by solid blue bars. In (a) ibmq_16_melbourne qubits 1,8 and 11 were control operand of three CNOT gates. Their corresponding target qubits were 0, 7 and 3, each prepared in equal superposition state. In (b) we applied a sequence of 24 Identity gates to each one of the qubits 2,4 and 5 on ibmqx4_tenerife device. Ideally, both circuits stabilize initial state (i.e. $|+\rangle$) of the qubits. However, the decoherence due to real noisy gates, was projected onto phase-flip errors when qubits were Measured in the X-basis. The qubit phase-flip error probabilities were obtained using 8192 x 3 = 24576 shots for each circuit. The Pearson correlation matrix Γ obtained from respective Measurement statistics, indicates correlations among qubits errors

joint failure of noisier qubit pairs (1, 11) and (4, 5) is significantly higher than several single-qubit errors (e.g. qubit-8 in ibmq_16_melbourne and qubit-2 in ibmqx4_tenerife). Clearly, one can significantly improve the fidelity of logical state of encoded qubit by correcting it for more probable two-qubit errors.

Organization of remaining discussion is follows: Section-2 describes the framework of experimentally calculating pde in the logical qubit protected by Steane code. The details of experiment setup are given in Section-3 while experimental results are presented and discussed in Section-4. Section-5 situates this work within relevant prior studies on fault-tolerance and error-correction in real quantum computers. Section-6 summarizes the manuscript with possible directions of the future work.

2. Calculating Phase-Flip Error Distribution for the Steane Encoded State

The Steane encoded $|+\rangle$ state contains equal superposition of all sixteen codewords of classical $[7, 4, 3]$ Hamming code $\mathbf{C}_1$. Its dual code $\mathbf{C}_2 = \mathbf{C}_1^{\perp} \subset \mathbf{C}_1$ is a classical

$[7, 3]$ code (minimum code-distance = 3) whose codewords constitute the support of X- and Z-Stabilizers of the Steane code. It is a distance-3 code and was originally invented to correct arbitrary single-qubit errors. However, Appendix A shows that it is possible to correct arbitrary two-qubit errors by sacrificing corresponding single-qubit error-correction. The trade-off provides leeway to select dominant high-weight errors for correction and improve the fidelity of Steane logical gates. Because of their crucial role in limiting the overall/average gate fidelity, only phase-flip errors are taken into consideration in our experimental results and analysis.

Fig-2 outlines Noise Operator Commute-Back method as experimental means of calculating probability distribution over errors in Steane logical gates by initializing its operand(s) in the equal superpositon state: $\rho_{sup} := \otimes_{i=1}^{7} |+\rangle\langle+|$. The preparation of a operand logical states $\rho_{enc} := |\bar{+}\rangle\langle\bar{+}| = \frac{1}{16}\sum_{x,y\in \mathbf{C}_2^{\perp}} |x\rangle\langle y|$ proceeds by applying an ideal codespace projection P to ρ_{sup}, which converts it into the ρ_{enc} (later, it will be shown how projection part can be simulated as classical post-processing step). Afterwards, as encoded state undergoes processing, the corresponding noisy logical gate operator ρ_{enc} may commute back to act on superposition state ρ_{sup} if $[P, \varepsilon] = 0$. This crucial commutation property lies at the heart of this work and exploits the fact that dephasing, being recognized as one of the most potent source of noise in transmon superconductor qubits [9, 32, 29], can be described as qubit-environment interaction shown in Fig-2 and Fig-A2 for logical identity and CNOT gate respectively. Hence, these logical gates can be directly applied to ρ_{sup} state and error statistics can be collected from the transversal Measurement of operand (physical) qubits. These statistics are converted into error probability distribution of encoded operand state ρ_{enc} by simulating ideal code-space projection P applied to ρ_{sup} carrying phase-flip errors. We would like to caution that Fig-2 and Fig-A2 show template noise operator which commute with P; other possibilities also exist. The error probability distribution remains valid for *any* ε that satisfies $[P, \varepsilon] = 0$.

The equal superposition state requires only single qubit Hadamard gates which can be executed with very high fidelity—their failure probability is reported to be an order of magnitude smaller than that two-qubit gates and measurements in IBM calibration data. The execution time of single qubit-rotation gates (usually in ns) is negligibly small compared to decoherence time constant T_2 (typically in tens of μs) which attributes lower decoherence noise to Hadamard gate. Therefore, small infidelity of superposition state can be safely ignored compared to those in case when qubits site idle for several no-ops(identity gates) or undergo CNOT gates. One caveat regarding phase-flip errors decoding is the readout noise which can significantly vary across IBMQ qubits—by nearly an order of a magnitude. This limits the choice of our operand qubits to those with acceptable readout failure probability. Alternatively, we either apply IBMQ readout noise compensation scheme or indirectly Measure qubit error by propagating these to qubits having lower readout noise. Corresponding experiment setup and relevant constraints are elaborated in the next section. For now, we return to the development of analytical tool for computing probability distribution of phase-flip

errors.

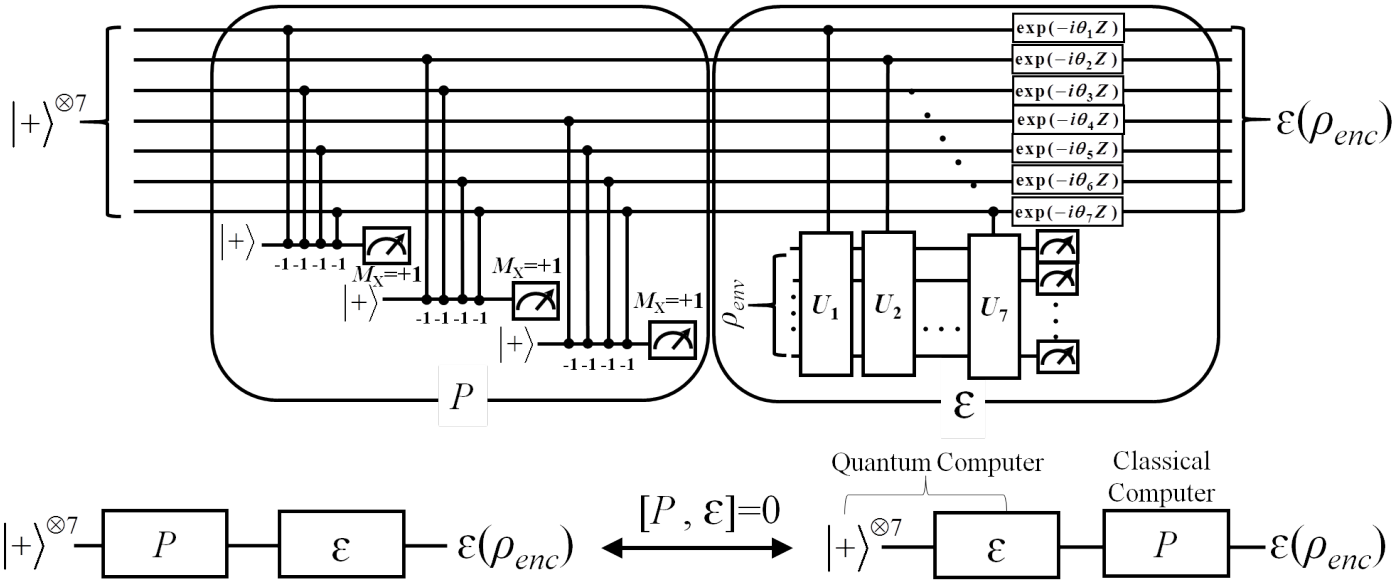


Figure 2. Noise Operator Commute-Back Method circumvents encoded state preparation for obtaining logical Identity gate error statistics. Noise corrupted $[[7, 1, 3]]$ encoded $|+\rangle$ state can be envisioned as an equal superposition state subject to non-unitary codespace P, followed by application of identity gate noise operator ε. If $[P, \varepsilon] = 0$ then noise operator ε commutes back to act on the superposition state. In case of dephasing channel, the controlled-U_i becomes controlled rotation about Z-axis. After obtaining ε induced probability distribution of phase-flip errors in superposition state from experimental statistics, the subsequent mapping of these errors onto encoded $|+\rangle$ state is offloaded to classical post-processing step which implements ideal projection P. The commutation relation $[P, \varepsilon] = 0$, provides reliable and efficient experimental means of indirectly computing phase-flip error probability distribution of the logical state

Note that in the framework of this study, error-correction (EC) means decoding errors on the logical qubit operand after its Measurement, followed by classical post-processing of 7-bit string. It is a (noisy) codeword in either $\mathbf{C}_2$ (which maps to logical $|+\rangle$ state) or in $\mathbf{C}_2^{\perp} \backslash \mathbf{C}_2$ (which maps to logical $|-\rangle$ state). Error-correction is declared successful if decoding recovers codeword of correct logical state. High-Weight EC is a strategy that prefers to correct the bit-string for two errors occurring with higher probability than corresponding low-weight counterparts (single errors). It is contrasted and quantitatively compared with Low-Weight EC which always corrects the bit-string for single errors.

2.1. Noise Operator Commute-Back Method

Define vector $\mathbf{k} \in \mathbb{Z}_2^7$ that identifies phase-flip errors in $|\bar{+}\rangle$ state by setting corresponding indices of error- and error-free qubits to 1 and 0 respectively. The calculation of

probability distribution over set $\mathbf{k}$ phase-flipped qubits in the noisy $|\bar{+}\rangle$, can be parsed into three-step procedure (1) preparation of an ideal encoded state $\rho_{enc} = |\bar{+}\rangle\langle\bar{+}|$ (2) Applying noise to ρ_{enc} and obtain noisy $\varepsilon(\rho_{enc})$ state (3) measuring the resulting noisy state for $\mathbf{k}$ errors. The $\rho_{enc} = \frac{1}{16}\sum_{x,y\in\mathbf{C}_2^\perp}|x\rangle\langle y|$ is prepared by projecting equal superposition state of seven qubit $\rho_{sup} = |+\rangle^{\otimes 7}$ onto $[[7,1,3]]$ codespace by using ideal projection P. We first write density matrix of ideal encoded state as

$$\rho_{enc} = 8P\rho_{sup}P^\dagger$$

Where pre-factor 8(=1/0.125) comes from the denominator in quantum Measurement expression that outputs ρ_{enc} with probability 0.125. Upon successful projection, the addition of noise converts the state into $\varepsilon(\rho_{enc})$. The probability $\Pr_{\mathbf{k}}$ that $\mathbf{k}$ qubits are phase-flipped in the noisy state is calculated by using quantum measurement expression:

$$\Pr_{\mathbf{k}} = \mathrm{tr}(M_{\mathbf{k}}M_{\mathbf{k}}^\dagger\varepsilon(\rho_{enc}))$$

where $M_{\mathbf{k}} = \frac{1}{16}\sum_{x,y\in\mathbf{C}_2^\perp}(-1)^{\mathbf{k}.(x\oplus y)}|x\rangle\langle y|$. Express ρ_{enc} in the form of ρ_{sup} to rewrite above expression as:

$$\Pr_{\mathbf{k}} = 8\mathrm{tr}(M_{\mathbf{k}}M_{\mathbf{k}}^\dagger\varepsilon(P\rho_{sup}P^\dagger)) \tag{1}$$

When noise operator ε commutes with P, it enables crucial reordering of operators in (1) so that experimentally infeasible preparation of ρ_{enc} state can be avoided. Then, reordering peddled by $[P,\varepsilon] = 0$, yields

$$\Pr_{\mathbf{k}} = 8\mathrm{tr}(M_{\mathbf{k}}M_{\mathbf{k}}^\dagger P\varepsilon(\rho_{sup})P^\dagger) \qquad \therefore [\varepsilon, P] = 0 \tag{2}$$

Being interested in phase-flipped errors only, we expand Kraus operator representation of $\varepsilon(\rho_{sup})$ such that each operator $Z_i = \sum_{x\in\mathbb{Z}_2^7}(-1)^{i.x}|x\rangle\langle x|$ flips qubits specified by the binary vector i, in the ρ_{sup} state with probability p_i i.e. $\varepsilon(\rho_{sup}) = \sum_{i\in\mathbb{Z}_2^7} p_i Z_i\rho_{sup}Z_i^\dagger$ where $\sum_{i\in\mathbb{Z}_2^7} Z_iZ_i^\dagger = I$. Substituting $\varepsilon(\rho_{sup})$ in (2) and bringing P, $P^\dagger$ inside the summation will give

$$\Pr_{\mathbf{k}} = 8\mathrm{tr}(M_{\mathbf{k}}M_{\mathbf{k}}^\dagger\textstyle\sum_{i\in\mathbf{C}_2^\perp} p_i PZ_i\rho_{sup}Z_i^\dagger P^\dagger)$$

Note that p_i is an experimentally measurable quantity and our goal is write $\Pr_{\mathbf{k}}$ in terms of p_i. It is clear from Fig-2 that $\forall_i\ [P, Z_i] = 0$, since phase errors in ρ_{sup} commute with the controlled-Z gates implementing P, and enter ρ_{enc} untransformed. Swap P with Z_i (thus also $P^\dagger$ with $Z_i^\dagger$), bring trace operator, $M_{\mathbf{k}}, M_{\mathbf{k}}^\dagger$ inside the summation and invoke permissible reordering of matrices insider trace operator to obtain:

$$\Pr_{\mathbf{k}} = 8\textstyle\sum_{i\in\mathbf{C}_2^\perp} p_i\mathrm{tr}(M_{\mathbf{k}}Z_iP\rho_{sup}P^\dagger Z_i^\dagger)$$

$$= \textstyle\sum_{i\in\mathbf{C}_2^\perp} p_i\mathrm{tr}(M_{\mathbf{k}}Z_i\rho_{enc}Z_i^\dagger)$$

where we have used the fact that $M_{\mathbf{k}}$ is hermitian and $M_{\mathbf{k}}M_{\mathbf{k}}^{\dagger} = M_{\mathbf{k}}$. Write trace input as product of two summations i.e. $M_{\mathbf{k}}Z_i\rho_{enc}Z_i^{\dagger} = \frac{1}{256}\sum_{u\in\mathbf{C}_2^{\perp}}(-1)^{u.(i\oplus\mathbf{k})}\sum_{x,y\in C}(-1)^{\mathbf{k}.x\oplus i.y}|x\rangle\langle y|$. The first summation is non-zero only when $i \oplus \mathbf{k} \in \mathbf{C}_2$. This leads to $\sum_{u\in\mathbf{C}_2^{\perp}}(-1)^{u.(i\oplus\mathbf{k})} = |\mathrm{C}_2^{\perp}| = 16$ and $\sum_{x,y\in\mathbf{C}_2^{\perp}}(-1)^{\mathbf{k}.x\oplus i.y}|x\rangle\langle y| = Z_i\rho_{enc}Z_i^{\dagger}$ since $(-1)^{\mathbf{k}.x\oplus i.y} = (-1)^{\mathbf{k}.x\oplus\mathbf{k}.y}$. Hence

$$M_{\mathbf{k}}Z_i\rho_{enc}Z_i^{\dagger} = \begin{cases} Z_i\rho_{enc}Z_i^{\dagger} & i\oplus\mathbf{k}\in\mathrm{C}_2 \\ 0 & \text{otherwise} \end{cases}$$

Since $\mathrm{tr}(Z_i\rho_{enc}Z_i) = 1$, the final expression of $\Pr_{\mathbf{k}}$ simplifies to

$$\Pr_{\mathbf{k}} = \sum_{i|i\oplus k\in\mathbf{C}_2} p_i \tag{3}$$

Therefore, the probability distribution over $\mathbf{k}$ phase-flipped qubits in the $n-$qubits encoded state can be calculated from the probability distribution (p_i) of phase-flipped qubits in the $n-$qubit equal superposition sate which can be transversally prepared on the quantum processor hardware. The same procedure and the result applies to $|-\rangle$ logical state, except that first three operand qubits are phase-flipped (Steane $\bar{Z} = Z_1Z_2Z_3$) after initialization in the superpositon state.

2.2. Connection with Error-Transparent Gates

Coincidentally, a condition similar to $[P, \varepsilon] = 0$, makes a pre-requisite of passively error-corrected logical gates known as error-transparent gates [51, 26, 36]. It requires gate Hamiltonian to commute with the noise operator throughout its evolution in order to uniquely identify and neutralize otherwise indistinguishable random qubit errors, occurring at different time instances during the gate execution. As a result, the error-transparent gates, in theory, have been shown to exhibit nearly an order of magnitude lower failure probability [26] without increasing the qubit life-times (T_1 or T_2). On the other hand, our study utilizes commuting noise operator to accurately uncover errors on logical gate so that it can be shown to have lower failure probability compared to its unprotected counterpart. Inspite of these similarities, noise operator commute-back condition has a very different goal—to completely skip operand state-preparation circuit for the exclusive quantification of logical gate failure probability.

Nevertheless, if error-transparent gates become physically realizable in future, it will be possible to incorporate noise models of the form other than ε shown in Fig-2. On such enhancement will encapsulate amplitude damping noise which is one of the main source of random errors in superconducting quantum computers. The canonical form of amplitude damping operator (Fig-8.13 in Ref [40]) does not seem to commute with CNOT gates in P. An error-transparent construction [26] of two-qubit gates robust to photon loss channel (a type of amplitude damping noise) may find a possible remedy to this problem. Therefore, our approach can indeed benefit from the said and other work in this direction.

2.3. Connection with Quantum Process Tomography and Randomized Benchmarking

It is worth situating Noise Operator Commute-Back method withing the framework of noise quantification schemes. One relevant scheme is logical randomized benchmarking [11] that quantifies average failure probability of logical gates. Unfortunately, it requires periodic application of error-correction in the random sequence of logical Clifford gates. This approach seems infeasible considering severe resource limitation of NISQ computers. If error-correction is skipped, it would let loose errors in noisy initial logical state to infect logical gates and produce convoluted noise. Consequently, it becomes difficult to separate gate errors from State Preparation And Measurement (SPAM) noise. Secondly, large state preparation noise will limit the length of randomized gate sequence; it will take only few gates to drive rapidly decohering logical qubit state to maximally mixed state. Both consequences severely undermine basic spirit and applicability of randomized benchmarking schemes [17, 31, 37, 14, 52]. In addition, these schemes are known to show inaccurate estimate of average error probability for unitary (coherent) [33] and correlated errors [6].

On the other hand, protocols based on quantum process tomography [42, 10] can accurately quantify any type of noise in the logical gate, although, at the expense of number of experimental runs scaling exponentially in the number of logical qubits. However, small size of NISQ computers is expected to limit near-term experiments to gate-level fault-tolerant circuit employing no more than two logical qubits. In this context, quantum process tomography, therefore, resurfaces as viable option for the in-depth investigation of noise patterns in the logical gate noise, provided that we can effectively address its main limitation—the sensitivity to SPAM errors. Fortunately, the Noise Operator Commute-Back method abridges the gap by eliminating logical state preparation of the gate operands. Together with quantum tomography approach, it becomes a valuable tool for exploring noisy patterns in small size logical circuits.

2.4. Scope of Noise Operator Commute-Back Method

The generality of proposed method empowers it to subsume variety of realistic noise models that can commute with code-space projection operator P. One interesting case is that of spatially and temporally correlated noise given in Ref [2]. Their noise operator (see Fig-3 and Fig-4 in Ref [2]) has the same form as that of ε used in this study, except for the unitary noise component. The mapping is very simple; the control unitary gate of ε become controlled rotations about z-axis where (small) rotation angle approximates the strength of correlated noise (please find detailed discussion on correlation strength parameter L_0 in Section-4 of Ref [2]). Another example of commuting noise is the depolarizing operation, its admissibility considerably broadens applicability of the method. By applying twirl operations to the operand qubits, one can easily convert arbitrary noise channel into depolarizing channel.

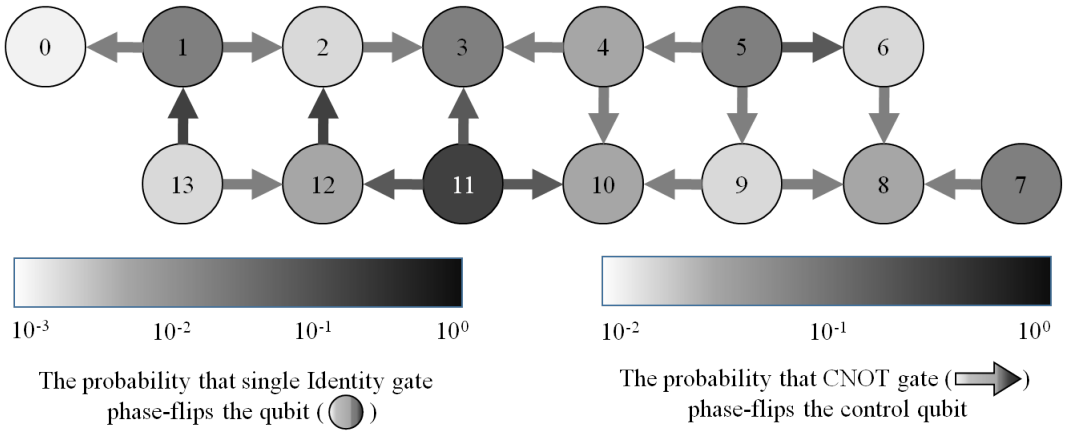


Figure 3. The error probability of ibmq_16_melbourne qubits (shaded circles) due to (a) Single Identity gate (b) CNOT gates (shaded arrows). These probabilities were obtained from Qiskit (https://qiskit.org) quantum state tomography routine. Although, these error-probabilities varied over time, this snapshot is most consistent with our experimental results and recent IBMQ calibration data. Note that the indicated error probabilities include respective qubit state-initialization and read-out errors

3. Experiment Setup

We designed our experiments for investigating errors in the $[[7, 1, 3]]$ encoded qubit subject to logical CNOT and Memory (Idle) gate. The nature of logical operations dictated the choice of quantum computing device–expected to be large enough to store at least two logical qubits and facilitated sufficiently large number of transversal physical CNOT gates. Another selection problem was the identification of operand physical qubits suitable for achieving considerably higher gate fidelity by High-Weight EC. We generated error profile of physical qubits and gates so that these could be discriminated on the basis of their respective noise levels. For quantitative comparison, we defined *fidelity gain* as the ratio of logical failure probability of Low-Weight EC to the logical failure probability of High-Weight EC. We noticed that fidelity gain was highlighted when logical operand contained noisier physical qubits in certain *optimal* proportions. Based on selective operand compositions, our experimental results showed that strict single-qubit error-correction frequently failed to reduce the failure probability of the logical gate below the break-even point i.e. average failure probability of corresponding physical gates (the discussion on computing this crucial parameter will appear shortly). By contrast, strategic correction of likely two-qubit errors achieved far more encouraging results by frequently lowering the logical failure probability below the break-even point.

3.1. Selecting the Quantum Computing Device

At the time of writing, the ibmq_16_melbourne superconductor quantum computer was the largest IBMQ quantum computer in our access, that can store up to two $[[7, 1, 3]]$ logical qubits and execute logical CNOT gate with a minor constraint to be discussed later. The device features ease of programming, accessibility, daily calibration, fast execution of quantum circuits and reproducibility of their results. Our six months long experimental study of this machine began soon after its introduction in Nov 2018. Nearly 500 experiments were spent in rigorously authenticating the substantial disparity in qubits decoherence levels. Although, bulk of our final results summarize findings from the most recent set of executions, large number of earlier experiments proved handful in systematically identifying an appropriate set of noisy qubits set (and CNOT gates) to constitute credible evidence of high-weight errors and the fidelity gain obtained by their correction.

3.2. Scheduling Experiments Around Device Calibration

The computer maintenance routine, in the form of periodic device calibration, significantly dictated the schedule our experiments. We note that the qubits error probability generally increased with the time elapsed since last calibration, mainly due to its increasing accumulated usage. Apparently, this two hours long process runs special quantum state/process tomographic as well as randomized benchmarking routines to determine noise levels in the hardware and reboots the device after retuning and refreshing the qubits. During the calibration interval, the device does not perform user experiments, instead, these are stored as long queue of pending jobs. Once calibration is complete, the device forthwith resumes execution of pending user experiments, the first job in the queue is likely executed with highest quality qubits and gates. To minimize the time-dependent coherence loss effect, we attempted to carefully schedule our experiments in order to minimize their wait time in the queue. To further increase the validity of our results displayed in Section-4, each data point on the graph was collected from the median output of at least three different executions of the exact same logical gate circuit.

3.3. Generating Qubits Errors Profile

The IBMQ platform also updates device calibration data after quantifying noise levels in the form of average-case error probabilities of single- and two-qubit gates. Although, average-case data is a valuable indicator of an overall performance of circuit components (qubits and gates), we independently generated their error profile based on the specific needs of our experiment setup. The profile was generated by running quantum state tomography routine provided by the Qiskit (https://qiskit.org) platform. It computed the likely density matrix of the qubit prepared in equal superposition state subject to memory or CNOT gate, both would ideally leave its state unchanged. The Fig-

3 uses gray-scale image to identify higher decoherence noise with dark shaded circles (qubits) and arrows (CNOT gates). It shows that qubit-11 is the noisiest qubit followed by qubits 1, 3 and 7. The indicated error probabilities were statistically computed by counting the fraction of times a qubit prepared in the $|+\rangle$ state, collapsed to -1 eigenstate of X operator upon Measurement i.e. it acquired phase-flip error. On the other hand, the CNOT gate induced qubit error probability was calculated from the statistical likelihood of the control qubit flipping from $|+\rangle$ to $|-\rangle$ state when both its operand qubits were initialized in $|+\rangle$ states. It was also obtained by quantum state tomography of the control qubit as it undergoes following circuit: State initialization$\rightarrow$ CNOT$\rightarrow$Measurement. From the comparison given in the map, the CNOT gates specified by their (control, target) qubit pairs (13,1), (12, 2) (11,3), (11,10) and (11,12) are more likely to phase-flip their control operand than the rest. Note that the likelihood of faulty state initialization and Measurement is included in the qubit error-probabilities of shown in Fig-3. Nevertheless, the error probability profile generated by our statistics are in close agreement with those published on the IBMQ website.

3.4. Calculating Failure Probabilities

The error-correction logical failure probability of the Steane code utilizes expression given in (3). Define $\mathrm{Pr}^{(0)} := \mathrm{Pr}_{\mathbf{k}=0}$ and $\mathrm{Pr}^{(\mathbf{L})} := \sum_{\mathbf{k}:\mathbf{H}_2^{\perp}\mathbf{k}=0,|\mathbf{k}|=3} \mathrm{Pr}_{\mathbf{k}}$ as probabilities of no error and *all* undetectable logical errors, respectively. Similarly, define $\mathrm{Pr}_{\mathbf{k}}^{|\mathbf{k}|=1} := \mathrm{Pr}_{\mathbf{k}:|\mathbf{k}|=1}$ and $\mathrm{Pr}_{\mathbf{k}}^{|\mathbf{k}|=2} := \mathrm{Pr}_{\mathbf{k}:|\mathbf{k}|=2}$ as probabilities of single-qubit and two-qubit errors respectively; the binary vector $\mathbf{k}$ locates error qubits in the codeword by 1 at the corresponding indices. These probabilities can be easily derived from (3). Then, by definition, the logical failure probability of Low-Weight EC (P_{lw}) becomes:

$$P_{lw} = \sum_{\mathbf{k}} \mathrm{Pr}_{\mathbf{k}}^{|\mathbf{k}|=2} + \mathrm{Pr}^{(\mathbf{L})} \tag{4}$$

Likewise, the logical failure probability of High-Weight EC (P_{hw}) becomes:

$$P_{hw} = \sum_{c\in\mathbf{Z}_2^3} \min_{\mathbf{k}:\mathrm{H}\mathbf{k}=c} (\mathrm{Pr}_{\mathbf{k}}^{|\mathbf{k}|=1}, \sum_{\mathbf{m}:\mathbf{H}(\mathbf{m}+\mathbf{k})=0} \mathrm{Pr}_{\mathbf{m}}^{|\mathbf{m}|=2}) + \min(\mathrm{Pr}^{(0)}, \mathrm{Pr}^{(\mathbf{L})}) \tag{5}$$

The expression (5) represents convex optimization problem with simple solution. It says that one should prefer to correct two-qubit errors whenever their cumulative probability exceeds that of their low-weight counterparts. Next, in order to quantify the improvement (or degradation) in the fidelity of logical gate when protected by error-correction, we compare the logical failure probability with un-encoded qubit error probability. However, the substantial disparity in physical error rates, complicates the selection of an appropriate statistical metric that faithfully mirrors the fidelity of physical gate which is un-encoded by definition. For comparison, we want a single figure of merit p_e to (i) reflect overall (in)fidelity of multi-qubit encoded state (ii) distributes overall infidelity *identically* among individual qubits on the basis of per-qubit error

probability [2]. For transversal Steane gate, we mathematically define p_e as solution to following set of non-linear equations:

$$(1-p_e)^7 = \mathrm{Pr}^{(0)} \tag{6}$$

$$7p_e(1-p_e)^6 = \sum_{\mathrm{k}} \mathrm{Pr}_{\mathrm{k}}^{|\mathrm{k}|=1} \tag{7}$$

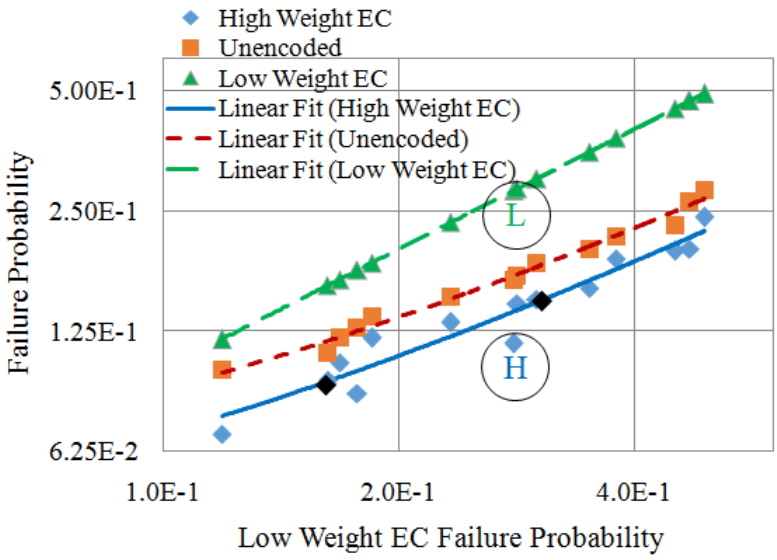
$$21p_e^2(1-p_e)^5 = \sum_{\mathrm{k}} \mathrm{Pr}_{\mathrm{k}}^{|\mathrm{k}|=2} \tag{8}$$

$$7p_e^3(1-p_e)^4 = \mathrm{Pr}^{(\mathrm{L})} \tag{9}$$

It is evident that p_e not only encapsulates error probability distribution of multi-qubit state and but also inherits a sense of per-qubit error probability. In practice, the four equality constraints from equations (6)—(9) generally lead to an approximate solution—one that minimizes the cumulative mean-square difference. The best-fit p_e was computed by solving above set of equations as an instance of non-convex optimization, and provides reference error-probability of un-encoded qubit, for comparison with P_{lw} and P_{hw} in Fig-4,5 and 6. The p_e value calculated this way, represents *average* un-encoded qubit error-probability.

3.5. Making High-Weight Error-correction Decisions

Which set of the two-qubit errors needs to corrected? the decision is based on experimental error-statistics collected from execution of the given circuit. If device error rates remain sufficiently stable, statistical variation in multiple experiments executing the same circuit (logical gate, operand qubits and their initial state remain unchanged) only cause inconsequential changes in the failure probability computations and does not impact error-correction decisions. Under this condition, strategy formulated by using statistics of an experiment remains adequate when it is subsequently reproduced multiple times. The Qiskit batched execution feature significantly reduces the delay between successive of the same logical gate and help achieve stable error profile. We extensively employed batched execution in our experiments to reduce standard deviation less than 10% of the computed failure probabilities values, which is lower enough to draw reliable conclusions. Therefore, High-Weight error-correction strategy, based on the error-statistics of *first* experiment was formulated and *invariantly* applied to the result of all experiments in the batch. In addition to the batch-level temporal invariance, the strategy also featured batch-level *state-invariance*. Same High-Weight error-correction scheme applied to the outcome of experiments dealing with $|+\rangle$ as well as $|-\rangle$ states for the given logical gate and operand qubits.



Low Weight Errors		High Weight Errors	
Error Qubit	Prob.	Error Qubits Pairs	Net Prob.
2	0.0097	(13,12), (5,6), (4,0)	0.146
4	0.022	(13, 5), (12,6), (2,0)	0.0355
12	0.23	(13, 2), (5,0), (4,6)	0.009
5	0.03	(13, 4), (2,6), (12,0)	0.015
0	0.0135	(13,6), (2,4), (12,5)	0.032
6	0.33	(13, 0), (12,4), (2,5)	0.015
13	0.137	(12,2), (4,5), (6,0)	0.021
None	0.238	Undetectable Logical Z Errors	0.009

Low Weight EC Failure Prob. at L is 0.283

High Weight EC Failure Prob. at H is 0.116

Figure 4. (Color online) Steane High-Weight EC lowers the failure probability of the CNOT gate for logical $|+\rangle$ state operands. Only control operand is referenced for comparison of failure probabilities. The graph plots triple (P_{hw}, p_e, P_{lw}) against P_{lw}. The triple plotted on the graph is the median of three triples, each obtained from logical CNOT gate experiment results. Each experiment computed its triple from the statistics collected from 8192 executions(shots) of the same logical gate. The logical failure probabilities were computed from these statistics by using expression given in (4) and (5). For the encircled data points, the syndrome-wise comparison between single-qubit error and their corresponding two-qubit errors, is listed in the table (all errors in each row yield same syndrome value). The shaded rectangles present components of failure probability of High-Weight EC, whereas those inside large thick outlined rectangle, represent components of Low-Weight EC failure probability

4. Experimental Results

The main objective of our experiments is the statistical calculation of logical failure probabilities for evaluating proposed error-correction scheme. Again, it is reminded that an error-correction (EC) procedure simply applies correction to the classical bit-string obtained from transversal Measurement of seven qubits initialized in the equal superposition state and processed by $[[7, 1, 3]]$ logical gates. We consider gate execution to be successful if the corrected readout yields a codeword either in (i) C_2, when the intended state of the operand is logical $|+\rangle$, or in (ii) $C_2^{\perp} \backslash C_2$, when the intended state of the operand is logical $|-\rangle$. Otherwise, it is counted towards logical failure. By statistically calculating the fraction of instances resulting in logical failures, we obtain P_{lw} and P_{hw} as described in the previous section.

For the sake of completeness, the section also includes experiments of preparing Steane logical $|+\rangle$ and $|-\rangle$ states using non fault-tolerant encoding circuit. It requires no additional qubits and maps large fraction of CNOT gates on adjacent encoding qubits

in ibmq_16_melbourne. With careful scheduling, circuit can be executed with small overhead of SWAP gates. The logical failure probability is quantified by the fraction of instances in which logical state is incorrectly interpreted upon readout and subsequent classical post-processing, described previously. One of the main reasons to include the results of non fault-tolerant logical state preparation is to show the effectiveness of High-Weight EC in removing correlated errors on the encoding qubits. Additionally, it benchmarks the performance of state preparation without the burdensome task of obtaining state fidelity from large number of experiments. Instead, it leverages more realistic figure of merit for the quantification of noise: the ability to distinguish between logical basis states, which can be achieved with significantly fewer error statistics of encoding circuit.

Contrary to some prior studies that control magnitude of noise by adjusting the rate at which pauli error gates are inserted into the circuit, our aim is to uncover intrinsic hardware errors. Naturally, such investigation cannot utilize noise control knob which can vary noise levels and makes a useful reference for generating and comparing the trends of P_{lw} and P_{hw}. In the absence of such reference, we have found it convenient to compare these probabilities on graphs whose abscissa is set to P_{lw}. It is because P_{lw} has higher variation compared to P_{hw} (or p_e), not only for different experimental configurations (e.g. selected device qubits) of the circuit but also for different runs of the same circuit (e.g. execution before or after device calibration). Wide range abscissa elegantly spreads data points and provides clearer visualization of failure probability patterns.

4.1. Logical CNOT

The first set of experiments is designed to calculate the probability distribution of the control operand of the Steane logical CNOT with both operands in the $|\bar{+}\rangle$ state. Based on the Section-2 analysis, actual preparation of logical state is not required, instead, gate can be directly applied to operand qubits initialized in equal superposition state as shown in Fig-A2. The gate is mapped to the subset of seven (out of eighteen) device-level CNOT gates indicated by edges in Fig–3. The qubit-qubit connectivity constraints can be understood by visualizing the device as a directed graph mapping qubits and CNOT gates to its vertices and edges, respectively. The vertex(qubit) at the arrow head is the recommended target operand of the corresponding edge (CNOT gate). IBMQ platform invites users to achieve high fidelity gate execution by mapping operand qubits in recommended control-target order specified by edge direction. The accuracy of the gate may be slightly lower if it is executed while its operands are mapped opposite to the edge direction (arrow pointing towards control qubit). We relax the operand order constraint at the expense of incurring some nominal gate infidelity. Then, the edge direction becomes unimportant and directed graph turns into fully connected (undirected) graph allowing any pair non-adjacent qubits to undergo CNOT gate by means of successive swap gates. Although, this flexibility expands numerous

permutations of encoding physical qubits placement, these can be shortlisted by the constraints of our experiment setup for logical CNOT gate, which require:

(i) Each constituent physical CNOT gate has unique control-target qubit pair.

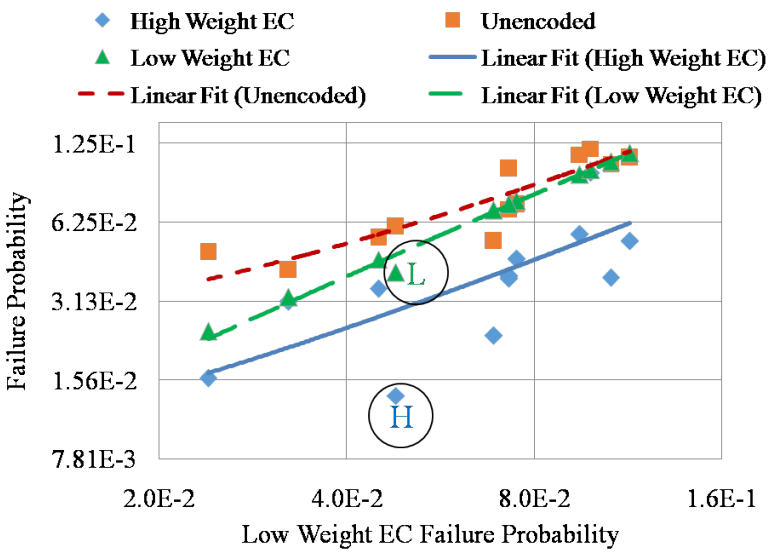
(ii) None of the gates acts on non-adjacent qubit pair. Otherwise, arbitrating (non fault-tolerant) swap gate can convert single qubit error into multi-qubit errors.

The first requirement is relatively straightforward; it arises from the innate transversality of Steane CNOT gate, and can be readily fulfilled. However, the second condition cannot be entirely met due to the structure of device connectivity graph. Essentially, it requires that matching number (size of maximum independent edge set) of the graph is at least seven. However, it is easy to show that Fig-3 graph has matching number = 6. This means we can only execute six physical CNOT gates transversally satisfying both conditions. Our analysis shows that the missing gate barely alters our results and conclusions whenever its error probability is set to the average error-probability of other six gates. We validate this conclusion in the execution results to be described shortly. Before proceeding, we list typical gate operands in the form of (control, target) encoding qubit pairs, in the decreasing order of their contribution to the results:

- $\{(13,1),(12,2),(10,11),(4,3),(5,9),(6,8),(0,7)\}$
- $\{(13,1),(12,11),(2,3),(4,10),(5,9),(6,8),(0,7)\}$
- $\{(13,1),(12,11),(2,3),(4,5),(8,7),(9,10),(6,0)\}$
- $\{(1,2),(13,12),(11,3),(4,5),(6,8),(9,10),(0,7)\}$

The list shows that our preferred compositions of logical control operands, contains qubits bearing lower state initialization failure probability, for example: 0,2,4,6,9 and 13). It is because error statistics obtained from logical CNOT experiments ($|+\rangle^{\otimes 7}$ state-initialization $\rightarrow$ CNOT $\rightarrow$ Measurement) always contain some inseparable component of unwanted state initialization and Measurement errors. Selection of mentioned qubits ensures that the contribution of undesired error probability remains reasonably smaller—about an order of magnitude lower in comparison to that of the respective CNOT gates. All compositions allowed six transversal gates on adjacent qubits. How to deal with the gate on the non-adjacent qubit-pair? will be answered next.

The non-local CNOT is converted into classically-controlled NOT gate after commuting it with the subsequent operand X-basis Measurement. It flips the control qubit Meaurement result when target qubit is readout in $|1\rangle$ state. This additional transformation is also carried out off-line and precedes error-correction applied to the readout result in software post-processing. While this transformation adequately captures error propagation feature of the gate, it may fall short of capturing (phase) errors introduced by the gate itself. Fortunately, it is possible to compensate for the CNOT gate noise by pulling qubits having higher readout noise into the control operand of CNOT gate. In Fig-3, a large fraction of nosier qubits (dark shaded circles) also accrue large readout noise; their Measurement and CNOT error rates have comparable



Low Weight Errors		High Weight Errors	
Error Qubit	Prob.	Error Qubits Pairs	Net Prob.
12	0.072	(13,10), (6,9), (5,0)	0.012
5	0.020	(13, 6), (10,9), (12,0)	0.002
10	0.238	(13, 12), (6,0), (5,9)	0.00036
6	0.007	(13, 5), (12,9), (10,0)	0.0022
0	0.0046	(13,9), (12,5), (10,6)	0.0035
9	0.0023	(13, 0), (10,5), (12,6)	0.0067
13	0.0019	(10,12), (5,6), (9, 0)	0.032
None	0.604	Undetectable Logical Z-Errors	0.0002

Low Weight EC Failure Prob. at L is 0.0482
High Weight EC Failure Prob. at H is 0.0136

Figure 5. (Color online) Extrapolation of Fig-4 in low-noise (Low-Weight EC failure prob. < 0.1) regime, was achieved by skipping some (but not all) CNOT gates. The missing gates were simulated as ideal CNOT gates (in classical post-processing) and corresponding both compensated and uncompensated triples points are included in the graph. Logistics of plotting the graph and calculations of probabilities remain the same as those described in Fig-4. The table shows breakdown of failure probabilities of encircled data points

probabilities ranging: $2.5 \times 10^{-2} - 5 \times 10^{-2}$. Higher readout noise in the control qubit of the missing non-local CNOT gate, adequately compensates for the noise that would have been accumulated had the missing gate had been executed without relocating its operand qubits. Our experimental results show that the missing CNOT gate noise compensation does not substantially impact general trends of comparison between Low-Weight EC and High-Weight EC failure probabilities, (shown in Fig-4), to be described shortly. Therefore, although majority of our data points are based on uncompensated CNOT configurations, a few compensated data points, both plotted and un-plotted, will be analyzed for their alignment with the general trend.

Fig-4 plots data triples (P_{hw}, p_e, P_{lw}) against P_{lw}. Each triple corresponds to median statistics of three logical CNOT experiments with same qubits composition of its operands. The three tuples (one from each CNOT experiment) were sorted by P_{hw} value and only median tuple was plotted on the graph. The comparison of logical failure probabilities evince fidelity gain of 2x–3x providing enough reduction to lower in P_{hw} just below p_e—the break-even point. Thus Steane code has improved the reliability of CNOT gate whose both operands are initialized in $|+\rangle$ state. Detailed insights can be obtained by comparing the logical failure probabilities of the triple $(P_{hw} = 0.116, p_e = 0.161, P_{lw} = 0.283)$ for the gate

operands composition:$\{(13,1),(12,11),(2,3),(4,10),(5,9),(6,8),(0,7)\}$. The table in Fig-4 elaborates breakdown of logical failure probabilities shown as encircled H and L data points for High- and low-Weight EC respectively.

Table 1. High-Weight error-corrected $[[7,1,3]]$ CNOT gate fails less often than physical CNOT gate. Both control and target operands are considered for comparison. The table lists readout-noise compensated probabilities, for selected control, target operands configurations used in Fig-4. Only one physical CNOT gate—on the non-adjacent qubits—was skipped from hardware execution in the first five table entries. The last logical CNOT, marked by *, executed all seven constituent gates

Composition of operands	Failure Probability					
	Control		Target		Overall	
Control , Target	Physical	Logical	Physical	Logical	Physical	Logical
$\{13,12,10,5,4,9,0\},\{1,2,11,6,3,8,7\}$	0.251	0.152	0.066	0.043	0.3	0.188
$\{8,5,9,4,12,13,2\},\{7,6,10,3,11,1,0\}$	0.116	0.076	0.05	0.027	0.161	0.101
$\{8,9,12,13,2,4,6\},\{7,10,11,1,3,5,0\}$	0.115	0.06	0.047	0.002	0.156	0.061
$\{13,12,10,4,5,6,0\},\{1,2,11,3,9,8,7\}$	0.144	0.009	0.139	0.063	0.262	0.071
$\{0,2,13,10,5,6,9\},\{1,3,12,11,4,8,7\}$	0.1	0.046	0.121	0.026	0.208	0.071
$*\{7,9,12,2,4,5,13\},\{8,10,11,1,3,6,0\}$	0.139	0.095	0.070	0.020	0.199	0.113

The syndrome-wise comparison between single- and two-qubits error probabilities shows that qubits 13, 12 and 6 are distinctly noisier in the control operand; their two-qubit errors combinations e.g. (13,12),(13,6) and (12,6), are more probable then their corresponding single-qubit counterparts (qubits 2,4 and 0). By prioritizing the correction of faultier pair of qubits, significant reduction in P_{hw} becomes possible. Therefore, by virtue of High-Weight EC, control operand fails less frequently for logical CNOT gates for all the triples. Furthermore, it should be noted that encircled data point does not aberrantly deviate from trend-line for compensated CNOT configuration. For example, when the operands qubits are swapped on the last pair and qubit-7 becomes control qubit (and 0 becomes target), then the high readout noise on qubit-7 adequately fills the shoes of missing CNOT gate. The corresponding triple simply drifts along the trend-line and is re-situated within close vicinity of existing triples. On one instance, the compensated version relocates it to ($P_{hw} = 0.092$, $p_e = 0.11$, $P_{lw} = 0.162$), on other, it maps it to ($P_{hw} = 0.16$, $p_e = 0.2$, $P_{lw} = 0.35$). Shown as black diamonds on the Fig-4, both triples reinforce the existing trend-line. Thus, the figure accurately reflects the fidelity gain of High-Weight EC for the complete logical CNOT gate.

The missing CNOT problem actually proves to be a valuable tool of extrapolating Fig-4 curves for comparison in the low noise regime where $P_{lw} < 0.1$. When multiple physical CNOTs are replaced with ideal gates in post-processing, their corresponding control qubits gather lesser noise and lower P_{lw}. The corresponding p_e and P_{hw} values are shown in the Fig-5 for uncompensated version of logical CNOT. It shows that P_{hw}

remains consistently lower than p_e and so do the smaller P_{hw} values. However, as their respective trend-lines approach 0.1, P_{lw} converges to p_e, while P_{hw} remains notably smaller as shown by the gap between corresponding trend lines at the end ($P_{lw} = 0.12$). Upon extrapolation in high-noise regime (higher P_{lw} values), these data triples and trend lines faithfully transform into those in Fig-4 (where $P_{lw} > 0.11$). The encircled data point presents an example in which two CNOT gates (12,2) and (11,10) were physically executed, whereas, the remaining five gates (13,1), (5,4), (6,8), (9,3), (0,7) were classically executed. The table shows that elimination of the two-qubit errors (12,5) and (10,12) at the expense of uncorrected co-syndrome single-qubit errors on qubits 9 and 13, provides nearly three-fold reduction on logical failure probability.

4.1.1. Suppression of Readout Noise Above results describe the performance of logical gate without taking target operand into consideration. However, since several qubits, with high readout noise, enter the target operand, it is important to correct the operand error probabilities for large readout noise. Fortunately, this can be efficiently accomplished by invoking Qiskit readout noise filtration routines. We apply these routines in a way that qubits readout noise was directly profiled by executing prescribed test circuits on the device hardware. For each set of seven physical qubits comprising the target operand, a total of 128 test circuits are executed. Apparently, each test initializes the qubits in one of 128 possible classical states (0000000...1111111) and Measure these in $Z-$basis to compute corresponding readout error-probability distribution. After computing a set of 128 distributions, one routine seems to register complete readout noise profile in the form of 128 x 128 conditional error probabilities. Another routine then uses this profile to correct the results of separately executed user-defined circuit to yield new statistics compensated for readout noise. The p_e and P_{hw} of the target operands of selected Fig-4 logical CNOT gates, are obtained from the readout noise compensated error probability distribution and listed in Table-1.

To show that high-weight error-correction improves the reliability of quantum gate, the overall P_{hw} of logical CNOT gate must be less than the p_e value (average failure probability of physical CNOT gates). To this end, we also recompute control operand readout-noise compensated P_{hw} for the selected set of logical CNOT gates. The new P_{hw} of both logical operands and their corresponding p_e are also juxtaposed in Table-1. The comparison reveals that overall failure probabilities are smaller in case of logical gates. The last entry of the table contains failure probabilities for the complete Steane CNOT gate executing all seven constituent physical gates. The seventh gate is a non-local gate containing non-adjacent operand qubits: 13 and 0. It was realized by applying local CNOT(13,1) after swapping qubits 1 and 0. The lower failure probability of complete Steane CNOT gate further reinforces the efficacy of High-Weight EC.

The logical failure probability can be shown lower than p_e for one or more $|-\rangle$ state operand(s). Our more recent experiments on upgraded ibmq_16_melbourne device for more comprehensive quantification of logical gate noise by taking into account fidelity gains for all four combinations of $|+\rangle, |-\rangle$ state operand(s). Upgraded device

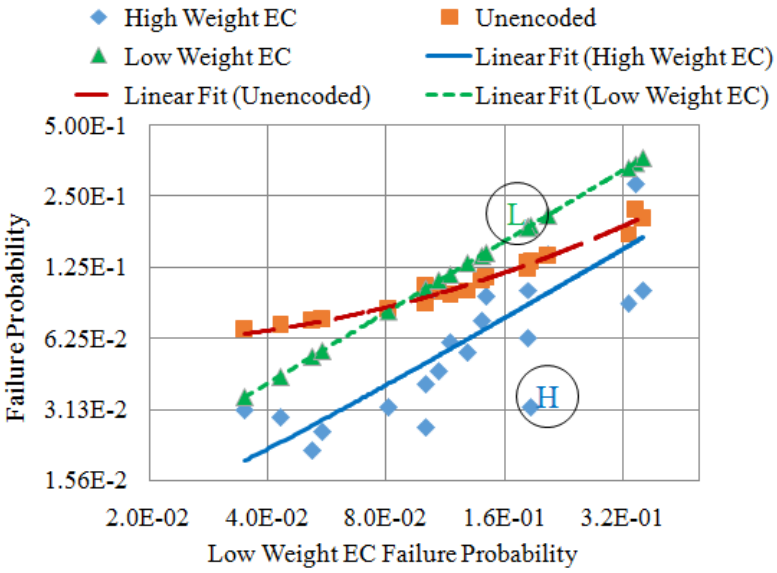
(available online since Dec 26, 2019) added a qubit (qubit-14) adjacent to qubit-0 and 13, enabling execution all 7 physical CNOT gates on disjoint qubit pairs without SWAP gate. For (control, target) = ($\{13, 7, 2, 4, 5, 11, 1\}$, $\{14, 8, 12, 10, 6, 3, 0\}$) configuration, we compared P_{hw} with p_e considering total noise in both operand (as in the last column of Table-1) in states: ($|+\rangle$, $|+\rangle$), ($|+\rangle$, $|-\rangle$), ($|-\rangle$, $|+\rangle$) and ($|-\rangle$, $|-\rangle$). Corresponding $P_{hw} = 0.25, 0.22, 0.21, 0.22$ while $p_e = 0.30, 0.26, 0.28, 0.29$. By averaging over four pairs of states (assuming these are equally probable), we obtained $P_{hw}(avg) = 0.225$ while $p_e(avg) = 0.282$. On the other hand, $P_{lw}(avg) = 0.45$ significantly exceeded p_e. This shows that although $|-\rangle$ state operands may raise failure probabilities, these do not undermine overall efficacy of High-Weight EC. It is vital to note that High-Weight EC strategy must be kept same for all four pairs, since error-correction must be completely oblivious to the logical state. Therefore, in each of the four cases, we corrected single-qubit errors in the control operand for only two syndrome values: $\{-1, +1, -1\}$ and $\{-1, -1, -1\}$. By contrast, target operand was corrected for the two-qubit errors when syndrome was either $\{+1, -1, +1\}$ or $\{-1, -1, -1\}$.

4.2. Logical Memory

The memory errors arise due to the decoherence in logical operand as it undergoes sequence of identity (no-operation) gates. The complete experiment executes: State initialization $\rightarrow$ Identity gate sequence $\rightarrow$ Measurement. Before proceeding, we consider it important to point out a noteworthy behavioral variation observed in ibmq_16_melbourne qubits. In early days, the error-probabilities of device qubit, increased with the length of identity gates sequence. However, since May 4, 2019, this trend has been gradually fading—perhaps due to the systematic improvement in in qubits coherence time—and has now become somewhat difficult to reproduce. Yet, occasional device overuse still results in accelerated decoherence of more vulnerable qubits. Fig-6 shows data triples for various idle time intervals (ranging from single to 250 identity gates). Approximately half of all data triples predate May-4 and remain more or less trend-wise indistinguishable from those of later experiments. Several different subsets of seven qubits participated in the comparison, some of which are listed in the decreasing order of their contribution in the plots:

- $\{0, 7, 2, 11, 12, 8, 4\}$
- $\{1, 3, 7, 13, 11, 6, 5\}$
- $\{13, 12, 11, 3, 7, 6, 5\}$
- $\{13, 12, 11, 3, 8, 6, 5\}$

The figure shows that High-Weight EC provides significant fidelity gain for several values of P_{lw}. More crucially, it keeps logical failure probability below p_e even when $P_{lw} \geq p_e$. In this region, an encircled data point has been selected for deeper insight into the fidelity gain, while its comparison breakdown is shown in the table. The data point is an output of experiment (dated July 6) applying five identity gates to the qubits set



Low Weight Errors		High Weight Errors	
Error Qubit	Prob.	Error Qubits Pairs	Net Prob.
13	0.0083	(12,5), (11,3), (6,8)	0.0584
6	0.0034	(12,11), (5,3), (13,8)	0.048
5	0.1247	(12, 13), (11,8), (6,3)	0.0029
11	0.1635	(12, 6), (13,3), (5,8)	0.0034
8	0.0046	(12, 3), (13,6), (5,11)	0.0638
3	0.1069	(12, 8), (5,6), (13,11)	0.0035
12	0.0545	(13,5), (6,11), (3, 8)	0.0037
None	0.3479	Undetectable Logical Z -Errors	0.0019

Low Weight EC Failure Prob. at L is 0.186
High Weight EC Failure Prob. at H is 0.032

Figure 6. (Color online) High-Weight error-correction lowers the failure probability of $[[7,1,3]]$ encoded qubit in logical $|+\rangle$ state as it undergoes sequence of Identity gates (consisting of 1—250 gates). While Low-Weight EC becomes counterproductive ($P_{lw} > p_e$) after the cross-over point (intersection between p_e and P_{lw} trend-lines), High-Weight EC continues to keep P_{hw} lower than p_e before eventually converging to p_e at the end. Logistics of plotting the graph and calculations of probabilities remain the same as those described in Fig-4. The table shows breakdown of failure probabilities of encircled data points

$\{13, 12, 11, 3, 8, 6, 5\}$. In this case, the elevated likelihood of High-Weight errors can be ascribed to the joint failure of qubits selected from the subset $\{11, 5, 3\}$ containing three noisier qubits. The table shows that correcting logical operand for errors on qubit pairs (11,5),(11,3) and (3,5), in place of those on qubits 8, 13 and 6 delivers nearly six fold reduction in logical failure probability.

A crucial constraint in the logical memory experiment setup was the mitigation of readout noise due to the inclusion of several high state initialization and Measurement error encoding qubits (for example qubits: 1,3,7 and 11). If these qubits had been directly (destructively) Measured, the likely read-out inaccuracy would have artificially raised the joint failure probability of two (or more) qubits. We solved this problem by deploying unused qubits for indirectly (non-destructively) Measuring dark shaded qubits (Fig-3) with higher accuracy. Fortunately, these auxiliary qubits (e.g. 0,2,8 and 10) contain lower state initialization/Measurement noise and can reliably replicate phase-error from memory (identity) gate qubits through the CNOT gate (whose control operand is the auxiliary qubit initialized in the $|+\rangle$ state, the memory qubit acts as target operand). A good indicator of reduction in readout noise is the decrease in P_{lw} since inflated high-weight error probability is discounted. Therefore, non-destructive

Measurements were applied whenever reduction in P_{lw} was possible. It lowers the failure probabilities in several triples including $(P_{hw} = 0.0625, p_e = 0.125, P_{lw} = 0.18)$ for the experiment containing memory qubits set $\{1, 12, 11, 3, 7, 6, 5\}$. In this case, auxiliary qubits: 0, 13, 10, 2 and 8 destructively Measure memory qubits: 1,12,11,3 and 7 respectively, reducing triple to $(P_{hw} = 0.045, p_e = 0.098, P_{lw} = 0.109)$. Yet, High-Weight EC continues to lower the decoherence rate of logical memory.

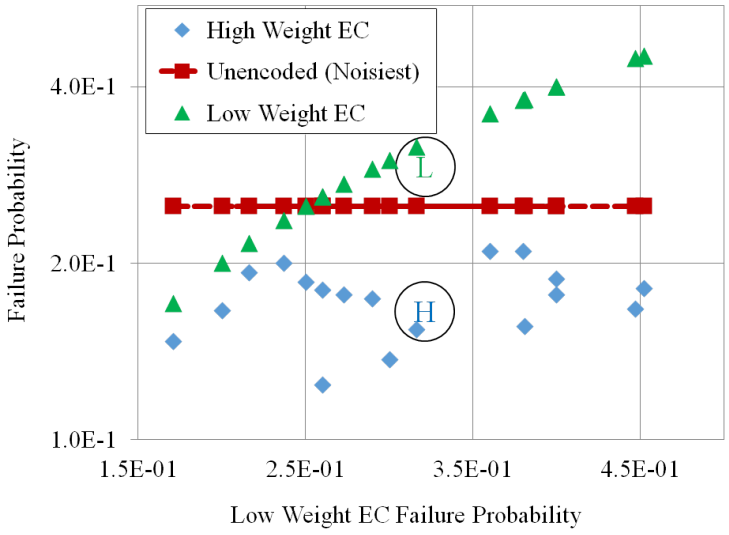
Finally, it should be noted that Qiskit readout noise compensation routines can be used to further suppress the readout noise. Preliminary comparative analysis reveals that enhanced noise reduction lowers all the curves in Fig-6 by approximately the same factor and does not introduce meaningful change in their overall trends. Since the principle advantage of High-Weight EC remains intact, therefore, these plots become somewhat superfluous and have been excluded from the manuscript.

4.3. State-Preparation and Measurement of Logical $|+\rangle$, $|-\rangle$ States

The last set of experiments describes the role of two-qubit error correction in distinguishing between Steane $|+\rangle$ and $|-\rangle$ states prepared on ibmq_16_melbourne. Immediately after its preparation, the encoded state was transversally readout in X-basis using Steane type Measurement. The resulting seven bits string—a noisy codeword of $[7, 4, 3]$ Hamming code—is error-corrected and decoded to reveal outcome of the Measurement. A mismatch between prepared encoded state and Measurement outcome was counted as logical error. The probability of logical error was computed from the fraction of experimental runs ending in the mismatch. Higher logical error probability value increases the likelihood misinterpreting the encoded state. Hence, our ability to distinguish between the logical $|+\rangle$,$|-\rangle$ states, determines the magnitude of logical phase-flip noise gathered by the encoding circuit [19].

Fig-A3 shows circuit for encoding $|+\rangle$ state. Once mapped to ibmq_16_melbourne hardware, it has one CNOT gate on non-adjacent qubits 9 and 12 (see Fig.A3(a)), which requires translation with the help of SWAP gates in order to comply with qubit-qubit connectivity constrains. After reordering the gates in original circuits and canceling some CNOT gates with those in the SWAP gates, the optimized circuit was obtained (Fig.A3(b)) and executed on the hardware. This optimization was powered by the commutation property of gates in the original circuit, that is, all CNOT gates commute with one another and can be scheduled in any arbitrary order. It is worth noting that in comparison with the circuit compiled by the Qiskit, our optimized circuit contains significantly fewer overall CNOT gates. The Fig-7 provides execution results of the optimized circuit for the comparison between two error-correction strategies.

Due to the non fault-tolerant nature of the circuit, logical failure probabilities of encoded state have acquired expectedly large values. Unlike transversal construction of logical CNOT and Memory, the non fault-tolerant state preparation allows error on single encoding qubit to transform into errors on encoding qubits, eventually causing



Low Weight Errors		High Weight Errors	
Error Qubit	Prob.	Error Qubits Pairs	Net Prob.
5	0.429	(4,10), (11,3), (9,12)	0.0074
12	0.0156	(10,11), (3,4), (5,9)	0.0512
4	0.0393	(5, 10), (9,11), (3,12)	0.0214
11	0.018	(10,12), (3,5), (4,9)	0.0764
9	0.0289	(3, 10), (5,12), (4,11)	0.0522
3	0.0343	(9, 10), (4,12), (5,11)	0.0383
10	0.0156	(4,5), (11,12), (3, 9)	0.0565
None	0.102	Undetectable Logical Z-Errors	0.013

Low Weight EC Failure Prob. at L is 0.316
High Weight EC Failure Prob. at H is 0.154

Figure 7. (Color online) High-Weight EC reduces Steane $|+\rangle$, (or $|-\rangle$) SPAM failure probability below the reference physical qubit SPAM error probability reference labeled as Unencoded (Noisiest). The reference was set to highest SPAM error probability of all the encoding qubits, averaged over seven sampling days. Each plotted data point represents the median failure probability of three experimental results. Each result consisted of Measurement statistics collected from 8192 executions(shots) of the same logical CNOT circuit. For the encircled data points, the syndrome-wise comparison between single-qubit error and their corresponding two-qubit errors, is given in the table (all errors in each row yield same syndrome value).

uncorrectable error. The *noisiest* encoding qubit, therefore, crucially determines the fate of decoding outcome, hence, the logical failure probability. For State Preparation And Measurement (SPAM) of logical qubit, we benchmark error-correction schemes by setting our reference to the error probability of the noisiest encoding qubit, instead of *average* error probability of encoding qubits, used for logical operations. However, a meaningful comparison requires us to juxtapose logical qubit SPAM failure probability with physical qubit SPAM error probability. Therefore, the criterion of selecting noisiest qubit eventually restricts us to select encoding qubit with highest SPAM error probability. The plotted data points are obtained from experiments executed in the last two months. In this period, the highest SPAM error probability in ibmq_16_melbourne hardware has remained more or less stable (mean value = 0.26 with std = 0.013). This value was obtained from the runs of Qiskit quantum state tomography routines on seven different days for qubits initialized in $|+\rangle, |-\rangle$ logical states. The encoding circuit always contained highest SPAM error qubit for the each data point in Fig-7. The plotted data is obtained from circuits containing only following two sets of encoding qubits:

(i) $\{3, 4, 5, 9, 10, 11, 12\}$

(ii) $\{4, 5, 6, 7, 8, 9, 10\}$

The figure shows that High-Weight EC successfully lowers the logical failure probability below physical noise threshold—the error probability of noisiest qubit encoding qubit. As before, the table sheds detailed insights into a sample (encircled) data points for comparison based on encoding qubits set (i). It shows that correcting the readout result for weight-2 errors for as many as five error syndromes, halves the logical failure probability. The data points in the figure can be loosely classified into two groups, one has fidelity gain (2 or higher) and the other in which fidelity gain is marginally higher than 1. Their corresponding encoding qubits are contained in sets (i) and (ii) respectively. It should be noted that our experiment produced more or less same logical failure probabilities irrespective of the intended logical state to be prepared and decoded. In this vein, data points are evenly split between $|+\rangle$, $|-\rangle$ logical states, although, without explicit labels. Yet, same High-Weight EC strategy was applied to the given encoding qubits set for both logical states.

The encoding circuit was executed without additional verification gates for preventing correlated errors. Therefore, one may be tempted to map unchecked noise correlation onto high-weight errors in this case. To this end, we refer back to the table in Fig-7 and find that high weight errors manifest higher probabilities for the majority of error syndromes (5/7), when contrasted with the previous experiments (only 3/7 error syndromes). This observation alludes to the likely connection between noise correlation and elevated probability of the two-qubit errors, although precise share of correlation needs more investigation and remains integral part of our future research.

5. Background and Previous Work

The theory of fault-tolerant quantum computation [30] enables error correction to lower decoherence rate of the encoded qubit by preventing faulty gate operations to accumulate errors on the encoding qubits. Founded on the assumptions that qubit-environment interaction keeps decoherence rate per qubit below certain limit [1, 4] and confines errors to exponentially small subset of qubits, it has naturally steered conventional error-correction schemes towards correcting logical qubit for small number of encoding qubits in errors—the defining attribute of the local noise model [4, 48]. Unfortunately, real quantum hardware invalidate these assumptions by significantly raising decoherence levels among certain qubits and elevating joint probability of noisier qubits in error [50]. Such behavior is clearly visible in qubits error probability distribution shown in Fig-1.

For a distance $d = (2d_e - 1)$ code, an occurrence of errors on d_e or more codeword qubits likely belongs to a set of uncorrectable error events that result in the incorrect decoding of faulty qubits, followed by undetectable alteration of the logical qubit state during recovery phase. If a quantum hardware distributes decoherence rates unevenly among the encoding qubits, the likelihood of logical qubit failure is at least the joint probability of d_e noisiest qubits failing to escape uncorrectable errors. For example, the logical qubit protected by the phase-flip code (Fig-1) has logical failure probability dictated by elevated likelihood of errors on frequently failing qubit pairs (1,11 in

experiment (a)) and (4,5 in experiment (b)). Whenever this joint failure probability exceeds physical qubit error probability, the encoding can only increase decoherence rate of logical qubit. That is when error-correction becomes counterproductive by gathering errors faster than the rate of their correction. To date, despite numerous efforts of realizing small-size fault-tolerant logical qubits [39, 34, 46] (when $d \leq 3$), practical error-detection [12, 28, 43] and correction [13, 41, 23] have shown qualified success in counteracting arbitrary noise patterns in real quantum computers.

Thus, it comes as no surprise that only a few studies have attempted to evaluate fault-tolerance on recently showcased quantum computing devices that can easily fit Gottesman's $[[4, 2, 2]]$ encoded qubit [21]. Among these studies, even fewer [49, 35, 22, 47] have managed to show that encoded qubits and gates exhibit higher fidelity. However, Gottesman's $[[4, 2, 2]]$ being an error-detecting code, finds limited applications in a more realistic scenario in which logical qubit can only be discarded upon final read-out instead of on each occasion when an error has been detected. For practical purposes, error-correction, active [44] or passive [24], is expected to remain an indispensable tool of increasing longevity of the logical qubit. The latter form of error-correction is a contemporary pragmatic concept wherein qubit-environment interaction is carefully engineered [25] so that the occurrence of multi qubit errors (e.g. two photon loss in Ref [34]) helps preserve logical qubit state. Ideas presented in our study partly shares the theme of passive error-correction in a sense that higher likelihood of certain multi-qubit errors can improve our ability to discriminate between orthogonal encoded qubit states, which lowers logical noise level.

6. Conclusion

Error correction is an indispensable tool of protecting quantum information from noise. In this paper we presented a novel approach of error-correction, that convert errors into non-trivial code space Stabilizers. It allows quantum error-correcting codes to correct longer strings of errors contrary to what has been previously envisioned. The efficacy of proposed approach was validated by experiments on IBMQ quantum processor executing [[7, 1, 3]] noisy logical gates. These experiments were designed to indirectly infer probability distribution of errors in the logical gate operand, from the Measurement of encoding qubits after the application of gate. Remarkably, these qubits were not required to encode experimentally infeasible [[7, 1, 3]] logical state, instead, their initialization in an equal superposition state sufficed. In this sense, the logical state-preparation errors were discounted from distribution; however, errors in qubits initialization logical and Measurements were duly taken into consideration.

In this setting, our experimental results showed that the new approach led logical gate circuit to output intended state with higher probability than the corresponding physical gate. For completeness, we included experiments to analyze error distribution in the complete $[[7, 1, 3]]$ state preparation and Measurement circuits. Their error-statistics were used to examine the efficacy of high-weight error-correction strategy in the non

fault-tolerant circuits. Although our work delineates novel approach of countering noise patterns expected in NISQ era devices, we believe that it merits further investigations on device technologies other than superconductors. In particular, what type of device-specific environments raise high-weight noise floor to justify application of proposed scheme? Apparently, if decoherence rates shrink in future, multi-qubit errors are unlikely to sustain large enough value, unless qubits and gates correlate their errors or establish their interdependencies in some unknown manner. Moreover, fault-tolerant preparation of a logical state, protected by full error-correcting code, has remained a daunting task to date. These and other relevant challenges indeed deserve more insights and tools to achieve fault-tolerance in real quantum processor.

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Table A1. Correcting two-qubit phase-flip errors in $[[7,1,3]]$ code

Two phase-flips errors	Syndrome			Product of the pairs of phase-flips errors
	S_1^X	S_2^X	S_3^X	
(Z_1Z_2),(Z_5Z_6),(Z_4Z_7)	-1	-1	$+1$	$S_1^Z S_2^Z$, S_3^Z, $S_1^Z S_2^Z S_3^Z$
(Z_1Z_5),(Z_2Z_6),(Z_3Z_7)	$+1$	$+1$	-1	$S_1^Z S_2^Z$, S_1^Z, S_2^Z
(Z_1Z_3),(Z_5Z_7),(Z_4Z_6)	$+1$	-1	$+1$	S_1^Z, $S_1^Z S_3^Z$, S_3^Z
(Z_1Z_4),(Z_3Z_6),(Z_2Z_7)	-1	$+1$	-1	$S_1^Z S_3^Z$, S_2^Z, S_1^Z, S_2^Z
(Z_1Z_6),(Z_3Z_4),(Z_2Z_5)	-1	-1	-1	$S_1^Z S_3^Z$, $S_2^Z S_3^Z$, $S_1^Z S_2^Z$
(Z_1Z_7),(Z_2Z_4),(Z_3Z_5)	$+1$	-1	-1	$S_1^Z S_2^Z S_3^Z$, S_1^Z, $S_2^Z S_3^Z$
(Z_2Z_3),(Z_4Z_5),(Z_6Z_7)	-1	$+1$	$+1$	$S_2^Z S_3^Z$, S_2^Z, S_3^Z

Appendix A. Proof-of-Concept High-Weight Error Correction using Distance-3 CSS Codes

A distance-3 CSS code can decode single syndrome into multiple two-qubit errors. These can be corrected by mutually augmenting a pair of these errors to enact Stabilizer on the encoded state. This section exemplifies High-Weight error correction using Steane $[[7,1,3]]$, Bacon-Shor $[[9,1,3]]$ and Kitaev $[[13,1,3]]$ surface code.

Appendix A.1. Steane $[[7,1,3]]$ *code*

The Steane code [8, 45], non-degenrate by design, can correct for arbitrary two-qubit errors. It confines logical qubit within the Stabilizer space spanned by six Stabilizers: $S_1^X : X_1X_3X_5X_7$; $S_2^X : X_2X_3X_6X_7$; $S_3^X : X_4X_5X_6X_7$; $S_1^Z : Z_1Z_3Z_5Z_7$; $S_2^Z : Z_2Z_3Z_6Z_7$; $S_3^Z : Z_4Z_5Z_6Z_7$. While correcting weight-2 errors, it becomes a degenerate code; the product of any two co-syndrome errors constitutes the Stabilizer operation on the code space. Table-A1 enumerate all possible weight-2 phase-flip errors. Each row lists degenerate errors along with their combinations leading to the non-trivial Stabilizers (trivial Stabilizers are omitted). Since all two-qubits bit- and phase-flip errors are shown to be corrected, therefore, Steane $[[7,1,3]]$ code corrects arbitrary two-qubit phase-flip errors. Likewise, it can be easily shown that it also corrects arbitrary two-qubit bit-flip errors.

Table A2. Gauge operators of $[[9,1,3]]$ Bacon-Shor code

X-Gauge operators		Z-gauge operators	
$G_{1,4}^X = X_1X_4$	$G_{2,5}^X = X_2X_5$	$G_{1,2}^Z = Z_1Z_2$	$G_{4,5}^Z = Z_4Z_5$
$G_{4,7}^X = X_4X_7$	$G_{5,8}^X = X_5X_8$	$G_{2,3}^Z = Z_2Z_3$	$G_{5,6}^Z = Z_5Z_6$

Appendix A.2. Bacon-Shor $[[9,1,3]]$ *code*

The nine-qubits Bacon-Shor code is a sub-system code [5] containing four stabilizers: $S_1^X : X_1X_2X_3X_4X_5X_6$, $S_2^X : X_4X_5X_6X_7X_8X_9$, $S_1^Z : Z_1Z_2Z_4Z_5Z_7Z_8$, $S_2^Z : Z_2Z_3Z_5Z_6Z_8Z_9$. It encodes five logical qubits; one belongs to the *system*, used for storage and computation, while the rest comprise sub-system [3]. The state of system qubit remains unaffected by the applying logical X and Z gates to sub-system qubits. The Measurement of these logical operators, provides redundant means of syndrome extraction that gauges system for the presence of likely errors. The sub-system qubits are gauge qubits and their corresponding logical Pauli operations are gauge operators [3], listed in Table-A2. These can be leveraged to simplify the error correction procedure, might it be Low-Weight or High-Weight by nature. In latter case, these gauge operators compensate for the weight deficit when a pair of two-qubits errors to completes weight-6 Stabilizers. For Bacon-Shor code, the task of completing the code space stabilizer becomes a task of completing the its Stabilizer(s) modulo gauge operators.

A small subset of correctable two-qubits phase-errors are listed in Table-A4. It shows both the Stabilizers and concomitant gauge operators which become prominent when the pair of errors only enacts trivial Stabilizers on the code space (e.g. when $S_1^X = +1$ and $S_2^X = -1$). In general, these pairs comprise non-trivial Stabilizer upto appropriately chosen gauge operators. Finally, note that the table contains only handful of errors to exemplify proof-of-concept generalized error correction. However, like Steane code, it can be shown that one can correct arbitrary two-qubit errors in the Bacon-Shor code as well.

Table A3. Correcting two-qubit phase-flip errors in $[[13,1,3]]$ code

Two phase-flips errors	Syndrome						Product of the pairs of two phase-flips errors
	S_x^1	S_x^2	S_x^3	S_x^4	S_x^5	S_x^6	
(Z_4Z_6), (Z_7Z_9)	+1	-1	+1	-1	+1	+1	S_Z^3
(Z_4Z_9), (Z_6Z_7)	-1	-1	+1	-1	-1	+1	S_Z^3
(Z_4Z_9), (Z_6Z_9)	-1	+1	+1	+1	-1	+1	S_Z^3
(Z_5Z_7), (Z_8X_{10})	+1	+1	-1	+1	-1	+1	S_Z^4
(Z_5Z_{10}), (Z_7X_8)	+1	-1	-1	+1	-1	-1	S_Z^4
(Z_5Z_8), (Z_7Z_{10})	+1	-1	+1	+1	+1	-1	S_Z^4
(Z_9Z_{11}), $(Z_{10}Z_{13})$	+1	+1	+1	+1	-1	+1	$S_Z^5S_Z^6$
(Z_9X_{10}), $(X_{11}X_{13})$	+1	+1	+1	-1	+1	-1	$S_Z^5S_Z^6$
(Z_9Z_{13}), $(Z_{10}Z_{11})$	+1	+1	+1	-1	-1	-1	$S_Z^5S_Z^6$
(Z_1Z_3), (Z_4Z_5)	-1	+1	-1	+1	+1	+1	$S_Z^1S_Z^2$
(Z_1X_4), (Z_3Z_5)	+1	-1	+1	+1	+1	+1	$S_Z^1S_Z^2$
(Z_1Z_5), (Z_3Z_4)	-1	-1	-1	+1	+1	+1	$S_Z^1S_Z^2$

Table A4. Correcting two-qubit phase-flip errors in $[[9,1,3]]$ Bacon-Shor code

Syndrome	Two phase-flips errors	Stabilizers	Gauge Operators
$S_1^X = +1, S_2^X = -1$	(Z_1Z_4), (Z_2Z_5)	I	$G^Z_{1,2}, G^Z_{4,5}$
	(Z_2Z_5), (Z_3Z_6)	I	$G^Z_{2,3}, G^Z_{5,6}$
	(Z_1Z_5), (Z_3Z_6)	I	$G^Z_{1,2}G^Z_{2,3}G^Z_{5,6}$
$S_1^X = -1, S_2^X = +1$	(Z_5Z_8), (Z_4Z_7)	S^Z_1	$G^Z_{1,2}$
	(Z_5Z_8), (Z_6Z_9)	S^Z_2	$G^Z_{2,3}$
	(Z_4Z_9), (Z_6Z_7)	$S^Z_1S^Z_2$	$G^Z_{1,2}G^Z_{2,3}$
$S_1^X = -1, S_2^X = -1$	(Z_1Z_7), (Z_2Z_8)	S^Z_1	$G^Z_{4,5}$
	(Z_2Z_8), (Z_3Z_9)	S^Z_2	$G^Z_{5,6}$
	(Z_1Z_9), (Z_3Z_7)	$S^Z_1S^Z_2$	$G^Z_{4,5}G^Z_{5,6}$

Appendix A.3. Kitaev $[[13,1,3]]$ *Surface code*

The surface codes [7], known for very high accuracy threshold [18, 15, 18], can efficiently decode errors on the codewords qubits, mapped to a two-dimensional grid, using nearest-neighbor parity check operations. The resulting local Stabilizer Measurements can not only correct less than d_e weight errors, but can also decode high-weight errors on the qubits located sufficiently far apart. In case of High-Weight error-correction, this spatial non-locality conditions resurfaces with far greater importance with crucial implications. On one hand, the local Stabilizer Measurement stipulates that the degenerate errors are located in vicinity to yield the same syndrome. On the other hand, these local errors can string a chain of faults realizing unwanted logical operation on the code space. Thus, while Table-A3 enumerates several correctable two-qubit phase-flip errors which can mutually constitute a Stabilizer operation, Fig-A1 depicts a situation in which a pair of these errors enacts logical-Z operation on the encoded qubit. This counter example shows that surface code [[13, 1, 3]] can only correct a subset of two-qubit errors.

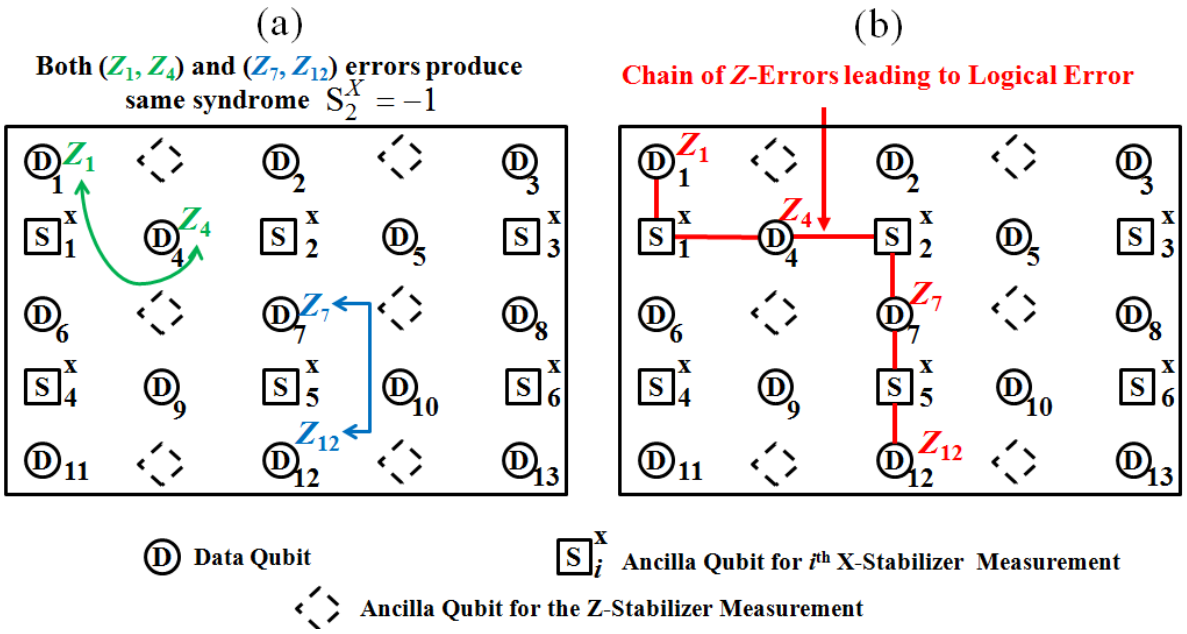


Figure A1. (Color online) A pair of co-syndrome two-qubit errors doesnot constitute Stabilizer operation. Instead, it afflicts logical Z-operation on the codespace. The counterexample example shows that surface code doesnot correct *arbitrary* two-qubit errors

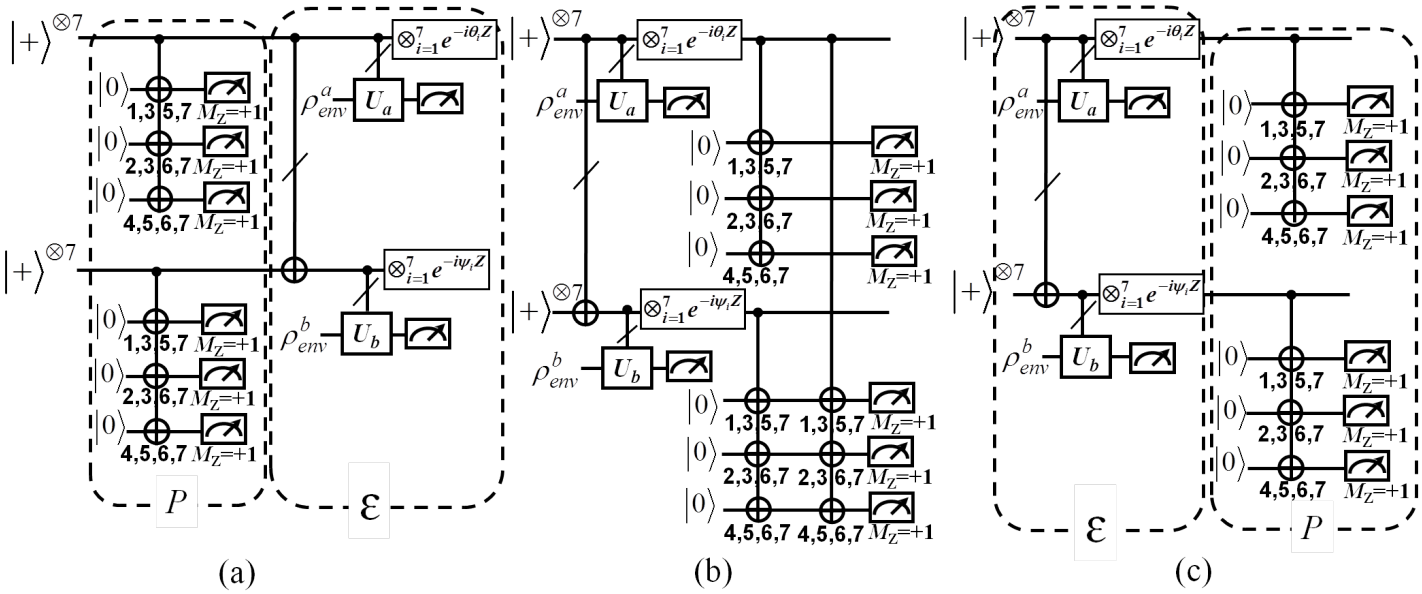
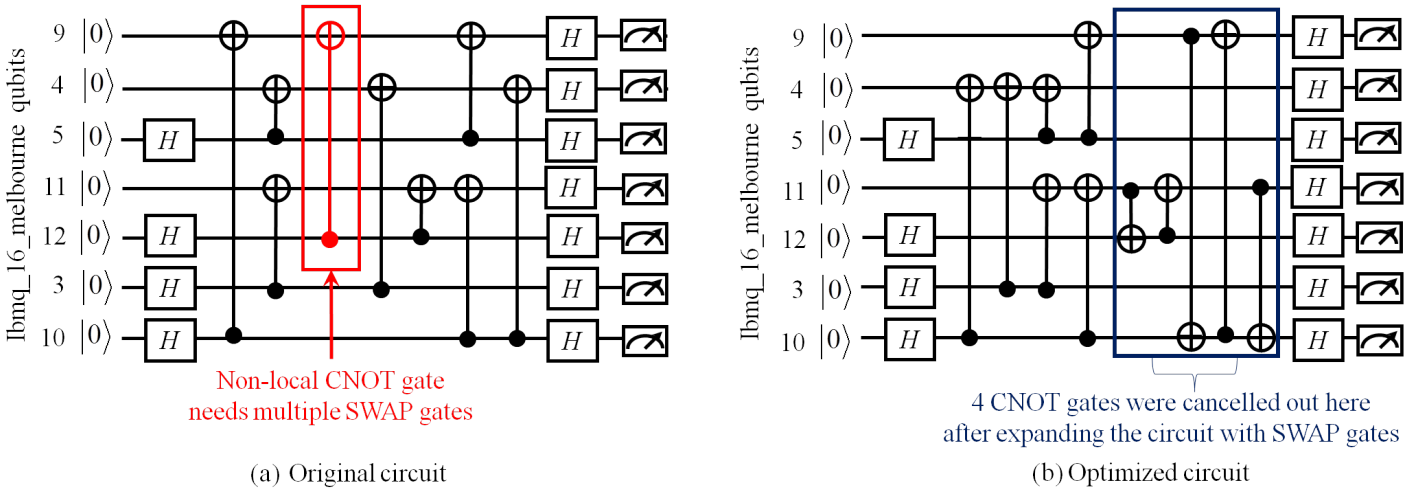


Figure A2. Noise operator commute-back procedure for estimating error probability distribution in the noisy Steane CNOT gate. In (a) the noisy CNOT gate operator ε is applied to the encoded state $|+\rangle$ obtained by projecting superpositon state onto codespace by the projector P. This is equivalent to first applying ε to the superposition state, followed by its projection (by applying P) onto the code-space. We ascribe this reordering is to an important property of CNOT gates: CNOT(op_1, op_2) CNOT(op_2, op_3) = CNOT(op_1, op_3) CNOT(op_2, op_3) CNOT (op_1, op_2) shown in (b). Afterwards, (b) reduces to (c) since P remains unchanged by the superfluous joint projection of both operands onto the codespace. Note that P is considered ideal projection and it is simulated in the classical post-processing, whereas, ε is enacted in quantum hardware



(a) Original circuit

(b) Optimized circuit

Figure A3. (Color online) Steane $|+\rangle$ encoding-decoding circuit. Original circuit (a) contains a CNOT on non-adjacent qubits which requires swapping of qubits. The equivalent optimized circuit (b) obtained by rearranging gates in the original circuit and canceling some of these with those in the SWAP operations. It offers significantly lower gate count compared to that outputted by the Qiskit transpiler. Note that Steane $|-\rangle$ state can be prepared and Measured by the same circuit except that it phase-flip all the qubits before Measuring them in X-basis (Hadamard gates followed by Z-basis Measurement).