

# A Resource-Efficient 4-Qubit Circuit for Bit-Flip Error Correction Using Feynman Gates

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**Abstract:** Quantum systems are inherently prone to errors caused by decoherence, noise, and imperfect gate operations. Effective error correction is essential to preserving quantum information, especially under hardware constraints. In this paper, we present a resource-efficient 4-qubit quantum circuit designed to detect and correct single-qubit bit-flip errors within a 3-qubit data block. The circuit uses Feynman (CNOT) and NOT gates alongside an ancillary qubit to implement full correction logic with minimal overhead. Compared to well-known approaches like the 9-qubit Shor code, our design achieves equivalent fidelity (100%) using fewer qubits, making it highly suitable for near-term quantum devices. Simulation results, obtained using IBM Quantum Composer and Qiskit, confirm the circuit's correctness and reliability across all bit-flip scenarios. The design also introduces a reusable unitary block for efficient implementation. This work offers a scalable and practical solution to quantum error correction using minimal hardware resources.

**Keywords:** ancilla qubit; controlled-NOT gate; quantum error detection; quantum fault tolerance; bit-flip error; quantum circuit design

## 1. Introduction

As we stand on the precipice of a new era in computation, quantum computing emerges not merely as a theoretical marvel but as a transformative technology poised to redefine the landscape of computational power, cryptography, and information processing. Central to realizing the vast potential of quantum computing is the robustness and reliability of quantum information processing. However, quantum systems are inherently sensitive to external disturbances and internal imperfections, leading to errors that can significantly derail computational accuracy and reliability. This fragility underscores the critical importance of quantum error correction circuits, a cornerstone upon which the practical realization of quantum computing rests.

Quantum Error Correction (QEC) circuits are sophisticated mechanisms designed to protect quantum information from the deleterious effects of noise, decoherence, and operational inaccuracies. By encoding the fragile quantum information across multiple qubits and implementing precise correction algorithms, QEC circuits enable the detection and correction of errors without collapsing the quantum state—a feat unattainable in classical computing paradigms. This error correction is pivotal, not only for maintaining the integrity of quantum computations but also for enabling scalable quantum computing systems capable of solving problems beyond the reach of classical computers.

The development and refinement of QEC circuits thus represent a vital field of research in quantum computing. A robust QEC system can dramatically increase the fault tolerance of quantum computers, paving the way for their application in a wide array of disciplines, from materials science to cryptography and beyond. Among the diverse strategies for quantum error correction, the implementation of circuits utilizing minimal resources, such as fewer qubits or simplified gate operations, is particularly compelling. It promises to enhance the feasibility and efficiency of quantum computing by reducing the overhead required for error correction.

Despite significant advances in quantum error correction, most existing methods such as the Shor code and Surface code [1,2] require a large number of qubits and complex gate arrangements. These approaches, while theoretically

robust, impose substantial resource demands that make them impractical for near-term quantum devices with limited qubit availability and coherence times.

In this context, our study introduces an approach to quantum error correction with a 4-qubit quantum circuit that adeptly identifies and corrects errors within a 3-qubit system, employing a strategic use of Feynman gates and an additional (ancilla) qubit. This design not only demonstrates the practical application of QEC principles but also highlights the potential for optimizing error correction methods to accommodate the constraints of quantum computing systems. By exploring the capabilities and limitations of this circuit, our work contributes to the ongoing quest for more reliable and efficient quantum computing architectures, marking a significant step forward in the journey toward fully realized quantum computing technologies.

It is worth noting that the term Feynman gates is used frequently throughout this article. In quantum computation, the Feynman gate is another name for the controlled-NOT (CNOT) gate. Additionally, the proposed circuit also utilizes the Toffoli gate (or CCNOT gate). These gates are essential in reversible and quantum logic and are often generalized as multi-controlled-NOT operations. In this paper, the term Feynman gates is used in a broad sense to describe both CNOT and multi-controlled-NOT gates used in the construction of the proposed error-correcting circuit. Structure of the Paper: The remainder of this paper is organized as follows. Section 2 presents a review of the current research landscape in quantum error correction. Section 3 outlines the research approach and theoretical basis for the proposed method. Section 4 describes the design and functionality of the proposed 4-qubit error-correcting circuit, broken down into three functional segments. Section 5 discusses the implementation, simulation setup, and results, highlighting the effectiveness and fidelity of the circuit. Section 6 provides a comparative analysis with existing methods, emphasizing resource efficiency. Finally, Section 7 concludes the paper with a summary of findings and directions for future work.

## 2. Related Work

Quantum Error Correction (QEC) is a cornerstone of fault-tolerant quantum computing, essential for preserving quantum information against noise and decoherence. Over the years, several foundational approaches have been proposed.

One of the earliest methods is the repetition code, which redundantly encodes a single qubit state across multiple qubits to detect and correct errors. Newman [3] and implementations by QuTech [4] demonstrated the viability of these simple schemes, though they are generally limited to correcting bit-flip errors and require significant qubit redundancy.

More sophisticated codes, such as the Shor code and Surface Code, can correct both bit-flip and phase-flip errors [1,2,5]. While powerful, these codes typically require 9 or more qubits, complex gate sequences, and high overhead in physical qubits and control systems, making them less suitable for near-term quantum hardware. Steane [6], Preskill [7], and Watrous [8] offer detailed theoretical foundations for these techniques.

Recent works focus on fault-tolerant architectures and efficient simulation tools, such as those by Girvin [9] and Padma Priya et al. [10], which support scalable error correction implementations. Other contributions, like those of Chatterjee et al. [11], provide accessible summaries of QEC principles, while Wootton and Loss [12] explore large-scale repetition codes with 15 qubits.

Despite these advances, a critical limitation persists: high resource requirements. Large-scale codes are not yet feasible on today's limited-qubit quantum processors. This motivates the need for minimal-qubit QEC architectures [13] that can still perform effective correction, particularly for specific error types like bit-flips.

In response, this paper introduces a resource-efficient 4-qubit circuit designed specifically for single-qubit bit-flip correction. By leveraging Feynman (CNOT) and NOT gates along with an ancillary qubit, our approach minimizes overhead while retaining high fidelity, making it highly relevant for near-term quantum computing systems.

### 2.1. Reversible Logic and Its Role in Quantum Error Correction

Reversible logic plays a fundamental role in quantum computing, where all quantum operations must be inherently reversible to preserve unitarity. Unlike classical logic gates such as AND, OR, or NAND, which lose information and increase entropy, reversible gates retain full input-output mapping, making them suitable for quantum implementations.

Quantum gates such as the NOT, Feynman (CNOT), and Toffoli (CCNOT) gates are examples of reversible operations. These gates form the basis of both quantum algorithms and quantum error correction schemes, where reversibility ensures that operations can be undone or corrected without measurement-induced collapse.

In our design, the proposed 4-qubit circuit relies entirely on reversible logic elements. By leveraging CNOT and CCNOT gates, we ensure that the circuit maintains reversibility while enabling deterministic error detection and correction through conditional logic on the qubits.

Reversible computing has also been explored in emerging nanotechnologies such as Quantum-dot Cellular Automata (QCA), where logic elements can be physically implemented with low energy dissipation. Several works in this area, such as [14–16], have demonstrated efficient and low-power designs for reversible gates, comparators, and switching networks using QCA.

Although QCA is a different physical model than gate-based quantum systems, the principles of reversible logic design and modularity apply directly to our circuit. The inspiration from these works reinforces the importance of using compact, low-overhead reversible structures for error correction in quantum computing.

In addition to foundational reversible gate research, recent works have demonstrated the applicability of reversible design principles in nanoscale environments. Other designs, such as a testable QCA full adder and a quantum-based serial-parallel multiplier circuit using efficient nanoscale serial adders, further emphasize the value of modular, fault-tolerant, and power-aware logic construction. These studies reinforce the importance of reversible, compact architectures, a philosophy echoed in the modular structure of our 4-qubit error-correcting circuit.

## 2.2. Note on QCA Clocking

Quantum-dot Cellular Automata (QCA) circuits rely on a specialized four-phase clocking mechanism (Switch, Hold, Release, Relax) to guide signal flow and ensure synchronization. While this model differs from gate-based quantum computing, the design principle of precise, step-wise control in QCA is conceptually aligned with the modular operation of our proposed circuit. This reinforces the value of low-overhead, reversible logic structures in scalable nanocomputing environments.

## 3. Research Approach

To obtain single-qubit correction within a three-qubit cluster is equivalent to developing a quantum circuit with the following truth table shown in Table 1.

**Table 1.** Truth table of the intended operation.

Column1	Column2	Column3
	Input State	Expected Output State
0	$ 000\rangle$	$ 000\rangle$
1	$ 001\rangle$	$ 000\rangle$
2	$ 010\rangle$	$ 000\rangle$
3	$ 011\rangle$	$ 111\rangle$
4	$ 100\rangle$	$ 000\rangle$
5	$ 101\rangle$	$ 111\rangle$
6	$ 110\rangle$	$ 111\rangle$
7	$ 111\rangle$	$ 111\rangle$

If we stick to the 3-qubit layout, then the matrix representation of the operation should be as shown in Table 2.

**Table 2.** Matrix representation of a 3-qubit layout process.

(000 000)	(000 000)	(000 000)	(000 111)	(000 000)	(000 111)	(000 111)	(000 111)
(001 000)	(001 000)	(001 000)	(001 111)	(001 000)	(001 111)	(001 111)	(001 111)
(010 000)	(010 000)	(010 000)	(010 111)	(010 000)	(010 111)	(010 111)	(010 111)
(011 000)	(011 000)	(011 000)	(011 111)	(011 000)	(011 111)	(011 111)	(011 111)
(100 000)	(100 000)	(100 000)	(100 111)	(100 000)	(100 111)	(100 111)	(100 111)
(101 000)	(101 000)	(101 000)	(101 111)	(101 000)	(101 111)	(101 111)	(101 111)
(110 000)	(110 000)	(110 000)	(110 111)	(110 000)	(110 111)	(110 111)	(110 111)
(111 000)	(111 000)	(111 000)	(111 111)	(111 000)	(111 111)	(111 111)	(111 111)

To achieve single-qubit error correction within a 3-qubit system, we first constructed a truth table representing the desired transformation logic, shown in Table 1. This defines the target behavior of the correction mechanism. We then derived the corresponding matrix representation of this process assuming a 3-qubit system (shown in Table 2) and analyzed the matrix resulting from this construction (Table 3). However, as demonstrated, the final matrix is not unitary, meaning that such an operation cannot be physically realized within a 3-qubit quantum system.

**Table 3.** Matrix representation of a 3-qubit layout result.

<b>1</b>	<b>1</b>	<b>1</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>

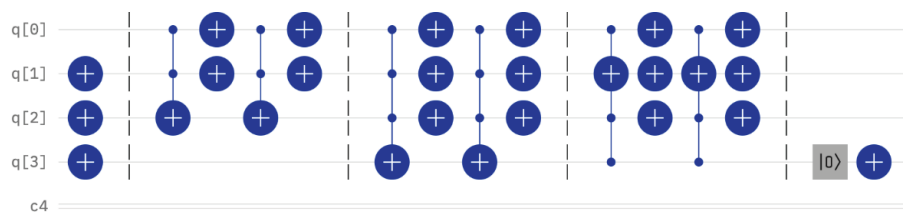
This finding justifies the necessity of extending the system to four qubits, enabling a unitary transformation that performs the desired error correction function. The solution developed in the following sections is based on this expanded 4-qubit architecture.

#### 4. The Proposed Circuit

To facilitate a comprehensive understanding, the proposed circuit has been conceptually divided into three distinct sections (named Part 1, Part 2, and Part 3, in the respective figures). Each section is designed to address specific aspects of the error correction process, thereby simplifying the analysis and implementation of the circuit's functionality. This division not only aids in the elucidation of the circuit's operational dynamics but also highlights the modular approach taken in its design, enabling a step-by-step exploration of its error correction capabilities.

Initially, our focus is on a system comprising three qubits, which may exhibit a single bit-flip error, accompanied by an additional qubit that is consistently initialized to the state  $|1\rangle$ . Within this triplet of qubits, an error manifests as any deviation from the target states—illustratively, configurations such as  $|001\rangle$ ,  $|101\rangle$ , or  $|100\rangle$ . These errors indicate the presence of one erroneous qubit amidst two accurate ones, necessitating a correction to achieve the desired uniform state of either  $|000\rangle$  or  $|111\rangle$ .

The circuit's architecture is strategically partitioned into three segments, with the first two (Figure 1, Figure 2) primarily dedicated to detecting and rectifying errors within the three-qubit ensemble, assuming the presence of an error. Conversely, should the input state already match one of these correct configurations ( $|000\rangle$  or  $|111\rangle$ ), the initial segments inadvertently generate an incorrect output—a discrepancy rectified by the circuit's third and final segment (Figure 3), ensuring the integrity of the output, regardless of the input's initial correctness.

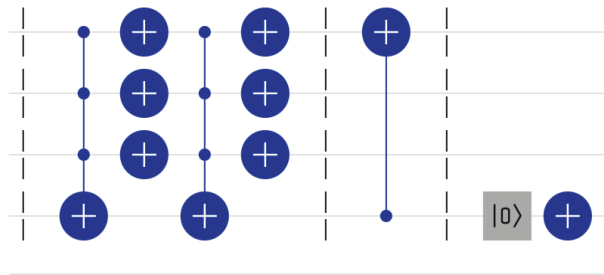


**Figure 1.** Gate-Level Diagram—Part 1 of the Proposed Error Correction Circuit (Correction of  $q[2]$  and  $q[1]$ ).

In the initial stage of the circuit's operation (Figure 1), we proceed under the presumption of an existing error. The correction process begins with qubit  $q[2]$ , the third in the sequence. This correction is contingent upon the first two qubits,  $q[0]$  and  $q[1]$ , exhibiting identical states. The deployment of multiple NOT gates throughout the circuit alters qubit states as necessary, facilitating conditions under which the Toffoli gate can be activated with both control qubits set to  $|1\rangle$ .

Subsequently, the state of the auxiliary qubit is adjusted to  $|0\rangle$ , but only when the circuit achieves one of the predefined correct outputs, either  $|000\rangle$  or  $|111\rangle$ . Should the circuit's output deviate from these targets, the auxiliary qubit retains its initial state of  $|1\rangle$ .

Completing the first segment of part 1 of the circuit, we address the correction of qubit  $q[1]$ , the second in the sequence. This step again operates on the assumption of an error's presence. The criterion for this correction is twofold: firstly, qubits  $q[0]$  and  $q[2]$  must match in state, secondly, the auxiliary qubit must remain in the state of  $|1\rangle$ . At the end of part 1, the auxiliary qubit is set to state  $|1\rangle$ .



**Figure 2.** Gate-Level Diagram—Part 2 of the Proposed Circuit (Verification and Adjustment of  $q[0]$ ).

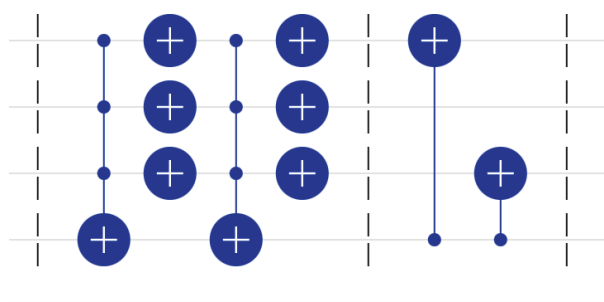
In the subsequent phase, the circuit undergoes a verification process to ascertain whether the target states,  $|000\rangle$  or  $|111\rangle$ , have been successfully achieved (Figure 2). Should the circuit be in one of these desired configurations, the auxiliary qubit is set to the state  $|0\rangle$ . Otherwise, the state of the auxiliary qubit remains at  $|1\rangle$ , reflecting its status following the completion of the first segment.

This stage introduces the use of a Controlled NOT (CNOT) gate to modify the state of the first qubit,  $q[0]$ , but only under the condition that the circuit has not yet reached its target states, which means the auxiliary qubit maintains its state at  $|1\rangle$ . This mechanism ensures that any remaining discrepancies are addressed, aligning the circuit closer to its intended outcome.

By the conclusion of this second segment, the circuit is designed to have rectified any initial errors, thereby aligning its output to one of the predetermined correct states,  $|000\rangle$  or  $|111\rangle$ , given that the input possessed an error. At the end of part 2, the auxiliary qubit is set to state  $|1\rangle$ .

As delineated in the preceding sections, should the initial state of the circuit exhibit an error, it will be rectified by the conclusion of the second segment. However, in scenarios where the input state was already correct, the interventions made in the first two segments inadvertently introduce inaccuracies, resulting in a misleading final output. Specifically, a correct input such as  $|000\rangle$  or  $|111\rangle$  undergoes unintended alterations, yielding  $|101\rangle$  and  $|010\rangle$ , respectively, after the first two parts. This occurs due to the system's error-correction mechanism acting upon an already accurate configuration, mistakenly identifying it as flawed.

To rectify this case, the third and final segment of the circuit (Figure 3) plays a critical role. It preserves the state of the auxiliary qubit at  $|1\rangle$  should the circuit not yet align with its target states of  $|000\rangle$  or  $|111\rangle$ . Leveraging a Controlled NOT (CNOT) gate, it then proceeds to adjust the first and last qubits, effectively correcting the previously induced errors. Conversely, if the circuit's output after the first two parts is already correct, the auxiliary qubit's state transitions to  $|0\rangle$ , thereby neutralizing the potential impact of the CNOT gates on the circuit's state.



**Figure 3.** Gate-Level Diagram—Part 3 of the Proposed Circuit (Final Correction Based on Auxiliary State).

This strategic arrangement ensures that by the end of the third part (Fig. 3), irrespective of the input's initial condition—whether erroneous or accurate—the circuit invariably converges to one of the desired states,  $|000\rangle$  or  $|111\rangle$ . This design highlights the circuit's comprehensive error-correction capability, meticulously addressing both actual and induced errors to achieve faultless quantum computation.

### *Error Correction Logic Overview*

The proposed circuit assumes that only a single bit-flip error occurs on one of the three data qubits ( $q[0]$ ,  $q[1]$ ,  $q[2]$ ). The auxiliary qubit ( $q[3]$ ), initialized to  $|1\rangle$ , serves both as a trigger and an indicator during the error correction process.

The core logic operates as follows:

In Part 1, the circuit uses Toffoli gates to correct  $q[2]$  if  $q[0] = q[1]$ , then attempts to correct  $q[1]$  if  $q[0] = q[2]$  and  $q[3] = |1\rangle$ .

In Part 2, it checks whether the corrected output matches target states  $|000\rangle$  or  $|111\rangle$ , and adjusts  $q[0]$  if needed.

In Part 3, it compensates for false positives from earlier stages and ensures the output settles into either  $|000\rangle$  or  $|111\rangle$ .

Example Case –  $|001\rangle$  to  $|000\rangle$ :

For the input  $|001\rangle$  (where  $q[2]$  is flipped), the logic identifies that  $q[0] = q[1] = |0\rangle$ , and triggers the Toffoli gate to flip  $q[2]$  from  $|1\rangle$  to  $|0\rangle$ . The circuit then confirms the corrected state and preserves the result through the remaining stages.

### *Figures 1–3 Analysis*

Figure 1–Part 1 of the Circuit

Figure 1 illustrates Part 1 of the proposed circuit, where the initial error correction process begins. It shows the gate configuration responsible for correcting qubit  $q[2]$ , followed by  $q[1]$ , using Toffoli gates conditioned on the matching state of the other two data qubits. This segment assumes the presence of an error and prepares the system for subsequent verification.

Figure 2–Part 2 of the Circuit

Figure 2 presents Part 2 of the circuit, which functions as a verification stage. It adjusts the auxiliary qubit based on whether the system has reached a valid output state ( $|000\rangle$  or  $|111\rangle$ ). If not, additional correction is applied to  $q[0]$  using a CNOT gate, ensuring proper alignment of all data qubits.

Figure 3–Part 3 of the Circuit

Figure 3 depicts Part 3 of the circuit, which serves to reverse unintended modifications introduced by Parts 1 and 2 when the input state was already correct. It performs a conditional correction using the auxiliary qubit to finalize the system's output, guaranteeing convergence to  $|000\rangle$  or  $|111\rangle$  regardless of initial state correctness.

#### *4.1. Unitary Optimization of Repeated Subcircuit*

The full 4-qubit circuit includes a substructure that appears identically across all three main segments of the design. This repeated block involves a sequence of Feynman (CNOT) and NOT gates acting on all four qubits, as illustrated in Figure 4.

To simplify the circuit representation and improve simulation efficiency, we precomputed the unitary matrix of this sub-circuit. Since unitary operations are composable and reversible, this allows the repeated gate sequence to be replaced by a single named unitary operation, significantly reducing visual and computational complexity.

Let UR denote the unitary matrix representing this repeated block. Then, the overall circuit can be expressed as a composition of unitary submodules:

$$U_{\text{Total}} = U_3 \bullet U_2 \bullet U_1$$

where  $U_1$ ,  $U_2$ ,  $U_3$  each include the UR module within their structure (Figure 1, Figure 2, Figure 3).

The computed UR matrix is shown below (Table 4):

**Table 4.** Substructure-Block Unitary Matrix.

0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

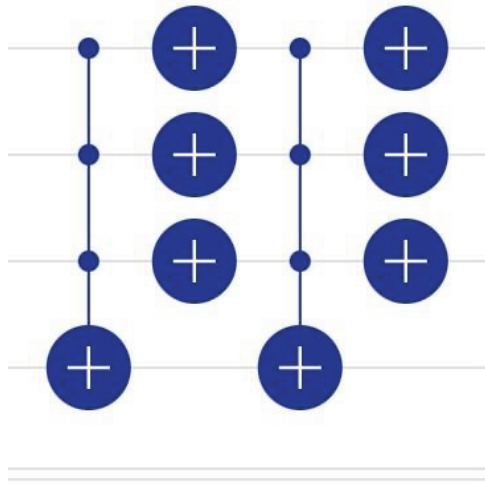
*Figures 4 and 5 Analysis*

Figure 4—Repeated Subcircuit Block

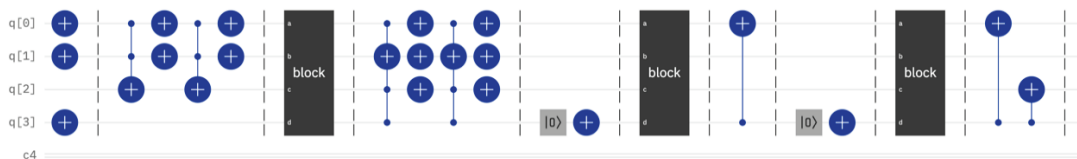
Figure 4 shows the repeated subcircuit block composed of CNOT and NOT gates. This block is used identically in all three main parts of the full circuit and was isolated to enable modular analysis and optimization.

Figure 5—Unitary Matrix of the Subcircuit

Figure 5 presents the  $16 \times 16$  unitary matrix UR representing the repeated subcircuit shown in Figure 4. This matrix confirms that the subcomponent performs a valid unitary transformation, supporting its use as a reusable logic block within the overall architecture.



**Figure 4.** Repeated Subcircuit Block (Used in All Three Parts of the Circuit).



**Figure 5.** Block Diagram of the Full 4-Qubit Bit-Flip Error Correction Architecture.

## 4.2. Methodology for Computing the Unitary Matrix

To validate the functionality and isolate the behavior of the repeated subcircuit block, we computed its unitary matrix and truth table using Qiskit, a widely used open-source framework for quantum computing.

The specific block was extracted from the full circuit design and modeled independently within the Qiskit environment. Using the Operator and Quantum Circuit modules, Qiskit allows the conversion of any quantum circuit into its corresponding unitary matrix representation.

The following steps were taken:

The repeated gate block was defined using Qiskit’s graphical interface (Quantum Composer) and exported to a Qiskit script.

The unitary matrix was obtained using:

```
from qiskit.quantum_info import Operator
unitary_matrix = Operator(circuit).data
```

Additionally, the circuit’s truth table was generated to confirm its behavior across all possible input basis states (Table 5).

**Table 5.** Substructure-Block Truth Table.

Column1	Column2	Column3
Row	Input State	Output State
R1	0000	1000
R2	0001	0001
R3	0010	0010
R4	0011	0011
R5	0100	0100
R6	0101	0101
R7	0110	0110
R8	0111	1111
R9	1000	0000
R10	1001	1001
R11	1010	1010
R12	1011	1011
R13	1100	1100
R14	1101	1101
R15	1110	1110
R16	1111	0111

## 4.3. Block-Based Representation of the Full Circuit

To improve the readability and modular structure of the complete 4-qubit error-correcting circuit, the repeated subcircuit discussed in Sections 4.1 and 4.2 was encapsulated into a unitary block. This approach not only reduces visual complexity but also highlights the logical repetition and internal consistency of the design. Figure 5 illustrates the full circuit structure, where each instance of the reusable unitary subcircuit is represented as a compact block module. This abstraction was implemented in IBM Quantum Composer, and the unitary behavior of each block was confirmed via Qiskit.

## 5. Simulation and Results

To evaluate the effectiveness of the proposed 4-qubit error-correcting circuit, simulations were conducted using IBM Quantum Composer, a graphical design and testing environment integrated with the Qiskit framework. This tool enabled the visual construction and testing of quantum circuits on the QASM simulator, allowing for clear observation of state evolution and measurement outcomes.

### 5.1. Simulation Setup

The circuit was constructed using IBM Quantum Composer’s visual interface, employing Feynman (CNOT), NOT, and Toffoli gates along with measurement components. Simulations were executed on the QASM simulator, which supports state vector fidelity analysis and probabilistic behavior modeling.

## 5.2. Evaluation Method

For each test case, a 3-qubit system was initialized in a correct state  $|000\rangle$  or  $|111\rangle$ . A single bit-flip error was manually introduced to one of the three data qubits. The full 4-qubit circuit, including the ancillary qubit, was applied to **perform** error detection and correction. The outcomes were compared to the target states to measure fidelity and correctness.

Metrics recorded:

- Detection Accuracy: Whether the ancillary qubit accurately flagged the presence or absence of an error.
- Correction Fidelity: The overlap between the circuit’s output and the original uncorrupted state.
- Error Types Simulated: All possible single-qubit bit-flip cases.

## 5.3. Results

To systematically evaluate the performance of the proposed circuit, we tested all possible input states corresponding to valid and single-bit-flip error configurations. Table 6 summarizes the results of these simulations, detailing the original error states, the expected corrected states, and the corresponding detection accuracy and correction fidelity obtained through 1024 measurement shots per scenario using the IBM QASM simulator.

**Table 6.** Simulation results showing fidelity comparison across all test cases.

Error State	Target State	Detection Accuracy	Correction Fidelity
$ 001\rangle$	$ 000\rangle$	100%	100%
$ 010\rangle$	$ 000\rangle$	100%	100%
$ 100\rangle$	$ 000\rangle$	100%	100%
$ 110\rangle$	$ 111\rangle$	100%	100%
$ 101\rangle$	$ 111\rangle$	100%	100%
$ 011\rangle$	$ 111\rangle$	100%	100%
$ 111\rangle$	$ 111\rangle$	100%	100%
$ 000\rangle$	$ 000\rangle$	100%	100%

## 5.4. Fidelity Analysis

In the context of quantum error correction, fidelity is a critical metric that quantifies the similarity between the corrected output state and the intended target state. Mathematically, for pure states  $|\psi\rangle$  and  $|\phi\rangle$ , fidelity is defined as:

$$F = |\langle\psi|\phi\rangle|^2$$

Based on this mathematical definition, if the states  $|\psi\rangle$  and  $|\phi\rangle$  are the same, then  $F = 1 = 100\%$ .

In our simulations, fidelity was estimated based on output measurement statistics from the IBM Quantum Composer. The circuit was tested on the QASM simulator with 1024 measurement shots per input state. For each error scenario, the fidelity was computed as the ratio of the number of correct output results to the total number of measurements:

$$F = (\text{Total shots}) / (\text{Number of correct outputs})$$

In all tested cases—including single bit-flip errors on any of the three data qubits or no errors at all the circuit consistently produced 100% correct outputs, indicating perfect fidelity under ideal simulation conditions. This confirms that the proposed 4-qubit architecture reliably restores the original quantum state in the presence of single-qubit bit-flip errors.

## 5.5. Discussion

The circuit demonstrated consistent and perfect error correction across all tested single-bit-flip scenarios. Fidelity reached 100% in each case, confirming the reliability and correctness of the proposed architecture under ideal simulation conditions. The use of only four qubits—which is the absolute minimum as we showed theoretically—highlights the circuit’s potential for near-term, hardware-constrained quantum processors.

Furthermore, its modular design and low gate complexity make it suitable for future extension to handle more complex error types.

## 6. Comparison with Existing Methods

To assess the practical advantages of the proposed 4-qubit error-correcting circuit, we conducted a comparative analysis with established quantum error correction approaches, focusing on resource usage, gate complexity, and error detection capabilities. Table 7 presents a comparison between the proposed circuit and standard techniques such as the 9-qubit Shor code and 7-qubit Steane code.

The comparison (Table 7) highlights the significant reduction in required qubits and gate complexity offered by our design, without sacrificing error correction accuracy for single-qubit bit-flip errors. This makes the circuit highly suitable for implementation on near-term quantum devices with limited resources.

**Table 7.** Comparison of Error-Correcting Circuit Approaches.

Feature	Proposed Circuit	Shor Code (9-Qubit)	Steane Code (7-Qubit)
Total Qubits Required	4	9	7
Correctable Error Types	Bit-flip	Bit + Phase	Bit + Phase
Ancilla Qubits Used	1	$\geq 3$	$\geq 2$
Gate Types Used	CNOT, NOT	CNOT, H, S, T	CNOT, H, S, T
Circuit Depth (approx.)	Low	High	High
Implementation Complexity	Low	High	High
Detection Accuracy (simulated)	100%	100% (theoretical)	100% (theoretical)
Fidelity (ideal simulation)	100%	100%	100%
Simulation Tool Used	IBM Composer	Theoretical	Theoretical

Recent advances in hardware-efficient design techniques, particularly in QCA and quantum-dot-based computing, highlight the growing need for fault-tolerant circuits with minimal complexity. Works such as [17–20] have explored scalable, low-cost architectures for logic operations and data processing in nanoscale environments. Although these approaches differ in physical implementation, the underlying design philosophy aligns with our proposed 4-qubit architecture—emphasizing minimal overhead and practical implementability.

### 6.1. Percentage Improvement

Compared to the 9-qubit Shor code, the proposed circuit achieves equivalent fidelity using 55% fewer qubits ( $(9 - 4) / 9 * 100 = 55\%$ ), with a simpler gate structure and reduced circuit depth.

### 6.2. Advantages of the Proposed Circuit

Compared to classical approaches such as the 9-qubit Shor code and 7-qubit Steane code, the proposed 4-qubit circuit achieves equivalent single-qubit bit-flip error correction with 55% fewer qubits, lower gate complexity, and a modular structure based entirely on reversible gates (CNOT and CCNOT). This significantly reduces circuit depth and makes the design feasible for NISQ (Noisy Intermediate-Scale Quantum) devices with limited coherence time and qubit availability.

Additionally, the circuit was validated using IBM Quantum Composer and Qiskit, with simulation results showing 100% fidelity for all single-qubit bit-flip errors. The results demonstrate successful correction across all eight test cases and confirm the logic integrity of the design.

### 6.3. Limitations and Considerations

While the proposed design efficiently corrects single-bit-flip errors, it does not address phase-flip or multi-qubit errors, which are common in more generalized error models. Furthermore, the circuit has not yet been tested under real

quantum hardware noise, where gate errors, decoherence, and readout noise may reduce fidelity. Future work could expand the architecture to correct other error types or incorporate code concatenation strategies like Cat codes [21].

Despite these limitations, the simplicity and low overhead of the proposed design make it a strong candidate for integration into larger quantum error correction frameworks or experimental quantum processors. Its modularity also supports future expansion into hybrid or concatenated architectures.

## 7. Conclusions and Future Work

In this work, we presented a resource-efficient 4-qubit quantum circuit designed to correct single-qubit bit-flip errors in a 3-qubit data system. The proposed architecture makes use of Feynman (CNOT) and NOT gates, along with an ancillary qubit, to detect and correct errors with minimal resource overhead. The design is particularly well-suited for near-term quantum devices, where qubit availability and circuit depth are limited.

Simulations conducted using IBM Quantum Composer confirmed that the circuit achieves 100% correction fidelity across all possible single-bit-flip error states. Compared to traditional error correction methods such as the 9-qubit Shor code and 7-qubit Steane code, the proposed solution requires significantly fewer qubits and gates, while still delivering high detection accuracy and reliability under ideal conditions.

The simplicity and modularity of the circuit make it an ideal candidate for experimental implementation on current quantum processors and for integration into larger, more complex quantum error correction schemes.

Future work will focus on:

- Extending the circuit's capability to detect and correct phase-flip errors and multi-qubit errors.
- Integrating the circuit into fault-tolerant quantum computing frameworks and exploring hybrid architectures that combine it with classical error mitigation techniques.

This contribution lays a promising foundation for practical quantum error correction in constrained environments and opens the door to more scalable quantum information systems.

### Author Contributions

Conceptualization, D.G. and K.N.S.; methodology, D.G.; software, D.G.; validation, D.G. and K.N.S.; formal analysis, D.G. and K.N.S.; investigation, D.G. and K.N.S.; resources, D.G. and K.N.S.; data curation, D.G. and K.N.S.; writing—original draft preparation, D.G. and K.N.S.; writing—review and editing, D.G. and K.N.S.; visualization, D.G. and K.N.S.; supervision, K.N.S.; project administration, K.N.S. All authors have read and agreed to the published version of the manuscript.

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The authors declare no conflicts of interest.

### Data Availability Statement

The data presented in this study are available on request from the corresponding author. No publicly archived datasets were used or generated during this study.

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