Journal of
Instrumentation

ECON-T and ECON-D: Endcap Concentrator ASICs for the CMS HGCAL

To cite this article: G. Bergamin *et al* 2025 *JINST* **20** C03054

Published by IOP Publishing for Sissa Medialab

Received: *November 2, 2024*
Revised: *January 28, 2025*
Accepted: *February 11, 2025*
Published: *March 28, 2025*

Topical Workshop on Electronics for Particle Physics
University of Glasgow, Scotland, U.K.
30 September–4 October 2024

ECON-T and ECON-D: Endcap Concentrator ASICs for the CMS HGCAL

G. Bergamin[b,1] **D. Ceresa**[b,1] **D. Coko**[c,1] **G. Cummings**[a,1] **V. Gingu**[a,1] **M. Hammer**[d,1] **J. Hirschauer**[a,1] **J. Hoff**[a,1,*] **N. Kharwadkar**[a,1] **S. Kulis**[b,1,2] **M. Lupi**[b,1] **C. Mantilla-Suarez**[a,1] **D. Noonan**[a,1] **P. Rubinov**[a,1] **S. Scarfi**[b,1] **A. Shenai**[a,1] **C. Syal**[a,1] **X. Wang**[a,1] **R. Wickwire,**[a,1] **J. Wilson**[e,1] **J. Babbar,**[g,1] **B. Bam,**[f,1] **A. Campbell,**[f,1] **P. Klabbers,**[a,1] **Y. Miao,**[h,1] **R. Francisco,**[b,2] **D. Gong,**[j,2] **D. Guo,**[j,2] **P. Leitao,**[b,2] **P. Leroux,**[i,2] **P. Moreira,**[b,2] **J. Prinzie,**[i,2] **D. Yang**[j,2] **and J. Ye**[j,2]

[a] *Fermi National Accelerator Laboratory, Batavia, IL 60510, U.S.A.*
[b] *European Organization for Nuclear Research (CERN), CH-1211 Geneva 23, Switzerland*
[c] *Faculty of Electrical Engineering, Mechanical Engineering and Naval Architecture, University of Split, R. Boškovića 32 Split, Croatia*
[d] *Argonne National Laboratory, Lemont, IL 60439, U.S.A.*
[e] *Department of Physics, Baylor University, Waco, TX 76706, U.S.A.*
[f] *Department of Physics, The University of Alabama, Tuscaloosa, AL 35401, U.S.A.*
[g] *Department of Physics, Panjab University, Sector 14 Chandigarh, India*
[h] *Department of Physics, Northwestern University, Evanston, IL 60208, U.S.A.*
[i] *Katholieke Universiteit Leuven, 3000 Leuven, Belgium*
[j] *Southern Methodist University, University Park, Texas, U.S.A.*

E-mail: jimhoff@fnal.gov

Abstract: With over 6 million channels, the High Granularity Calorimeter (HGCAL) for the CMS HL-LHC Upgrade presents a unique data challenge. The ECON ASICs provide critical on-detector data reduction for the 40 MHz trigger path (ECON-T) and 750 kHz data acquisition path (ECON-D) of the HGCAL. The ASICs, fabricated in 65 nm CMOS, are rad-tolerant (600 Mrad) with low power consumption (<2.5 mW/channel). This presentation is the first comprehensive description of the ECON designs, first functionality and radiation tests for the ECON-T ASIC, and first results from the full production of 75k ECON-D and ECON-T ASICs.

Keywords: Digital electronic circuits; Front-end electronics for detector readout; Radiation-hard electronics; VLSI circuits

*Corresponding author.
[1] Design and test of ECON-T and ECON-D ASIC.
[2] Design of IP included from lpGBT ASIC.

https://doi.org/10.1088/1748-0221/20/03/C03054

2025 JINST 20 C03054

Contents

1 **Introduction** 1

2 **Design decisions regarding IP common to both ECON-D and ECON-T** 1

3 **Block diagrams** 2

4 **Radiation tolerance by design** 4

5 **Results and conclusions** 4

2025 JINST 20 C03054

1 Introduction

The CMS HGCAL is a 47-layer sampling calorimeter that features fine readout segmentation and which replaces the existing endcap calorimeter detectors for the High Luminosity phase of the LHC (HL-LHC) [1]. Overall, the HGCAL has more than six million channels spanning an area of 600 m^2 with 0.5–1.0 cm^2 sensor pads. The sensor signals are digitized by HGCROC ASICs [2, 3]. This digitized data must then be processed and zero-suppressed along two different pathways. The *trigger path* is the responsibility of the ECON-T and it concentrates charge sum data that it provides to the Level 1 Trigger at the 40 MHz beam crossover rate. The *data path* is the responsibility of the ECON-D and it concentrates complete data packets at the L1A accept rate (750 kHz). Each path serializes its concentrated data and sends it onto lpGBT ASICs [4] that are responsible for sending the information off-detector. Inbound clock and control information is likewise received by lpGBT ASICs and then fanned-out simultaneously to the front-end HGCROCs and the ECONs.

2 Design decisions regarding IP common to both ECON-D and ECON-T

The specifications of ECON-D and ECON-T have a great many similarities. For example, both ECON chips receive the same 320 MHz system clock and fast command stream from the back end. From these, both chips are required to produce the same beam synchronous 40 MHz clock. Both designs receive slow control data as a means of user-defined programming. What differentiates the two chips is the data frame that is received (i.e. charge sum frame (ECON-T) or triggered data frame (ECON-D)) and the nature of the algorithm performed on that data frame. Because of the similarity in specification, a deliberate design decision was made to make the two chips as identical in architecture as possible. That being said, it was determined that because the data frames and data processing algorithms were so different, it was impractical to design ECON-D and ECON-T as the same chip with different modes of operation. Consequently:

- Both chips receive a user programmable number of 1.28 GHz serial input streams from HGCROC front end chips (1–12 links for each chip). These serial input streams are captured by lpGBT eRX receivers and ePortRXGroup modules [4].

- Both chips produce a user programmable number of 1.28 GHz serial output streams to be sent to lpGBT chips for transmission off-detector (1–6 for ECON-D and 1–13 for ECON-T). These serial output streams are driven by lpGBT eTX drivers.
- Both chips use the same modules for Fast Command reception and interpretation [5]. This is the same IP used in the HGCROC.
- Both chips use the same modules for word/frame alignment of input data streams. These modules are custom ECON IP and were silicon proven in ECON prototype submissions.
- Both chips use the same serializer to prepare output streams for the lpGBT eTX drivers. These modules are also custom ECON IP and were silicon proven via prototype submissions.
- Both chips use the same module for slow control reception. This module is based very strongly on the I^2C-slave IP developed for the SSA chip [6, 7].
- Finally, both chips use the same IP to generate and distribute their 40 MHz master clocks and the various asynchronous resets used on the chip (hard reset, soft reset, etc.). Like the serial inputs and serial outputs, this is lpGBT IP.

3 Block diagrams

The block diagrams for both chips are shown in figure 1. The highlighted blocks are the IP common to both designs. The unique blocks such as the ECONT_core, the autoencoder,[1] the ECOND_core, and the ECOND_right are responsible for data processing, outbound packet assembly, and, in the case of ECON-D, inbound frame assembly.

The key to understanding the ECON-T is the 32-bit "trigger word" it receives every beam crossover period from each of the 1–12 HGCROCs that connect to the ECON-T. The trigger word consists of a 4-bit header (by defaut either 1010_2 or 1001_2 for bunch number 0) and four 7-bit floating point Trigger Cell sums (TCs) (3 bit mantissa with 4-bit exponent). For each beam crossover period, the TCs are independent of the TCs in the preceding and succeeding periods. The Mux-Fix-Calib block is a switchbox that allows any physical TC to be logically moved to any location. At the same time, it converts each TC to a 21-bit fixed-point word that is calibrated by a unique, user-defined constant. The Algorithm block takes the ordered, calibrated trigger cell sums output by Mux-Fix-Calib and performs one of 5 algorithms on them:

1. *Threshold Sum (TS) Algorithm* — Variable length, variable latency. An individual TC is transmitted if it exceeds a user-programmable threshold. Thresholds are unique for each TC.
2. *Super Trigger Cell (STC) Algorithm* — Fixed length, fixed latency. Charges are summed from groups of adjacent TC. Transmits the sum along with the address of the TC with the maximum charge in each group. There are four STC Algorithm sub-types that vary the number of TCs that are summed.
3. *Best Choice (BC) Algorithm* — Fixed length, fixed latency. Sorts the 48 TC by charge magnitude and transmits the N TC with highest charge where N is user programmable.

[1] The autoencoder has been discussed elsewhere [8] and will not be covered in detail here.

2025 JINST 20 C03054

4. *Repeater (R) Algorithm* — The repeater algorithm takes the 22-bit data from the calibration block, encodes with 4E+3M and passes it directly to the formatter. This algorithm is intended for testing and debugging.

5. *Auto-encoder (R) Algorithm* — The AE algorithm is fully configurable network for compression of the 48 x 7-bit TC "image" based on machine learning.

The Formatter block demultiplexes the algorithm choice and presents its results to the buffer in a specific, internal format. Finally, the Buffer block buffers and outputs the resultant output frame.

Both designs were developed using an assumption of "system enforced coincidence of data". Since all ECONs and their associated HGCROCs are aligned in the same manner, connected to the same clocks, and obey the same fast commands, it can be assumed that, in the absence of errors or upsets, all HGCROCs are always outputting related information at the same time. This is particularly important for the ECON-D since each HGCROC outputs triggered data packets over 40 successive clock periods. The system enforced coincidence of data means that for each trigger, all HGCROCs output a header word at the same time and channel 0 data at the same time, etc. The ECOND_core utilizes this coincidence of data to extract information from each triggered HGCROC data packet simultaneously for presentation to the ECOND_right through the Ping-Pong Memory. The Ping-Pong memory allows the ECON-D to read the next packet while outputting the previous packet and it unscrambles the HGCROC data. Because of the system enforced coincidence of data, HGCROC data arrives channel ordered — each channel from each HGCROCs arrives at the same time. The ECON-D output packet transmits data in HGCROC order — all channels from HGCROC 1 followed by all channels from HGCROC 2, etc. ECOND_right takes the information extracted by the ECOND_core, formats it into the ECOND packet and transmits it to the HGCAL back-end.

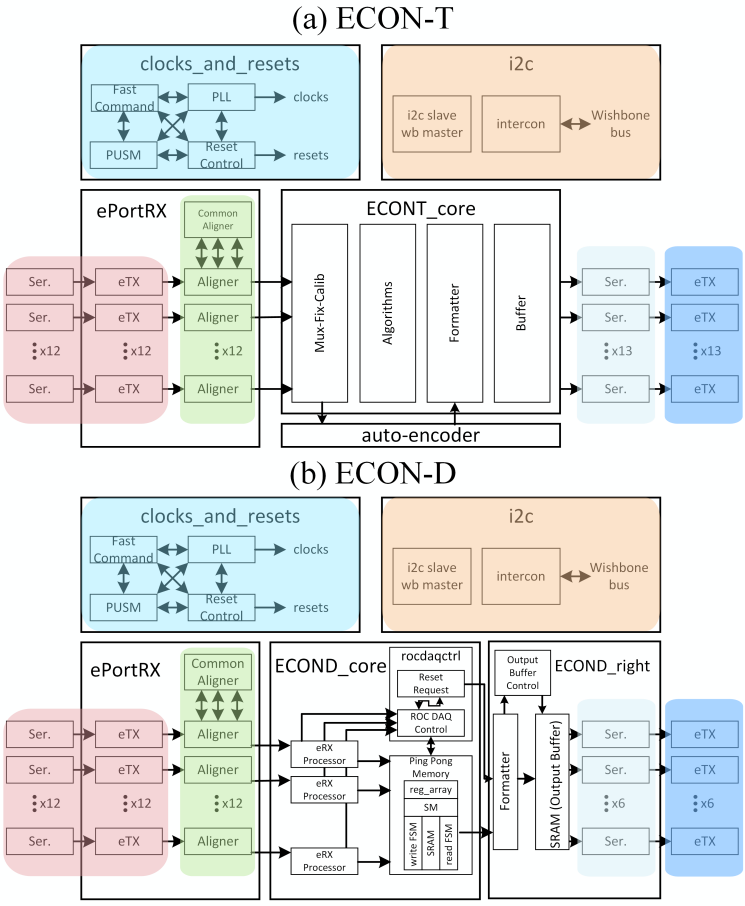

Figure 1. A block diagrams for (a)ECON-T and (b)ECON-D. The highlighted blocks are IP common to both ECON-T and ECON-D (clocks_and_resets, eRX, ePortRxGroup, Common Aligner and (channel) Aligner, I^2C slow control, Serializer and eTX).

4 Radiation tolerance by design

The overwhelming effort in this chip design was to achieve the extreme radiation tolerance required by CMS. The Total Ionizing Dose tolerance of 220 Mrad largely comes from our choice of technology (65 nm CMOS). Single-event tolerance (High Energy Hadrons (HEH) flux up to $3 \cdot 10^6$ cm^{-2} s^{-1}) comes from three principal mechanisms: Triple Modular Redundancy (TMR), Tolerance By Design, and Graceful Failure.

In ECON, full-TRM with triplicated data paths, triplicated registers, triplicated logic, triplicated voting and triplicated clocks was used everywhere possible. It was inserted in the RTL coding via the TMRG program [9].

Tolerance by Design means that the ECON chips are designed such that wherever possible, logic itself minimizes or eliminates Single Event Upset (SEUs) effects. Usually this is done by taking advantage of redundancies implicit in the system. For example, the headers of each HGCROC data packet should be identical for every front-end connected to a particular ECON-D. Vertical Reconstruction (figure 2) is a form of N-Modular Redundancy that processes each bit independently. It totals the number of observed 1 s and the number of observed 0 s and compares those totals to a user-defined threshold. If the number of 1 s is above threshold and the number of 0 s is not, the reconstructed bit is a 1 and *vice-versa*. If neither total is above threshold, the reconstruction is a failure. If both are above threshold, it is an ambiguous reconstruction. Since Single Event Effects (SEEs) in one HGCROC are unlikely to affect other HGCROCs, the Vertical Reconstruction method allows the reconstitution of critical event information in spite of the presence of SEUs. It also permits the monitoring of failures which can facilitate the back-end in its task of catching broken HGCROC-ECON links.

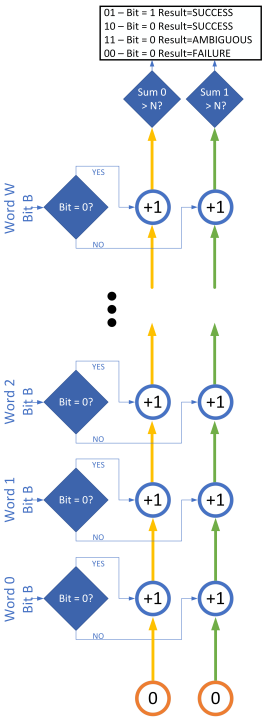

Figure 2. Vertical Extraction and Recovery.

Graceful Failure acknowledges that upsets are inevitable in a high-radiation environment. Consequently, even in the presence of significant upset and loss of data, there should always be a path back to idle that will allow operation to continue for future events without external intervention. In ECON-D all of its state machines complete the phase space set by the bit-width of the state machine even if doing so requires the creation of "useless" states. For example, in the state machine that governs ECOND_core, there are 48 useful states out of 64 possible states. In the event of an SEU that forces the state machine into one of the 16 useless states, the conclusion of an HGCROC packet will still bring the state machine back to its idle state, ready for the next packet. A data packet might be lost due to SEU, but operation can continue.

5 Results and conclusions

The first ECON-T prototype was submitted in June of 2021 [10]; the first ECON-D prototype was submitted in March of 2023; and final production versions of the chips were submitted for fabrication in December of 2023.

2025 JINST 20 C03054

Functional tests can be divided into three categories — those specific to ECON-T, those specific to ECON-D, and those common to both. Extrapolating from section 2, the common tests cover data inputs (e.g. phase alignment by fixed-phase mode, etc.), outputs (e.g. PRBS and Eye Diagrams, etc.), Fast Commands (e.g. receive and respond to good commands; receive and respond to erroneous commands, etc.), Alignment (e.g. automatic or manual word align, alternate IDLE words, etc.), I^2C (e.g. R/W to every register, R/W to every address, etc.), Clocks (e.g. PLL Lock to reference clock or test clock; measurement of VCO frequency, etc.). ECON-T specific tests include Mux/Cal (e.g. All MUX settings, all calibration values, etc.), Datapath (e.g. Threshold-Sum, Repeater algorithm, etc.), Formatter/Buffer (e.g. Fill/Empty buffer, etc.), and Power (e.g. with/without clock, Min/Max, etc.). ECON-D specific tests include Datapath (e.g. Pass-through mode, Event/Buffer/Orbit reconstruction and matching, varying zero suppression thresholds, etc.), Formatter/Buffer (e.g. Verify packets, Packet Vetos, etc.), and Power (e.g. nominal configurations and varying datasets, Min/Max, etc.).

Comprehensive chip testing of the prototypes revealed few issues and all of them minor. For example, shield metal placed over the VCO inductor affected the locking range of the PLL in the ECON-D prototype. Removal of this excess shield metal by Focused Ion Beam processing restored the correct frequency. In the ECON-T prototype, an RTL bug required all inputs to be active. Importantly, none of these minor issues affected prototype testing, and all of them were easily corrected in the final submission. Tests of the final production chips show full functionality with no further modifications of the digital logic necessary. A careful testbench-based analysis of "hard failures" — e.g. power out of specification, VCO frequency out of specification, etc. — showed a 97% yield across 900 chips. The main failure mode was power out of specification. Further robot-based testing of 6000 chips is ongoing, but is showing yields consistent with those of the initial 900. In addition to requiring chips to pass all functional QC tests, we plan to obtain chips for use on-detector by preferentially selecting chips with the lowest minimum operating voltage (VDD) required to pass the functional tests because such chips are observed to have more robust TID tolerance in TID testing. Studies of the relationship between this minimum VDD and TID tolerance are underway. Possible explanations include the possibility that chips with low minimum VDD have faster transistors or smaller internal voltage drop.

Radiation testing for total ionizing dose (TID) tolerance and SEEs robustness is on-going. Thus far, TID tests have been done using the CERN ObeliX x-ray machine at a dose rate of 9 Mrad/hr at a temperature of -20 C with the digital power rails set in a range from 1.08 V to 1.32 V (1.20 V nominal). Two ECON-T prototypes were tested to 300 and 660 Mrad, and three ECON-D prototypes were tested to 660 Mrad. One production ECON-T chip was tested to 660 Mrad, and five production ECON-D chips were tested in the range of 15–660 Mrad. In all cases, robust performance was observed at nominal voltages with the expected TID-dependence of the lpGBT Phase-Locked Loop capacitor banks and phase window. A detailed analysis of ECON-D SRAM performance as a function of temperature, operating voltage, and TID is in progress.

Three SEE test campaigns have been performed for both the prototype and production versions of the chips using 217 MeV protons at a flux of $1 \times 10^9 - 2 \times 10^{10}\,\mathrm{cm}^{-2}$ per second resulting in a total fluence of $4.4 \times 10^{14}\,\mathrm{cm}^{-2}$, which is approximately four times the equivalent HL-LHC fluence for HGCAL. During these tests zero errors requiring reset and zero configuration errors have been found. A preliminary SEU cross section in pre-voted flip-flops of $2.0 \times 10^{-14} - 2.5 \times 10^{-14}\,\mathrm{cm}^{-2}$ per bit is consistent across all tests performed thus far.

2025 JINST 20 C03054

Acknowledgments

The authors would like to gratefully acknowledge the assistance and support of the board/system architects especially Matt Noy; the HGCROC developers, especially Frederic Dulucq, Mowafak El Berni, Damien Thienpont, and Christophe de La Taille; the Back End FPGA developers, especially Andre Mendes and Paul Dauncey; and, finally, the HGCAL leadership, especially Paul Aspell, Jeremy Mans and Karl Gill.

References

[1] CMS collaboration, *The Phase-2 Upgrade of the CMS Endcap Calorimeter*, CERN-LHCC-2017-023 (2017) [DOI:10.17181/CERN.IV8M.1JY2].

[2] D. Thienpont and C. de La Taille, *Performance study of HGCROC-v2: the front-end electronics for the CMS High Granularity Calorimeter*, 2020 *JINST* **15** C04055.

[3] F. Bouyjou et al., *HGCROC3: the front-end readout ASIC for the CMS High Granularity Calorimeter*, 2022 *JINST* **17** C03015.

[4] lpGBT Design Team, *lpgbtv1 manual*, https://lpgbt.web.cern.ch/lpgbt/.

[5] M. Noy, *The HGCAL fast command and 320 MHz clock receiver block and verification test bench*.

[6] A. Caratelli, *I2c slave wishbone master*, (2021), https://gitlab.cern.ch/asic-design-support/digital_ips/i2c_slave_wb_master.

[7] A. Caratelli et al., *Performance characterization and radiation tolerance evaluation of the SSA2 ASIC, the strip sensor readout ASIC of the CMS Outer Tracker at the HL-LHC*, 2023 *JINST* **18** C01046.

[8] G. Di Guglielmo et al., *A Reconfigurable Neural Network ASIC for Detector Front-End Data Compression at the HL-LHC*, *IEEE Trans. Nucl. Sci.* **68** (2021) 2179 [arXiv:2105.01683].

[9] S. Kulis, *Single Event Effects mitigation with TMRG tool*, 2017 *JINST* **12** C01082.

[10] D. Braga et al., *First test results of the HGCAL concentrator ASICs: ECON-T and ECON-D*, 2024 *JINST* **19** C03050.

2025 JINST 20 C03054