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Status and Plan for The Upgrade of The CMS Pixel Detector

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Abstract

The silicon pixel detector is the innermost component of the CMS tracking system and plays a crucial role in the all-silicon CMS tracker. While the current pixel tracker is designed for and performing well at an instantaneous luminosity of up to $1 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$, it can no longer be operated efficiently at significantly higher values. Based on the strong performance of the LHC accelerator, it is anticipated that peak luminosities of two times the design luminosity are likely to be reached before 2018 and perhaps significantly exceeded in the running period until 2022, referred to as LHC Run 3.

Therefore, an upgraded pixel detector, referred to as the phase 1 upgrade, is planned for the year-end technical stop in 2016. With a new pixel readout chip (ROC), an additional fourth layer, two additional endcap disks, and a significantly reduced material budget the upgraded pixel detector will be able to sustain the efficiency of the pixel tracker at the increased requirements imposed by high luminosities and pile-up. The main new features of the upgraded pixel detector will be an ultra-light mechanical design, a digital readout chip with higher rate capability and a new cooling system. These and other design improvements, along with results of Monte Carlo simulation studies for the expected performance of the new pixel detector, will be discussed and compared to those of the current CMS detector.

Keywords: LHC, CMS, pixel detector, upgrade

1. Introduction

One of the key components for the success of CMS experiment [1] has been the good performance of the pixel detector. Throughout the Run 1 data taking period, the pixel detector has operated with more than 96% of the detector functional and with a tracking efficiency of 99% and good spacial resolution [2]. The current pixel detector was designed to operate and perform well at the LHC designed luminosity of $1 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$. The LHC is anticipated to deliver a peak luminosity reaching two times or more than the design value before 2022. The current readout chip (ROC) is estimated, from simulation, to suffer about 16% data loss for the innermost layer at a luminosity of $2\times10^{34}\text{cm}^{-2}\text{s}^{-1}$ in a 25 ns bunch spacing operation mode. This is equivalent to having 50 proton collisions (pile-up, or PU) for every bunch crossing. If instead LHC runs with a 50 ns bunch spacing mode, the data loss for the innermost layer will be on the order of 50 % at the same instantaneous luminosity. A pixel upgrade proposal [3, 4] was made based around a redesigned ROC and a light weight detector structure. The upgrade detector is scheduled to be installed during the extended technical stop at the end of 2016.

2. Detector Design and Layout

The upgrade pixel detector retains the barrel and endcap structure and consists of 4 layers in the barrel section and 3 disks in each endcap volume, as shown in Fig. 1. Compared to the 3 layers and 2 disks of the current pixel detector, the additional pixel hits will improve the tracking efficiency and vertex resolution that are essential for b-tagging algorithms. The additional layer

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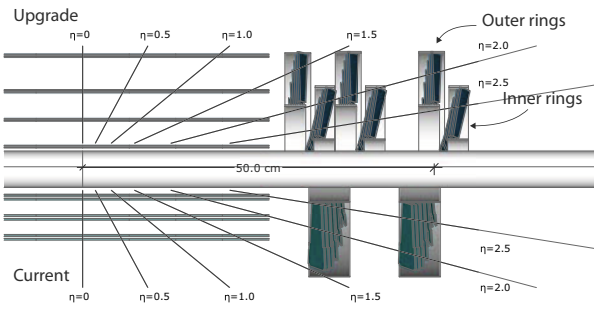

Figure 1: Layout of upgrade detector (top) and the current detector (bottom).

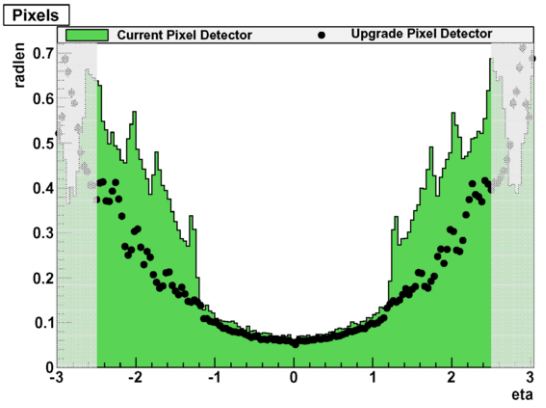

Figure 2: The material budgets, shown in units of radiation length as a function of η, of the upgrade detector, in black dots, and current detector, in the green histogram. The upgrade detector has less material even with an additional barrel layer and endcap disk.

of detectors results in a 60% increase in channels in the barrel and 2.5 times more channels in the endcap detector. The whole detector, therefore, consists of 1184 modules (79 million pixels) in the barrel and 672 modules (44 million pixels) in the endcap. The innermost layer of the upgrade detector will be placed at a 3 cm radius from the beam line, much closer than the 4 cm radius of the current detector.

The mechanical support and the cooling and electronics services of the upgrade detector are designed to be of lighter weight than the current detector. The new design uses an ultra-lightweight support and CO_2 cooling and relocates much of the passive material, such as electronics boards and connectors, out of the tracking volume. The mechanical part of the upgrade barrel detector, despite one more layer, weighs about 40% of what the current barrel detector does, and the endcap detector weighs about 80% of the current one. The material budget distribution, in units of radiation length and as a function of pseudo-rapidity (η)[1], is shown in Fig. 2.

3. Expected Performance

The physics performance of the upgraded detector is simulated and studied using several LHC running scenarios to compare to the current detector in the same data taking conditions. Figure 3 shows the tracking efficiencies and fake rates of the current and upgrade detectors in a scenario with 25 ns bunch spacing and $2 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ instantaneous luminosity. The improved data loss mechanism of the new ROC performs

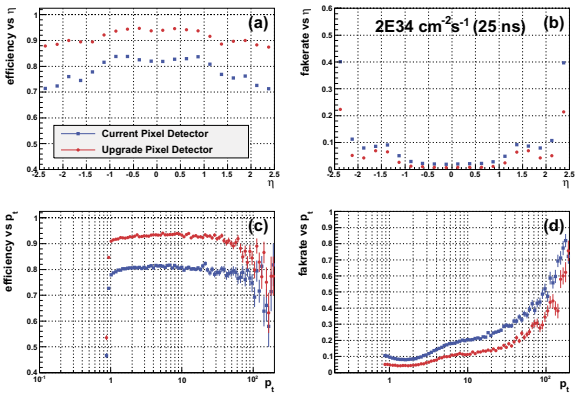

Figure 3: The tracking efficiencies (a) and fake rates (b) as a function of η of the current and upgrade detectors when running at $2 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ peak luminosity with 25 ns bunch spacing. The efficiencies (c) and fake rates (d) as a function of transverse momentum p_T in the same LHC conditions are also shown.

more efficiently in the harsh environment of the LHC operation. The impact parameter resolution of tracks has been improved in both the transverse direction (d_0) and longitudinal direction (z_0) in the high PU environment. This can be translated into better vertex resolution, which benefits the b-jet tagging [5] algorithm that is a fundamental tool for many physics analyses. The b-jet tagging performance can be seen in Fig. 4. The upgrade detector shows either higher tagging efficiency or lower light-jet fake rate depending on the selection criteria.

[1]CMS uses right-handed coordinate system, with the origin at the nominal interaction point, the x axis pointing to the center of LHC ring, the y axis pointing upward and the z-axis along the anticlockwise beam direction. The radial coordinate in xy plane is denoted by r. The polar angle θ is defined in the rz plane and the pseudo-rapidity $\eta = -ln(tan(\theta/2))$.

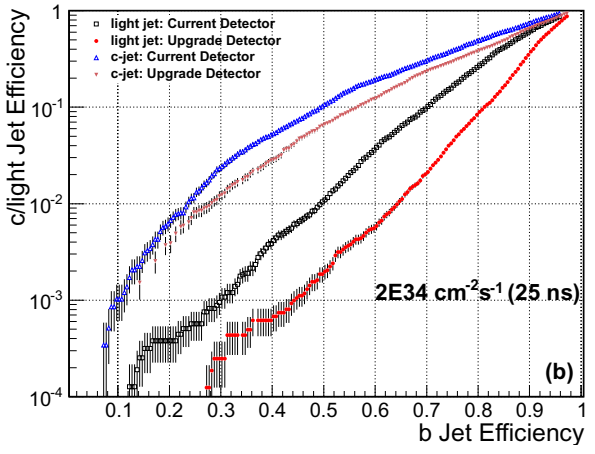

Figure 4: The b-jet tagging efficiencies versus light- and c-jet fake rates. The upgrade detector shows higher tagging efficiency or lower light-jet fake rate depending on the selection point.

4. Pixel Module and Components

The phase 1 upgrade project has moved from the R&D phase to the pre-production phase in 2014. During summer time, several production centers were producing a few pixel modules in order to finalize all the tools and facilities needed to produce modules. In the mean time, performance studies in details of various redesigned or newly designed components, such as the ROC and token bit manager (TBM) chips, were carried out. In the following section, some details of the design and characteristics together with testing results of the module components are described.

The design of the pixel sensors for the upgrade detector remains unchanged with respect to the current detector [6]. The pixel size is 150 μm $\times$ 100 μm with a sensor thickness of 285 μm. The sensor has an "n-on-n" layout, with n^+ implants on an n-type bulk silicon. The latest studies of radiation hardness [4] show that the sensor is capable of delivering enough signal for a bias voltage at or below 600 V, even after receiving 1.5 $\times$ 10^{15} n_{eq}/cm^2 of fluence, corresponding to 250 fb^{-1} integrated luminosity at a radius of 3 cm.

The readout chip has been redesigned to reduce inefficiencies from several data-loss mechanisms in the high luminosity environment. The new ROC layout uses the same 250 μm CMOS process as the current ROC. The new features of the ROC are as follows:

- New readout protocol : The new ROC runs on an internal clock of 160 MHz, four times the LHC 40 MHz clock. The ROC data is digitized and transmitted with a data serializer also running at 160MHz with a digital LVDS driver. The digital data output avoids the data transmission in analog form and the complex decoding of multi-level analog signal.

- Reducing data loss : New design has increased the number of time-stamp buffer cells (from 12 to 24) and data buffer cells (from 32 to 80) to reduce the probability of buffer overflow during data taking during the high instantaneous luminosity period. An additional buffer stage in the data readout periphery is introduced. Pixel data is transported internally to the new data buffer stages immediately after the trigger signal has arrived and awaits for the data readout token from CMS to issue the transfer to off-detector electronics. Combining all the above, the simulation indicates a significant reduction in data loss for the new ROC compared to the existing one in the high luminosity environment.

- Enhanced analog performance : Several improvements and adjustments were implemented on the analog part of the ROC. The current ROC has a noise level of 3500 electrons that is higher than expected mainly due to internal cross talk. A new power distribution inside the ROC including an additional layout layer and thicker top layer has reduced the cross talk. Along with other minor improvements, this results in an absolute operational threshold well below 2000 electrons, as seen in lab measurements.

A full pixel module contains 2 $\times$ 8 ROCs bump-bonded to pixel sensors, a pair of ceramic base strips and a high density interconnect (HDI) with components. Figure 5 shows the components of a full module and a prototype module assembled. The HDI is glued on top of the sensor and wire-bonded to ROCs and hosts a TBM chip that distributes the control, trigger and clock signals as well as collecting data streams from the ROCs and transmitting the streams to the off-detector electronics. The TBM has also been redesigned to cope with the digital format of the ROC output and a larger data volume resulting from the higher luminosity. The output of the TBM is based on a 400 MHz encoded data stream sent through a single fiber to off-detector DAQ electronics.

5. Detector Performance and Qualification

Tests and measurements in the laboratory and with particle test beams have been carried out to understand the performance of the new ROC. The pixel module

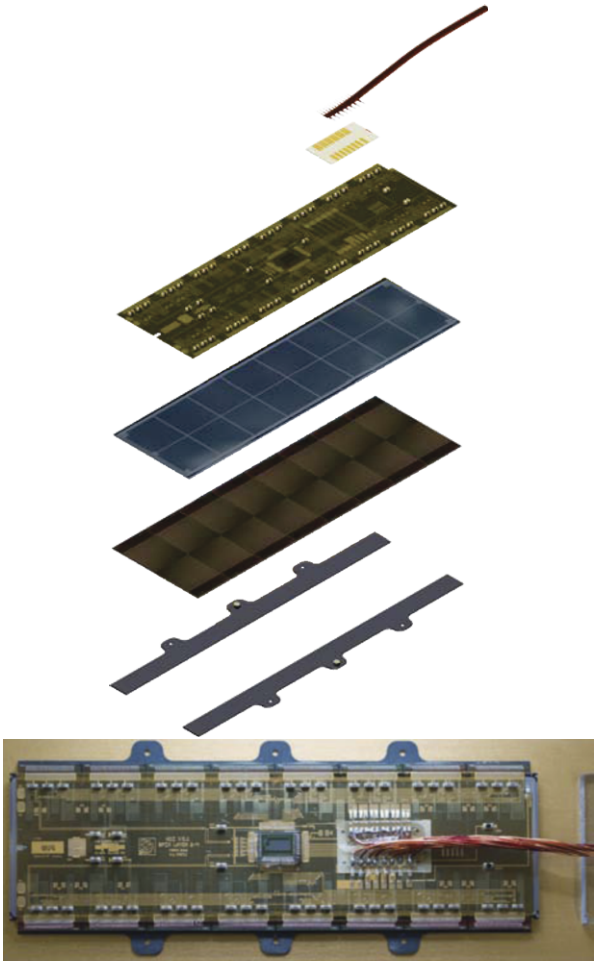

Figure 5: The illustration of a full pixel module and an assembled prototype module. The module components are, from top to bottom, twisted-pair cable, connector, HDI, pixel sensor, ROCs and base strips.

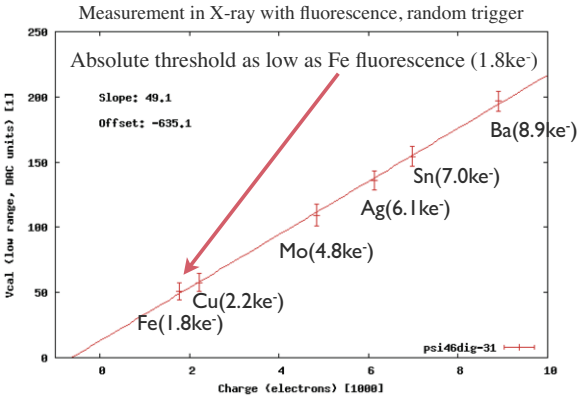

Figure 6: The measured peak position of X-rays coming from different sources in units of the internal charge injection, Vcal. A ROC is self-calibrated with respect to Vcal. One Vcal unit is typically equivalent to 50 electrons. The measured responses of ROCs under X-rays are used to calibrate the absolute scale of the Vcal unit of each individual chip.

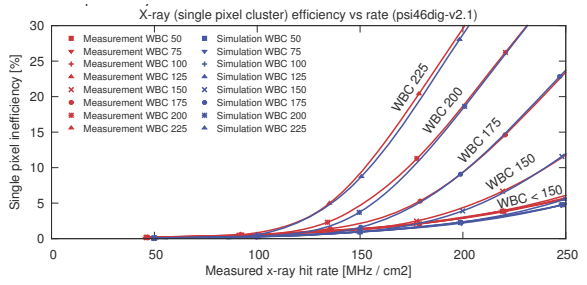

Figure 7: The data loss of the ROC as a function of X-ray flux and trigger latency (WBC). The layer-2 module corresponds to 120 MHz/cm^2 at a luminosity of 2.0 $\times$ 10^{15} n_{eq}/cm^2. With nominal CMS latency around 170 WBC, the data loss is estimated to be less than 1%. The data points of WBC setting below 150 are very close to each other and group together in the plot.

is measured to have a intrinsic noise level around 180 electrons. This makes future detector operation with a threshold below 2000 electrons very promising. X-ray fluorescence emission from various different sources provide spectra to calibrate the energy scale of modules. The new pixel module is able to measure as few electrons as the K_α line of an iron target, shown in Fig. 6. The measurement confirms that the noise level of a module is well below 2000 electrons. The X-ray tube can also generate high enough pixel hit rates, up to a few hundred MHz/cm^2, to study the data loss as a function of particle flux. The inefficiency of the ROC as a function of X-ray flux is measured to be consistent with the simulation, as shown in Fig. 7. Preliminary test beam results are consistent with the expected performance. The analyses are still ongoing with results to be reviewed.

All detector modules will go through at least 10 thermal cycles, between -25 and 20 degrees C, to satisfy the quality control procedures. Electrical tests will be performed at both room temperature and the lowest temperature during the thermal cycles. The test results will be used to grade a module.

6. Pilot Blade Project

During the first long shutdown (LS1) of the LHC in 2013 and 2014, CMS is installing eight upgrade pixel modules in the $-z$ side, four on each half cylinder, into the space preserved for the pixel endcap disks. The present detector design has three disks in each endcap,

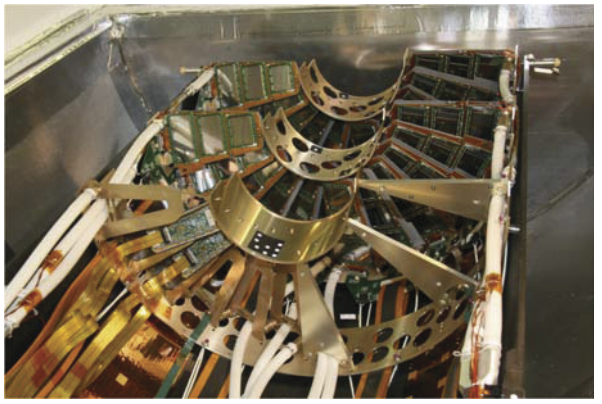

Figure 8: The pilot blade detector together with current FPIX modules that will be installed in CMS during LS1.

though only two were actually installed. Figure 8 shows the picture of two pixel modules installed in the present endcap half shell. Two layers of present pixel modules can been seen in the back. Sufficient infrastructure, such as optical fibers, power cables and cooling channels, is available to accommodate the upgrade pixel modules. The project represents the ultimate test beam experiment with LHC collisions. It helps to identify any challenges related to operation with beam and provides operational experience, especially for the newly designed components, such as new ROC, TBM, DC-DC power converter and DAQ off-detector electronics board. All the mechanical support and prototype modules have been prepared and the installation will be carried out during the pixel detector insertion at the end of 2014.

7. Summary

In preparing for the high luminosity era of LHC running, CMS has developed the upgrade project of the inner pixel detector. The upgrade detector includes one more layer in the barrel region and one more disk in each endcap volume. With the newly designed lightweight structure and CO_2 cooling, the upgrade detector contains less material than the current one. The redesigned readout chip significantly improves the efficiency during high instantaneous luminosity periods. This translates to improved physics performance in high pile-up conditions.

The pilot blade project will install eight upgrade pixel modules in CMS to gain experience operating the new devices. Mass production will take place from 2015 to early 2016 and the installation is scheduled for the extended technical stop at the end of 2016.

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