Available online at www.sciencedirect.com

SciVerse ScienceDirect

Physics Procedia 37 (2012) 1039 – 1045

Physics Procedia

TIPP 2011 - The Technology and Instrumentation in Particle Physics 2011

Recent Progress of Pixel Detector R&D based on SOI Technology

Toshinobu Miyoshi[a],Yasuo Arai[a], Youichi Fujita[a], Kazuhiko Hara[b], Ryo Ichimiya[a], Yoichi Ikegami[a], Yukiko Ikemoto[a], Hiroki Kasai[c], Hironori Katsurayama[d], Takashi Kohriki[a], Masao Okihara[c], Yoshimasa Ono[d], Yoshiyuki Onuki[d], Kohei Shinsho[b], Ayaki Takeda[e], Kazuya Tauchi[a], Toru Tsuboyama[a], Yoshinobu Unno[a]

[a]*Institute of Particle and Nuclear Studies, High Energy Accelerator Research Organization(KEK), Tsukuba 305-0801, Japan*
[b]*Graduate School of Pure and Applied Sciences, University of Tsukuba, Ibaraki 305-8571, Japan*
[c]*LAPIS Semiconductor Miyagi Co., Ltd., Ohhira, Miyagi 981-3693, Japan*
[d]*Graduate School of Science, Tohoku University, Aoba-ku, Sendai, Miyagi 980-8578, Japan*
[e]*Department of Particle and Nuclear Physics,Graduate School of High Energy Accelerator Science, The Graduate University for Advanced Studies (SOKENDAI), 1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan*

Abstract

We are developing truly monolithic pixel detectors with a 0.2 μm silicon-on-insulator (SOI) CMOS technology, which is intended to be utilized in various research fields, such as high-energy physics, X-ray material analysis, astrophysics and medical sciences. In the development project, KEK has organized several Multi Project Wafer (MPW) runs and the process has been incrementally improved. Czochralski (CZ-) and Float-Zone (FZ-) silicon has been used as a starting material for the detector fabrication. Using FZ-SOI wafers, the detectors worked at full depletion below the breakdown voltage. The up-to-date integration-type pixel detector with 14 μm pixel size has excellent spatial resolution.

Keywards: SOI; pixel; CMOS sensor

1. Introduction

Nowadays silicon-on-insulator (SOI) wafers have been used for CMOS circuits. It consists of two silicons and an insulator such as silicon oxide between them. Since we can choose the resistivity of the silicons respectively, we chose SOI wafers having different resistivity; high-resistivity silicon for the sensor part and low-resistivity for the CMOS circuit. This structure is ideal for a monolithic detector. The

E-mail address: tmiyoshi@post.kek.jp (Toshinobu Miyoshi)

 doi:10.1016/j.phpro.2012.02.450

development project of the SOI detector started in 2005 and we have developed several prototypes of the SOI detectors [1] [2]. In 2008, there were two major problems. One was the back gate effect by which the threshold of MOS transistors is changed when applying higher voltages to the back (bulk) side of silicon. We introduced a new process, Buried P-Well (BPW) and, as a result, higher back bias voltage can be applied without shifting the MOS transistor threshold. This has enabled us to evaluate the basic characteristics of the SOI detectors [3]. Another problem was the quality of the SOI wafer. We have used Czochralski (CZ) wafers in which the resistivity after LSI process was about 700 Ohm-cm. In this case, we require high voltage of more than 300 V to be fully depleted in 260 μm-thick silicon. Recently, the process to fabricate SOI detectors was improved and Float-Zone (FZ) wafer has been utilized since 2009. KEK have organized several multi project wafer (MPW) runs in recent years and therefore the SOI process has also been improved. In this document, we report recent progress of the development of SOI monolithic detectors and some results of evaluation test in SOI pixel sensors.

2. Process improvement

SOI detectors are developed using 0.2 μm low-leakage Fully-Depleted-SOI (FD-SOI) process by LAPIS Semiconductor Co. Ltd. (called *LAPISsemi* in this report). In Multi Project Wafer (MPW) runs, institutions and universities over the world participate to share the cost of the process mask. Fig. 1 shows an example of the mask designed in 2010. 23 designs and 3 *LAPISsemi* test groups were included. To use the detectors under the full depletion condition, higher back-bias voltages must be applied. Before 2008, we were doing sensor tests with only 10V of back bias voltages because of the back gate effect. After the BPW process was developed, we started detector tests with higher voltages (about 100 V). The design rules were modified every MPW run and more relaxed conditions can be used at the corner edge of n-sub and p-sub rings. In 2009, the breakdown voltages were increased to more than 200 V in a subset of sensor chips. However, we require higher voltages (more than 300 V) for the full depletion condition in 260 μm-thick bulk silicon because we utilize CZ-SOI wafers with lower (about 700 Ohm-cm) resistivity. In 2009, *LAPISsemi* succeeded handling FZ-SOI wafer while keeping higher resistivity during their process, and thus we have started developing FZ-SOI detectors in MPW runs since the end of 2009. As for other process improvements, the 5-th metal layer became available in 2010 and therefore more stable ground and power lines became available. We have also started to reduce pixel size of integration-type pixel detectors partly because the design rule about the MIM capacitor size was relaxed from the MPW 2010.

3. Integration-type pixel detectors

We have designed mainly integration-type and counting-type pixel detectors. In this report, we describes some integration-type pixel detectors to explain the recent progress of our R&Ds. Table 1 shows specification of integration-type SOI detectors which have been designed since 2008. INTPIX3a-e pixel circuits are shown in reference [4]. Fig. 2 shows DIPIX1 pixel layout. This is the smallest pixel size in KEK so far. The pixel included a BPW layer which connected to a sensor node and a correlated double sampling (CDS) circuit which reduce the reset noise. A MIM capacitor was used to store signals. From the process in 2010, the capacitance per micron was increased and therefore the size in the pixel area can be reduced with keeping the same value as the previous INTPIX designs.

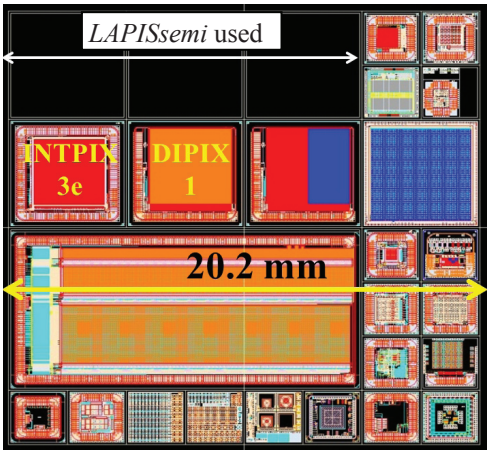


Fig. 1 An example of mask layout in MPW runs.

Table 1. Specification of integration-type pixel detectors fabricated since 2008

Chip name	Pixel size [μm]	# of pixels	Effective area [mm]	Chip area [mm]	Fabrication year	# of pixel type	CDS in pixel
INTPIX3a	20	128 x 128	2.56 x 2.56	5 x 5	FY2008	8	No
INTPIX3b	20	128 x 128	2.56 x 2.56	5 x 5	FY2009-1	8	No
INTPIX4	17	832 x 512	14.144 x 8.704	15.3 x 10.2	FY2009-1	1	Yes
INTPIX3c	20	128 x 128	2.56 x 2.56	5 x 5	FY2009-2	8	No
INTPIX3e	16	192 x 192	3.072 x 3.072	5 x 5	FY2010-1	1	No
DIPIX1	14	256 x 256	3.584 x 3.584	5 x 5	FY2010-1	1	Yes
DIPIX2	14	256 x 256	3.584 x 3.584	5 x 5	FY2010-1	2	Yes

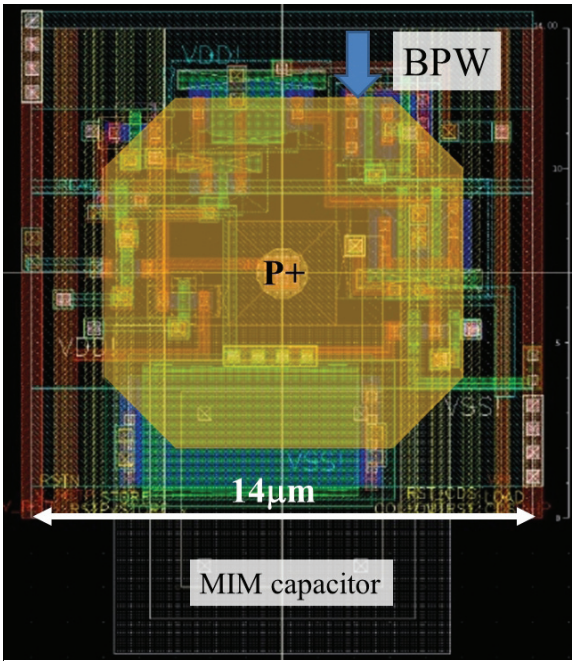


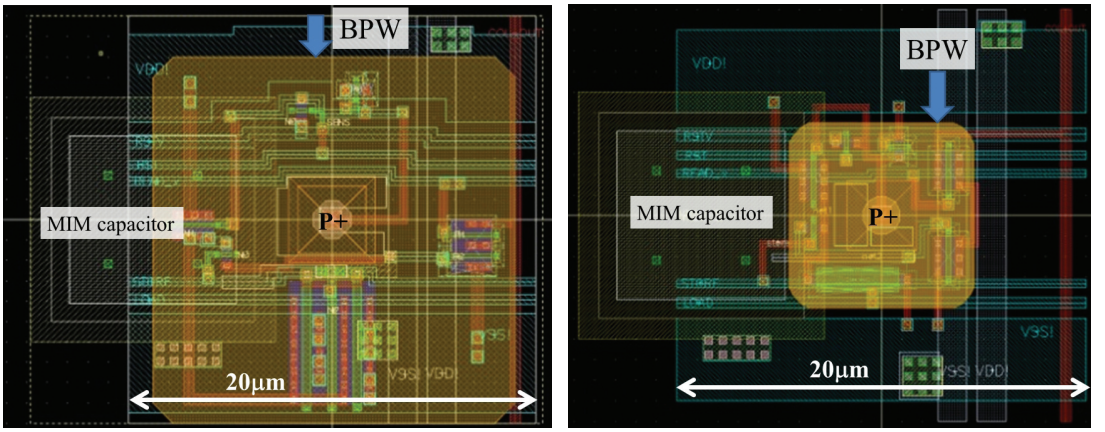
Fig. 2 DIPIX1 pixel layout.

4. Evaluation test of integration-type pixel detectors

In this report, three evaluation test results are described: (1) BPW effectiveness study in the (CZ-) INTPIX3a and INTPIX3b, (2) FZ-SOI wafer study in the (FZ-) INTPIX3e and (3) spatial resolution study in the (CZ-) DIPIX1.

4.1. BPW effectiveness study

The BPW process has been introduced since FY 2008. To evaluate the effectiveness, the integration-type pixel detector, INTPIX3a, was designed. It included 8 types of pixels. Fig 3(a) shows one of the pixels which include one p+ contact with a large area BPW. Because the size of the BPW connected to p+ sensor node was large, the sensor gain was small. Therefore, the size of the BPW inside the pixel was optimized. Fig 3(b) shows one of the pixels designed at the fabrication of INTPIX3b. In total, 16 pixel types with the BPW were designed and they were evaluated using monochromatic X-ray in KEK Photon Factory (KEK-PF). The sensor gain was evaluated with X-ray energy as shown in Fig. 4 [5]. The measurement was done at room temperature and the back bias voltage was 100 V. It showed that the sensor gain depends on the size of the BPW and was higher with a smaller BPW in a pixel. The sensor capacitance was calculated from the sensor gain and it was about 10 fF in the case of the pixel in Fig. 3(b), which is almost consistent with initially estimated values in SPICE simulation.



(a) (b)

Fig. 3 Pixel layouts included in (a) INTPIX3a and (b) INTPIX3b.

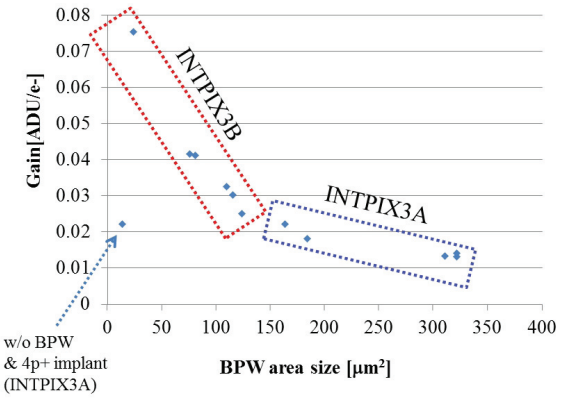


Fig. 4 The relationship between BPW area size and the sensor gain.

4.2. Evaluation test of the FZ-INTPIX3e

An integration-type pixel detector, INTPIX3e, was fabricated in 2010 using CZ- and FZ-SOI wafers. In this report, two evaluation test results of FZ-INTPIX3e are shown. First of all, a back illumination test was done to confirm that the sensor is fully depleted in lower back-bias voltages. A red laser (635 nm) was illuminated from the back side of the sensor and the output response was recorded with the back-bias voltage (*Vdet*). The result is shown in Fig. 5. The resistivity of n-type FZ-SOI bulk is about 7 k Ohm-cm, and the estimated value of the full depletion voltage is about 100 V. Below 100 V, the signals were very small because the laser light is absorbed at the surface in a few microns but the depletion depth doesn't reach at the back side. The increase of the output started at around 100 V in which the depletion depth reached to the back side of the sensor. The output was stable above about 220 V. The reason of the large "gap" (from 100 V to 220 V) is unknown. The second test aimed at the evaluation of the spatial resolution. In raw data, spatial resolution was poor as shown in Fig. 6(a) probably because generated charges in the sensor bulk were shared within multiple pixels. In INTPIX3e, the pixel size is much smaller than the bulk thickness of 500 μm. After charge sharing correction using adjacent pixels (corrected within 3 by 3 pixels), clear images can be obtained as shown in Fig. 6(b). However, INTPIX3e images in FZ-SOI water are noisy compared with that in CZ-SOI wafers. We are investigating the reason.

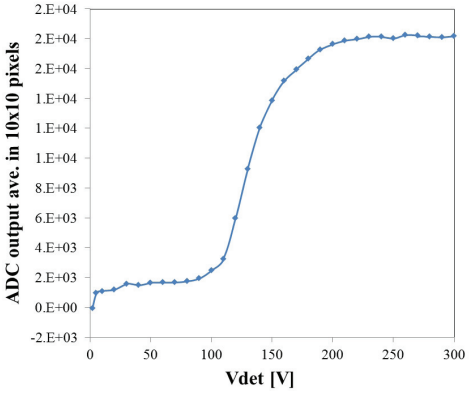


Fig. 5 The relationship between the back-bias voltage (*Vdet*) and sensor (ADC) output averages in 10 by 10 pixels

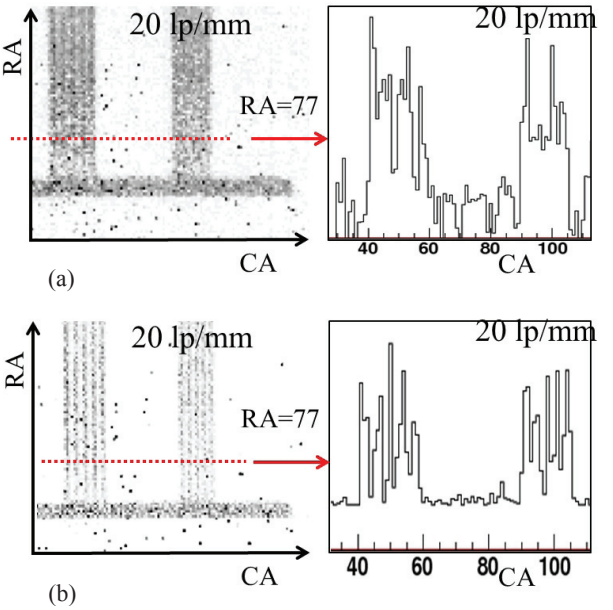


Fig. 6 Two-dimensional images of X-ray test chart (a) before and (b) after charge sharing correction

4.3. Evaluation test of DIPIX1 on spatial resolution

To confirm excellent spatial resolution in CZ-DIPIX1, the JIMA micro-chart was used [6]. Fig. 7 shows the lines and spaces pattern of the micro-chart. It was placed just in front of the detector and the distance is about a few mm. A normal focus X-ray generator, FR-D (Rigaku), was used for the imaging. In FR-D, a Cu target is installed and therefore the characteristic X-ray is about 8 keV. The detector was set far away about 300 mm from the target focus point. In this geometry, the contribution to spatial resolution from the focus size (0.3 mm) is small. Fig. 8 (a) shows a two-dimensional image of the chart with 40 kV – 50 mA of X-ray tube power. Since the lines are made from 1 μm-thick tungsten and silicon oxide, the X-ray absorption efficiency is very low and it requires longer time to obtain high contrast images. The output data was converted to negative contrast data and then averaged over 1000 images. The integration time in an image was set to 100 μs and therefore net integration

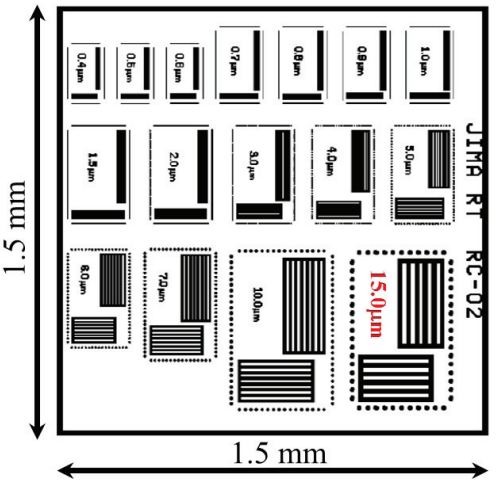


Fig. 7 lines and spaces pattern of the JIMA micro chart.

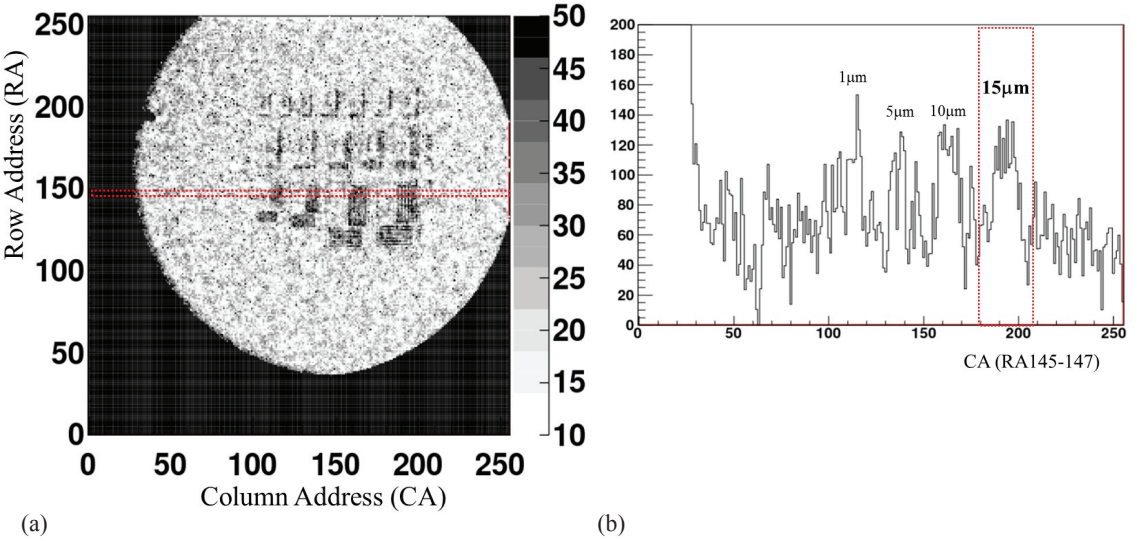


Fig. 8 (a) two-dimensional X-ray image of the JIMA micro chart and (b) column address profile indicated red dot lines in Fig. 8 (a). In Fig. 8 (b), the y-axis is in arbitrary unit.

time was 100 msec. Since the statistics were poor, 3 lines were summed up for one-dimensional projection. Fig. 8 (b) shows the projection distribution. It shows 5 lines of 15 μm slits can be seen. The important point is that it was measured not in a large magnification ratio with a micro-focus X-ray generator but in almost 1:1 with a normal-focus one with high power (a 3kW class). It proved the DIPIX1 has excellent spatial resolution, and even with a normal-focus X-ray generator, high resolution X-ray imaging can be achieved.

5. Current issues

The SOI pixel detectors were operated with the full depletion condition for the first time using FZ-SOI wafers. However, we also realized that the surface of the back side seems to have some problem. Fig. 9 shows I-V curve in FZ-INTPIX3e with different temperatures. The detector was set into a thermostat chamber to control the temperature. In this chip, the Chemical Mechanical Polishing (CMP) was treated at the back side and aluminium metals were not sputtered after the treatment. In Fig. 9, the X-axis is originally the back bias voltage but it is converted to estimated depletion depth with wafer resistivity (7 kOhm-cm) assuming the infinite bulk thickness. As mentioned in 4.2, the full depletion voltage might be about 100 V. When the estimated depletion depth exceeded 500 μm the leakage current started increase rapidly. It indicates that the further back side study is essential for the operation under full depletion condition. Thus

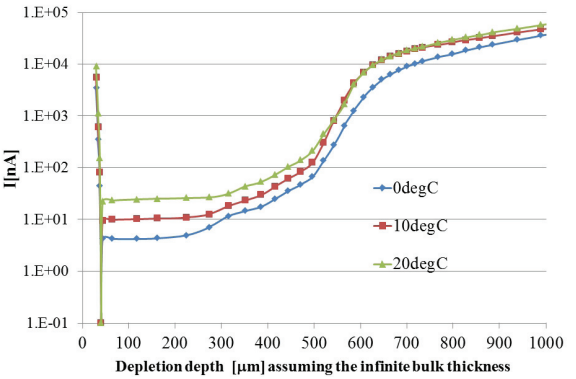


Fig. 9 Relationship between back bias current and calculated depletion thickness in FZ-INTPIX3e

we have started to optimize the back side and introduced additional processes such as an implantation at the back side and laser annealing and so on. After solving the back side issue, FZ-SOI detectors might be improved in spatial resolution, quantum efficiency, energy resolution, and MIP signal over full depletion condition.

6. Summary

Since 2005 we have designed several SOI pixel detectors and evaluated with visible light, X-ray and high energy charged particles. The fabrication process has recently been improved and CZ- and FZ-SOI detectors has been fabricated and tested. We found new process, BPW, affects the sensor gain and the BPW area size has to be decided carefully. Using the FZ-INTPIX3e detector, the first test chart images were obtained and the detector reached at full depletion condition. Because of the process improvements, we succeeded the reduction of pixel size in the integration-type pixel detectors and DIPIX1 showed an excellent spatial resolution. On the other hand, the detectors fabricated with FZ-SOI wafers have unknown problems to be figured out such as noise level and leakage current and the proper back side treatment is required. We will continue detailed studies and try further improvements in the quality of wafers, and then start demonstration for various application experiments.

Acknowledgements

The authors appreciate F. Takasaki and J. Haba for their continuing support to this project. The work is supported by KEK Detector Technology Project. The sensor gain measurements at KEK-PF were performed with the approval of KEK (Proposal No. 2009G617). This work is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration with Cadence Corporation, Synopsys Corporation, and Mentor Graphics Corporation.

References

[1] SOIPIX collaboration, http://rd.kek.jp/project/soi

[2] Y. Arai, et al., Nucl. Instr. And Meth. A 579 (2007) 706.

[3] Y. Arai, et al., Nucl. Instr. And Meth. A 636 (2011) S31.

[4] T. Miyoshi, et al., Nucl. Instr. And Meth. A 636 (2011) S237.

[5] T. Miyoshi, et al., in proceedings of the IEEE Nuclear Science Symposium Conference Record, 2010 IEEE, Oct. 30 2010-Nov. 6 2010 1885-1888

[6] Japan Inspection Instruments Mnufactures Association, http://jima.jp/english/index.html