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A COMPACT TIME DIGITIZER IN CAMAC FORMAT*

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ABSTRACT

A compact time digitizer containing 128 words of 16 bits each on a single width CAMAC module is described. Eight data channels are provided with a capacity of 16 words each. The unit has been used with a 50-MHz clock to encode data from magnetostrictive spark chambers and--with modifications--for the accumulation of data from multiwire proportional chambers.

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Introduction

A frequently encountered problem in the electronic processing of information is the measurement and recording of the time separation of a sequence of electrical signals. For example, in processing the information from a large assembly of magnetostrictive spark chambers, as many as 1000 independent measurements of this type may have to be made for a single event. Random access memory elements (RAM) offer great economical advantages for storage of such large quantities of data. However, it is often desirable to have better time resolution than can be obtained directly from the standard device. The goal of improved time resolution has been achieved in the present design by effecting an intermediate storage of two low order bits in a fast memory with subsequent transfer of the complete information to the RAM in synchronism with higher order clock bits (see block diagram, Fig. 1). The time resolution of the instrument is 20 nsec, but 10 nsec can be achieved with only minor modifications of the design.

It should be noted that the digitizer takes the timing information from the leading edge of the data pulse. However, signals from magnetostrictive chambers require timing of the centroid of the pulse for optimum resolution. Since a digital determination of the centroid would be quite impractical for the method of encoding used here, a preprocessing of the signals, e.g., through analogue center-finding circuitry, is necessary.

A further application for the digitizer is the encoding of information from proportional wire chambers (PWC). In this case the original information is contained as a bit pattern in a long shift register which

is read out serially. The digitizer performs the address encoding of the true bits and, since the shift-clock frequency can be matched to the time resolution of the RAM, there is no need for intermediate storage of low order bits.

Summary of Data Processing

Prior to the arrival of the data pulses, the time separation of which is to be determined, most of the digitizer circuitry is without power. A clear pulse provided on a bussed CAMAC patch pin brings power up, clears the address scalers for the RAMs, clears the central clock, clears the word count for the readout of the information and sets the unit into the mode for processing data pulses.

A few microseconds after the clear pulse, clock pulses are distributed to all units via a second patched CAMAC bus, incrementing the central clock (one per module). After a predetermined number of clock pulses, each unit will terminate the data acquisition cycle and be ready for readout of data via the CAMAC data bus.

During data acquisition, the time separation of up to sixteen data pulses in each of eight independent channels will be encoded. If more than 16 pulses are provided, later data will override the information in the last word of a given channel.

Test pulses can be distributed instead of normal data via a bussed CAMAC patch pin to all eight channels of each module. A computer program then tests the equality of the data in all the channels of the system.

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The last step in the sequence is the readout of the data, using the CAMAC block transfer. Power is switched off automatically after a predetermined time interval of several milliseconds, which must be matched to the read speed of the system. Alternately, power could be turned off after reading the last word, i.e., module is addressed and generates no Q response.

Circuitry for the Intermediate Storage of Low Order Bits

In order not to be limited by the time resolution of the RAM, a fast storage of two low order bits precedes storage of the complete information in the RAM (see block diagram, Fig. 1). Storage of only two bits rather than the complete word obviously results in significant savings in circuitry. However, due to the asynchronous arrival of signals relative to the internal clock, some logic has to be provided which locks in on the clock phase. Storage and synchronization is achieved using the circuitry shown in Fig. 2 in each channel. The lowest data bits (A and B in Fig. 2) are presented in the form of a Gray code which involves the change of only one bit in any time interval shorter than the resolving time.

An input signal activates the parallel clock input of the 7495 data storage register (CK2, Fig. 2), resulting in the storage of data bits A and B and raising of a flag at Q4. The flag clamps the parallel clock input and provides data to a latch bit (1/4 of 7495). The next pulse of the central clock starts the data transfer cycle by setting the latch bit which in turn switches the shift register into serial mode and removes the data to the latch bit. A second clock pulse lowers the flag in the data register by serially loading the low level at D_{ser} and resetting the latch. The input is now ready to accept the next signal.

The diagram shown in Fig. 3 indicates the time sequence of signal processing. The period of the lowest clock bit directly transferred to the RAM (data bit 3) is 80 nsec. This sampling time interval is subdivided into 20 nsec intervals by data bits A and B. (A third Gray code bit with a 20 nsec half-period could be added to give 10 nsec resolution.) The Gray code bits are then decoded into regular binary code through exclusive or gates, which is done most conveniently when transferring the information from the RAM to the CAMAC bus as shown in Fig. 8.

Input signals occurring near the limits of the sampling time interval may lock in on the previous or following sampling periods. Consider a pulse arriving at -21 nsec on the timing diagram (Fig. 3), i.e., within the 'input' range shown: the strobe locks in on the low phase of data bit 3 and the decoded time reads 3 units. An input signal arriving at -19 nsec, i.e., in the next sampling interval, will lock in on the phase where data bit 3 is high, corresponding to 4 time units. The Gray code bits have not changed, but their interpretation--with the help of data bit 3--now yields 0 (cf 3 previously). This method insures a monotonic encoding of time.

Depending on the relative phase of clock and input pulses, a pulse pair will be resolved when the pulses are from 120 to 200 nsec apart. This is relevant if data from PWC are to be encoded with the instrument as designed for spark chamber readout. Data can be provided at a maximum rate of 5 MHz and all addresses will increment in steps of 10 with this choice of frequencies.

Address Averaging for Proportional Wire Chamber (PWC) Data

When the passage of a single charged particle results in the setting of two adjacent wires, the average of these addresses will in general be used in the subsequent processing of the data. For this reason, a hardware system averaging neighboring addresses is implemented in the version of the digitizer used for PWC readout. This circuitry replaces the now unnecessary storage of low order bits. In this scheme all wire addresses are encoded in increments of two. When two adjacent wires are hit, the lowest order bit is also set, thus recording for n adjacent wires the (n - 1) average positions between them. Note that with this method of encoding the original wire addresses can always be reconstructed.

In a particular experiment, we found that an occasional long sequence of wire addresses would overflow the data buffer, resulting in a loss of information. The radical approach of truncating any sequence after the first two addresses solved this problem.

The logic for achieving the address averaging, both for complete and for truncated sequences, is explained with the help of Fig. 4. Incoming data are strobed into the shift register 7495 and shifted right by a succession of clock pulses. If a data bit is shifted into position Q2, an address will be stored in the RAM (except for the last hit in a sequence). In addition, the lowest bit will be set if position Q1 also contains data. The truth table (Table I) indicates the storage operations resulting from the different bit configurations.

Synchronous Clock

The circuitry (see Figs. 5 or 6 for spark chamber or PWC version respectively) provides the time reference for encoding the data pulses. It consists of a synchronous scaler generating the binary data bits for direct transfer to the RAMs and the Gray Code data bits A and B of the spark chamber version (Fig. 5). In addition, it provides strobe and clock pulses controlling the transfer of data. The highest bit indicates the end of the data acquisition cycle.

Data Format and Addressing of the Random Access Memory (RAM)

As there is no time to clear memory before data acquisition, an alternative method is used in the spark chamber version to indicate valid data (see Fig. 5). Data are written into memory in ascending order from address zero up to a maximum address of fifteen, activating the count up input of the addressing scaler 74193 (row 7) after each transfer.

Reading of the data proceeds in descending order cycling through all sixteen addresses, with each CAMAC read command generating a count-down transition for the addressing scaler at the end of each read cycle (Fig 5, pin 4, row 7). Address zero, which contains the first written word, puts up a flag on a high order bit (we use bit 18) to indicate the last valid word. (Data words after the flagged word are to be disregarded.) The ambiguity between no data and 16 words of data can be resolved by fiducial words or through the monotonic nature of the data. Due to the power pulsing (described below), old data are destroyed after each event. The up-down counter 74193 provides a carry

signal which is used for clamping at address 15 when writing into ascending locations. The last word will thus contain the arrival time of the last pulse of 16 or more. The borrow signal, when reading in descending order, provides the flag to indicate the last valid word. This can be used to transfer to the next channel if the transfer time has to be minimized.

In the version for PWC read out (Fig. 6), a more conventional scheme is used. Prior to reading a given channel, the word count is transferred to an auxiliary register (7495 in position A9, Fig. 6). The addressing scaler is then cleared and read out proceeds in ascending order, with the word count transferred from the auxiliary register as the last word of a channel.

Readout of the data is performed using the CAMAC block transfer mode (see Fig. 7). At the end of the encoding cycle, defined by the clock reaching a predetermined value, the first word is selected and will appear when the module is addressed with the read function (F0 or F2). Each S2-strobe advances selection to the next word. On the last word the card does not generate Q, signaling the end of the data block. The spark chamber version transmits the maximum of 128 words per card, but smaller numbers of words can be programmed, e.g. five per channel in the PWC version.

Gating of Data onto CAMAC Bus

The RAMs used here put out data during the storage operation. Thus, the presence of a digitizer in a CAMAC crate makes it impossible to read data from any module in the crate during data accumulation if no further gating is provided. Furthermore, many crate controllers do not lock out data when transmitting LAM information, which without further gating,

prevents determination of the LAM status of the CAMAC crate during the digitization. For these reasons, gating of data with the module address is advisable. A gating method involving a minimum of additional circuitry and wiring consists in buffering each bit through a section of a 7407 open collector driver (Fig. 8). Gating of the data is accomplished by turning the supply voltage of the 7407 on during read only. The response of this arrangement easily matches the speed requirements of the CAMAC read cycle. The decoding of the Gray Code bits A and B into regular binary code is most effectively done at this stage (insert "spark chamber version," Fig. 8).

Power Pulsing

The 32 units of 64-bit memory dissipate a considerable amount of heat with the complete module drawing 3 A at 6 V. Ten or more modules side-by-side in a CAMAC crate cannot be effectively cooled. For this reason, a power pulsing scheme has been used which keeps the circuitry very cool, insuring a long life of the integrated circuits. At event time, power is turned on and the logic cleared (Fig. 9). After 1 μsec, before arrival of the first signal, full DC power is established. The power is kept on during several milliseconds, during which time data are accumulated and transferred to the computer. Power is then switched off automatically.

Testing and Monitoring

For a thorough check of the instrument, a computer is nearly indispensable. It was found from experience that all bit combinations

have to be tested repeatedly because of unavoidable wiring and soldering errors and because of malfunctions of individual memory locations in the RAM itself. Through an or-circuit in the input (See Fig. 2, spark chamber version), all channels are permanently connected to a common test line. This test line carries computer-generated pulse trains of variable length and pulse separation. The time separation of these pulses is encoded in all channels simultaneously and the result is read back and checked against the expected numbers from the known pulse sequence. Any detected errors cause a detailed printout which provides the information needed to track down the malfunction.

Operational Experience

The digitizing system for encoding data from magnetostrictive spark chambers has been used in an experiment at Brookhaven National Laboratory since the winter of 1972. Up to ten modules with a total of 1280 words (filling one half of a CAMAC crate) have been operated simultaneously and with a minimum of maintenance after debugging of the system. The version for encoding PWC information--in which low order bit storage has been replaced by address averaging--has been in use in an experiment at SLAC since early 1975.

Acknowledgement

I am most grateful to Dr. W. E. Cleland for the many discussions of the design and suggestions for improvements. The computer-based test scheme, designed by him, proved invaluable in finding elusive or intermittent malfunctions.

FIGURE CAPTIONS

Fig. 1 Block diagram of data storage using a fast buffer for two two low order bits.

Fig. 2 Circuitry for intermediate storage of two low order bits and subsequent transfer to the main memory (RAM)--one of eight channels. The decoding of the Gray Code bits--shown here following storage in the intermediate register--is actually performed when reading the information from the RAM.

Fig. 3 Time sequence of signal processing for storage and transfer of low order bits.

Fig. 4 Circuitry for address averaging of two (or more) input signals arriving with a time separation of one clock period between successive signals. (Version for proportional wire chamber readout.)

Fig. 5 Circuit diagram for digitizer version for encoding data from magnetostrictive spark chambers.

Fig. 6 Circuit diagram for digitizer version for encoding data from proportional wire chambers.

Fig. 7 Readout logic for CAMAC block transfer. Sixteen words in each of eight channels are read in response to CAMAC read commands.

Fig. 8 Gating and decoding of data for CAMAC read operation.

Fig. 9 Power pulsing and initialization.

TABLE I

Truth table of storage operations as a function of bit patterns stored in the shift register. (Digitizer version for proportional wire-chamber readout.)

Q1	Q2	Q3	Version for Recording All Wire Addresses	Version to Suppress All but Leading Address of Sequence
0	1	0	transfer single address	
1	1	0	transfer averaged address	
1	1	1	transfer subsequent averaged address	no transfer
0	1	1	no transfer	

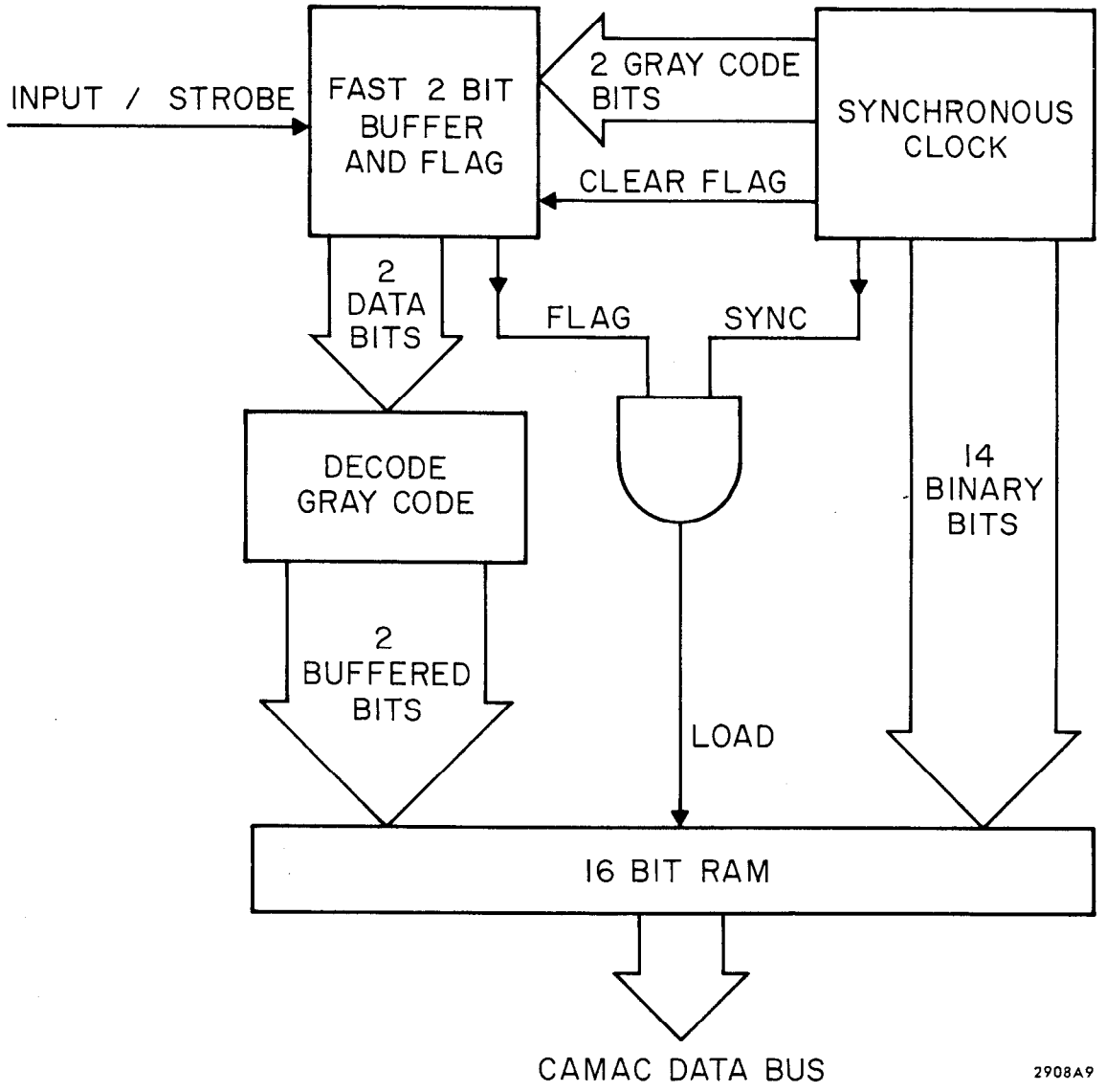
INPUT / STROBE
FAST 2 BIT BUFFER AND FLAG
2 GRAY CODE BITS
CLEAR FLAG
SYNCHRONOUS CLOCK
2 DATA BITS
FLAG
SYNC
DECODE GRAY CODE
14 BINARY BITS
2 BUFFERED BITS
LOAD
16 BIT RAM
CAMAC DATA BUS
2908A9

Fig. 1

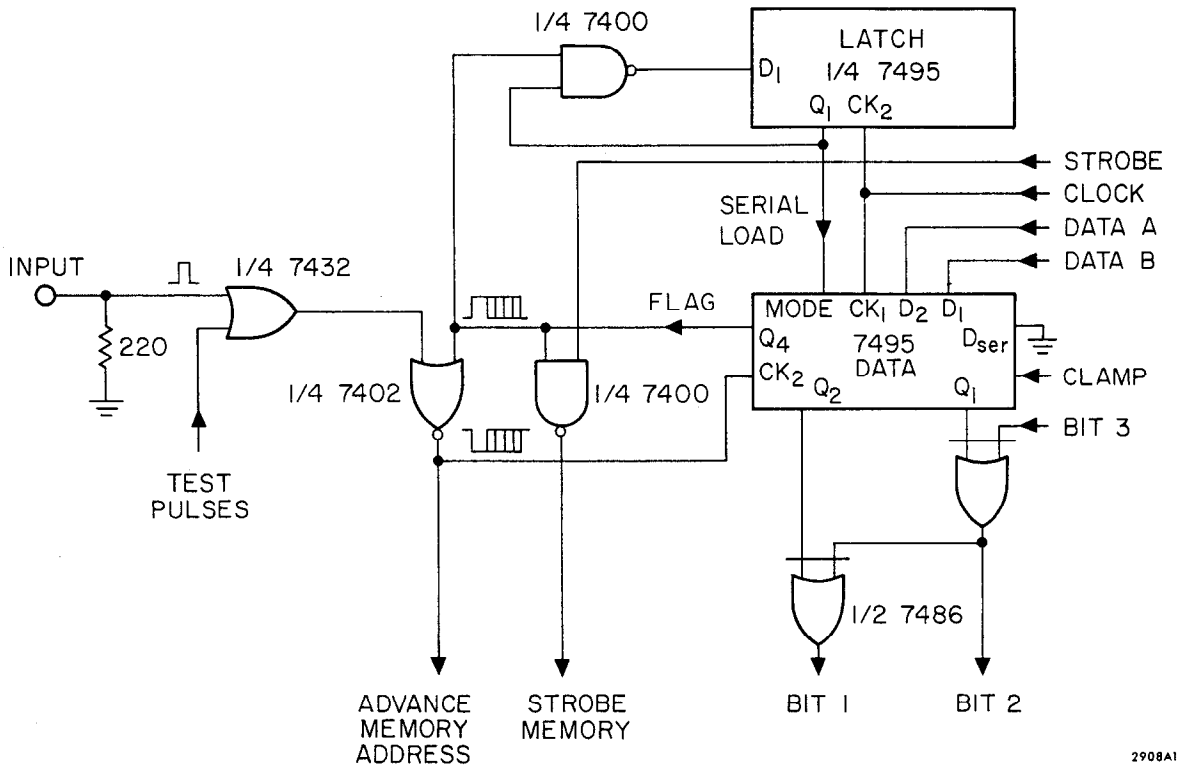
1/4 7400
LATCH
D1 1/4 7495
Q1 CK2
STROBE
CLOCK
DATA A
DATA B
SERIAL
LOAD
INPUT
1/4 7432
220
FLAG
MODE CK1 D2 D1
Q4 7495 Dser
CK2 Q2 DATA
Q1
CLAMP
1/4 7402
1/4 7400
BIT 3
TEST
PULSES
1/2 7486
ADVANCE
MEMORY
ADDRESS
STROBE
MEMORY
BIT 1
BIT 2
2908A1

Fig. 2

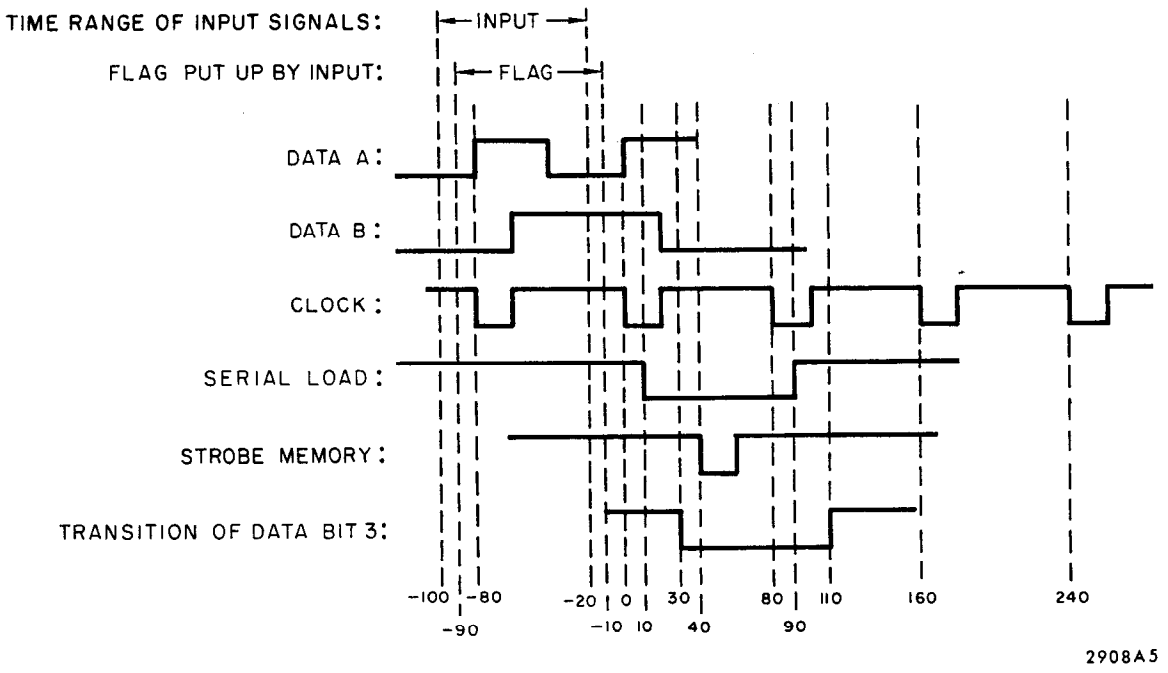
TIME RANGE OF INPUT SIGNALS:
INPUT
FLAG PUT UP BY INPUT:
FLAG
DATA A:
DATA B:
CLOCK:
SERIAL LOAD:
STROBE MEMORY:
TRANSITION OF DATA BIT 3:
-100
-90
-80
-20
-10
0
10
30
40
80
90
110
160
240
2908A5

Fig. 3

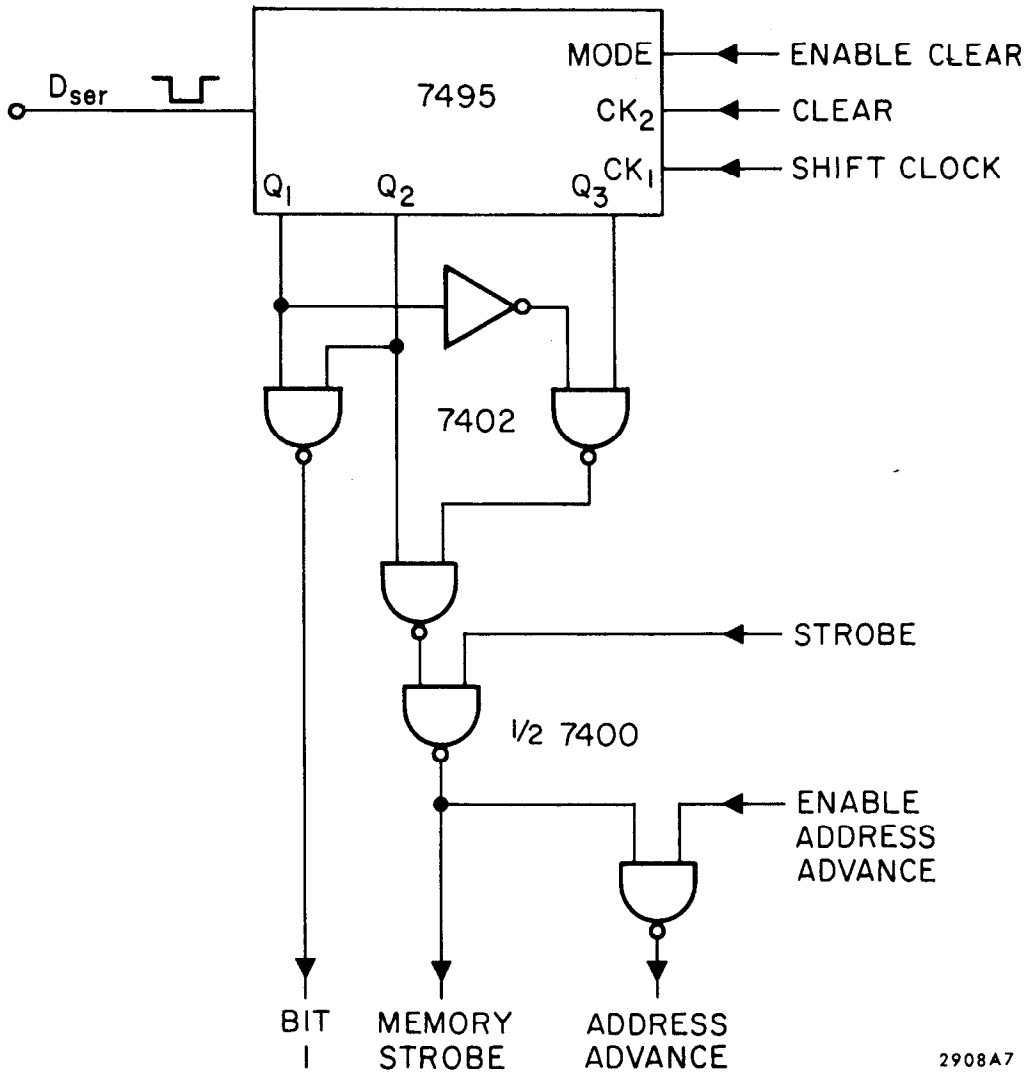
Dser
7495
MODE
CK2
CK1
Q1
Q2
Q3
ENABLE CLEAR
CLEAR
SHIFT CLOCK
7402
STROBE
1/2 7400
ENABLE
ADDRESS
ADVANCE
BIT
I
MEMORY
STROBE
ADDRESS
ADVANCE
2908A7

Fig. 4

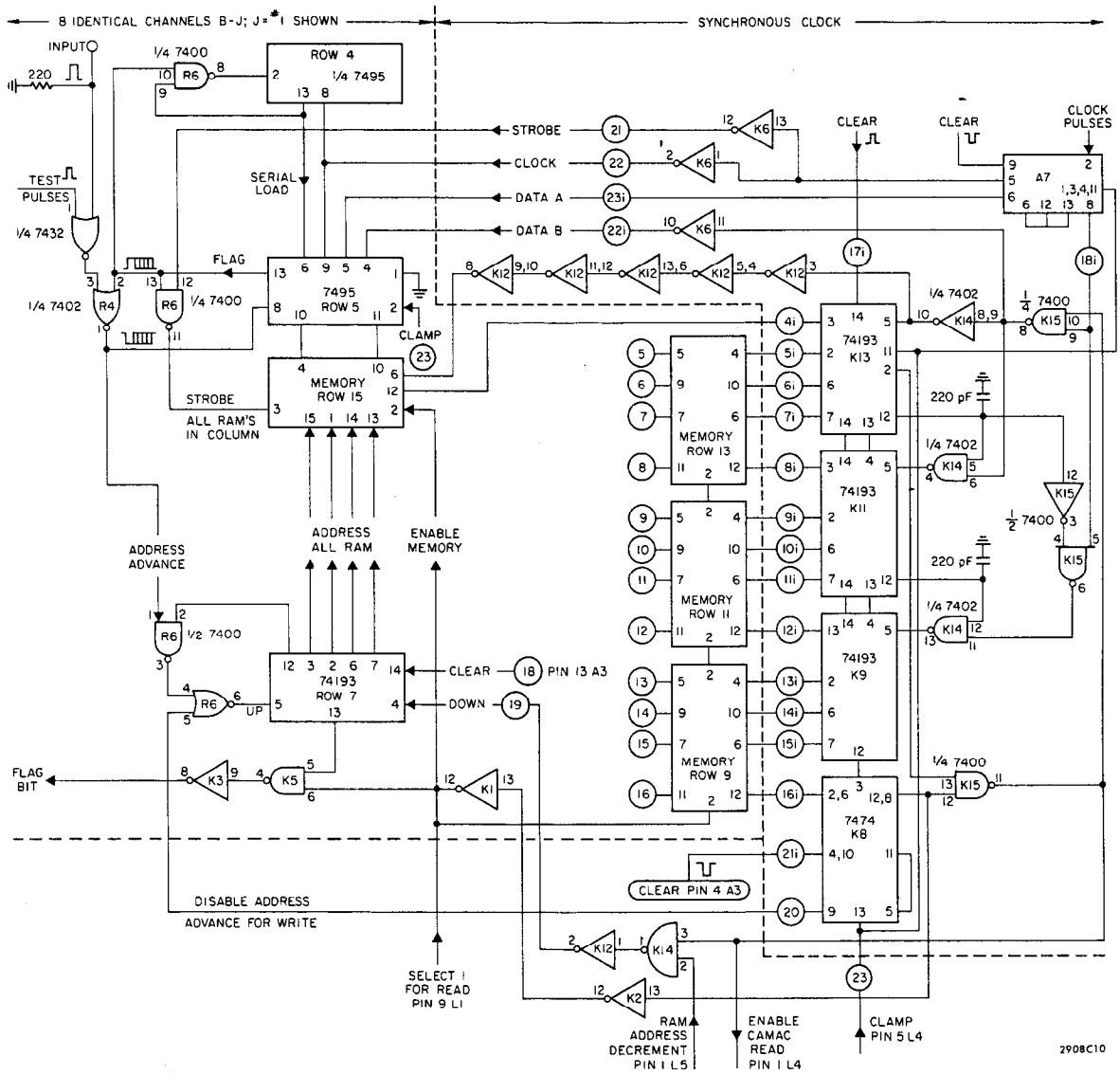
8 IDENTICAL CHANNELS B-J; J=*1 SHOWN
SYNCHRONOUS CLOCK
INPUT
220
1/4 7400
R6
ROW 4
1/4 7495
STROBE
CLOCK
DATA A
DATA B
SERIAL LOAD
TEST PULSES
1/4 7432
1/4 7402
R4
R6
1/4 7400
FLAG
7495 ROW 5
CLAMP
MEMORY ROW 15
STROBE ALL RAM'S IN COLUMN
ADDRESS ADVANCE
ADDRESS ALL RAM
ENABLE MEMORY
1/2 7400
74193 ROW 7 13
UP
DOWN
CLEAR
PIN 13 A3
FLAG BIT
K3
K5
K1
DISABLE ADDRESS ADVANCE FOR WRITE
SELECT 1 FOR READ PIN 9 L1
K12
K14
K2
RAM ADDRESS DECREMENT PIN 1 L5
ENABLE CAMAC READ PIN 1 L4
CLAMP PIN 5 L4
MEMORY ROW 13
MEMORY ROW 11
MEMORY ROW 9
74193 K13
74193 K11
74193 K9
7474 K8
CLEAR PIN 4 A3
K6
CLEAR
CLOCK PULSES
A7
1,3,4,11
220 pF
1/4 7402
1/4 7400
K15
2908C10

Fig. 5

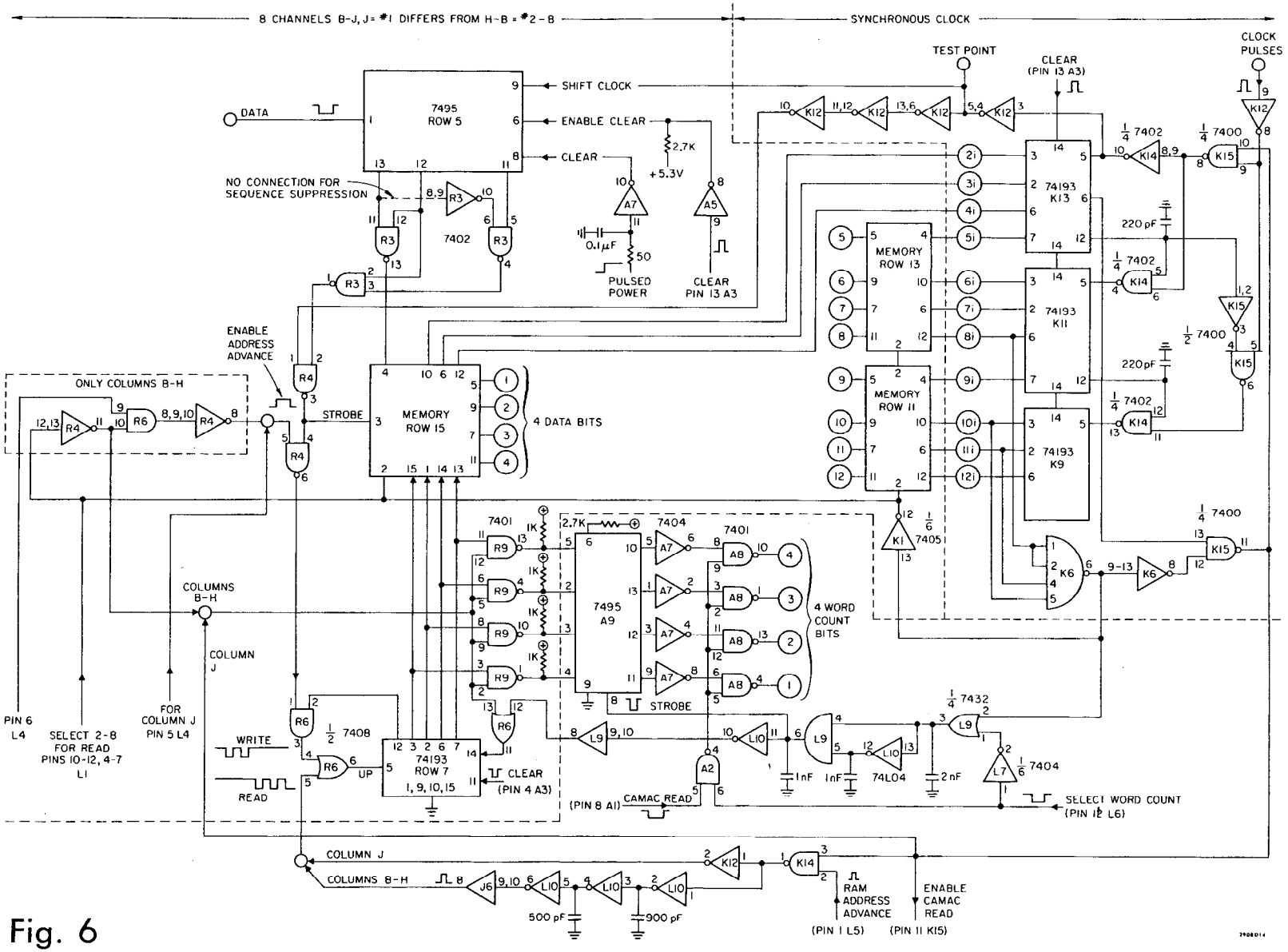
8 CHANNELS B-J, J= #1 DIFFERS FROM H-B = #2-8
SYNCHRONOUS CLOCK
TEST POINT
CLEAR (PIN 13 A3)
CLOCK PULSES
DATA
7495 ROW 5
SHIFT CLOCK
ENABLE CLEAR
CLEAR
2.7K
+5.3V
NO CONNECTION FOR SEQUENCE SUPPRESSION
7402
0.1μF
50
PULSED POWER
CLEAR PIN 13 A3
ENABLE ADDRESS ADVANCE
ONLY COLUMNS B-H
STROBE
MEMORY ROW 15
4 DATA BITS
MEMORY ROW 13
MEMORY ROW 11
74193 K13
74193 K11
74193 K9
220 pF
7400
7402
7405
7401
7404
7495 A9
4 WORD COUNT BITS
COLUMNS B-H
COLUMN J
PIN 6 L4
SELECT 2-8 FOR READ PINS 10-12, 4-7 L1
FOR COLUMN J PIN 5 L4
WRITE
READ
7408
UP
74193 ROW 7
1, 9, 10, 15
CLEAR (PIN 4 A3)
CAMAC READ
(PIN 8 A1)
74LO4
7432
7404
SELECT WORD COUNT (PIN 12 L6)
500 pF
900 pF
RAM ADDRESS ADVANCE (PIN 1 L5)
ENABLE CAMAC READ (PIN 11 K15)

Fig. 6

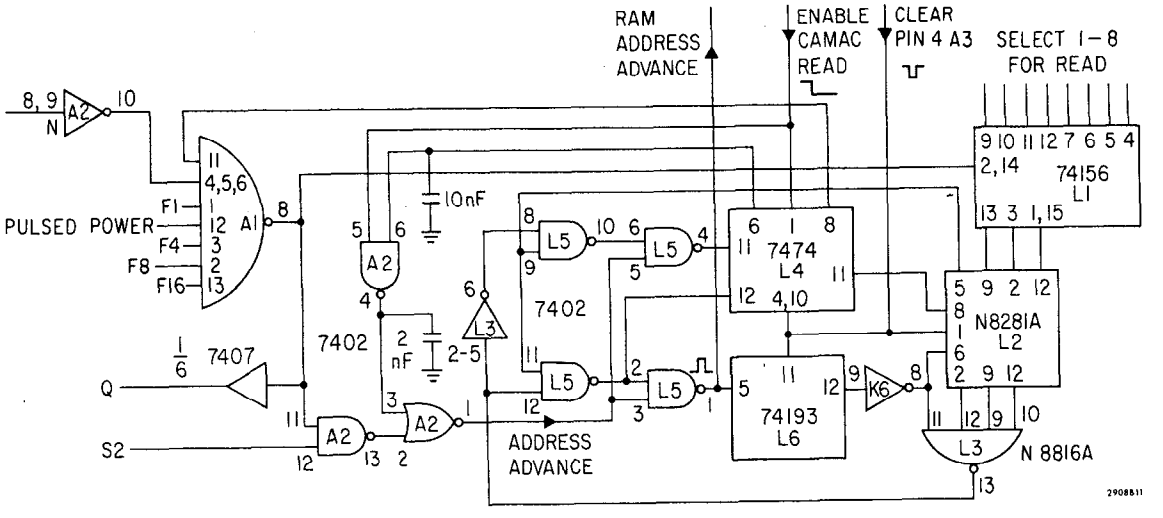
RAM
ADDRESS
ADVANCE
ENABLE
CAMAC
READ
CLEAR
PIN 4 A3
SELECT 1-8
FOR READ
8, 9
N
A2
10
PULSED POWER
F1
F4
F8
F16
11
4,5,6
1
12
A1
3
2
13
8
10nF
5
6
A2
4
7402
2
nF
2-5
6
L3
8
L5
10
6
9
L5
4
5
7402
11
L5
12
2
L5
3
1
6
1
8
11
7474
L4
11
12
4,10
5
11
12
74193
L6
9
K6
8
9 10 11 12 7 6 5 4
2,14
74156
L1
13 3 1,15
5
9
2
12
8
1
6
2
9
12
N8281A
L2
11
12
9
10
L3
N 8816A
13
1/6
7407
Q
S2
11
A2
12
13
2
A2
3
1
12
ADDRESS
ADVANCE
2908811

Fig. 7

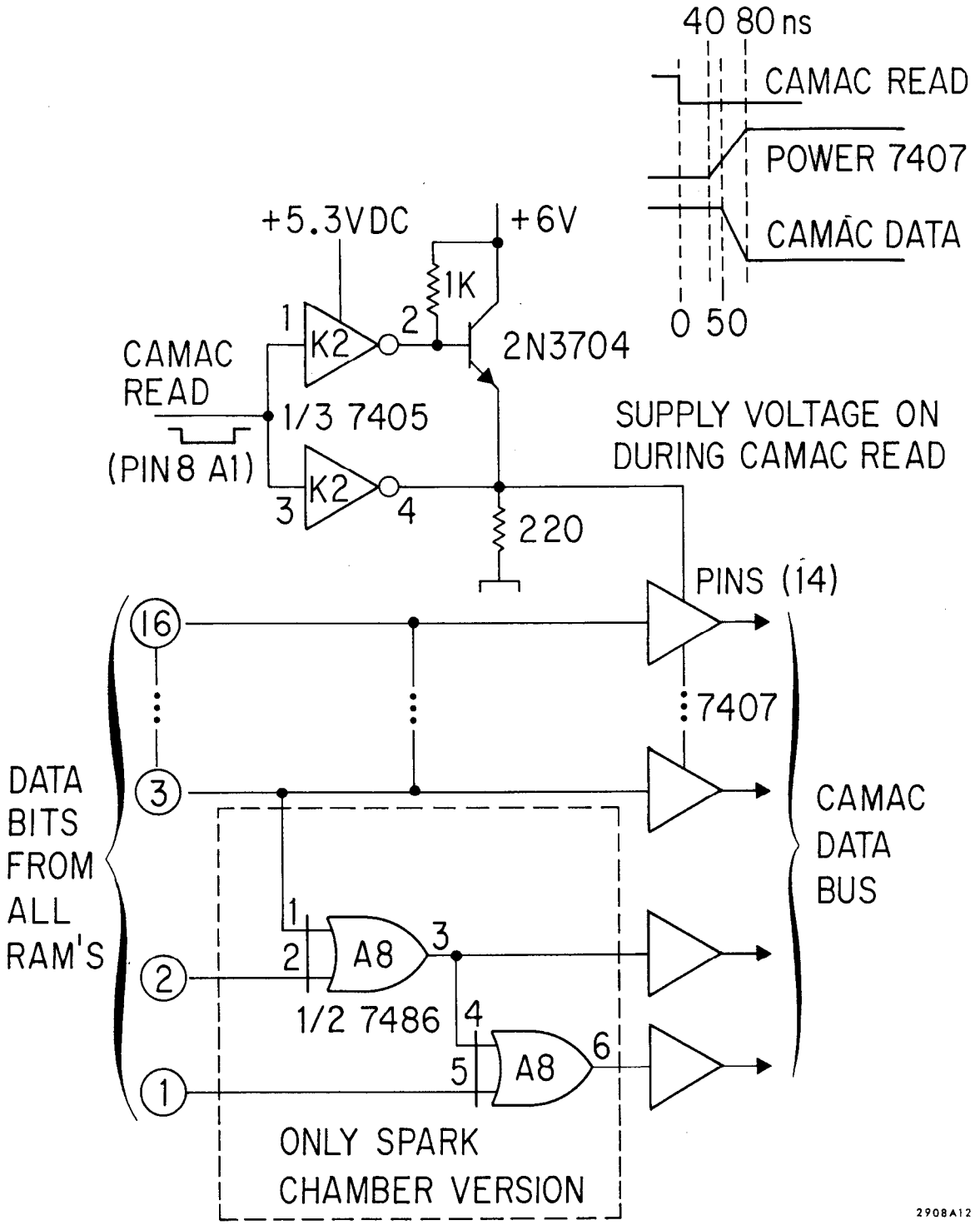
40 80 ns
CAMAC READ
POWER 7407
CAMAC DATA
0 50
+5.3VDC
+6V
1K
2N3704
CAMAC READ
(PIN 8 A1)
1/3 7405
K2
K2
220
SUPPLY VOLTAGE ON DURING CAMAC READ
PINS (14)
7407
DATA BITS FROM ALL RAM'S
CAMAC DATA BUS
A8
A8
1/2 7486
ONLY SPARK CHAMBER VERSION
2908A12

Fig. 8

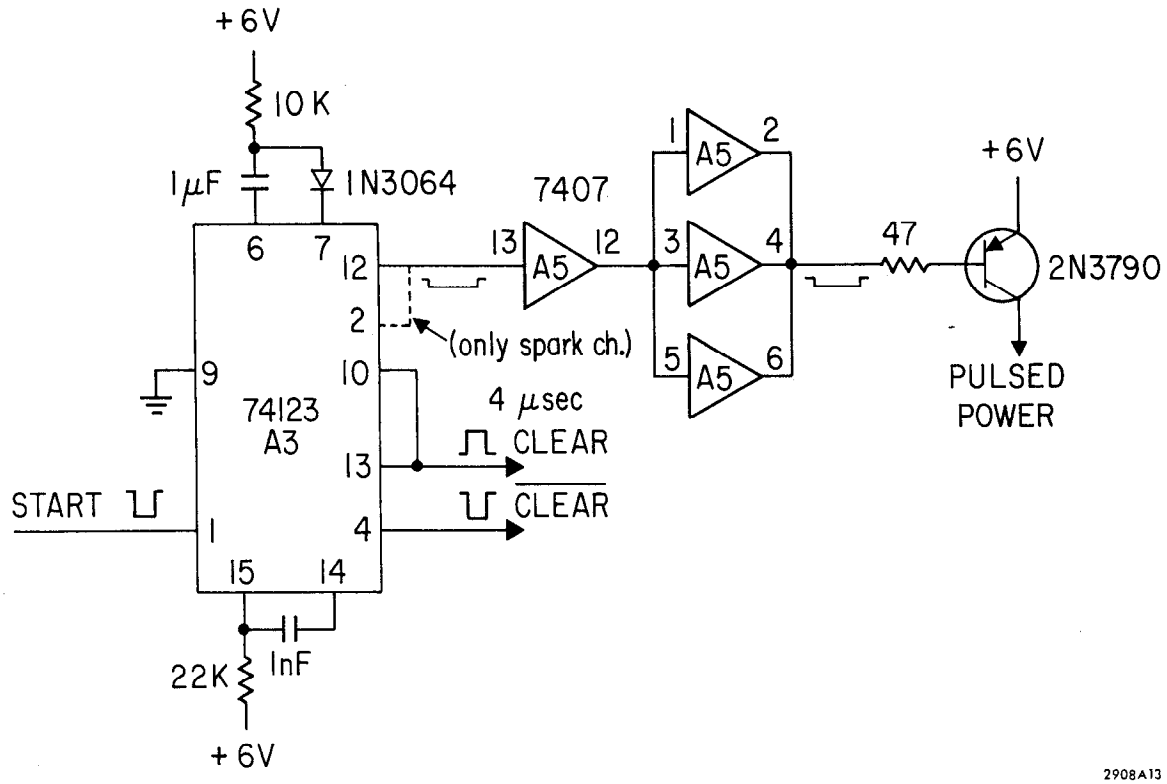
+6V
10K
1μF
1N3064
7407
74123
A3
START
(only spark ch.)
4 μsec
CLEAR
CLEAR
22K
1nF
+6V
A5
47
+6V
2N3790
PULSED
POWER
2908A13

Fig. 9