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DESIGN AND PERFORMANCE TEST OF 8 CHANNEL 125 MS/s DIGITIZER WITH 16-BIT RESOLUTION FOR BPM AND LLRF APPLICATION

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Abstract

In this paper, a mezzanine card is designed based on high speed ADC for particle accelerator field. FPGA firmware was built to realize high-speed A/D conversion. The performance of the ADC on the board was tested. The experimental results show that the ENOB of the ADC with a sampling rate of 125 MSPS can be as high as 12.6.

MANUSCRIPTS

In modern accelerator applications, stringent requirements are placed on the noise performance of digital converters. The noise from the digital converter will become part of the field noise seen by the beam, thus necessitating a low-noise, low-crosstalk digitizer. In response to this demand, this paper presents the design of a digital converter circuit board with 8 analog-to-digital converter (ADC) channels which has been subjected to testing. The test results indicate that the circuit board possesses low noise characteristics, rendering it suitable for reading accelerator signals.

Hardware Design

Figure 1 is the design block diagram of the mezzanine card. The circuit board has 8 SSMC RF connectors, providing 8 analog signal inputs for the ADC. The single-ended analog signal is converted into a differential signal after passing through the fully differential ADC driver. In addition, in order to facilitate the adjustment of the DC voltage component at the ADC input, the DAC output set voltage value is also required to be connected to the reverse input of the fully differential amplifier. The input clock of the ADC is 125 MHz, which is provided by the FMC connector. After the ADC collects and converts the analog signal, it is transmitted to the FMC connector in the form of an LVDS signal, and then provided to the FPGA.

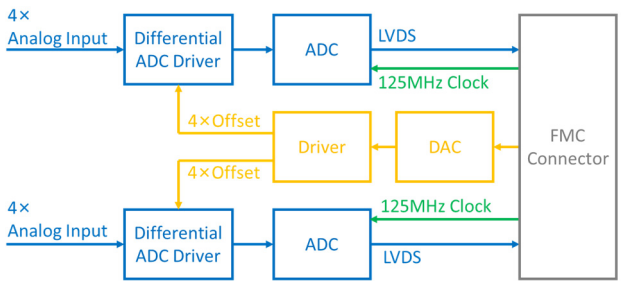

Figure 1: Block diagram of the design.

Figure 2 is the design PCB drawing of the mezzanine card, and Figure 3 is the actual picture of the PCB after welding. The PCB has a total of 8 layers, which can be divided into ground, power and signal layers. When designing, attention should be paid to impedance matching and data line length processing. In addition, during the design process, through a brief evaluation of noise, a low-noise power supply solution was selected to achieve better performance.

The ADC is ADI's AD9653, which is a 4-channel, 16-bit, 125 MSPS ADC with a conversion rate of up to 125 MSPS, excellent dynamic performance and low power consumption. The DAC is ADI's AD5686, which is a low-power, four-channel, 16-bit buffered voltage output DAC.

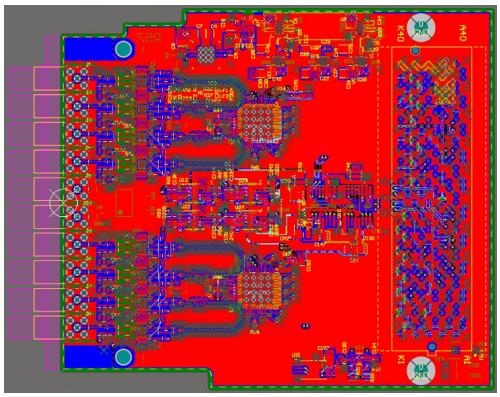

Figure 2: PCB design drawing.

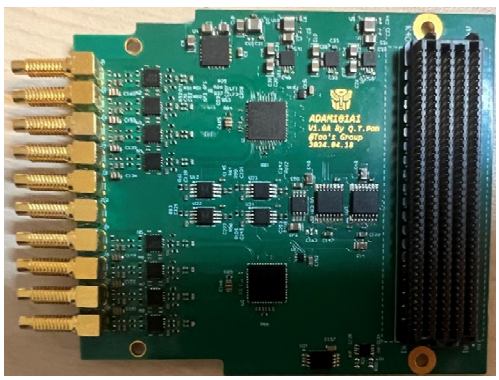

Figure 3: PCB picture.

Firmware Design and Experiment

The FPGA readout firmware is designed refer to the timing diagram in the AD9653's datasheet. The ADC readout firmware logic block diagram is shown in Figure 4. The figure shows the readout logic for only one channel; the other channels are similar.

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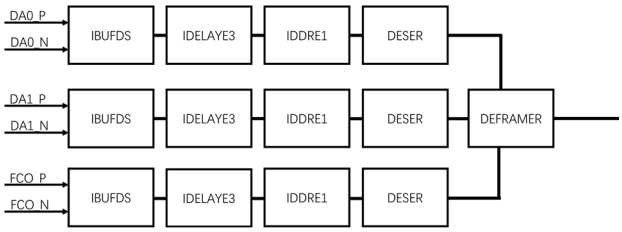

Figure 4: A one line figure caption is centred.

The experiment uses the SMA100B signal source to generate a sine wave signal and 125 MHz clock.

Change the registers of AD9653 through SPI protocol, so that they work in the appropriate state. The FPGA used for data readout is XCKU060-FFVA1156-2. The output of the ADC is read and analyzed by ILA.

Result

The ADC's ENOB can be as high as 12.6 when using an internal 1.3 V reference voltage. The experimental conditions for the figure on the right are an ADC sampling rate of 125 MHz and a sine wave signal source frequency of 10 MHz. Table 1 summarizes the ENOB test results of this design. The ENOB test results of the 8 channels are close, all above 12.6.

Table 1: ADC ENOB Experiment Result

Clock	Channel	ENOB
125MHz	ch0	12.6738
125MHz	ch1	12.6515
125MHz	ch2	12.6382
125MHz	ch3	12.6637
125MHz	ch4	12.6749
125MHz	ch5	12.6536
125MHz	ch6	12.6401
125MHz	ch7	12.6805

CONCLUSION

This paper designs a low noise data conversion module for BPM and LLRF applications. The ENOB of the ADC can be tested up to 12.6.