Design and Characterization of a Monolithic Non-delay Line Constant Fraction Discriminator for In-house Nuclear Physics Experiments with CPDA at VECC

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Introduction

Several discrete preamplifier and shaper modules from Mesytec [1] had been used as Front end Electronics (FEE) to process the signal of high-resolution, high-granularity 4π Charged Particle Detector Arrays (CPDA), developed at VECC. The preamplifier module, a sixteen channel charge sensitive amplifier (CSA), was placed near the detectors and another sixteen channel shaper-amplifier NIM module (MSCF-16), was housed 1-2 meter apart to shape and amplify the output of CSA. The energy spectroscopy was carried out by using a peak sensing ADC. The timing signal with amplitude walk of about ±1 ns of the shaper-amplifier module was used to generate the gate signal for the peak sensing ADC. The total number of modules for the complete CPDA was 72 and the heat dissipation per channel was of the order of 600 mW which is higher than the desired by the experiment. Apart from this, an unwanted noise was introduced due the different geographical placement of CSA and shaper modules.

To alleviate these problems, replacement of these modules in the form of ASIC was planned in-house with the motivation of developing low-cost indigenous compact front-end electronics to achieve the exact required specification for the CPDA in terms of low power, low noise and leakage current compensation circuit which are not present in these commercial modules. The CSA and shaper ASIC were already designed and tested. However, the monolithic design of the discriminator was taken separately due to several design challenges in terms of achieving sub-nanosecond timing resolution which are important to be addressed separately. The final designs were planned to be integrated in a single ASIC.

This paper describes the mixed-signal design and characterization of a non-delay line Constant Fraction Discriminator (CFD) using 0.18 µm CMOS technology of SCL, Chandigarh.

Design of Monolithic CFD Circuit

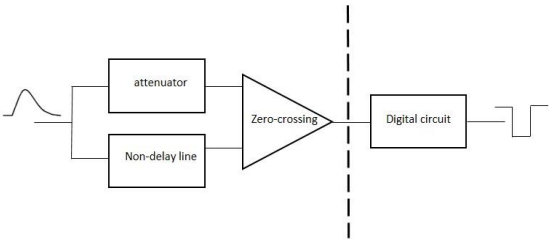

Fig. 1 *The mixed-signal blocks of discriminator*

A generic model of CFD was shown in Fig. 1. For monolithic implementation, the attenuator block of the non-delay line CFD was made using poly-resistors. The delay line was replaced with a first order low pass RC filter for designing non-delay line CFD [2], [4]. The RC circuit was made using a poly-resistor and a mim-cap. The RC time constant was kept 1 ns as the circuit was

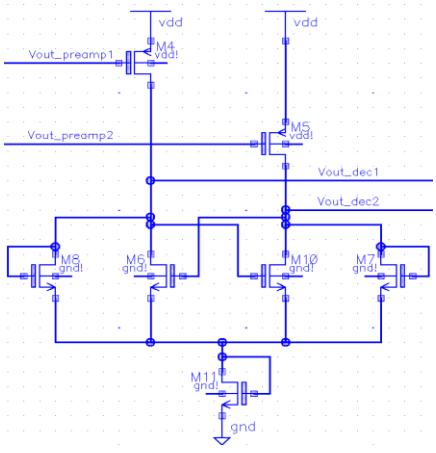

Fig. 2 *The regenerative comparator*

designed for input pulses having minimum value of rise time of about 25 ns. Both the outputs of the attenuator circuit and the RC filter circuit were followed by a voltage buffer to avoid loading effects. The outputs of the buffer were fed to a zero crossing circuit which consists of a difference amplifier and high performance comparator. The difference amplifier was needed to obtain the bipolar pulse whose zero crossing was independent of amplitude and rise time of the input pulse. The high-performance voltage comparator has a preamplifier, a regenerative comparator and an output buffer [3]. The output of the zero-crossing detector was the interface with the digital circuit. The positive-feedback regenerative circuit as shown in Fig. 2 and the output buffer was used to generate the logic signal. The output buffer was a self-biased differential amplifier followed by an inverter.

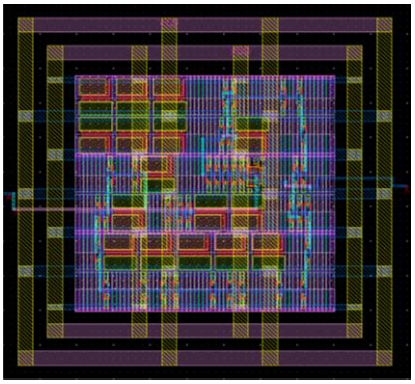

Fig. 3 *The layout of the digital circuit*

The purpose of the digital circuit, designed using the standard cells, was to generate a short trigger pulse compatible to drive the standard NIM modules. A series of inverters were used to delay and invert the comparator output from one path. A logical AND operation between the original comparator output and the delayed inverter output generated a short pulse. The layout of the digital circuit was shown in Fig. 3.

Results

The realistic simulations were performed to characterize amplitude walk, rise time walk and drift of the presented CFD. The peak amplitude of input pulse was varied from 100 mV to 1 V above the dc level and amplitude walk was measured. The maximum amplitude walk obtained was about 208 ps for 100 mV amplitude input. Similarly, the rise time walk by varying the rise time between 25 to 35 ns was measured at constant peak amplitude of 1 V and walk of about 29 ps was obtained. Fig. 4 shows plot of amplitude walk (lower x-axis) and rise time walk (upper x-axis) both.

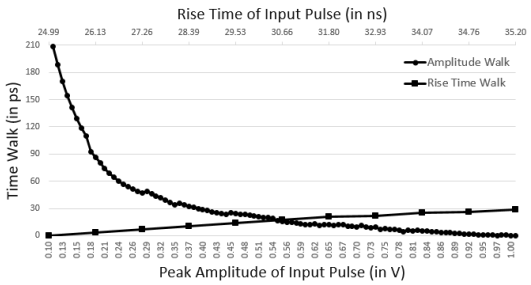

Fig. 4 *Time Walk of the CFD.*

The drift component of the CFD circuit was measured by varying fabrication process, temperature and data was generated from Monte Carlo simulations. As shown in Table 1, the standard deviation of time drift between 20-120 ^{o}C was approximately 400 ps.

Table 1: Time drift of CFD w.r.t Temp

Temperature (^{o}C)	Mean Drift (ns)	Std. Deviation (ps)
20	5.3	430
27	5.3	409
40	5.1	425
60	4.9	398
80	4.7	381
100	4.6	361
120	4.7	402

Conclusion

The results obtained was encouraging and the same design can be used for the applications with CPDA.

References

[1] https://www.mesytec.com/

[2] D. M. Binkley, IEEE Trans. Nucl. Sci. 41, no. 4, (1994).

[3] R. J. Baker, CMOS: Circuit Design, Layout and Simulation, 2nd ed. Wiley, 2009.