Supernova Detection With DUNE

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Introduction

Supernova bursts release enormous amounts of neutrinos. The Deep Underground Neutrino Experiment (DUNE) is engineered to detect supernovas by capturing and analyzing these neutrinos. Upon detecting the direction of a supernova, DUNE will dispatch signals to a network of observatories worldwide to enable multi-messenger astronomy (MMA). However, DUNE's vast data output poses many analytical challenges. The substantial processing time necessary to decipher this data may lead to delays in alerting observatories. These early-stage events are of significant scientific interest as they can provide pivotal insights into astrophysical processes, hence our imperative to enhance data processing efficiency.

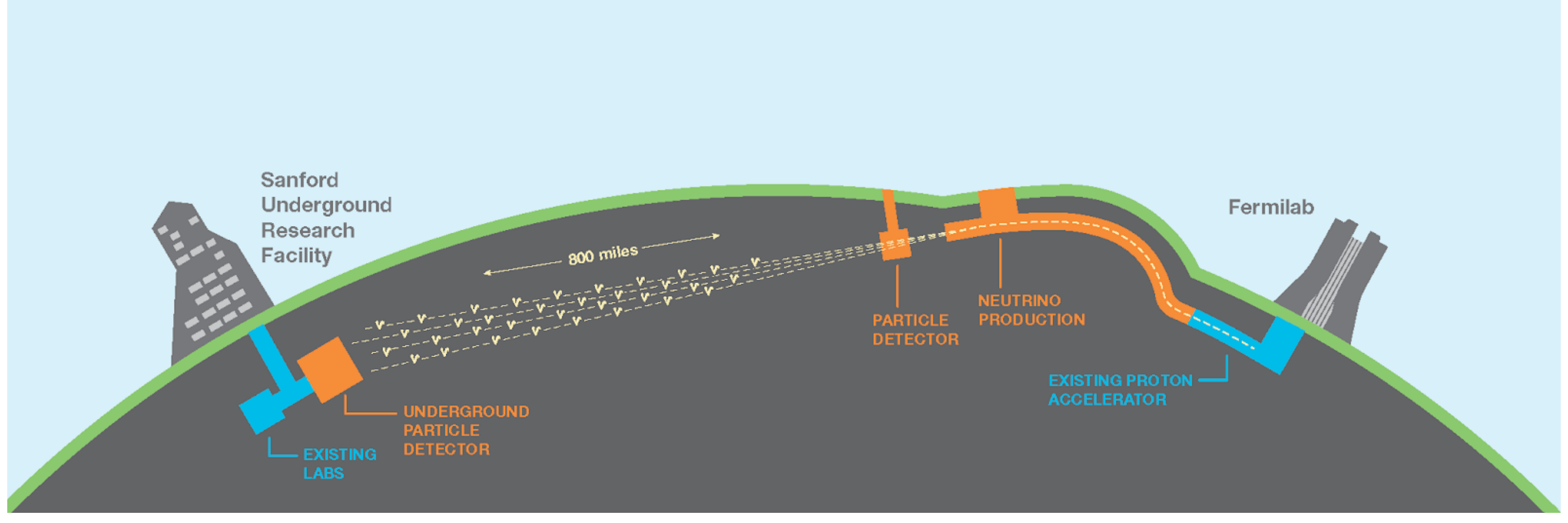
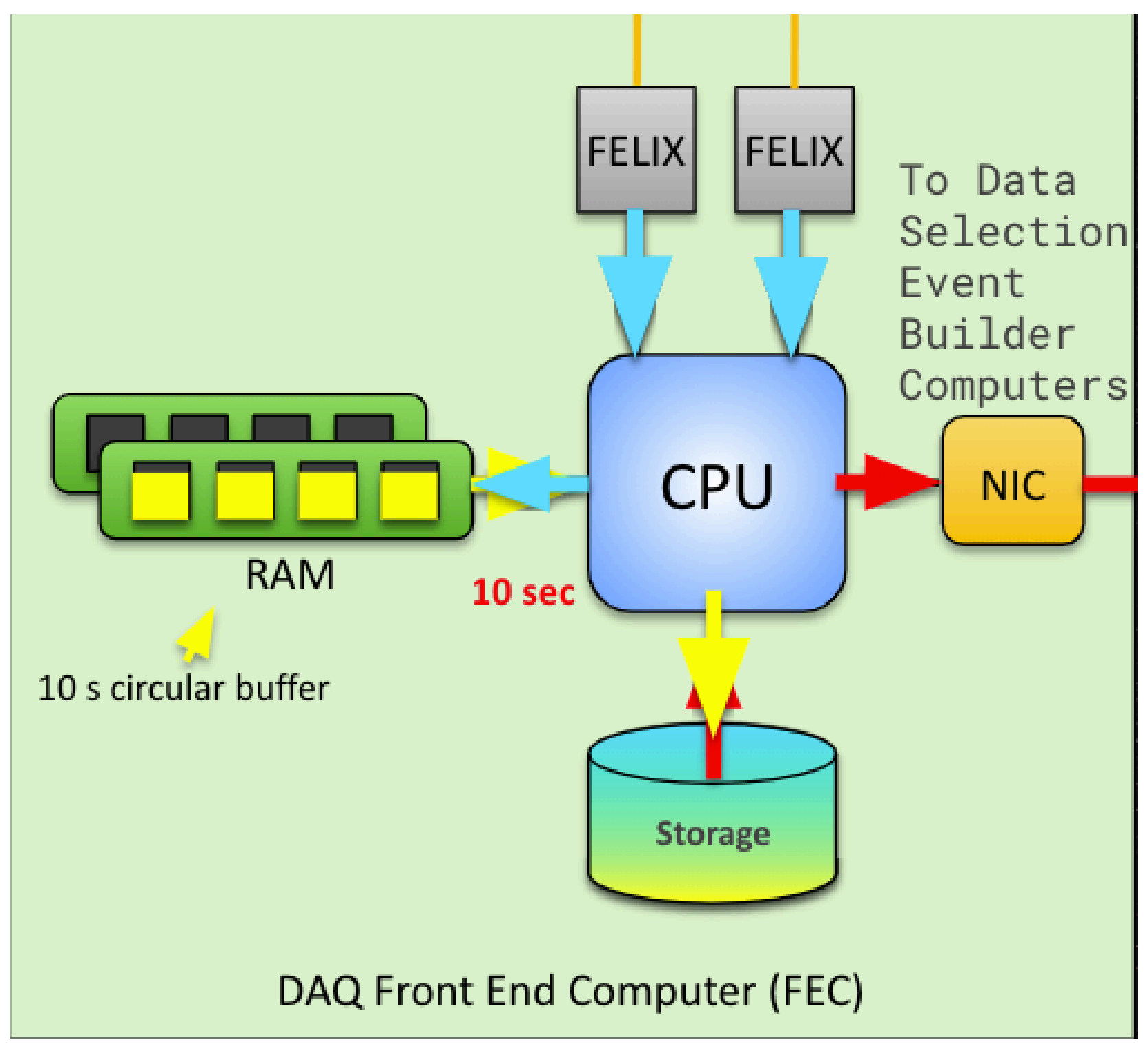


Figure 1: 2D representation of DUNE, FNAL and SLAC

In-Storage Computing with FPGAs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To Data Selection Event Builder Computers
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Figure 2: Current data processing method, CPU heavy.

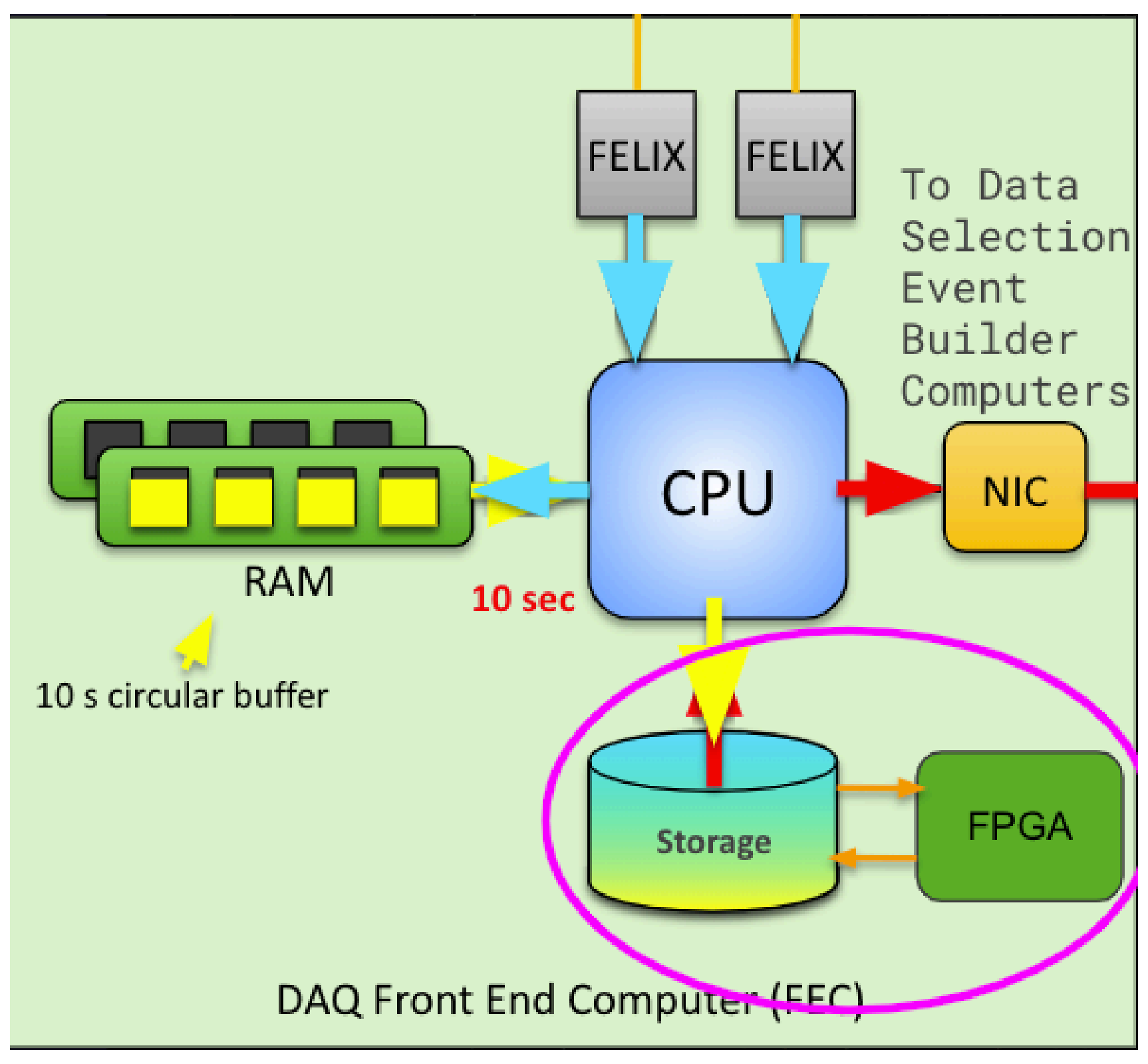
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Figure 3: Proposed solution, FPGA is able to perform processing without using host resources

The solution to large processing times lies in In-Storage Computing with Field Programmable Gate Arrays (FPGAs). Currently, the CPU is planned to be the primary handler of all data processing and Data Acquisition (DAQ) responsibilities. However, by strategically delegating some of these responsibilities, we stand to significantly enhance overall performance.

For these purposes, FPGAs are preferred. FPGAs are integrated circuits that can be configured to do specific tasks. Their ability to do multiple jobs simultaneously makes them perfect for complex computing tasks.

By shifting the processing workload from the CPU to the FPGA integrated within the storage system, we’re essentially bringing the computational process closer to where the data is stored. As a result, data doesn't have to be moved back and forth from the storage to the CPU. This data locality reduces latency, accelerates the processing speed, and reduces the amount of energy used.

2D CNN Implementation

In order for FPGAs to act as accelerators, we program them using AMD/Xilinx Vitis, a specialized development platform. The main function of our FPGA kernel code is to run a 2D Convolutional Neural Network (CNN) by converting raw data from DUNE sensors into a format that allows it to be passed into the CNN. A 2D CNN is a powerful, complex machine learning model capable of interpreting and analyzing multidimensional data. For our purposes, the 2D CNN will be synthesized and optimized through High-Level Synthesis for Machine Learning (hls4ml). Once the 2D CNN is called, the kernel code will be able to analyze the data in a way that allows us to find our desired signals.

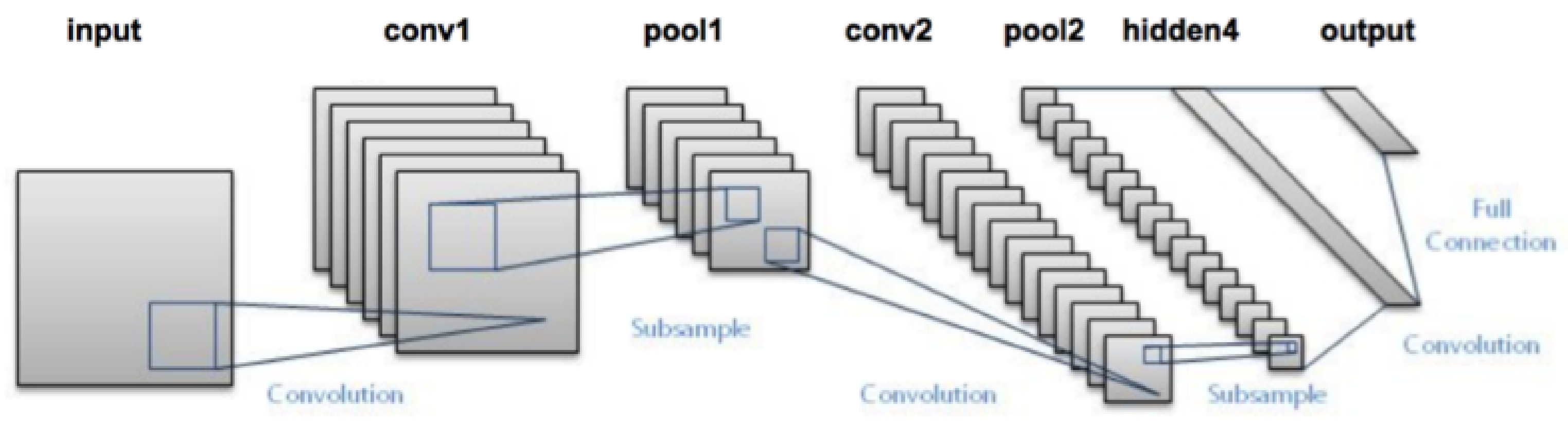

Figure 4: Example 2D CNN

Results

The FPGA kernel code up to the 2D CNN was successfully simulated and synthesized through Vitis HLS. We were also able to optimize it and reduce the required resources. This process allows our code to be used in low level hardware. Complementing this process, we used data visualization to intuitively understand the kernel code's operation and performance. We employed an example datafile filled with representative data the code would typically process. Running this datafile through the kernel code, we observed firsthand how it managed real-world data. Importantly, our code successfully prepared the expected signals, confirming its readiness to be passed into the 2D CNN.

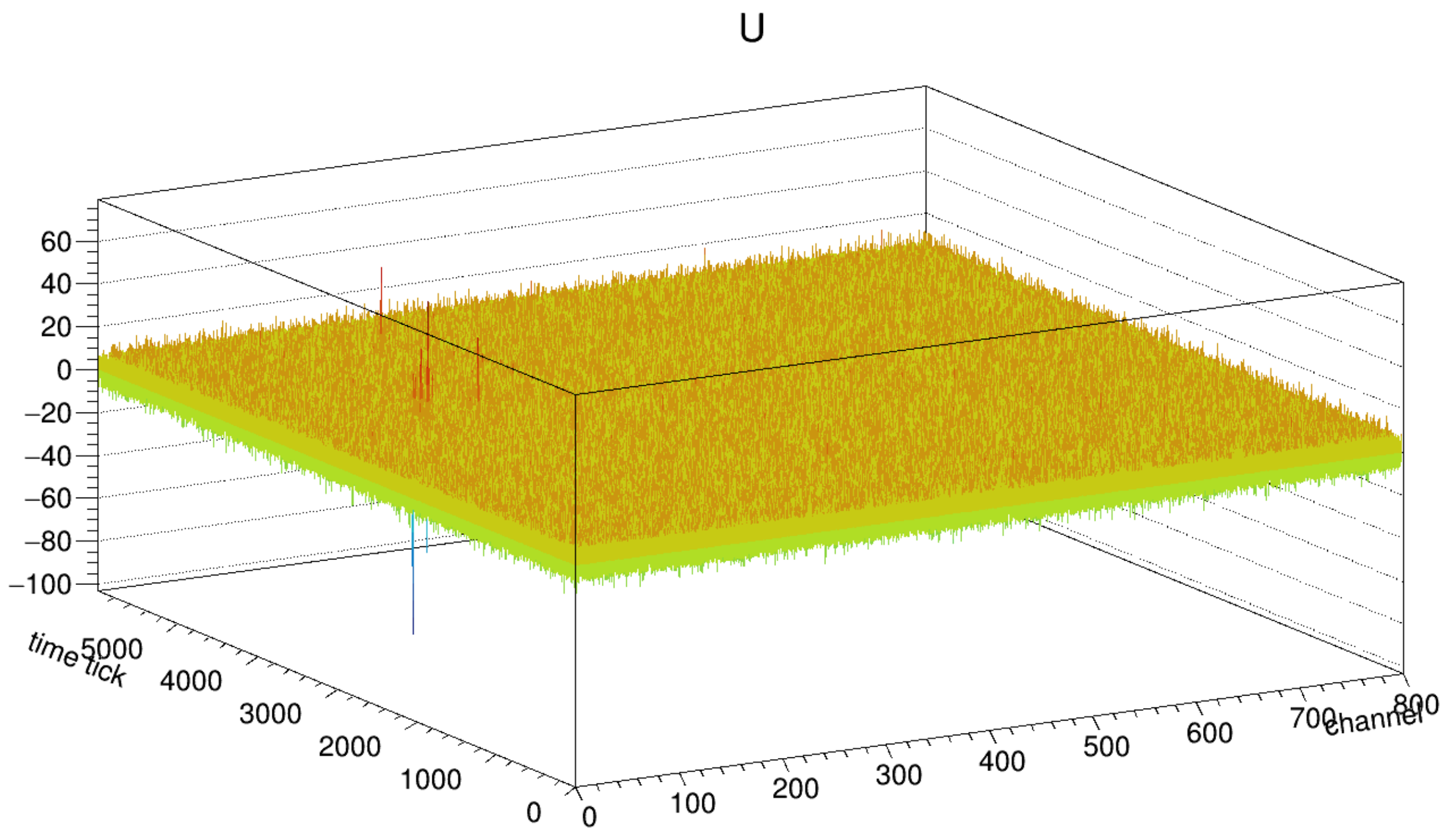

Figure 5: Signal from an example event found from Vitis kernel code as a histogram

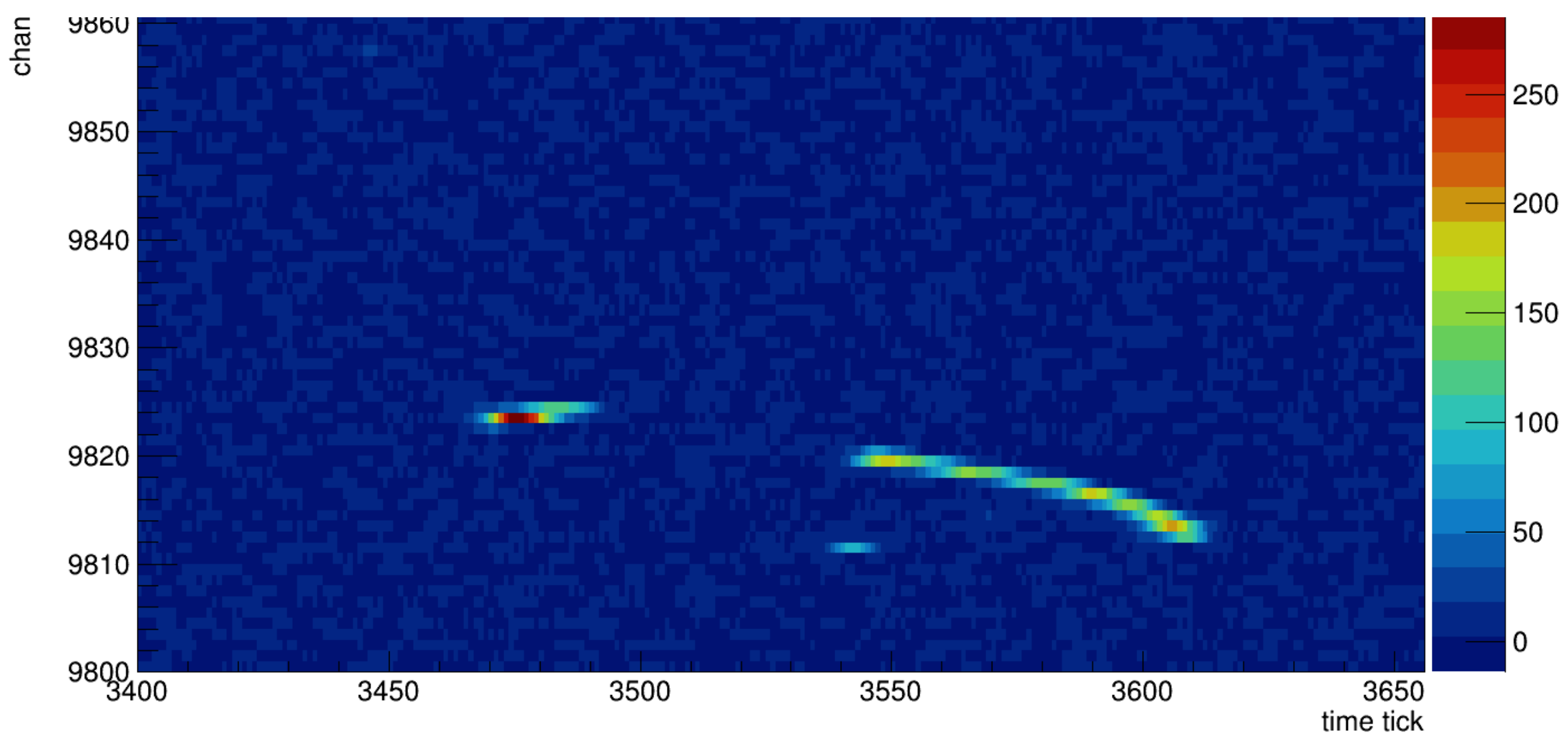

Figure 6: Zoomed in version of the signal as a heat map

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