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Characterization of radiation effects in 65 nm digital circuits with the DRAD digital radiation test chip

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ABSTRACT: A Digital RADiation (DRAD) test chip has been specifically designed to study the impact of Total Ionizing Dose (TID) (<1 Grad) and Single Event Upset (SEU) on digital logic gates in a 65 nm CMOS technology. Nine different versions of standard cell libraries are studied in this chip, basically differing in the device dimensions, V_t flavor and layout of the device.

Each library has eighteen test structures specifically designed to characterize delay degradation and power consumption of the standard cells. For SEU study, a dedicated test structure based on a shift register is designed for each library.

TID results up to 500 Mrad are reported.

Contents

1 Introduction

Radiation effects concerning on-detector electronic systems are one of the main challenges for ASIC design engineers. The unprecedented radiation environment of the HL-LHC detectors requires significant investigation of very high total ionization dose effects not only on the single MOS device alone but also on the digital logic gates.

Studying the impact of high radiation levels on digital electronics in 65nm CMOS technology is vital for key sub-detectors of the ATLAS and CMS upgrades. ATLAS and CMS pixel detector chips (RD53 collaboration [1]) require radiation tolerance of up to 1Grad for a 10 years lifetime for the inner layers of the vertex detectors. Outer tracker detectors require radiation tolerance of the order of 100 Mrad (e.g. the MPA [2] chip for the CMS tracker upgrade) and high speed optical link chips for LPGBT [3], require very high circuit speeds after radiation damage.

The aim of the DRAD chip is to measure the delay degradation under different TID on different customized libraries composed of ten combinational and two sequential cells in a 65 nm CMOS technology. These libraries differ in minimum device dimensions (both L and W), type of transistors (Normal V_t, Low V_t and High V_t) and layout of the device (normal and enclosed layout)

The delay degradation of test structures is measured using delay chains and ring oscillators with different gates (NAND, NOR, XOR, buffers and inverters, flip-flop and latch) for each standard cell library. To deal with sequential elements, specific test structures have been designed for the measurement of setup and hold time. In addition a 24-bit synchronous counter is included for the study of radiation effects in a typical digital composite circuit. To study the effect of SEU, a long shift register is implemented in each library. Specific high speed structures (VCO and counters)

Table 1. Description of the libraries of the DRAD chip.

Library	Description
7T_HVT	7-tracks, High V_t, foundry library $W_p \geqslant 150\,\text{nm}$, $W_n \geqslant 150\,\text{nm}$, L = 60 nm
9T_HVT	9-tracks, High V_t, foundry library, $W_p \geqslant 210\,\text{nm}$, $W_n \geqslant 190\,\text{nm}$, L = 60 nm
9T_NVT	9-tracks, Normal V_t, foundry library , $W_p \geqslant 210\,\text{nm}$, $W_n \geqslant 190\,\text{nm}$, L = 60 nm
9T_NVT_2W	9-tracks, Normal V_t, modified width: $W_p \geqslant 300\,\text{nm}$, $W_n \geqslant 190\,\text{nm}$, L = 60 nm
12T_HVT	12-tracks, High V_t, custom: $W_p \geqslant 700\,\text{nm}$, $W_n \geqslant 390\,\text{nm}$, L = 60 nm
12T_NVT	12-tracks, Normal V_t, custom: $W_p \geqslant 700\,\text{nm}$, $W_n \geqslant 390\,\text{nm}$, L = 60 nm
12T_LVT	12-tracks, Low V_t, custom: $W_p \geqslant 700\,\text{nm}$, $W_n \geqslant 390\,\text{nm}$, L = 60 nm
12T_NVT_2L	12-tracks, High V_t, custom: $W_p \geqslant 920\,\text{nm}$, $W_n \geqslant 410\,\text{nm}$, L = 130 nm
18T_LVT	18-tracks, Low V_t, custom made with ELT transistors $W_p \geqslant 3740\,\text{nm}$, $W_n \geqslant 1420\,\text{nm}$, L = 60 nm

are included only for the fastest library which has enclosed layout and low V_t transistors for future high speed optical link chips. The test structures have been optimized and verified using 200 and 500 Mrad transistor models from the radiation working group of the RD53 collaboration.

A test system has been developed for the DRAD chip to enable radiation tests to be performed in X-ray facilities, and it can be adapted for other radiation test facilities (Cobalt, Ion beam, Proton beam).

2 Description of the chip

2.1 Libraries and standard cells

The DRAD chip is composed of 9 digital libraries with different properties summarized in table 1.

The chip explores libraries with different heights, expressed by the number of tracks (the number of wires that can be routed in parallel with minimum pitch: 7, 9, 12 and 18 tracks, identified as 7T, 9T, 12T and 18T) and threshold voltage flavours of the transistors (normal V_t, low V_t and high V_t, identified as NVT, LVT and HVT).

In terms of device dimensions, some modifications of the foundry libraries were implemented: in the case of the 9T_NVT_2W library, the width of the internal transistors of the sequential cells was increased to be twice wider than the 9T_NVT foundry library (300 nm instead of 150 nm). Also, the 12T_NVT_2L library has transistors with double length with respect the 12T_NVT library, 130 nm instead of 60 nm.

Finally, the 18T_LVT library was full custom made with Enclosed Layout Transistors (ELT). As this library is expected to be the most radiation-hard, it was used for the general and configuration logic of the chip.

Each library is composed of ten combinatorial cells and two sequential ones described in table 2. The cells have different number of inputs (indicated after the name of the gate) and driving strength (identified with the number after letter D).

Table 2. Description of the standard cells included in each library.

Standard Cell	Description
INVD1	Inverter with driving strength = 1
INVD4	Inverter with driving strength = 4
ND2D1	2-input NAND gate with driving strength = 1
ND4D1	4-input NAND gate with driving strength = 1
NOR2D1	2-input NOR gate with driving strength = 1
NOR4D1	4-input NOR gate with driving strength = 1
XOR2D1	2-input XOR gate with driving strength = 1
CKBD1	Clock buffer with driving strength = 1
CKBD4	Clock buffer with driving strength = 4
CKBD16	Clock buffer with driving strength = 16
DFCNQD1	Flip-Flop with asynchronous clear and driving strength = 1
LHCNQD1	Latch with asynchronous clear and driving strength = 1

2.2 Test structures and test strategy

Delay chain and ring oscillator test structures are used in order to measure delay degradation. The schematic of this test structure is shown in figure 1 for an inverter, and it is replicated for the rest of the standard cells of each library.

The test structure can be set in ring oscillator mode or in delay chain mode thanks to a multiplexer in the input. The frequency of the oscillator can be measured setting the test structure in mode 1 (see multiplexer in figure 1), while the time delay from low to high and high to low of the gate can be extracted setting the test structure in mode 0 and sending an input signal to excite the delay chain.

The parasitic delay introduced by the extra logic needed to route the signals can also be measured and subtracted from the delay measurements by measuring the delay between signals OUT_S and OUT in figure 1 when a pulse is sent in delay chain mode.

Also, dedicated test structures have been designed for the measurement of setup and hold time of flip-flops and latches: in these test structures both input and clock signals can be delayed independently thanks to small chains of inverters, characterized with previous test structures.

Figure 1. Typical schematic of ring oscillator/delay chain test structure and input/output signals used to measure the time delay of the standard cell.

Setup and hold time can be estimated by varying the delay of one signal with respect the other (clock vs input data) and detecting when the output changes state.

Finally, a long shift register is implemented in each library for Single Event Upset (SEU) studies.

## 3 Description of the test system and x-ray facility

A test system (figure 2) has been developed based on an Atlys evaluation board [4] with a Spartan 6 FPGA, an interface board (uASIC board, [5]) in charge of powering the chip, power monitoring and the conversion between signaling standards, and a small passive carrier board with a wire bonded DRAD chip. The power is monitored independently for each size of library.

Delay characterization and frequency measurement is performed with an external high speed sampling oscilloscope, controlled via Ethernet with SCPI commands.

IPbus protocol [6] is used for computer-FPGA communication in order to perform the data acquisition and execution of the different tests.

Test are executed by a computer with a Python software environment.

A system composed of an x-ray machine (Seifert RP149, [7]) and a chiller needed to maintain the temperature of the chuck where the chip is placed was used in order to irradiate the DRAD chip at a high dose rate (9 Mrad/h, expressed in SiO_2 equivalent). Test structures are dynamically changing state during irradiation in order to have a duty cycle of 50%.
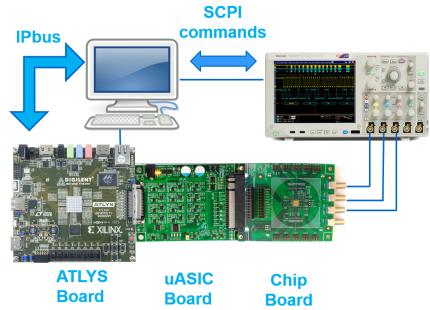
Figure 2. Scheme of the test system.

4 Radiation tests

Several irradiation campaigns were carried out for different total ionizing doses. So far results of tests up to 200 Mrad and 500 Mrad are available and they are shown in the following sections:

4.1 200 Mrad at room temperature

A first campaign was accomplished reaching 200 Mrad of TID at room temperature. After irradiation, the chip was annealed at room temperature for a week, followed by high temperature annealing (100°C). Figure 3 shows the time delay increase of all the standard cells of one of the libraries (9T_NVT) at the end of irradiation and annealing.

All gates show a small improvement after room temperature annealing. However, after annealing at high temperature a degradation in the performance of the gates can be seen being more significant in the case of the NOR gates, which have two or four PMOS transistors in series. This big difference in the NOR gates has been seen in all the libraries explored in the DRAD chip. NOR gates behavior can be explained thanks to measurements taken at transistor level [8], showing significant degradation in PMOS transistors compared to NMOS transistors. The relative behavior between libraries is shown in figure 4. The average time delay of all the cells increases. As expected, libraries with smaller size transistors show bigger degradation. Between libraries with the same size transistors a slight difference can be seen: those with higher V_t behave worse than libraries with lower V_t, but the difference is minimal (of the order of 3%). Also, the maximum time delay per library is shown, being always the NOR gates after annealing at high temperature.
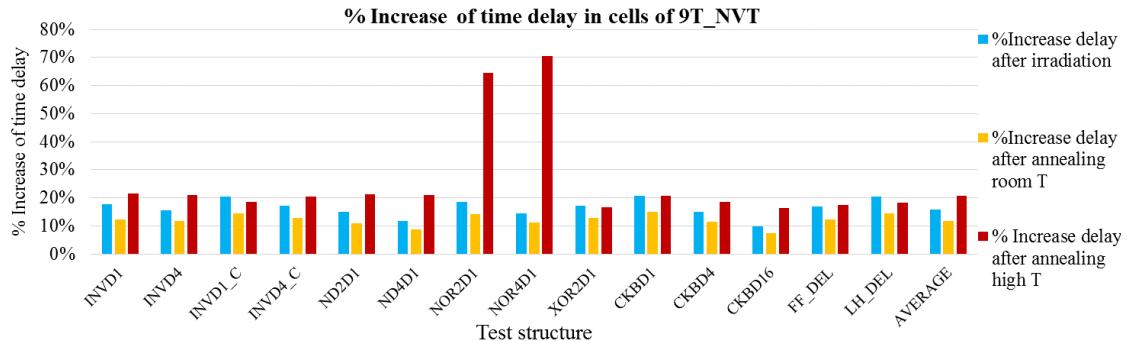
Figure 3. Time delay increase in all the 9T_NVT gates.
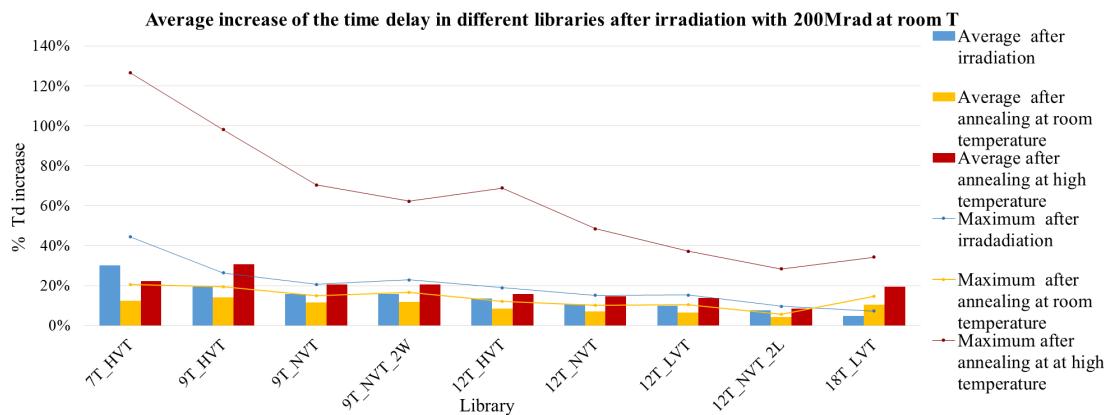
Figure 4. Average time delay increase of all cells for each library, after irradiation with 200 Mrad at room temperature.

Comparing results of libraries 9T_NVT and 9T_NVT_2W (increased width of the internal transistors of sequential cells, see description in section 2.1), a slight improvement (~4% for the latches and flip flops) has been seen in the modified library.

In the case of 12T_NVT and 12T_NVT_2L (with transistors twice longer, description in section 2.1) the latter presents a smaller relative degradation. However, 12T_NVT_2L is intrinsically slower than 12T_NVT.

While all libraries present an improvement during annealing at room temperature, the 18T_LVT library shows degradation. This is still not well understood and will be studied with future tests.

4.2 200 Mrad at -20°C

A second irradiation campaign performed reaching 200 Mrad keeping the chip at low temperature (-20°C) followed by room temperature annealing and finally annealing at 60°C. The degradation seen in the previous campaign during high temperature annealing at 100°C happened quickly (after few hours), making it difficult to monitor the time delay degradation of the cells. To solve that, 60°C temperature was chosen now in order to have a better track of the delay degradation during annealing. Figure 5 shows the average increase of the time delay of all the cells for each library. In this case, the data plotted takes as a reference the time delay before irradiation at low temperature.
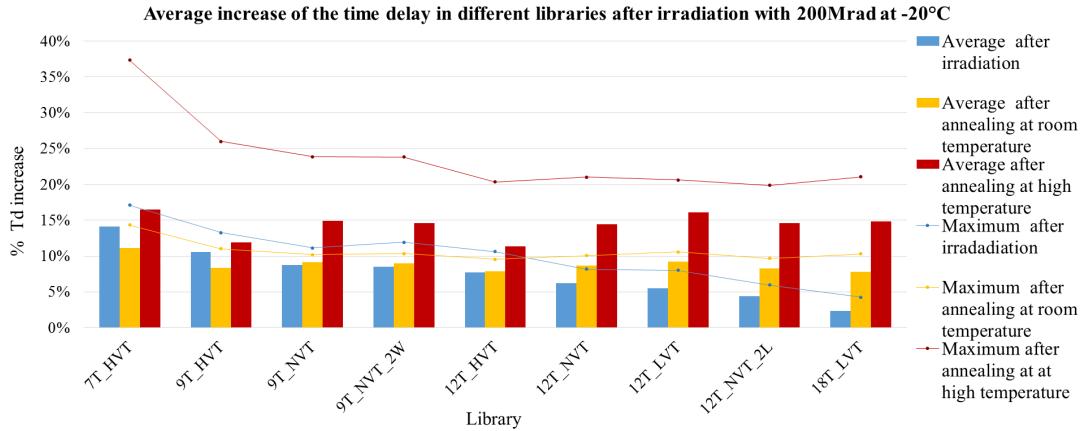
Figure 5. Average time delay increase of all cells for each library after irradiation with 200 Mrad at -20°C.

The results of annealing at high temperature correspond to one week at 60°C: however, as shown later in figure 7, the degradation of the cells still continues. Figure 6 shows the relative delay degradation of the cells for the 9T_NVT library, taking as a reference the delay before irradiation at -20°C. The first measurement corresponds to the room temperature delay, while the last one shows the first measurement after reaching the 200 Mrad of TID and keeping the chip at -20°C, showing the start of the recovery of the time delay.

Figure 7 shows the evolution for the annealing at 60°C started after annealing at room temperature. The first point shows the last measurement before the 60°C annealing, showing the magnitude of the recovery during annealing at room temperature. NOR gates present an increasing degradation during annealing, while the rest of the cells degrade slower and tend to reach a plateau, except for the XOR gates that present an intermediate state between both cases. However, during the submission of this paper the annealing process at 60°C was still on going, so this tendency could change in the coming days. Special attention must be taken for the unexpected delay evolution of the clock buffer CKBD16, fluctuating during annealing.

4.3 500 Mrad at room temperature

A 500 Mrad room temperature campaign was carried out following a similar protocol as the previous campaign (annealing at room temperature and one week 60°C annealing). Results summarizing the degradation of each library can be seen in figure 8. Delay degradation during irradiation and annealing at 60°C can be seen in figures 9 and 10.

In this case, the behavior difference between libraries with different threshold voltage is more noticeable (15% difference between 12THVT and 12TLVT). Again, the annealing at 60°C shows a bigger worsening for NOR gates than for the rest of the cells. XOR gates presents two clear tendencies, seeing a small improvement at the beginning and a worsening after around one day. As in the previous case, the annealing process is still on going.

4.4 Comparison with simulations

Simulations were made using 200 Mrad and 500 Mrad transistor models from the radiation working group of the RD53 collaboration, showing the results in figure 11 for one of the libraries (9T_NVT).
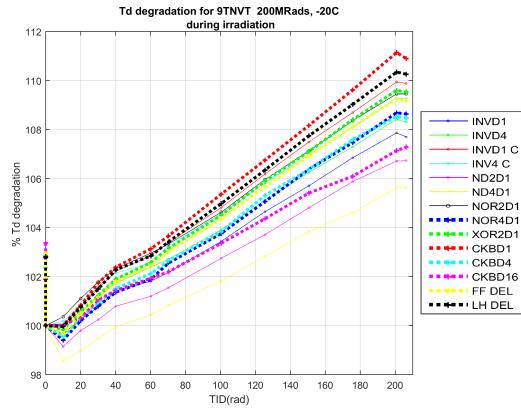
Figure 6. Delay degradation during irradiation up to 200 Mrad at -20°C for cells of 9T_NVT library.
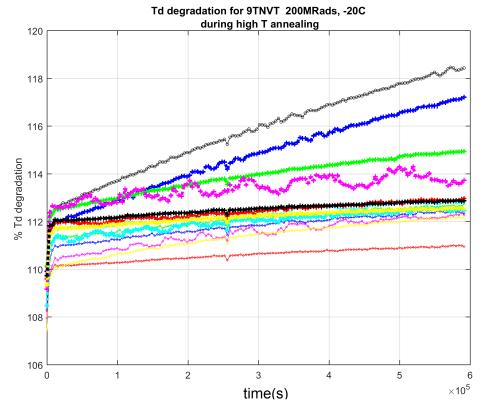
Figure 7. Delay degradation during one week annealing at 60°C for cells of 9T_NVT library.
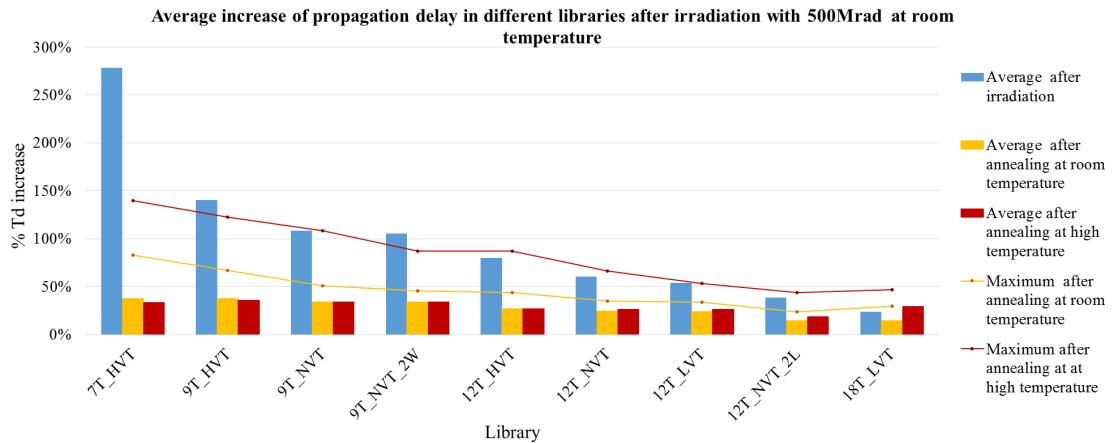

Figure 8. Average time delay increase of all cells for each library, after irradiation with 500 Mrad room temperature.

The simulations models cover the effects after irradiation, but no annealing is taking into account. Experimental data shown in the plots corresponds to the measurements just after irradiation.

While simulations before irradiation fit well with measurements, the results of simulations with 200 and 500 Mrad transistor models are more pessimistic than the measurements results. It is known that the degradation due to irradiation in small transistors is dependent on the bias [8]. The difference in the results plotted can be explained knowing that the transistor models were developed for the worst case bias, while in our setup the test structures are continuously changing state.

5 Conclusions

Studies of the TID radiation effects in 65 nm technology have been performed with the DRAD chip up to different dose levels followed by room temperature and high temperature annealing, exploring the behavior of standard cells in libraries with different properties, as size of the transistors and V_t flavours.
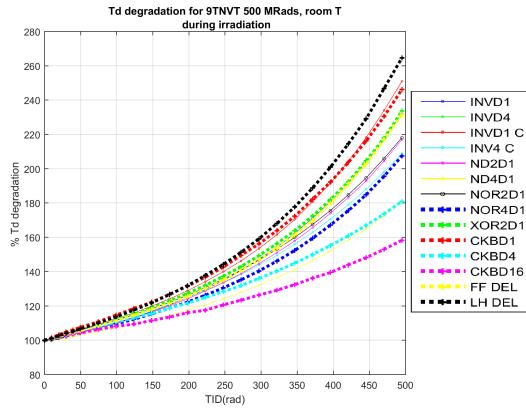
Figure 9. Delay degradation during irradiation up to 500 Mrad at room temperature for cells of 9T_NVT library.
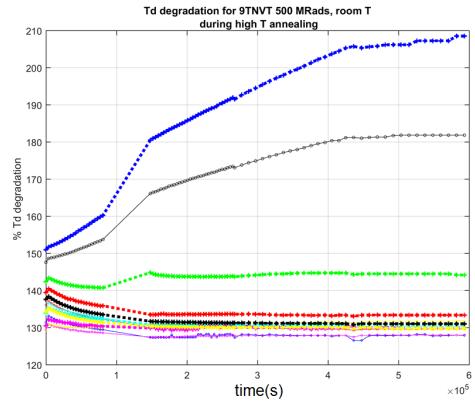
Figure 10. Delay degradation during one week annealing at 60°C for cells of 9T_NVT library.
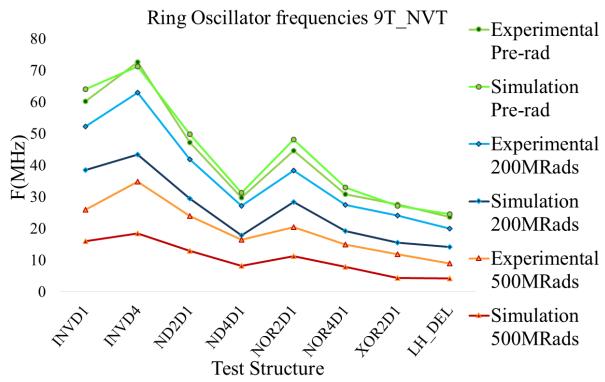
Figure 11. Comparison of measurements and simulations results made for standard cells of the 9T_NVT library before irradiation and after 200 and 500 Mrad.

The relationship between different libraries is as expected, seeing higher degradation for the libraries with smaller transistors. Taking as a reference the 9T_NVT library, a 20% degradation of the propagation delay of the standard cells was observed after 200 Mrad, while a 100% degradation was seen when reaching 500 Mrad, both at room temperature. Results after annealing at high temperature show a significant worsening in the delay of the standard cells with multiple PMOS transistors in series (NOR gates). These results indicate the importance of performing high temperature annealing tests after irradiation in order to characterize the behavior of digital circuits. Also, results confirm previous studies showing that the effect of slow annealing can be avoided in cooled detectors.

Comparing results of tests reaching the same dose but irradiating at different temperatures, a better behavior was observed when irradiating at low temperature: for the 9T_NVT library and 200 Mrad test a 20% degradation was seen for the room temperature test in comparison with the 8% degradation observed at -20°C.

Simulations made with the RD53 transistor models for 200 and 500 Mrad show a pessimistic prediction of the behavior of the standard cells respect the measurements, mainly due to the fact that the models were developed for the worst case bias.

New irradiation campaigns will be carried out varying the temperature and total ionizing dose reaching 1000 Mrad, as well as annealing process without biasing the chips.

Acknowledgments

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