HN 101

Fermi National Accelerator Laboratory

DELAY/ENCODER

HARDWARE DESCRIPTION

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1. General Information

1.1. Purpose

The front end readout electronics for the Silicon Strip Detector is designed to process data at the RF bucket frequency, 53MHz. The Delay/Encoder(DE) module has been specified to accept data at 53MHz, provide a delay mechanism while a trigger decision is made, and generate an address hit list upon a Level 1 accept signal. A simplified block diagram is provided in Figure 2.

The delay element continuously stores data while the level 1 system is processing data corresponding to previously stored events. The delay is implemented in RAM and it is required for the control system to map the level 1 decisions into an eight bit address. The current implementation assumes that processing of an event takes about 1μsecond from the time that it is loaded into the DE. It is mandatory that the event acceptance be time ordered and the decision time be fixed with respect to the event occurrence. The address of accepted events is broadcasted by the Master Timing Controller to all Sequencer modules in the system and each Sequencer addresses the DE in its crate. The addressing mechanism triggers the DE to read the event from memory and transfer it to the encoder section.

The data encoding scheme uses the trigger bucket and the previous bucket simultaneously to generate an address hit list. A flag is asserted whenever the previous bucket has the bit set for the address being output. The address hit list is transmitted synchronously to a crate Sequencer module which serves as a crate controller and event builder for two planes of silicon strip data. The Sequencer is capable of transmitting hit data over fiber optic at 40Mbytes/sec or read out by a Fastbus master.

This document includes figures and timing diagrams intended to simplify the specifications. In some cases, specifically the timing diagrams, the information is an attempt to specify the module and its interface with other system components.

1.1.1. Silicon Strip Readout System

This section presents a simplified block diagram of the silicon strip readout system. Figure 1 shows the interconnection of all the modules that are referenced in this document. A brief description of each module follows.

PC - PostAmp/Comparator board, 12 per crate. Processes 128 pre-amp silicon strip signals, outputs discriminated data to the Delay/Encoder and outputs analog and digital sums to Level 1.

DE - Delay/Encoder board, 12 per crate. Provides event buffering for the PC discriminated data and for level 1 accepted event transmits a hit list to the Sequencer.

SEQ - Sequencer board, 1 per crate. Fans out system clock to PC and DE, initiates the encoding of a event, stores, pipelines and transmits encoded events to the next level. The events can be readout by a FASTBUS master.

FSCC- Fastbus Smart Crate Controller board, 1 per crate. Initializes the crate by exercising control over the SEQ, runs local diagnostics and provides an alternate data path to readout events.

MTC- Master Timing Control board, 1 per silicon strip readout system. The MTC synchronizes the 12 SEQ in the system by providing timing and control. Some of the functions that it performs are listed below:

- Distributes the RF clock to all SEQs.
- Maps a level 1 accept signal into an address of the DE memory and transmits addresses to all SEQs.
- Queue level 1 accepted events.
- Controls the write enable signal for the DE.
- Responds to READY and ERROR condition from the SEQs.
- Interface with the overall experiment controller.
- Synchronize System.

The readout system consists of 12 readout crates and a control crate that contains the MTC and other special modules. Each of the readout crates processes two planes of silicon strip data. Data processing is done in groups of 128 strips by a PC and DE pair. The 12 DEs in a crate send data, in parallel, to the crate SEQ. For a formal description of the system refer to the 'Silicon Strip Readout Implementation Plan' document.

In the context of this specification an **event** is the output of the PC and they are generated every 18.9nanoseconds.

1.2. Application

The DE is being designed for the Silicon Strip Readout System for E771 and E789. The function of the module is hardwired and there is no other application for it beyond the ones described on this document.

1.3. Packaging

The board is a single width FASTBUS module that does not contain a FASTBUS interface.

1.4. Power Requirements

The maximum and typical current for the module are listed below.

Voltage	Current Max.	Typical Current
-5.2V	17A	14A
-2.0V	6A	6A
+5.0V	<.5A	

The typical power dissipation for the module is 85 W. For protection fuses and tranzsorbs are used for each power supply. The recommended number of fuses is: -5.2v - three 5A and one 3A , -2.0v - three 3A and 5.0v - one 1/2A.

1.5. Cooling Requirements

The module will operate at the temperature range provided by the FASTBUS cooling system.

2. Theory of Operation and Operating Modes

The DE module is a single width board packaged in FASTBUS that does not implement a FASTBUS interface. The DE accepts PC discriminated data from 128 silicon strips, provides event buffering, encodes and transmits accepted events to a crate SEQ. The module communicates with the PC and SEQ through a special FASTBUS auxiliary backplane. The auxiliary connector signals for the DE are described in Appendix A.

The module is divided in two independent functions; the Delay element and the Encoder, see Figure 2. The following sections provide a brief description for each function.

2.1. Delay

The Delay element receives 128 channels of discriminated data from the associated PC and provides buffering for 256 events (~4.8 μseconds). During data acquisition the DE continuously stores data in a FIFO like memory, while the level 1 system is making decisions for previously stored events. The DE does not implement any logic to prevent overwriting interesting events. This operation is delegated to the MTC which keeps track of the system write pointer (for DE) and the queued events. For system implementation reasons, it is mandatory that event acceptance be time ordered and the decision time be fixed with respect to the event occurrence.

The delay element control logic requires that the 53MHz input (CLK2) be a 50% duty cycle clock. The logic splits the 18.9 nanoseconds time slice of each bucket into a read and write periods for a combined bandwidth of 106MHz. The write operation uses an address counter clocked by CLK2 and a write enable signal (WRITE*, asserted low) generated by the MTC and distributed in each crate by the SEQ.

The WRITE* signal is send 128 cycles before the SYNC* pulse. The DE retime the signal with the SYNC* to synchronize the start of event acquisition, see timing 2. The DE starts writing data synchronously with SYNC*, but stops writing data asynchronously when WRITE* is deasserted. The DE will track their synchronization by checking that the write address is zero when the SYNC* signal is asserted. Note that prior to the assertion of WRITE* the DEs had been reset, which forces the write address to zero.

The readout of an event occurs when the MTC receives an accept pulse from the level 1 trigger system. The MTC maps the pulse into an address for the DEs memory and sends the address to all SEQs in the system. The address generated by the MTC shall correspond to the previous bucket location. The previous and accepted buckets are loaded into registers and the Encoder is enabled to begin encoding that particular event.

2.2. Encoder

The Encoder is a simultaneous two bucket hit-list address generator. The encoding is performed in two stages, byte and bit levels, see Figure 3. At load time, the byte encoder performs byte integration, see Figure 4. The output of this process is a 16-bit word with a bit set for bytes with hit channels. At encoding time the byte encoder sequentially selects bytes to be

processed by the bit encoder. The bit encoder (block ENCODER-8) loads the input data when ready and outputs a byte wide address stream of asserted bits. The encoded address is formed by concatenating the byte address with the bit address. In addition the bit encoder sets a flag (DATA0) whenever the previous bucket has a hit for the address being output. The hit list is generated from low to high address and no hit count is generated by the DE. An example of byte encoding is shown below:

Bit # Bucket	Previous Bucket	Trigger Bucket	Hit Type	Bit ADD (HEX)	Flag
7	1	0	A	7	1
6	0	0	-	-	-
5	0	1	B	5	0
4	1	1	C	4	1
3	0	0	-	-	-
2	0	0	-	-	-
1	1	1	C	1	1
0	0	1	B	0	0

Note: The encoder never looks at addresses without hits, this is represented with "-".

The option to remove type A hits is implemented on the prototype. There are two options for the address hit list data transfer, 53MHz or 26.5MHz, CLK2 and CLK3 respectively. These options are switch selectable for each DE. Currently only the 26.5MHz transfers have been tested and the present version of the SEQ does not support the 53MHz transfer rate.

From the encoding table shown above two modes of operation are derived: **Mode 1** in which type A, B and C hits are included; **Mode 2** where type B and C hits are included.

3. Input/Output Specifications

The DE is a two port module, PC port and a SEQ port, See Figure 2. Both of these ports are implemented on an application specific Fastbus Auxiliary backplane that pairs a PC with a DE and has separate connections between each DE and the SEQ.

3.1. Communication Interfaces

3.1.1. PostAmp/Comparator Port

The PC port is a 128 bit uni-directional single-ended ECL connection from a PC to the associated DE. Synchronization of this port is controlled by the SEQ supplied CLK1 and CLK2 clocks. CLK1 is remotely programmed through FASTBUS and the rising edge is used by the PC to latch the silicon strip discriminated data. CLK2 is referenced (delayed) to CLK1 such that the PC output data is valid while the DE is asserting the Write* signal for the memories, see Timing 1. It is required that data on this port be valid for at least 12 nanosececonds simultaneously at all DE in a crate.

3.1.2. Sequencer Port

The Sequencer port is the access port for the SEQ to readout the level 1 accepted events. This data port is a byte wide point-to-point connection designed to support a 53MHz data transfer rate. Currently this port is operated a 26.5MHz.

The port provides an address bus, a data bus and control signals. To initiate a transfer the Sequencer supplies the DE with an event address and asserts the Add_Valid signal. After a fixed delay the Encoder will assert a Data_Valid signal (if hits present) and start transmitting the address hit list to the SEQ until completion. The data transfer is synchronous with CLK2 or CLK3 depending on the user selected encoder operating frequency. A non-detailed timing diagram is provided in Timing 4.

3.1.3. Front Panel

The DE front panel is intended to provide information that will help diagnose data encoding problems, refer to Figure 5 for the layout of the front panel. The front panel provides the byte mask (B1_Byt(0:7) and B2_Byt(0:7)) which describes the bytes that have hits. Note that the byte mask provides a bit for each of the 16 bytes of the 128 channels. In addition the front panel provides the bytes that will be loaded next by the Bit_Encoder (TB(0:7) and RPB(0:7)). This information combined with the signal Clk_Byt* provides everything that is required to trace the encoding operation of the DE. Description of the front panel signals is provided on appendix A.

Other signal provided are TC*, 53M* and a sync error led.

4. Initialization

Initialization of the DEs is achieved by deasserting the Write_En* signal and pulsing the SSD Reset signal. Then the MTC initiates the enable of the write process and after the appropriate delay the enable of the Level 1 system. The DE will start writing data synchronously after receiving Sync* when the Write _En* signal is asserted.

After reset, the write counter points to location zero, the Encoder is in the ready state and all control signals driven by the DE are negated. The read counter is not initialized because it is loaded on demand when an event is accepted.

5. Module Diagnostics

5.1. Hardware Test

The DE does not implement any internal diagnostic tests or FASTBUS interface to access it's memory. The decision of excluding these features is based on timing and power considerations.

The Test Stand Module (TSM) is the test module used to debug the DE. The TSM implements a 256 x 128 memory used to emulate the PC output port and one port of the SEQ. The TSM is operated by a FASTBUS master, i.e. the FSCC. In brief the user will load the memory, initiate the data transfer from TSM to DE and then request events to be encoded by the DE (from it's memory). The encoded event is read out from the TSM and compared with the expected result. A detailed description of the DE software diagnostics is provided in the Software Document **PN434**.

5.2. System Test

For system diagnostics the PC provides a maximum of 256 data patterns generated by a counter. The counter can be programmed to count or hold the loaded value. The data is stored by the DE into it's memory an events to be encoded are requested through the SEQ. Synchronization is achieved by the initialization of the SSD system and from the match between the 256 different patterns and the 256 memory locations on the DE.

6. Appendix A

This appendix describes the DE auxiliary connector signals used on the silicon strip readout crates and the signals provided in the front panel. In addition any other signals of interest are described.

A.1 Auxiliary Connector

CLK1 - A 53MHz clock driven by the SEQ and used by the PC to latch data. This clock is remotely programmable through the FASTBUS port on the SEQ.

CLK2 - A 53MHz clock driven by the SEQ. The clock is a delayed version of CLK1 used to synchronize the write process in the DE with the output data of the PC, to generate internal timing and as a reference when transmitting data to the SEQ at 53MHz.

CLK3 - A 26.5MHz clock driven by the SEQ. The clock used to transmit data to the SEQ. The DE samples the 26.5MHz on the backplane with the internal 53MHz clock.

DI(0:127) - Input discriminated data driven by the associated PC. A 100 ohms termination is provided by the DE.

Address(0:7) - The address bus (bussed to all DE) driven by the SEQ to transfer event addresses to the DE.

Add_Valid - Signal driven by SEQ to validate ADD(0:7).

Write_En* - Write enable signal distributed on the backplane by the SEQ. The signal is controlled by the MTC or through a FASTBUS register on the SEQ.

Sync* - Synchronization signal generated by the MTC and used by the DEs to test write counter synchronization at each zero crossing. If a DE has a

write counter different from zero then it is out of synchronization.

Sync_Err - Signal asserted by a DE that is out of synchronization and received by the SEQ. The signal is wire-ored on the backplane.

Reset - Reset signal distributed on the backplane by the SEQ.

Data_X(0:7) - Encoded hit list data bus for Delay/Encoder X, where X is a hex number assigned to each DE. Terminated by the SEQ.

Data_ValidX - Data valid signal asserted by Delay/Encoder X, where X is a hex number assigned to each DE. Terminated by the SEQ.

A.2 Front Panel Signals

B1_Byt(0:7) * - This are the lower 8 bits of the byte encoding process implemented by the logic in Figure 4.

B2_Byt(0:7)* - This are the upper 8 bits of the byte encoding process implemented by the logic in Figure 4.

TC* - This signals is asserted low every time that the write counter of the DE is at FFh. This signal should remain at a fixed reference relative to the system Sync signal.

53M* - A buffered inverted sample of the 53MHz clock received by the DE from the backplane.

Error - RED LED that is on when the DE detects that is out of synchronization with respect to the Sync signal on the backplane.

Clk_Byt* - Clock pulse that signals that a new byte is being loaded into the Bit-Encoder. Also the lowest bit in

B1_Byt(0:7), B2_Byt(0:7) will be set, meaning that the corresponding byte is being processed.

TB(0:7)* - The Trigger bucket loaded into the Bit_Encoder when Clk_Byt* was pulsed.

RPB(0:7)* - The Previous bucket loaded into the Bit_Encoder when Clk_Byt* was pulsed.

7. Appendix B

This appendix covers the switches and switch setting for the DE. The switches or jumper (label as TP) points are implemented with wire-wrap pins to limit the problems of wrong set ups. For the operation mode refer to Section 2.2.

SW1 - Selects for the encoding clock (same clock used to transfer data to the SEQ). The default is pin-2 to pin-1, the 26MHz is selected

SW2 - Selects the clock that increments the write counter. The default is connect pin-2 to pin-3, the write counter is incremented with a signal derived from the write signal going to the memories.

SW3 - Selects the the select line for the address mux. The default is pin-2 to pin-3, use CLKB4 which is a 53MHz signal.

SW4 - This switch was implemented to disable the write signal during the time that an event was being read out into the registers (the write would be disable for 40nsec. approximately). The default is the open position, this is no wire.

Mode 1 Setting

TP1 and TP2 shorted, this allows both buckets to be included on the generation of the byte mask shown in Figure 4. In addition the following pairs on TP must be shorted: TP4-TP8, TP5-TP9, TP6-TP10, TP7-TP11, TP12-TP16, TP13-TP17, TP14- TP18, TP15-TP19.

Mode 2 Setting

TP1 and TP2 open, this disables the previous bucket from being included in the generation of the byte mask. In addition the set of pins mentioned in Model 1 (TP4 ..... TP19) must be open. The following pins are to be tied to an ECL high; TP4, TP5, TP6, TP7, TP12, TP13, TP14 and TP15.

8. Appendix C

Encoder Module Pin List

(Viewed From Front of Crate-10/1/90)

C01-N/C	B01-Post/Disc Ch.00	A01-Post/Disc Ch.01
C02-GND	B02-Post/Disc Ch.02	A02-Post/Disc Ch.03
C03-N/C	B03-Post/Disc Ch.04	A03-Post/Disc Ch.05
C04-GND	B04-Post/Disc Ch.06	A04-Post/Disc Ch.07
C05-GND	B05-Post/Disc Ch.08	A05-Post/Disc Ch.09
C06-GND	B06-Post/Disc Ch.10	A06-Post/Disc Ch.11
C07-GND	B07-Post/Disc Ch.12	A07-Post/Disc Ch.13
C08-Reset	B08-Post/Disc Ch.14	A08-Post/Disc Ch.15
C09-Sync	B09-Post/Disc Ch.16	A09-Post/Disc Ch.17
C10-GND	B10-Post/Disc Ch.18	A10-Post/Disc Ch.19
C11-GND	B11-Post/Disc Ch.20	A11-Post/Disc Ch.21
C12-Sync Err	B12-Post/Disc Ch.22	A12-Post/Disc Ch.23
C13-GND	B13-Post/Disc Ch.24	A13-Post/Disc Ch.25
C14-GND	B14-Post/Disc Ch.26	A14-Post/Disc Ch.27
C15-GND	B15-Post/Disc Ch.28	A15-Post/Disc Ch.29
C16-GND	B16-Post/Disc Ch.30	A16-Post/Disc Ch.31
C17-GND	B17-Post/Disc Ch.32	A17-Post/Disc Ch.33
C18-GND	B18-Post/Disc Ch.34	A18-Post/Disc Ch.35
C19-GND	B19-Post/Disc Ch.36	A19-Post/Disc Ch.37
C20-GND	B20-Post/Disc Ch.38	A20-Post/Disc Ch.39
C21-Hit Data 0	B21-Post/Disc Ch.40	A21-Post/Disc Ch.41
C22-Hit Data 1	B22-Post/Disc Ch.42	A22-Post/Disc Ch.43
C23-GND	B23-Post/Disc Ch.44	A23-Post/Disc Ch.45
C24-Hit Data 2	B24-Post/Disc Ch.46	A24-Post/Disc Ch.47
C35-Hit Data 3	B25-Post/Disc Ch.48	A25-Post/Disc Ch.49
C26-GND	B26-Post/Disc Ch.50	A26-Post/Disc Ch.51
C27-Hit Data 4	B27-Post/Disc Ch.52	A27-Post/Disc Ch.53
C28-Hit Data 5	B28-Post/Disc Ch.54	A28-Post/Disc Ch.55
C29-GND	B29-Post/Disc Ch.56	A29-Post/Disc Ch.57
C30-Hit Data 6	B30-Post/Disc Ch.58	A30-Post/Disc Ch.59
C31-GND	B31-Post/Disc Ch.60	A31-Post/Disc Ch.61
C32-Hit Data 7	B32-Post/Disc Ch.62	A32-Post/Disc Ch.63
C33-Data Valid	B33-Post/Disc Ch.64	A33-Post/Disc Ch.65
C34-GND	B34-Post/Disc Ch.66	A34-Post/Disc Ch.67
C35-26 MHz Clock	B35-Post/Disc Ch.68	A35-Post/Disc Ch.69
C36-GND	B36-Post/Disc Ch.70	A36-Post/Disc Ch.71
C37-Event Address Valid	B37-Post/Disc Ch.72	A37-Post/Disc Ch.73
C38-Event Address Wrt. En.	B38-Post/Disc Ch.74	A38-Post/Disc Ch.75
C39-GND	B39-Post/Disc Ch.76	A39-Post/Disc Ch.77
C40-Event Address 0	B40-Post/Disc Ch.78	A40-Post/Disc Ch.79
C41-Event Address 1	B41-Post/Disc Ch.80	A41-Post/Disc Ch.81
C42-GND	B42-Post/Disc Ch.82	A42-Post/Disc Ch.83
C43-Event Address 2	B43-Post/Disc Ch.84	A43-Post/Disc Ch.85
C44-Event Address 3	B44-Post/Disc Ch.86	A44-Post/Disc Ch.87
C45-GND	B45-Post/Disc Ch.88	A45-Post/Disc Ch.89
C46-Event Address 4	B46-Post/Disc Ch.90	A46-Post/Disc Ch.91
C47-Event Address 5	B47-Post/Disc Ch.92	A47-Post/Disc Ch.93
C48-GND	B48-Post/Disc Ch.94	A48-Post/Disc Ch.95
C49-Event Address 6	B49-Post/Disc Ch.96	A49-Post/Disc Ch.97
C50-Event Address 7	B50-Post/Disc Ch.98	A50-Post/Disc Ch.99
C51-GND	B51-Post/Disc Ch.100	A51-Post/Disc Ch.101
C52-GND	B52-Post/Disc Ch.102	A52-Post/Disc Ch.103
C53-GND	B53-Post/Disc Ch.104	A53-Post/Disc Ch.105

C54-GND	B54-Post/Disc Ch.106	A54-Post/Disc Ch.107
C55-GND	B55-Post/Disc Ch.108	A55-Post/Disc Ch.109
C56-GND	B56-Post/Disc Ch.110	A56-Post/Disc Ch.111
C57-GND	B57-Post/Disc Ch.112	A57-Post/Disc Ch.113
C58-GND	B58-Post/Disc Ch.114	A58-Post/Disc Ch.115
C59-GND	B59-Post/Disc Ch.116	A59-Post/Disc Ch.117
C60-GND	B60-Post/Disc Ch.118	A60-Post/Disc Ch.119
C61-GND	B61-Post/Disc Ch.120	A61-Post/Disc Ch.121
C62-H53MHZ,Ø2 Clock	B62-Post/Disc Ch.122	A62-Post/Disc Ch.123
C63-L53MHZ,Ø2 Clock	B63-Post/Disc Ch.124	A63-Post/Disc Ch.125
C64-N/C	B64-Post/Disc Ch.126	A64-Post/Disc Ch.127
C65-N/C	B65-GND	A65-N/C

9. Appendix D

Figures and Timing Diagrams

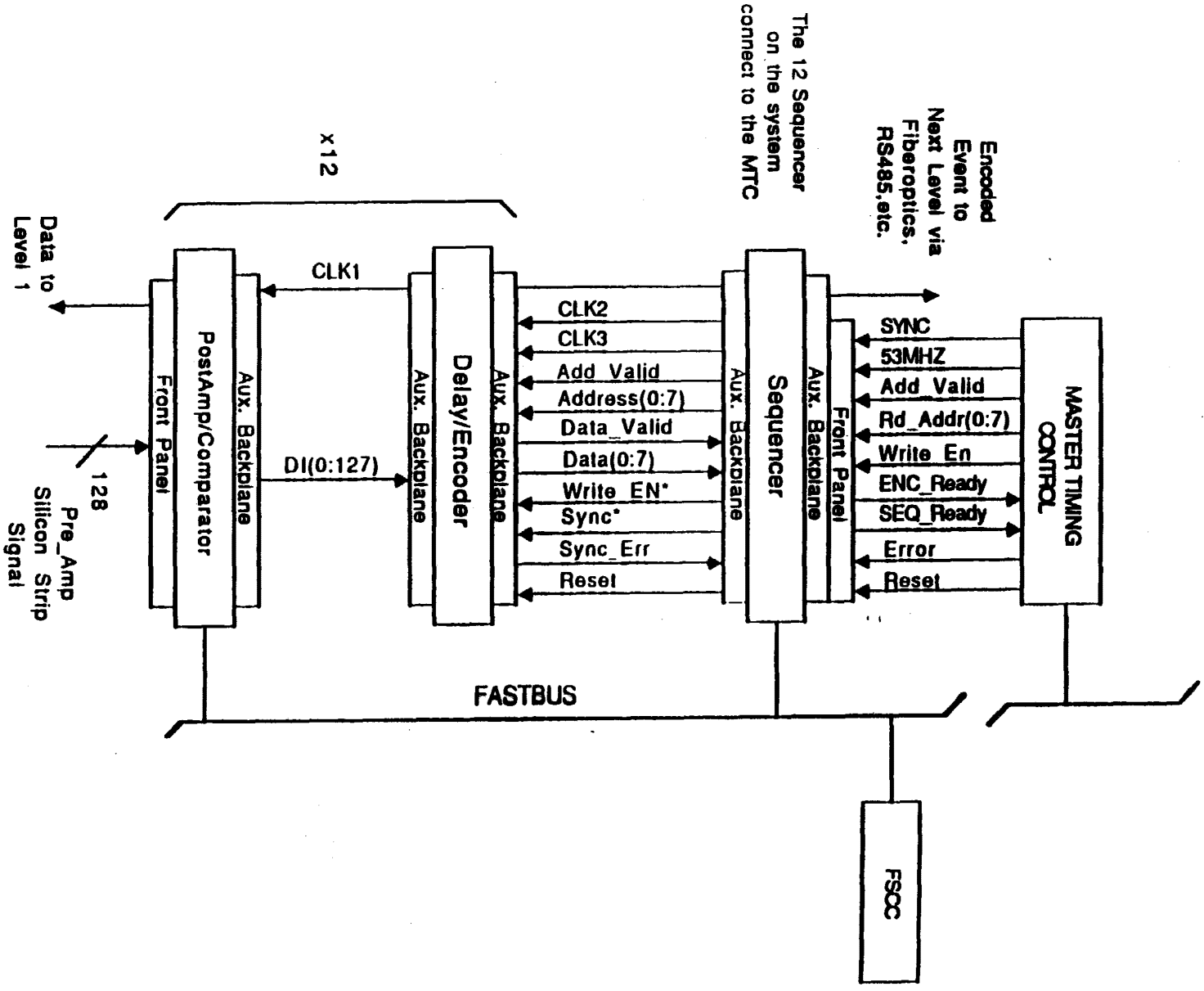
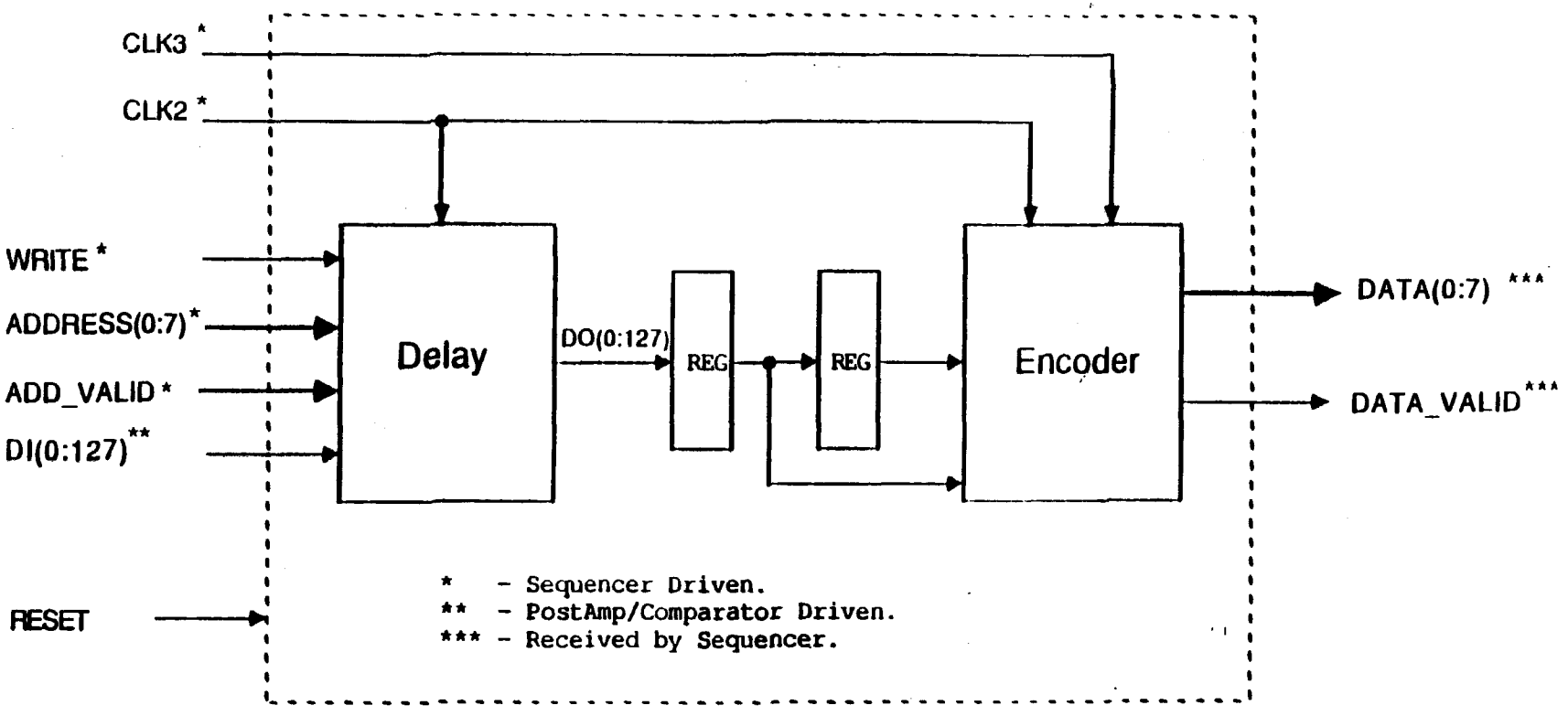


FIGURE 1: Silicon Strip Readout System



PC PORT:

DI(0:127)	- PC output data.

SEQ PORT:

WRITE	- Write enable for the delay memory.
ADDRESS(0:7)	- Accepted bucket address.
ADD_VALID	- Validates ADDRESS(0:7).
DATA(0:7)	- Channel to transmit the address hit list.
DATA_VALID	- Enable the Sequencer to clock data into its FIFO.

Figure 2: Delay/Encoder Block Diagram

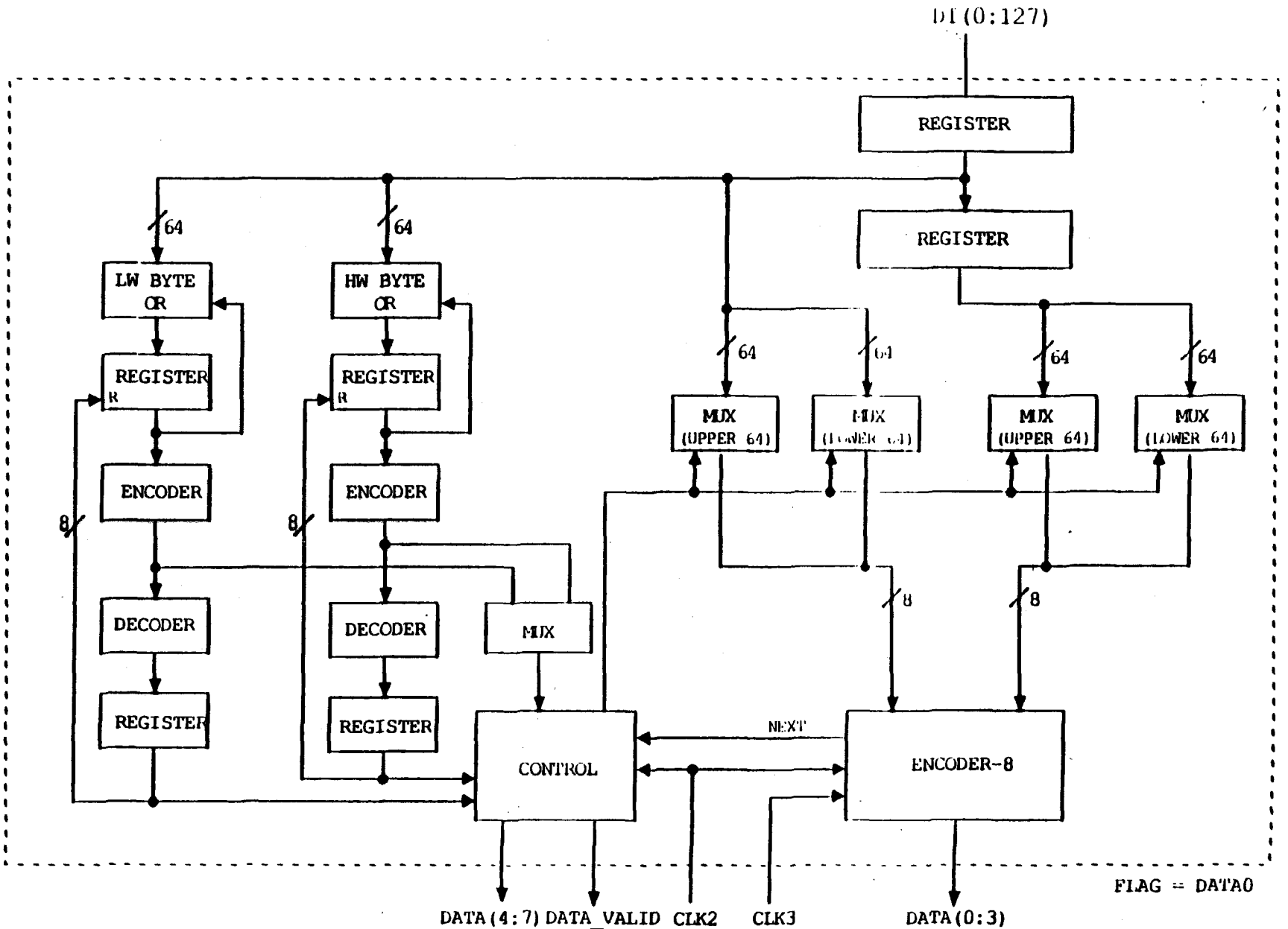


Figure 3: 128-BIT ENCODER

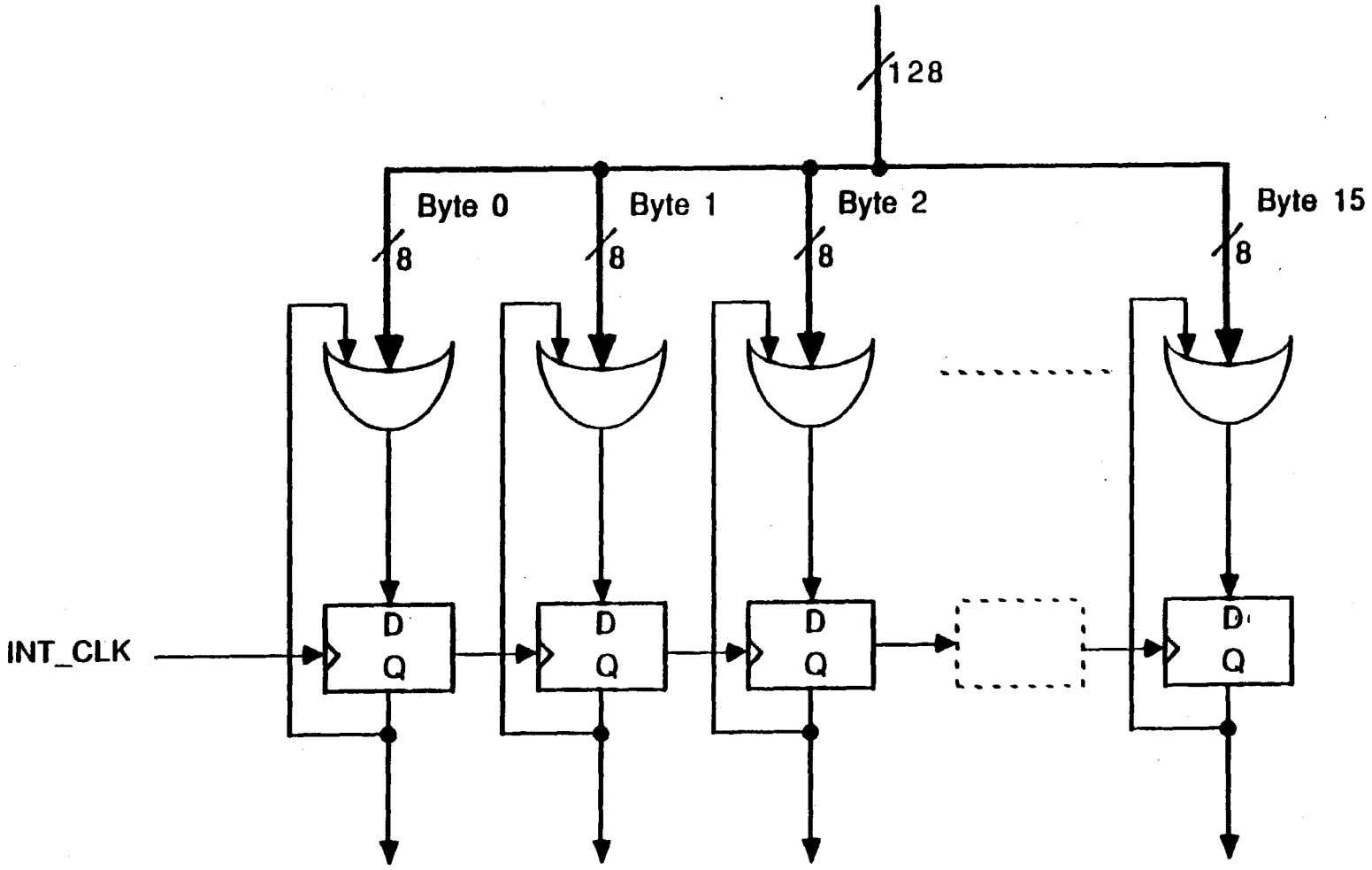


Figure 4: Byte Integration

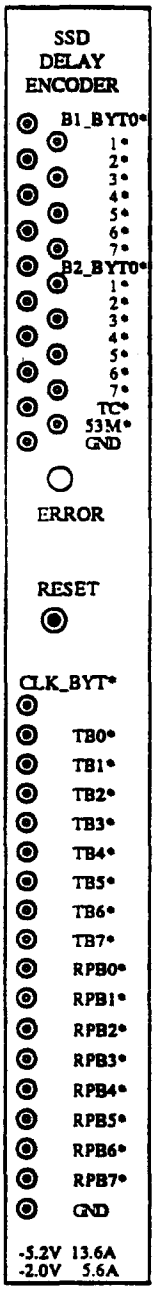
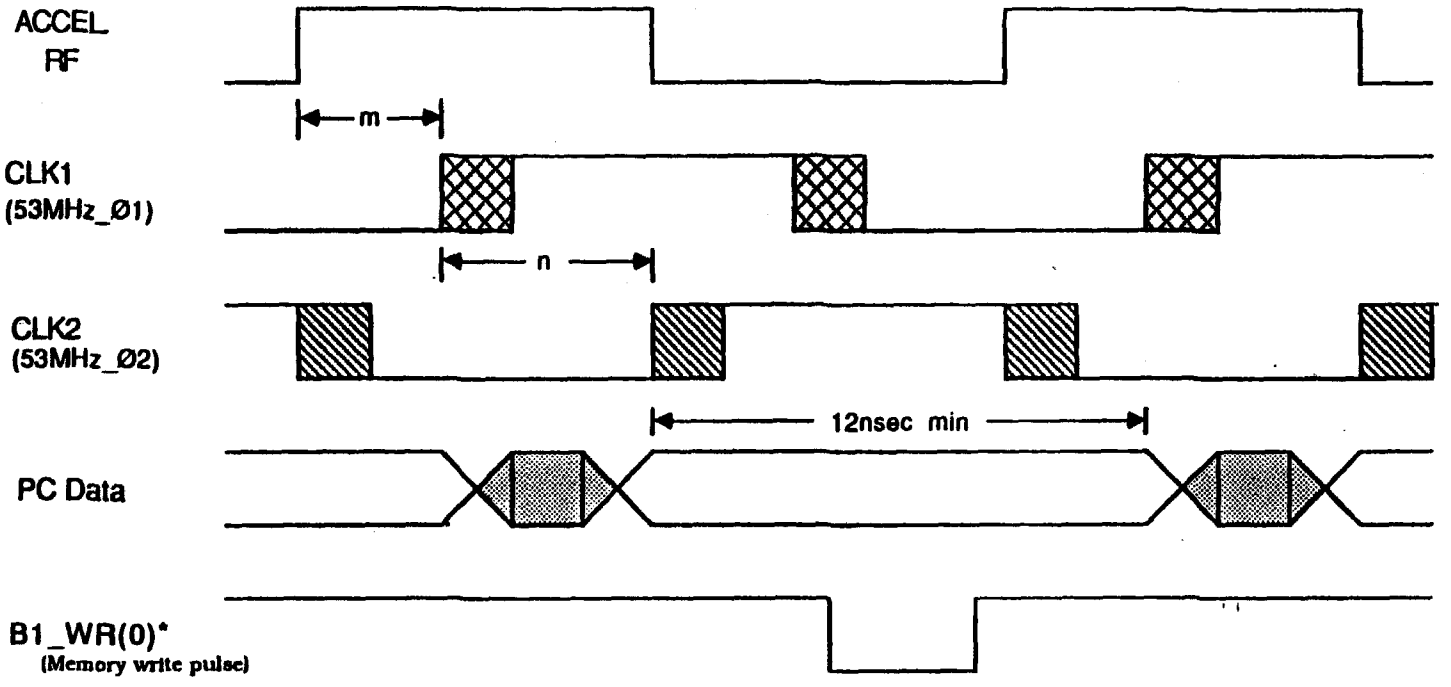
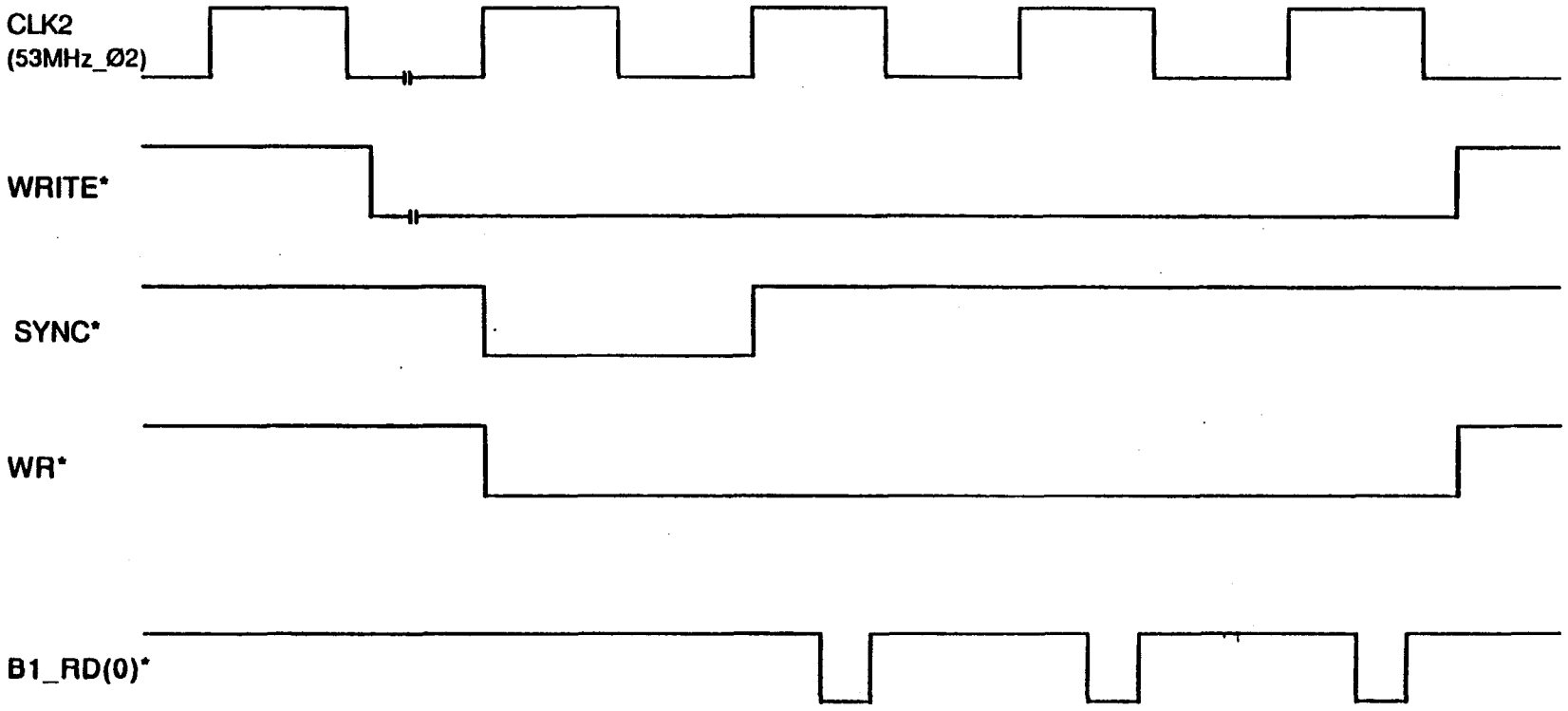


Figure 5: Front Panel Layout



m - Delay added to synchronize the PC to the accelerator RF.
n - Delay added to CLK1 clock to synchronize the DE to the PC output data.

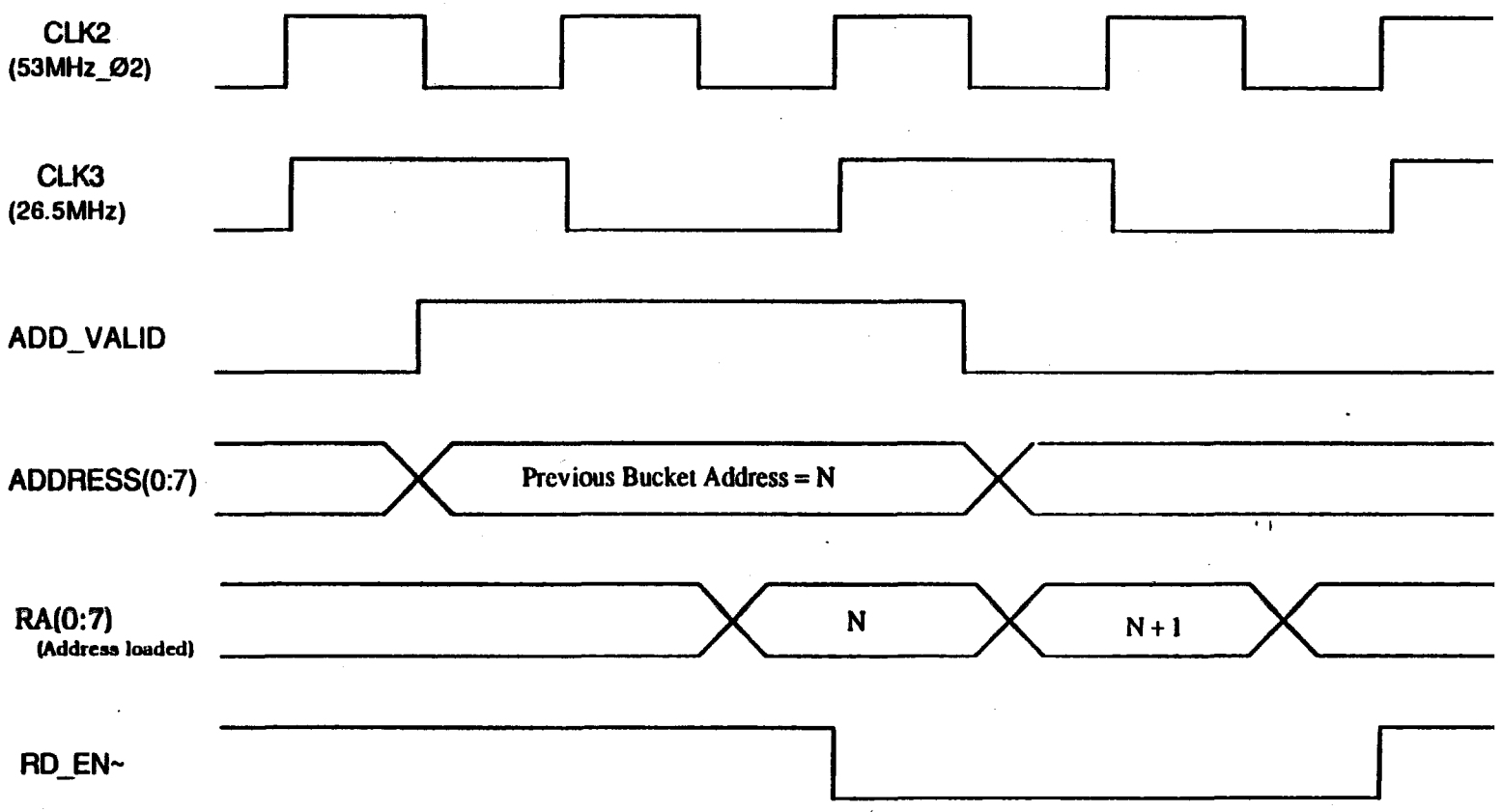
Timing 1: Synchronization of DE to PC.



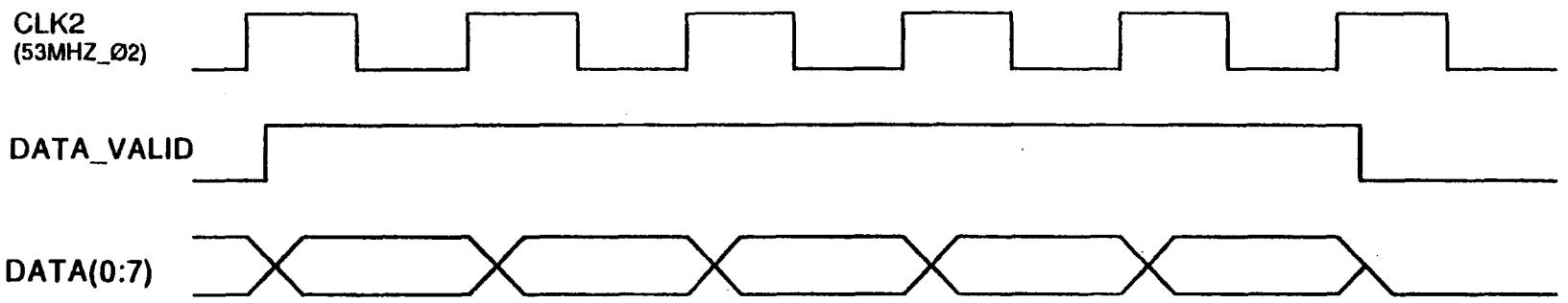
DESCRIPTION:

WRITE*	- Write enable signal on the auxiliary backplane driven by Sequencer.
SYNC*	- Synchronization signal generated by MTC and driven on the backplane by the SEQ.
WR*	- DE internally synchronized write enable signal.
B1_WR(0)*	- A typical write pulse for the memories.

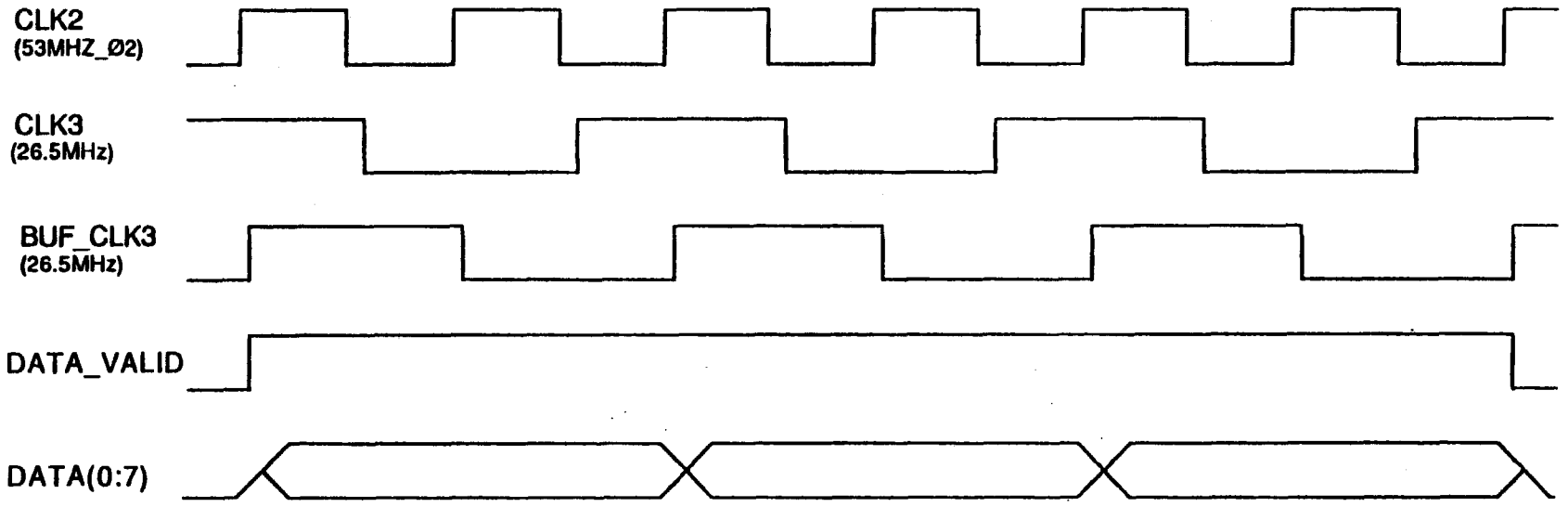
Timing 2: Write Enable Synchronization.



Timing 3: Address Transfer from SEQ to DE.



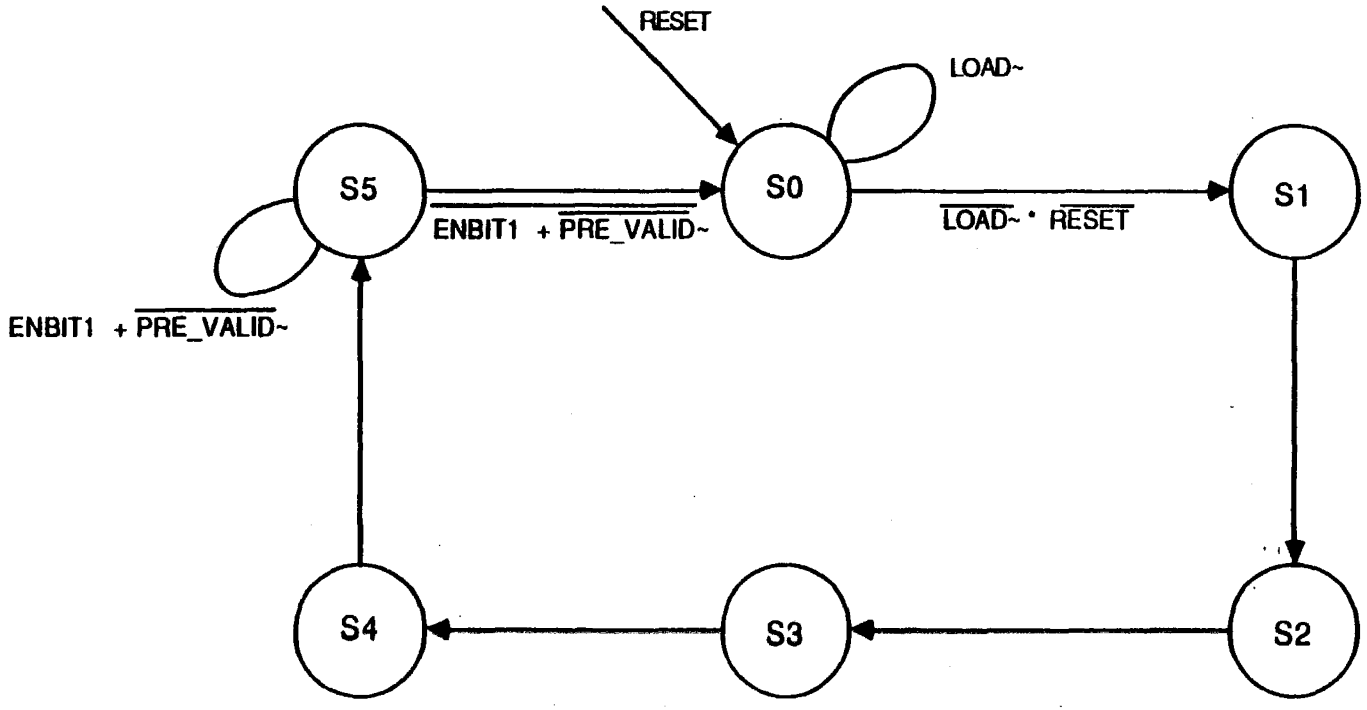
Timing 4a : 53MHz Encoded Event Transfer



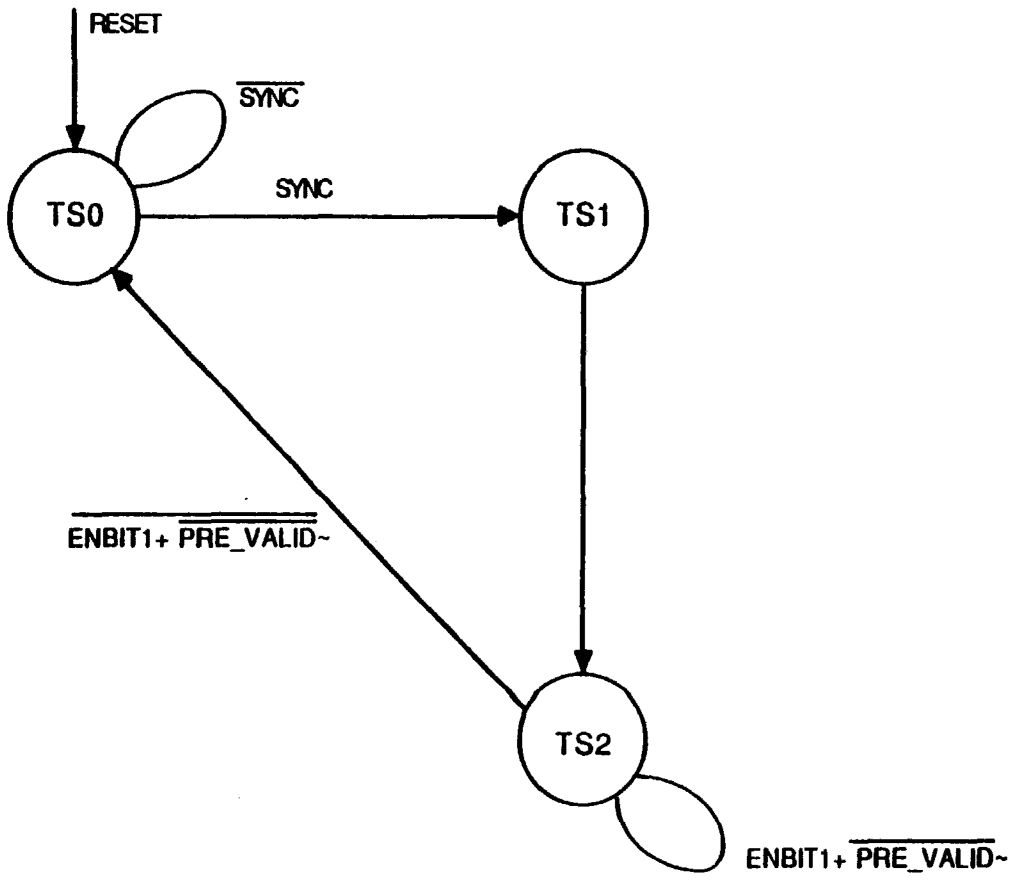
Timing 4b: 26.5MHz Encoded Event Transfer

10. Appendix E

State Machine
and
Pal Equation Used in DE



ENCODER PRIMARY STATE MACHINE



ENCODER DATA TRANSFER STATE MACHINE

EQUATIONS:

S0 = RESET + S0 * LOAD~ + S5 * (NOT (ENBIT1 + NOT (PRE_VALID~))): ;

S1 = S0 * (NOT LOAD~) * (NOT RESET);

S2 = S1;

S3 = S2;

S4 = S3;

S5 = (NOT RESET) * (S4 + S5 * (ENBIT1 + NOT (PRE_VALID~)));

TS0 = RESET + TS0 * (NOT SYNC) + TS2 * (NOT (ENBIT1 + PRE_VALID~)));

TS1 = TS0 * SYNC * (NOT RESET);

TS2 = (NOT RESET) * (TS1 + TS2 * (ENBIT1 + (NOT PRE_VALID~)));

```
module DE_CONTROL

title    'State Control for the Delay/Encoder

            Revisions:

                    Hector L. Gonzalez
                    January 29, 1990'

        DE_CNTRL            DEVICE          'EC20P8M';

"inputs

        S0, S3, S4, S5              PIN     1, 2, 3, 11;
        RESET                       PIN     9;
        SYNC                        PIN     10;
        !LOAD                       PIN     13;
        !EN_BIT1                    PIN     14;
        !PRE_VALID                  PIN     15;
        TS0, TS1, TS2               PIN     16, 22, 23;

"outputs

        PS0, PS1, PS4, PS5          PIN     [illegible]
        PTS0, PTS1, PTS2            PIN     [illegible]


equations

        PS0  =  RESET
              # S0 & !LOAD & !RESET
              # S5 & !(EN_BIT1 # PRE_VALID) & !RESET;

        PS1 =   S0 & LOAD & !RESET;

        PS4 =   S3 & !RESET;

        PS5 =   S4 & !RESET
              # S5 & (EN_BIT1 # PRE_VALID) & !RESET;

        PTS0 = RESET
              # TS0 & !SYNC & !RESET
              # TS2 & !(EN_BIT1 # PRE_VALID) & !RESET;

        PTS1 = TS0 & SYNC & !RESET;

        PTS2 = TS1 & !RESET
              # TS2 & (EN_BIT1 # PRE_VALID ) & !RESET;

end  DE_CONTROL
```

11. Appendix F

Parts List

DELAY 24

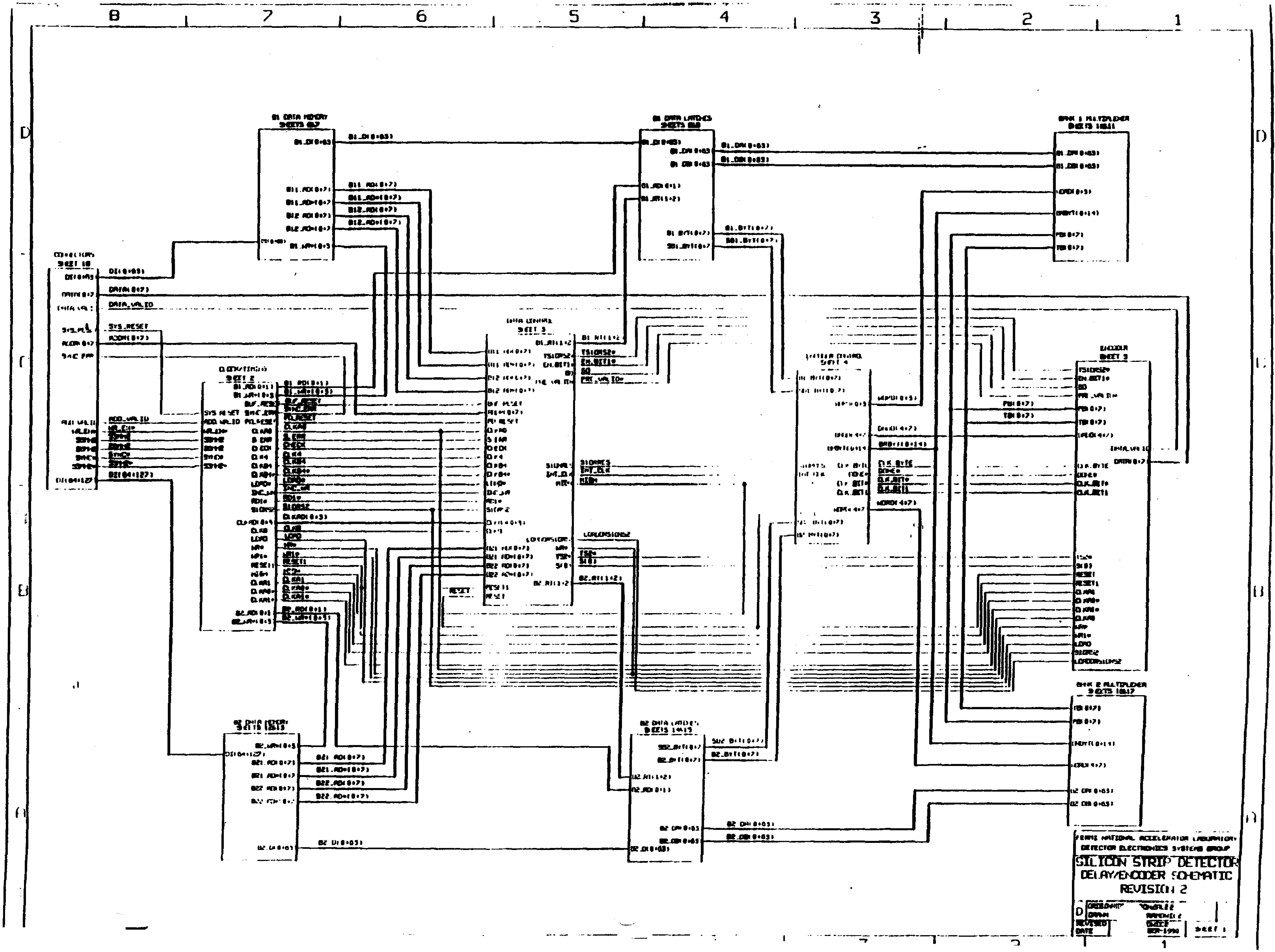
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
1	Part Number	Quantity/	IEE(mA)	IEE(mA)	IEE(typ)	IEE(max	Price /	Cost/	Parts	Spares	Total	Parts	Qty. to	Qty.	Qty.	Total Cost /
2		Board	Typical	Maximum	Total	Total	1000 Qty	Board	Needed	Needed	Needed	on hand	Order	Ordered	Rec'd.	24
3																
4	MC10E016FN	2	151	181	0.30	0.36	$28.20	$56.40	48	5	53	49	4	0	0	$1,494.60
5	MC10H101P	7	20	26	0.14	0.18	$0.60	$4.20	168	17	185	161	24	0	0	$111.00
6	MC10H102P	6	20	26	0.12	0.16	$0.60	$3.60	144	14	158	374	-216	0	0	$94.80
7	MC10H103P	6	21	26	0.13	0.16	$0.60	$3.60	144	14	158	272	-114	0	0	$94.80
8	MC10H104P	2	35	35	0.07	0.07	$0.60	$1.20	48	5	53	109	-56	0	0	$31.80
9	MC10H107P	4	28	28	0.11	0.11	$0.65	$2.60	96	10	106	217	-111	0	0	$68.90
10	MC10H109P	18	11	14	0.20	0.25	$0.76	$13.68	432	43	475	793	-318	0	0	$361.00
11	MC10E111FN	1	48	60	0.05	0.06	$23.47	$23.47	24	2	26	41	-15	0	0	$610.22
12	MC10E112FN	1	47	56	0.05	0.06	$9.00	$9.00	24	2	26	36	-10	0	0	$234.00
13	MC10H131P	12	45	56	0.54	0.67	$1.50	$18.00	288	29	317	600	-283	0	0	$475.50
14	MC10H131FN	16	45	56	0.72	0.90	$1.90	$30.40	384	38	422	385	37	0	0	$801.80
15	MC10E131FN	3	58	70	0.17	0.21	$12.60	$37.80	72	7	79	131	-52	0	0	$995.40
16	MC10E151FN	6	65	85	0.39	0.51	$13.76	$82.56	144	14	158	162	-4	0	0	$2,174.08
17	MC10H158P	3	38	48	0.11	0.14	$1.35	$4.05	72	7	79	106	-27	0	0	$106.65
18	MC10H159FN	32	42	53	1.34	1.70	$2.03	$64.96	768	77	845	849	-4	0	0	$1,715.35
19	MC10H162P	3	61	76	0.18	0.23	$1.50	$4.50	72	7	79	82	-3	0	0	$118.50
20	MC10H164P	1	60	75	0.06	0.08	$1.45	$1.45	24	2	26	31	-5	0	0	$37.70
21	MC10H165P	3	105	131	0.32	0.39	$5.10	$15.30	72	7	79	187	-8	0	0	$402.90
22	MC10H176P	46	88	112	4.05	5.15	$2.36	$108.56	1104	110	1214	1202	12	0	0	$2,865.04
23	MC10H186P	6	88	110	0.53	0.66	$3.25	$19.50	144	14	158	143	15	0	0	$513.50
24	MC10H188P	1	42	42	0.04	0.04	$1.00	$1.00	24	2	26	31	-5	0	0	$26.00
25	MC10198P	1	80	100	0.08	0.10	$13.00	$13.00	24	2	26	47	-21	0	0	$338.00
26	MBM10422-5	32	150	175	4.80	5.60	$8.33	$266.56	768	77	845	9000	-8155	0	0	$7,038.85
27	TIE10H16P8-6	1	210	210	0.21	0.21	$30.41	$30.41	24	2	26	35	-9	0	0	$790.66
28	ICO-324-SGG SOC.	1	0	0	0.00	0.00	$1.65	$1.65	24	2	26	100	-74	0	0	$42.90
29	FDD3510	1	0	0	0.00	0.00	$8.00	$8.00	24	2	26	0	26	0	0	$208.00
30	FDD4010	1	0	0	0.00	0.00	$8.00	$8.00	24	2	26	100	-74	0	0	$208.00
31	FDA6010	3	0	0	0.00	0.00	$8.00	$24.00	72	7	79	78	1	0	0	$632.00
32	FDA7010	1	0	0	0.00	0.00	$8.00	$8.00	24	2	26	19	7	0	0	$208.00
33	4309R-101-470	8	0	0	0.00	0.00	$0.15	$1.20	192	19	211	69	142	0	0	$31.65
34	4308R-101-101	72	0	0	0.00	0.00	$0.15	$10.80	1728	173	1901	3000	-1099	0	0	$285.15
35	4309R-101-101	59	0	0	0.00	0.00	$0.20	$11.80	1416	142	1558	2500	-942	0	0	$311.60
36	2-532956-0	1	0	0	0.00	0.00	$9.50	$9.50	24	2	26	0	26	0	0	$247.00
37	534974-9	1	0	0	0.00	0.00	$26.00	$26.00	24	2	26	0	26	0	0	$676.00
38	50 OHM RES.	16	0	0	0.00	0.00	$0.04	$0.64	384	38	422	0	422	0	0	$16.88
39	100 OHM RES.	4	0	0	0.00	0.00	$0.04	$0.16	96	10	106	0	106	0	0	$4.24

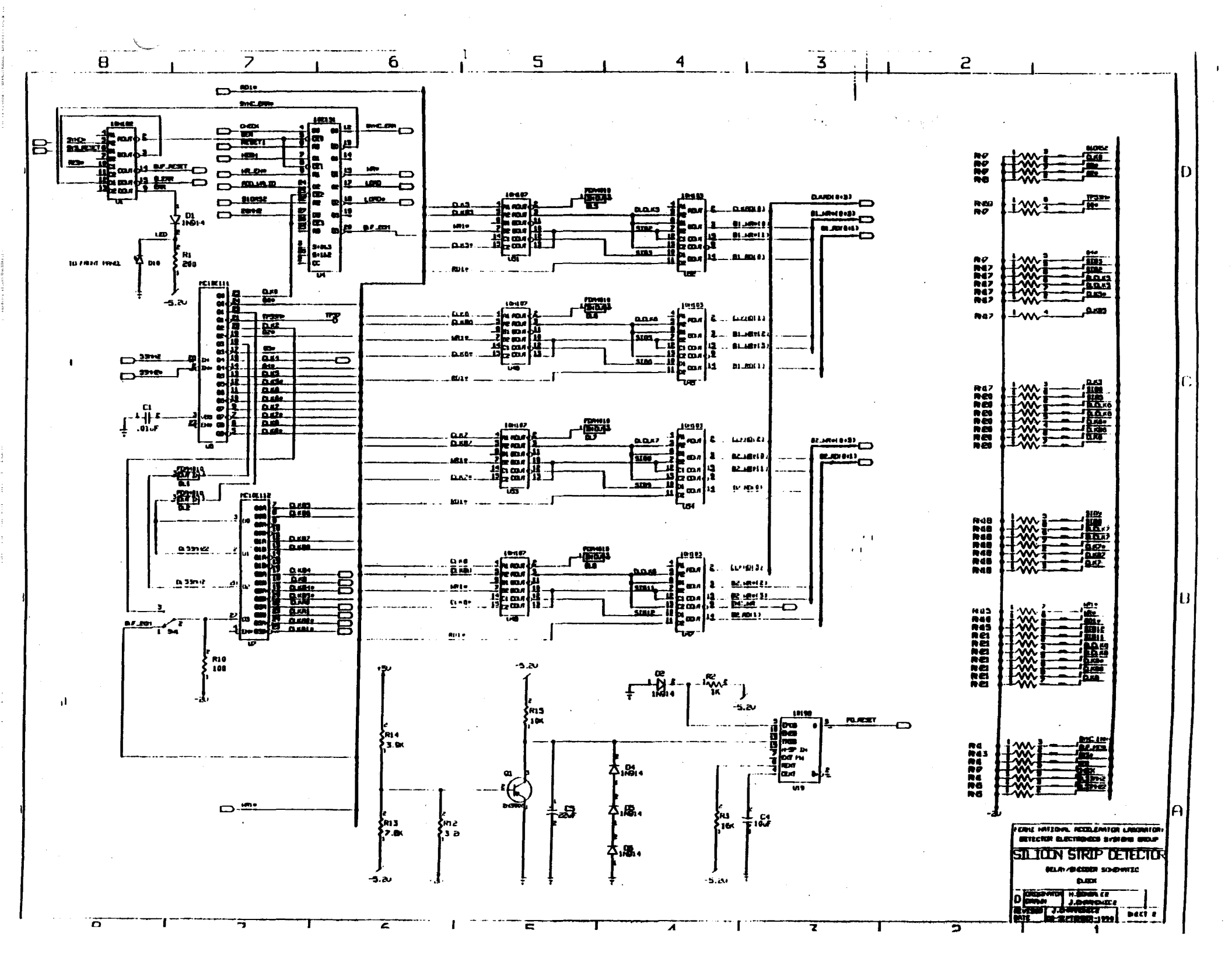
DELAY 24

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
1	Part Number	Quantity/	IEE(mA)	IEE(mA)	IEE(typ)	IEE(max)	Price /	Cost/	Parts	Spares	Total	Parts	Qty. to	Qty.	Qty.	Total Cost /
2		Board	Typical	Maximum	Total	Total	1000 Qty	Board	Needed	Needed	Needed	on hand	Order	Ordered	Rec'd.	24
3																
40	200 OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
41	1K OHM RES.	3	0	0	0.00	0.00	$0.04	$0.12	72	7	79	0	79	0	0	$3.16
42	3.2K OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
43	3.9K OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
44	7.8K OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
45	10K OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
46	16K OHM RES.	1	0	0	0.00	0.00	$0.04	$0.04	24	2	26	0	26	0	0	$1.04
47	20 pF CAP	4	0	0	0.00	0.00	$0.20	$0.80	96	10	106	0	106	0	0	$21.20
48	KEMET 4.7 uF CAP	10	0	0	0.00	0.00	$0.14	$1.40	240	24	264	245	19	0	0	$36.96
49	10uF CAP.	1	0	0	0.00	0.00	$0.75	$0.75	24	2	26	0	26	0	0	$19.50
50	22UF CAP.	1	0	0	0.00	0.00	$0.75	$0.75	24	2	26	0	26	0	0	$19.50
51	47uF CAP.	2	0	0	0.00	0.00	$0.75	$1.50	48	5	53	0	53	0	0	$39.75
52	1N914 DIODE	7	0	0	0.00	0.00	$0.15	$1.05	168	17	185	0	185	0	0	$27.75
53	2N3906 TRANS.	1	0	0	0.00	0.00	$0.20	$0.20	24	2	26	36	-10	0	0	$5.20
54	ICTE-5 DIODE	2	0	0	0.00	0.00	$0.75	$1.50	48	5	53	0	53	0	0	$39.75
55	TP12H9AB SW.	1	0	0	0.00	0.00	$4.53	$4.53	24	2	26	31	-5	0	0	$117.78
56	275005 FUSE	7	0	0	0.00	0.00	$0.75	$5.25	168	17	185	0	185	0	0	$138.75
57	2-331272-2 SOC.	16	0	0	0.00	0.00	$0.23	$3.68	384	38	422	0	422	0	0	$97.06
58	40F6261 TEST PT.	37	0	0	0.00	0.00	$0.37	$13.69	888	89	977	1200	-223	0	0	$361.49
59	1447-0475 RED LED	1	0	0	0.00	0.00	$0.20	$0.20	24	2	26	0	26	0	0	$5.20
60	923CZ5U103M050B	221	0	0	0.00	0.00	$0.20	$44.20	5304	530	5834	4800	1034	0	0	$1,166.80
61	CIRCUIT BOARD	1	0	0	0.00	0.00	$400.00	$400.00	24	0	24	0	24	0	0	$9,600.00
62	FRONT PANEL	1	0	0	0.00	0.00	$31.00	$31.00	24	0	24	0	24	0	0	$744.00
63	PNL. MTG. HDWR.	1	0	0	0.00	0.00	$1.00	$1.00	24	0	24	0	24	0	0	$24.00
64																
65	*IEE Typical =*	*14.71*	*Amps*	*IEE Max =*	*17.99*	*Amps*	*Cost/Bd.=*	*1,437.41*								
66	*Power Typ =*	*76*	*Watts*	*Power Max=*	*94*	*Watts*										
67																
68	*Last Updated:*	17-Oct		*Total # of*	*Boards*	24	*Ttl. Cost =*	*34,497.84*								

12. Appendix G

Circuit Diagrams


B1 DATA MEMORY
B1 DATA LATCHES
BANK 1 MULTIPLEXER
CONNECTORS
DATA CONTROL
CLOCK/TIMING
ENCODER
B2 DATA MEMORY
B2 DATA LATCHES
BANK 2 MULTIPLEXER
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP
SILICON STRIP DETECTOR
DELAY/ENCODER SCHEMATIC
REVISION 2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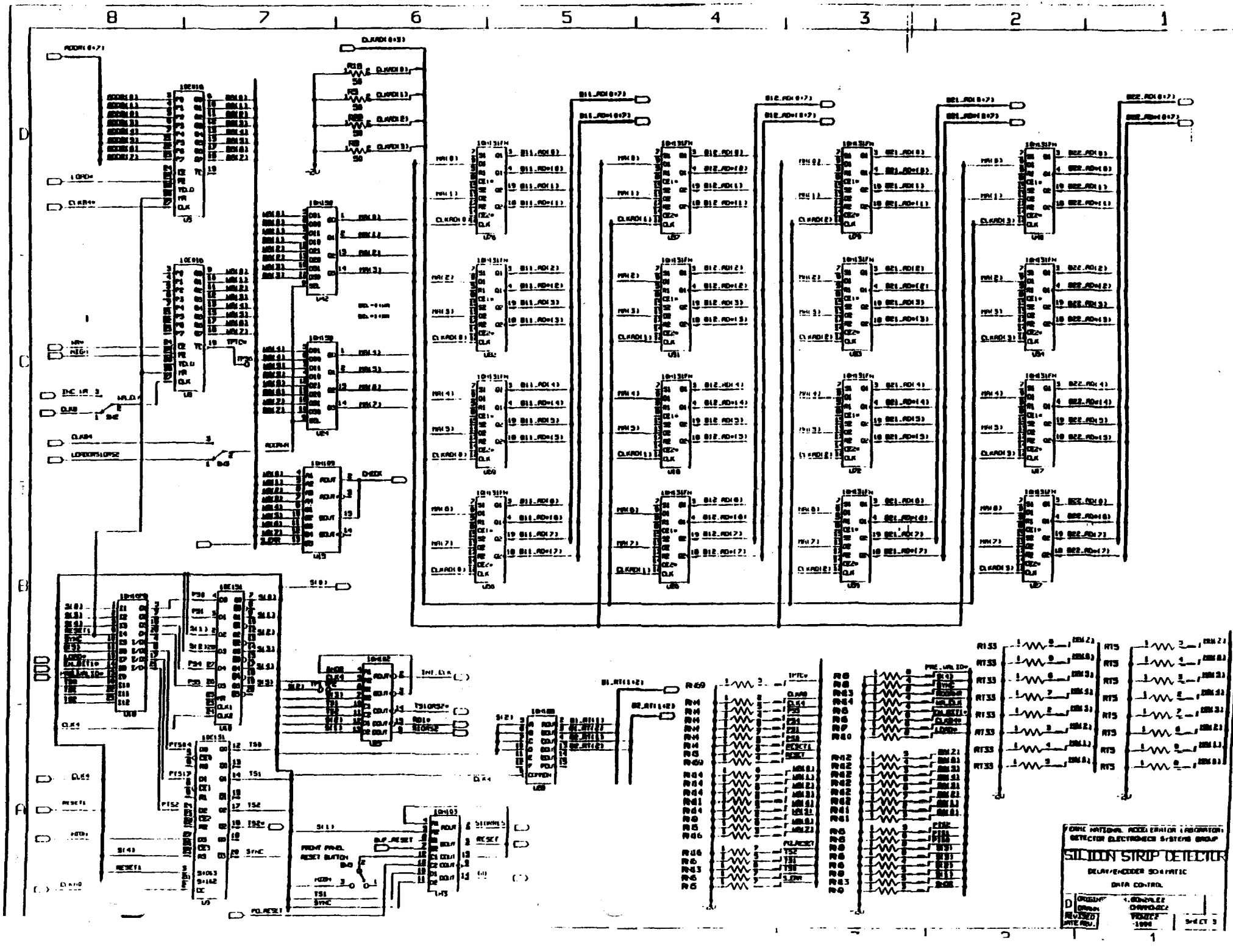
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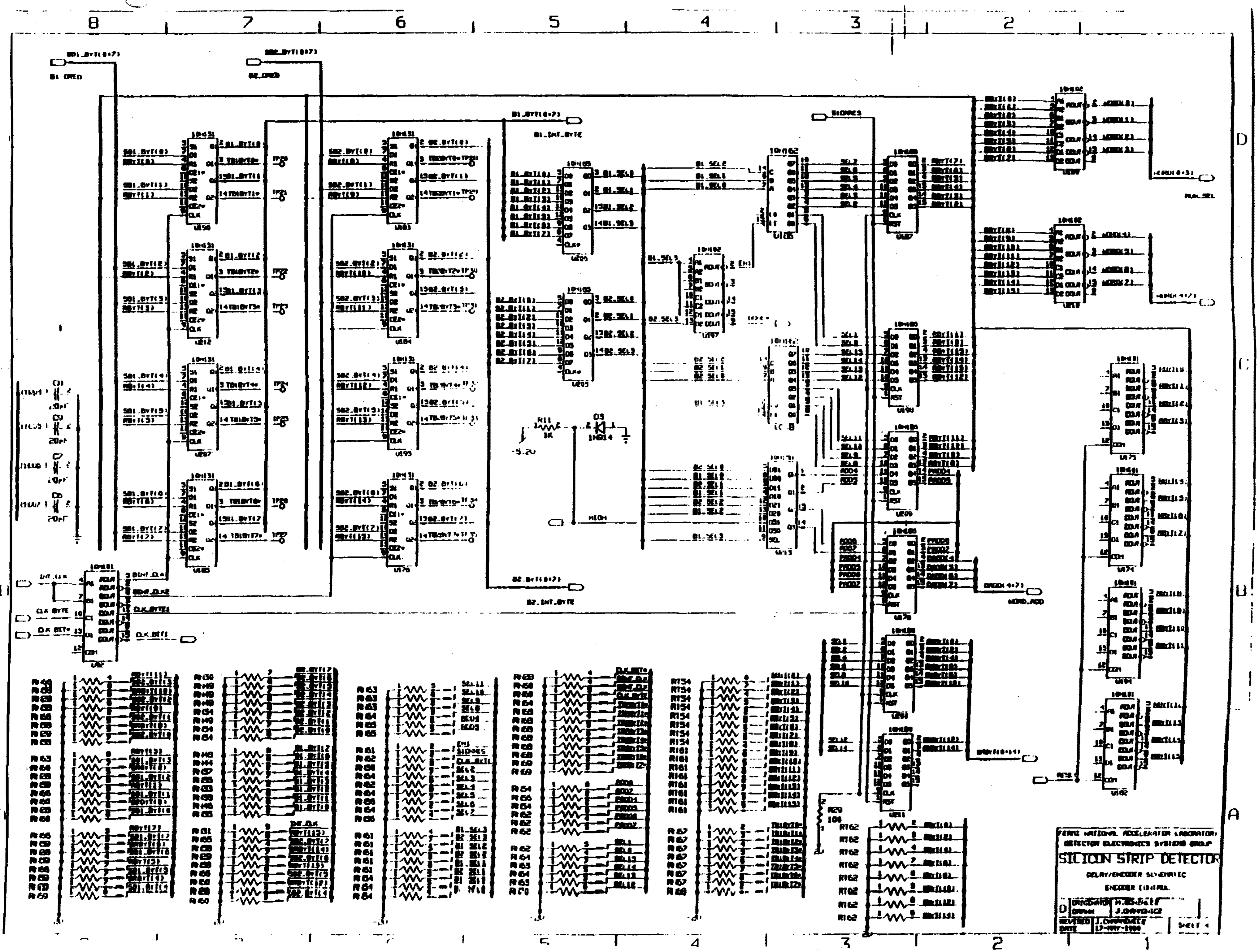
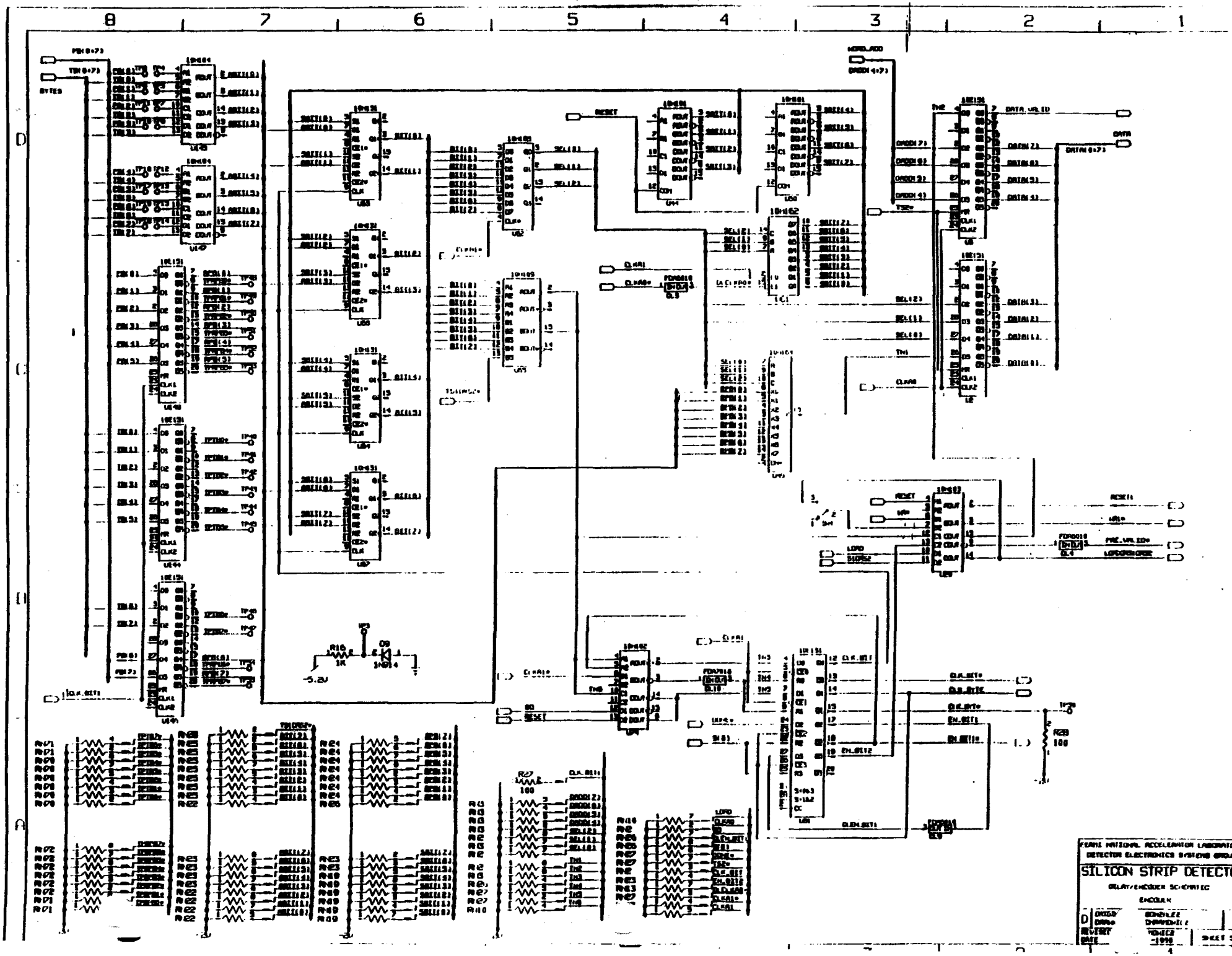
DELAY/ENCODER SCHEMATIC
DATA CONTROL


FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP
SILICON STRIP DETECTOR
DELAY/ENCODER SCHEMATIC
ORIGINATOR
DRAWN
REVISED
DATE
SHEET 4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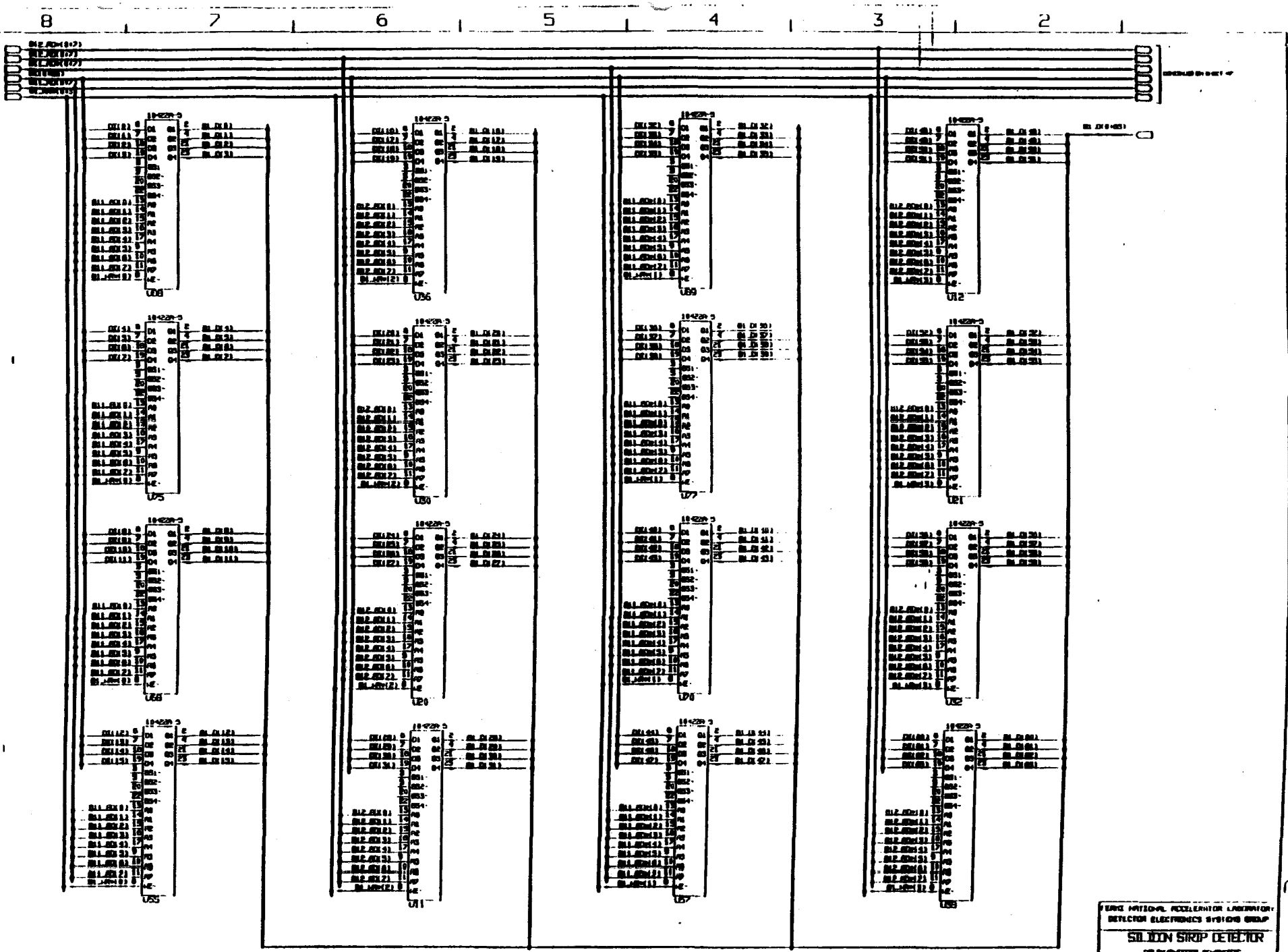
DATA
-5.2V
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP
SILICON STRIP DETECTOR
DELAY/ENCODER SCHEMATIC
ENCODER



FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

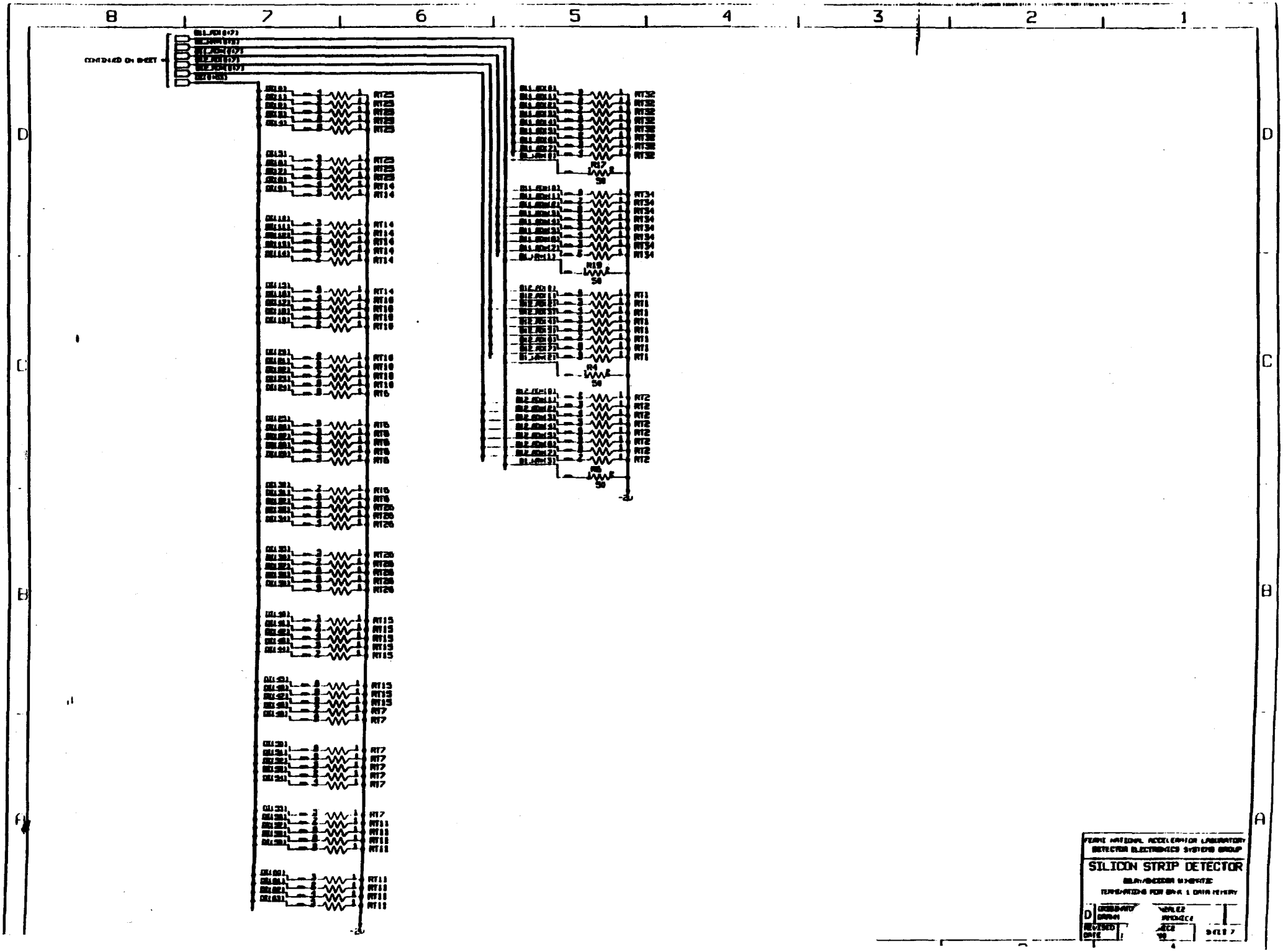
SILICON STRIP DETECTOR

DELAY/DECODER SCHEMATIC

BANK 1 DATA MEMORY

D	ORIGINATOR	W.BOWDEN
	DRAWN	J.CHRONOWICZ
	REVISED	J.CHRONOWICZ
	DATE	17-NOV-1988

SHEET 8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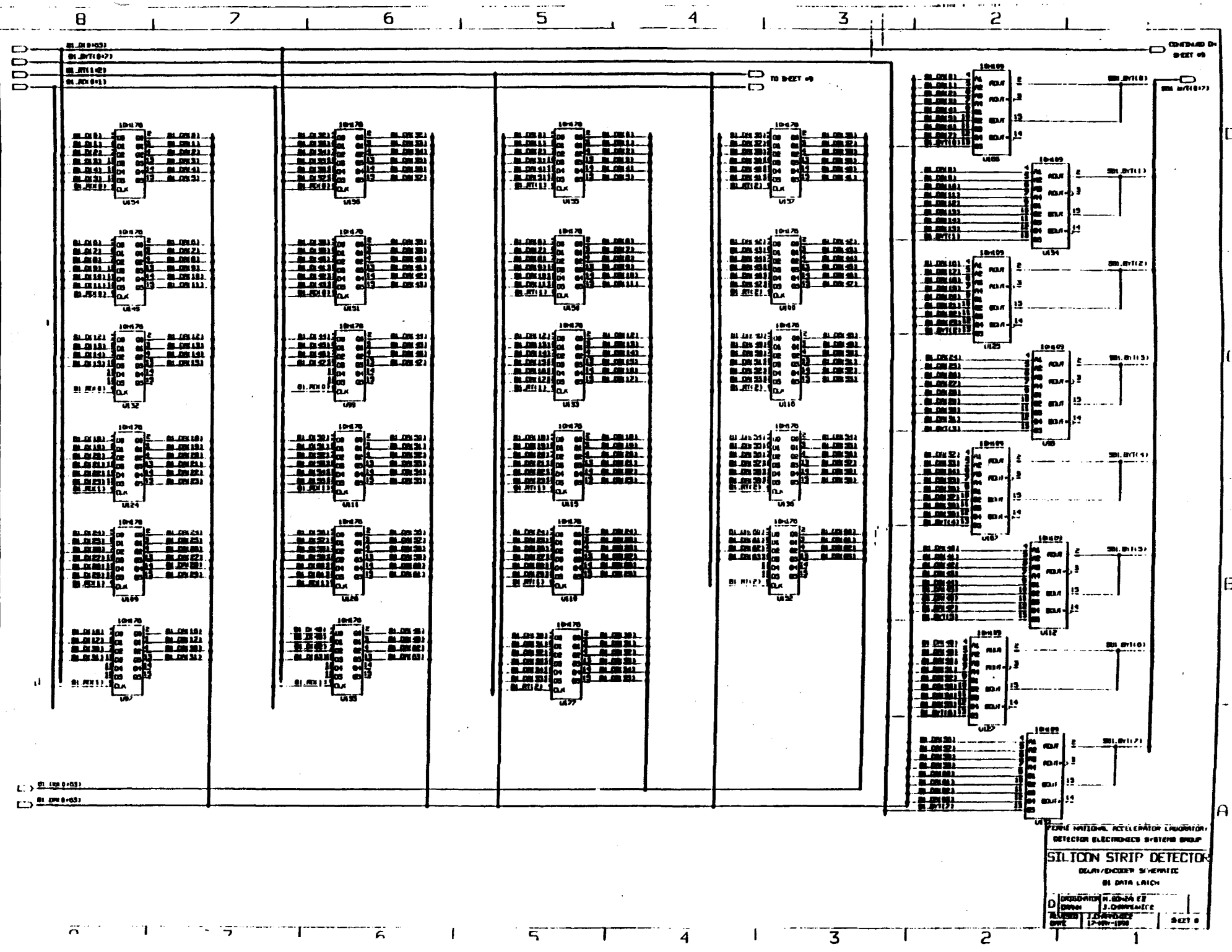
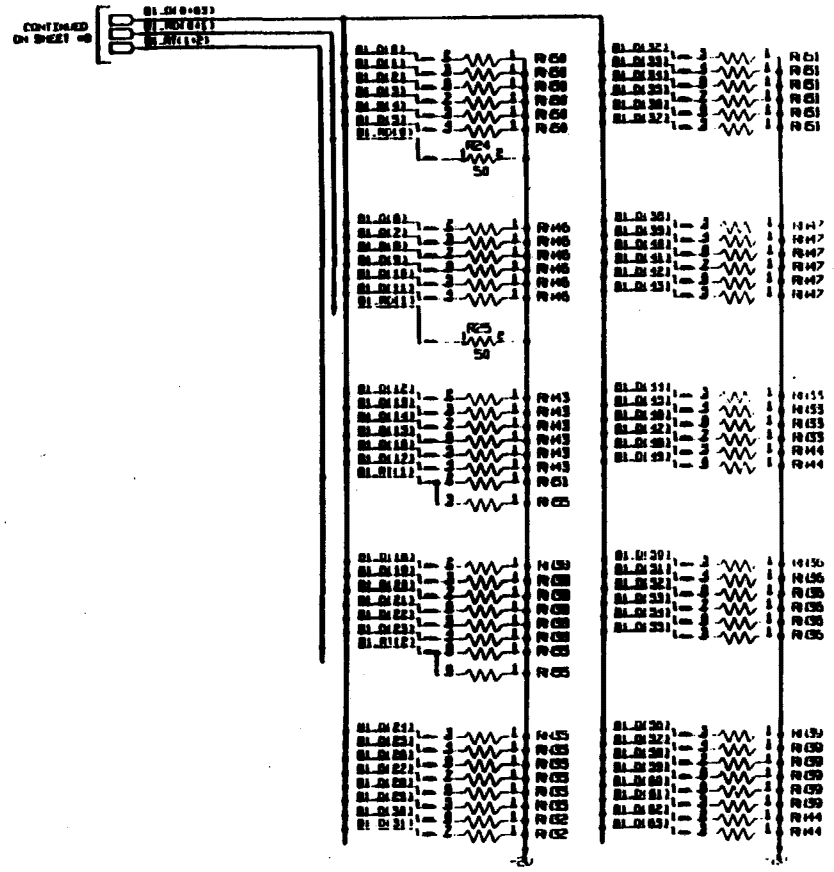
SILICON STRIP DETECTOR


TO SHEET #9
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP
SILICON STRIP DETECTOR
DELAY/DECODER SCHEMATIC
BI DATA LATCH



TERMINATORS FOR BANK 1 DATA LATCHES
(SHEET 9)

FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

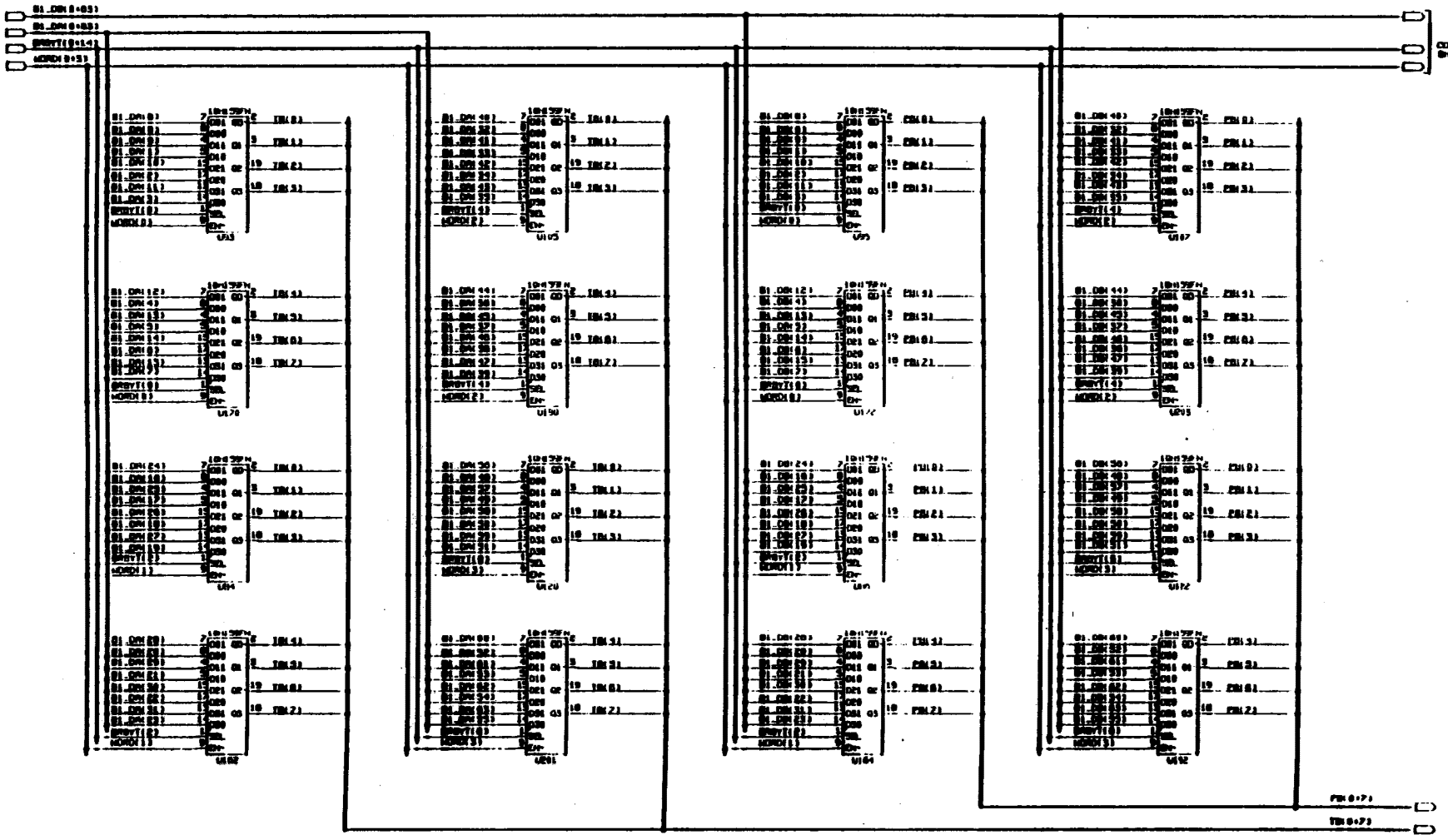
SILICON STRIP DETECTO

DELAY/ENCODER SCHEMATIC

TERMINATORS FOR BANK 1 DATA LATCHES

D

SHEET 9



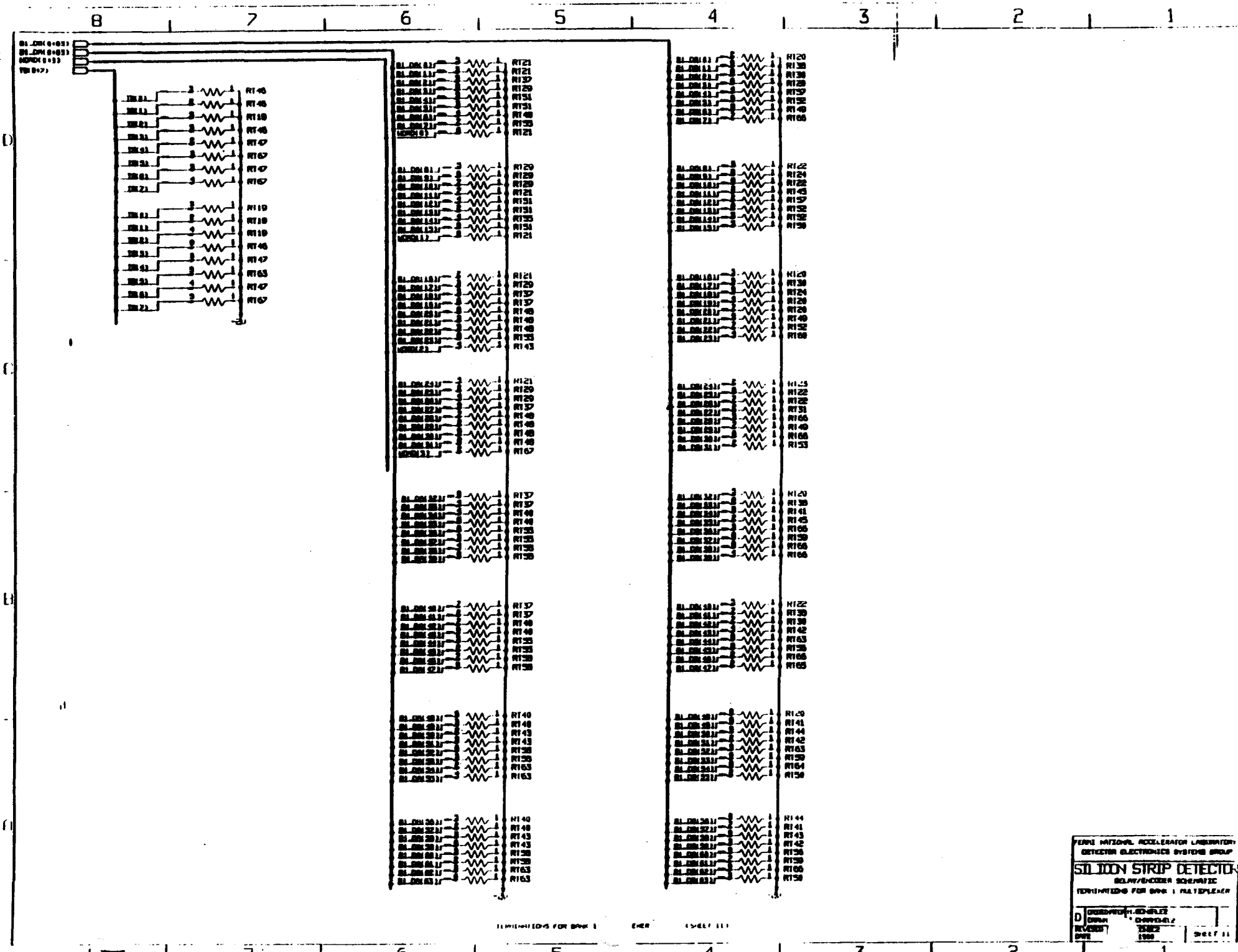
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

SILICON STRIP DETECTOR

DELAY/DECODER SCHEMATIC

ONE 1 MULTIPLEXER

0	DESIGNED	K.GOBLE
	DRAWN	J.DAWKINS
REVISED	J.DAWKINS	SHEET 10
DATE	12-FEB-1990	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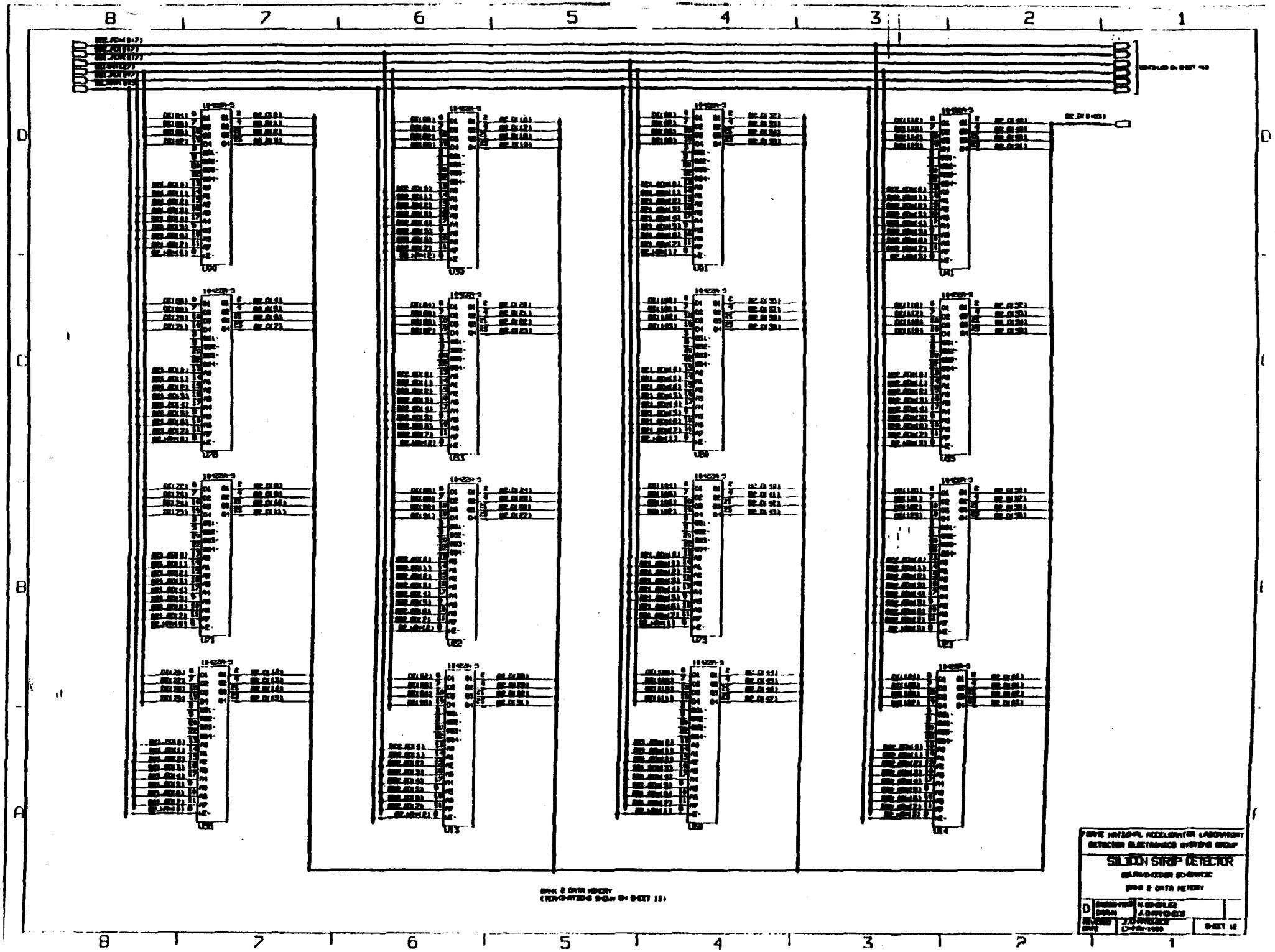
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP
SILICON STRIP DETECTOR
DELAY/ENCODER SCHEMATIC
TERMINATIONS FOR BANK 1 MULTIPLEXER
D
DRAWN
CHECKED
REVISED
DATE
1990
SHEET 11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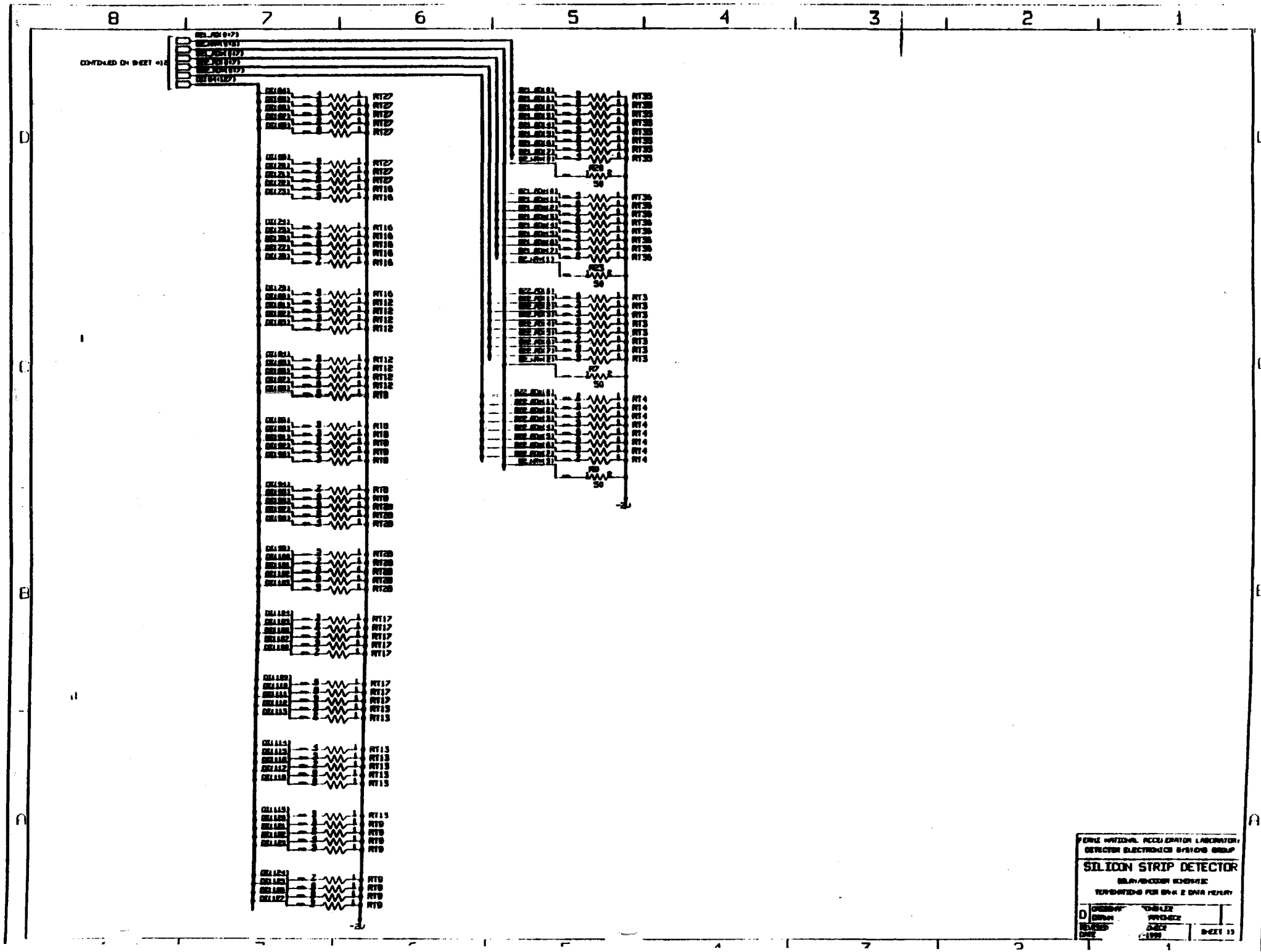
SILICON STRIP DETECTOR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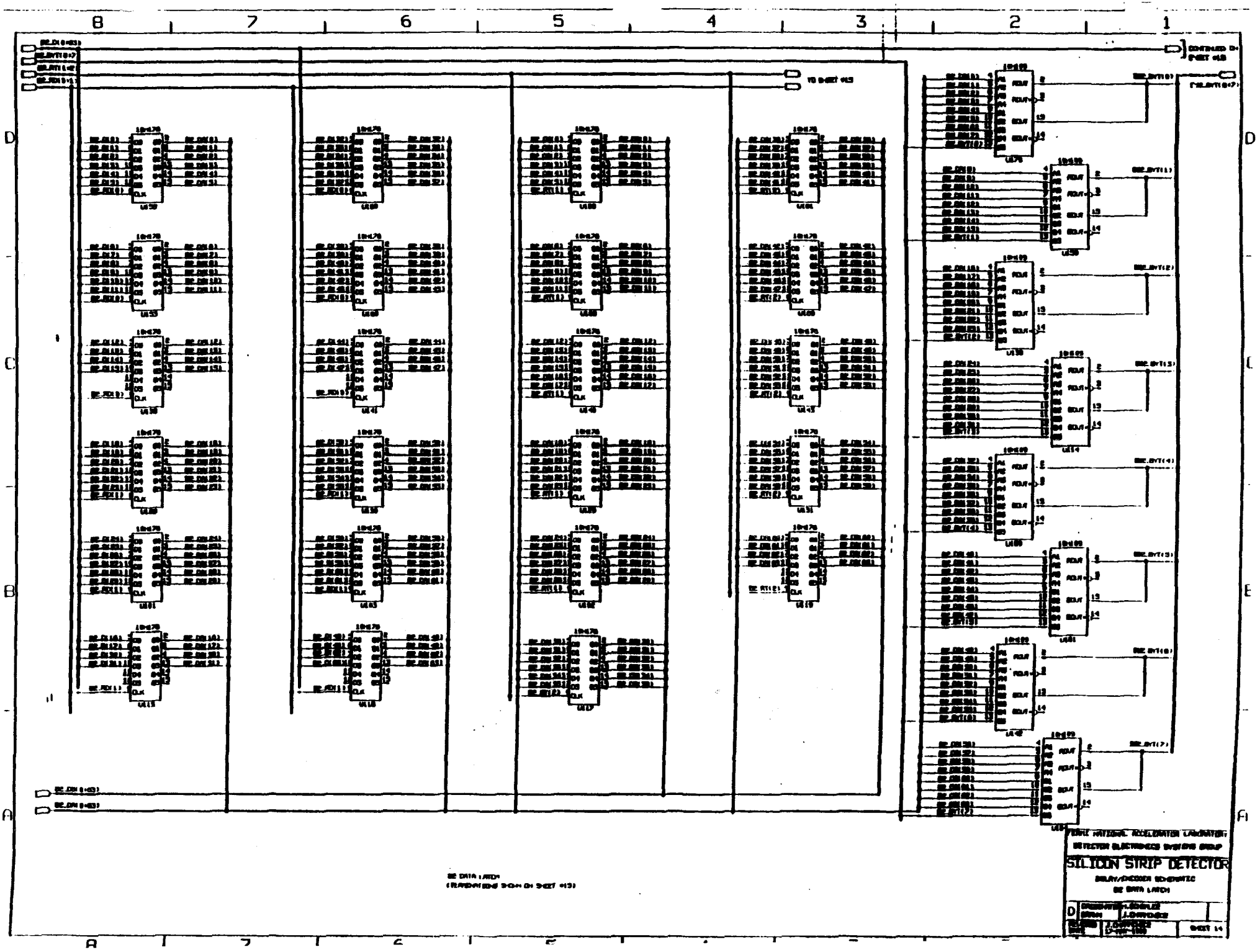
CONTINUED ON SHEET
SILICON STRIP DETECTOR
TERMINATIONS FOR SVX II DATA RETURN
SHEET 13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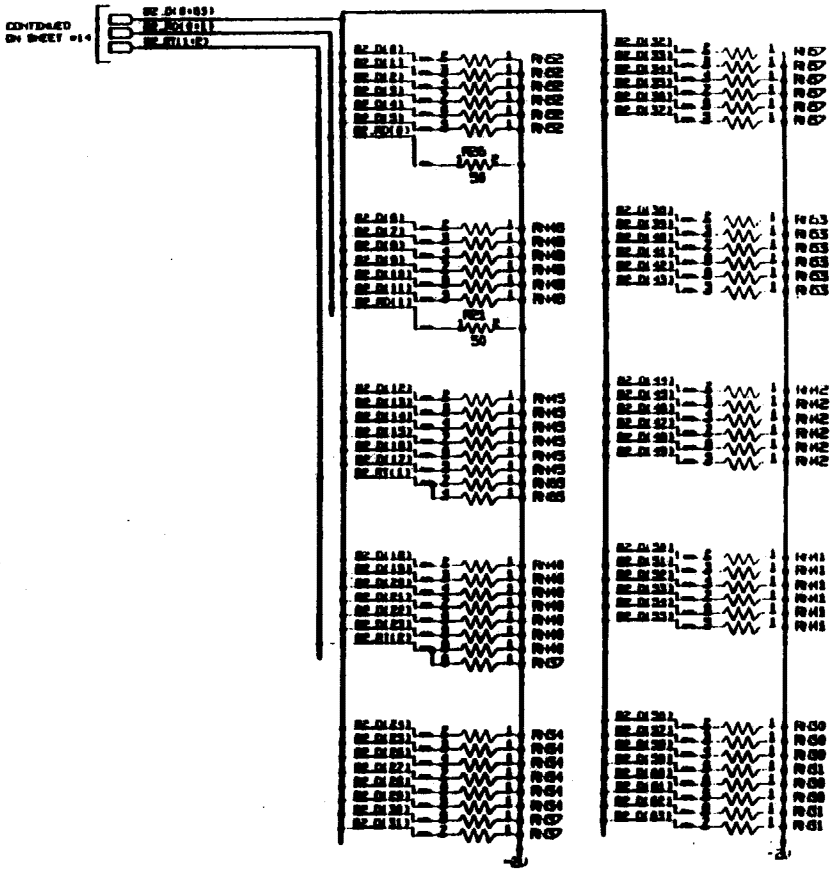
SILICON STRIP DETECTOR



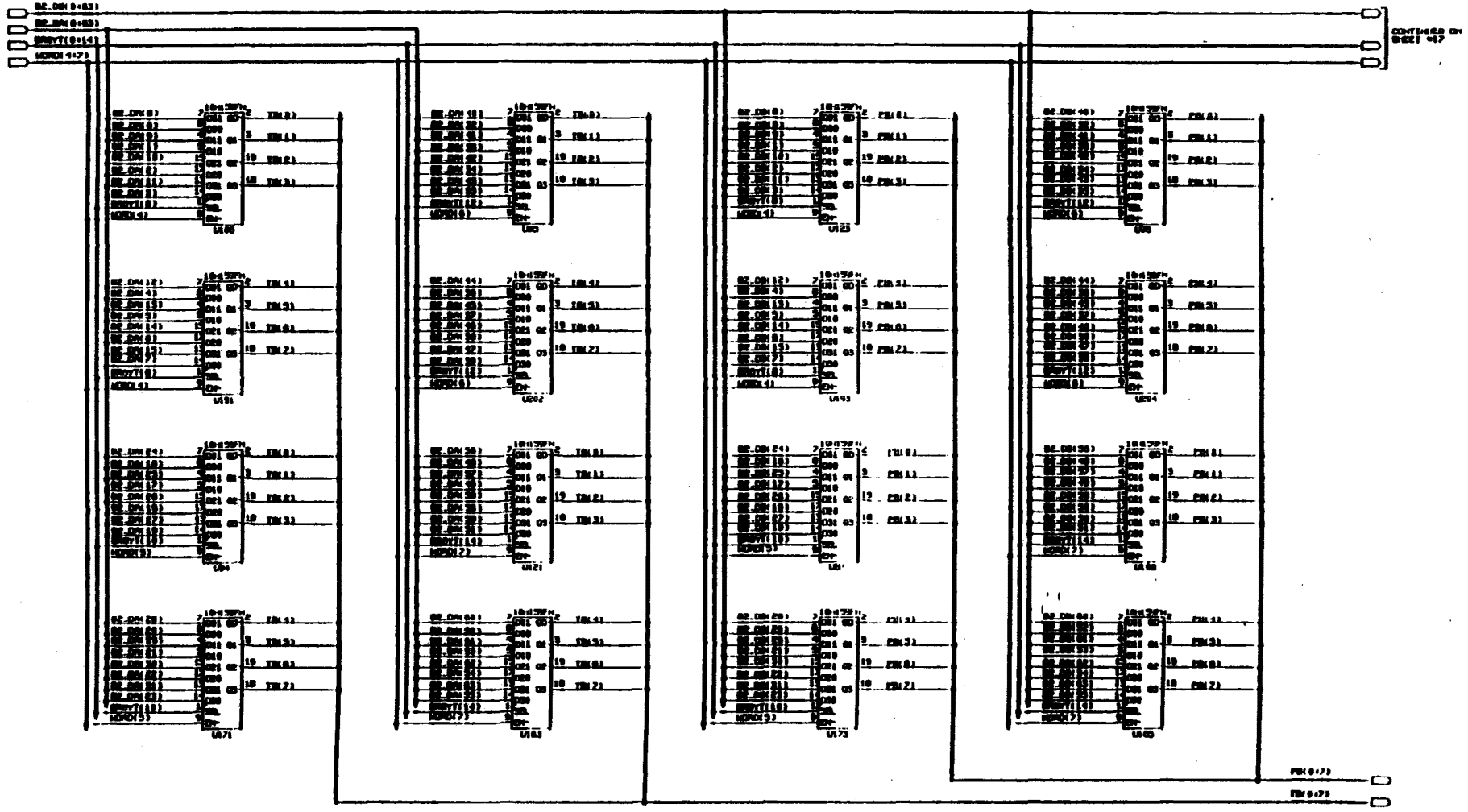
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

SILICON STRIP DETECTOR

DELAY/DECODER SCHEMATIC

TERMINATIONS FOR BANK 2 DATA LATCHES

D



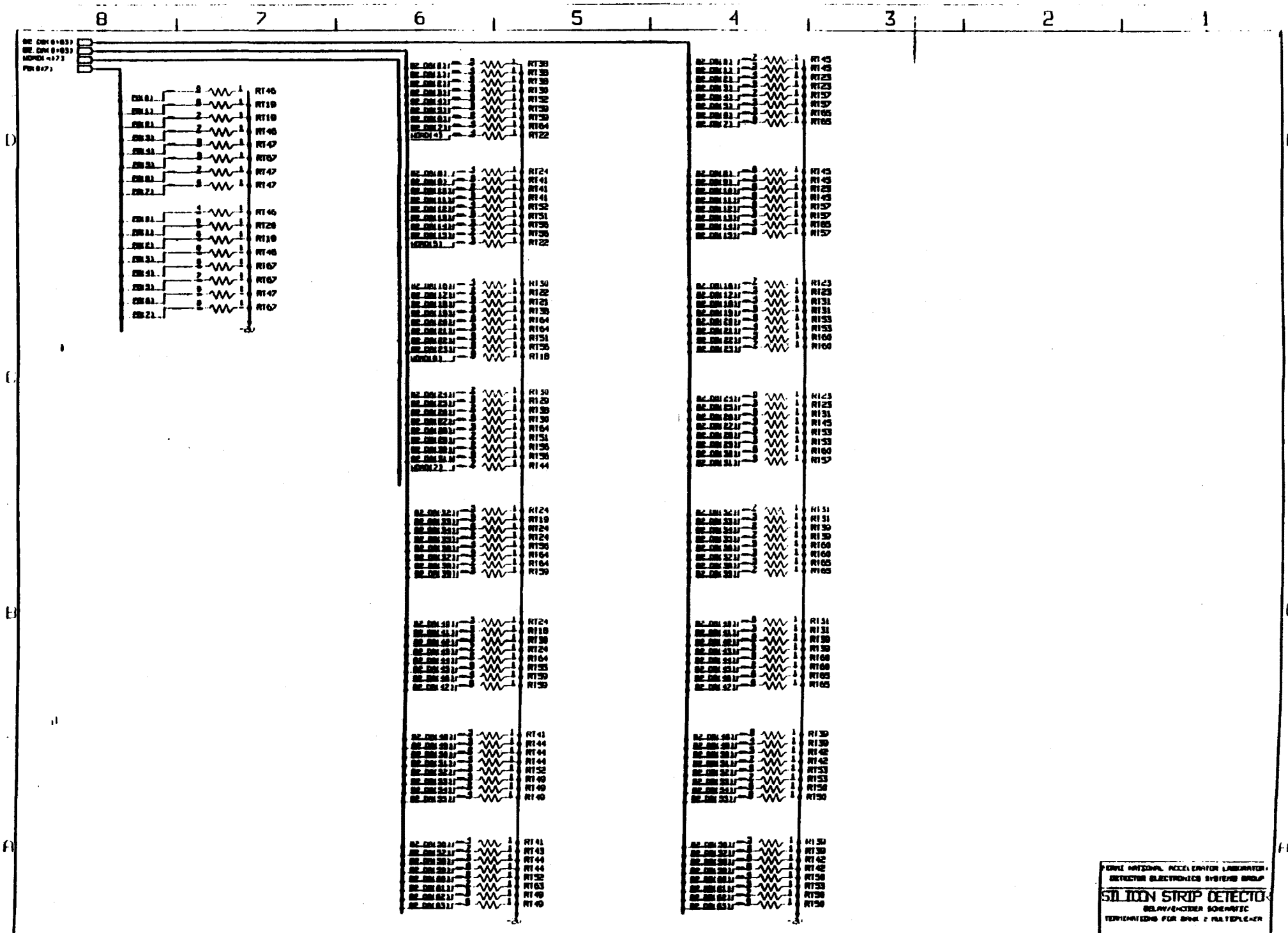
FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

SILICON STRIP DETECTOR

DELAY/ENCODER SCHEMATIC

DRWG 2 MULTIPLEXER

D	DESIGNED BY: J.DAWSON DRAWN: J.DAWSON	
REVISED DATE	J.DAWSON 12-DEC-1990	SHEET 16

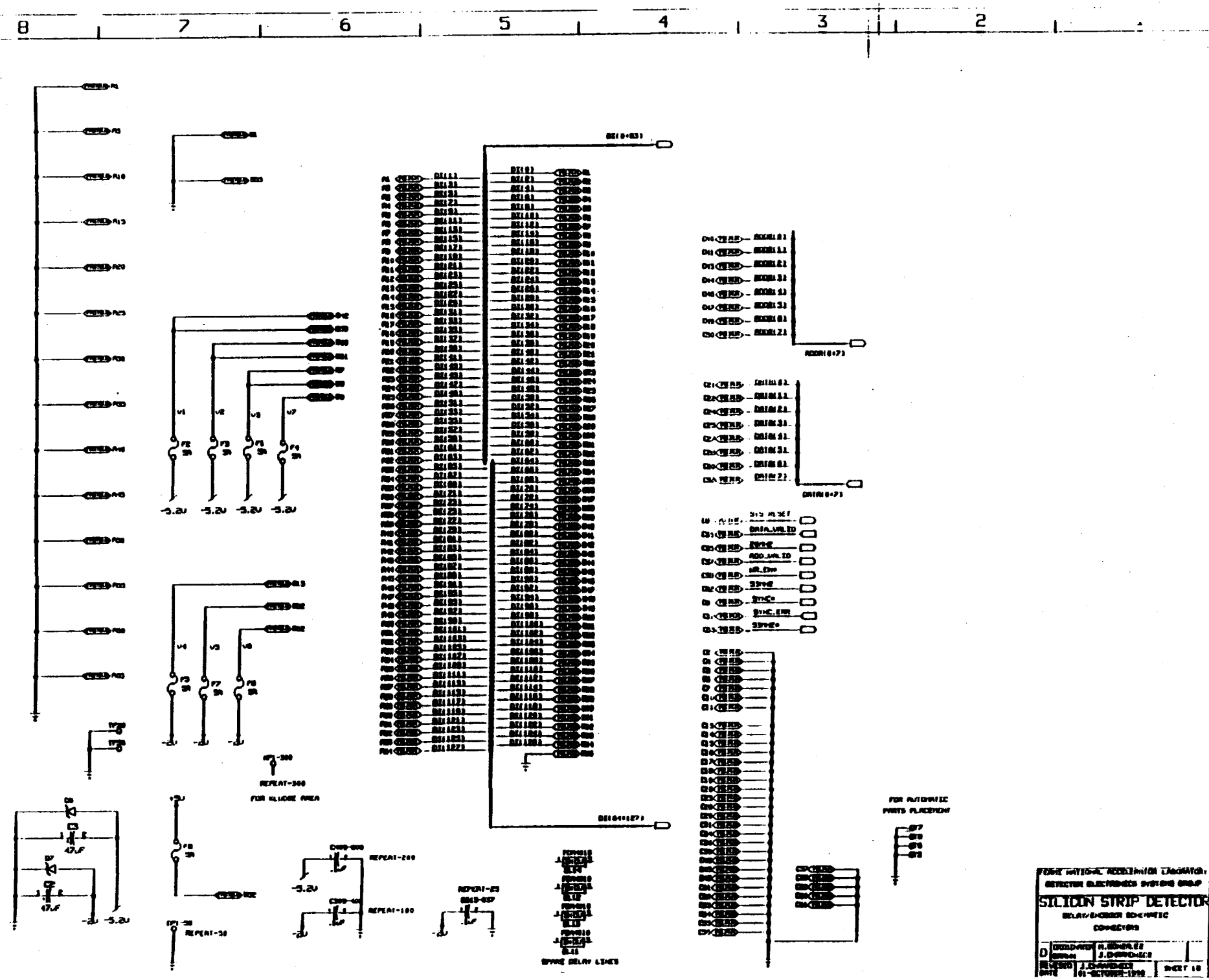


TERMINATIONS FOR BANK 3 ... (SHEET 17)

FERMI NATIONAL ACCELERATOR LABORATORY
DETECTOR ELECTRONICS SYSTEMS GROUP

SILICON STRIP DETECTO...
DELAY/ENCODER SCHEMATIC
TERMINATIONS FOR BANK 2 MULTIPLEXER

D


8
7
6
5
4
3
2
D
C
B
A
-5.2V
REPEAT-300
FOR GLIDE AREA
REPEAT-200
REPEAT-100
REPEAT-30
FOR AUTOMATIC
PARTS PLACEMENT
SILICON STRIP DETECTOR
DELAY/ENCODER SCHEMATIC
CONNECTORS
SHEET 10