Simulations and electronics development for the LHAASO experiment

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Simulations et développement d'électronique pour l'expériment LHAASO

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„Zwei Dinge erfüllen das Gemüt mit immer neuer und zunehmender Bewunderung und Ehrfurcht, je öfter und anhaltender sich das Nachdenken damit beschäftigt: Der bestirnte Himmel über mir, und das moralische Gesetz in mir.“

— Immanuel Kant,„Kritik der praktischen Vernunft“, 1788

"Two things fill the mind with ever new and increasing admiration and awe, the oftener and more steadily we reflect on them: the starry heavens above me and the moral law within me."

— Immanuel Kant, “Critique of Practical Reason”, 1788

“这世上有两样东西，对其日久弥坚的思考，总会在我的心灵深处唤起无尽的赞叹与敬畏：一是顶上浩瀚无垠的星空，二是根居内心的道德法则。”

— 伊曼努尔·康德，《实践理性批判》，1788

Abstract

This thesis is focused on the study of the front-end electronics for one of the large high altitude air shower observatory (LHAASO) detectors, which is the wide field of view Cherenkov telescope array (WFCTA). It covers six main topics from the physical simulation to the implementation of the data acquisition system.

First, the principles of cosmic rays and the situation of the LHAASO experiment were reviewed and presented as the foundation of our discussion. Then, physics simulations were made to understand the propagation of cosmic rays in the atmosphere and to figure out the characteristics of the input signal of the electronics. These simulations were also used to deepen the understanding of the specifications of the telescope and to cross-check them.

Next, a new PMT model was successfully built to be used for both physical and electronic simulations. This new model and another four different PMT models were compared and discussed in details to reveal their advantages and disadvantages. By using this PMT model, the behavior models for the designs based on the classical electronics and application-specific integrated circuit (ASIC) were built and studied. Both solutions fit the requirements of the telescope, but considering the development of the micro-electronics, the electronics of the future and high-performance telescopes should be based on the ASICs.

After that, the selected ASIC, which is PARISROC 2, was evaluated by using the existing application boards. The results showed that those designs cannot fully demonstrate the true performance of the chip. Therefore, a prototype LHAASO-oriented front-end electronic board that is based on ASIC was designed, implemented and fabricated. Several modifications and enhancements were made to improve the performance of the new design. A detailed description of the development is presented in the thesis.

Finally, a series of tests have been performed to verify the concept of the design and to evaluate the application board. The preliminary results show the good general performance of the ASIC and that this design nearly meets the specifications of the WFCTA.

Acknowledgements

It is a long and tough journey to pass the defense and get a Ph.D diploma and has no shortcut. No one could achieve success without guidances and help from others. However, no matter how long and how difficult the journey is, I come close to the end of it now. At this point, I would like to express my gratitude to all of the people who supported me and helped me during the writing of the thesis.

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Besides, my appreciation goes to all my friends. It is you who make my life so exciting and fascinating. Ernest Hemingway once said that *"If you are lucky enough to have lived in Paris as a young man, then wherever you go for the rest of your life it stays with you, for Paris is a moveable feast."*. They might be the best years of my life. I will remember the days always.

Finally, above all, my deepest gratitude goes to my beloved family and my girlfriend. You are always standing behind me and supporting all my decisions without a word of complaint. Thank you and thank you for all.

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Chapter 1

Introduction

Humanity continuously sought the meaning and the purpose of the life for thousands of years, but still without an exact answer. For the ancient Greek philosophers, Socrates and Plato, it was *"Know thyself"* [Plato, 1892], which was inscribed in the pronaos of the Temple of Apollo at Delphi. For the French post-impressionist, Paul Gauguin, it was the answer of ≪*D'où Venons Nous ? Que Sommes Nous ? Où Allons Nous ?*≫ [Gauguin, 1898], which was written at the upper left corner of the Gauguin's most famous painting that shares the same name. These questions are considered as the more popular version of the Plato's philosophical principle. For our Chinese philosophers, the journey is a progress of pursuing *"Tao"* [Laozi, 2004]. An ancient Chinese philosopher, Lao Tzu once said, *"Man models himself after Earth. Earth models itself after Heaven. Heaven models itself after Tao. And Tao models itself after Nature."* [Lao-Tzu, 1996]. Based on this theory of the *Taoism*, the mortals could achieve self-knowledge by means of exploring the nature. Conversely, if we could reflect ourselves, we are able to master the natural laws.

Therefore, in order to explain and predict both ourselves and the universe, we acquired and systematized knowledge about the natural world based on facts learned through experiments and observation [Merriam-Webster, 2014]. This kind of knowledge or the body of knowledge can be called as "Science" or "Natural Philosophy" [Lindberg, 2007]. On one hand, from Aristole to Einstein, the history of science proves that the imagination of the human beings are unlimited. On the other hand, from the wheel to the Large Hadron Collider (LHC) [Evans and Bryant, 2008], it is also proved that the confinement of science is the instrument. Without the instruments, we have no way to escape from the "Cognitive prison" [Wilson, 1998].

As an example, due to the invention of the electroscope and the improvement of it, V. F. Hess discovered and started the research of cosmic ray about a century ago [Hess,

1912]. Since then, hundreds of experiments have been designed and built to study this issue and achieved great progresses. However, owing to the lack of the appropriate instruments and the limitations of different detection technologies, we are still puzzled on the origin of cosmic rays.

Nowadays, the Large High Altitude Air Shower Observatory (LHAASO) experiment, which is proposed by Chinese scientists, is planned. The aim of this project is to study the high-energy gamma rays and attempt to answer this mysterious question of the origin of cosmic rays, which is one of the most important issues in Astroparticle Physics.

For a physics experiment, to design and build the detectors is the most important part. Meanwhile, the electronic system plays special role in the modern detectors. Therefore, the purpose of this thesis is to study and design a suitable front-end electronic system for LHAASO project. Nevertheless, it is impossible to discuss the design of all the detectors in a single thesis. The main purpose of this thesis aims to the simulation and implementation of the front-end electronics system for the Wide Field of view Cherenkov/fluorescence Telescope Array (WFCTA) [Zhang et al., 2011]. It provides a full solution of the design that covers from the physical simulation to the design of the DAQ system. The whole thesis can be divide into six parts. Each of them focuses on a corresponding aspect of the design and is listed as following:

Chapter 2 provides a brief overview of the principles of cosmic rays including the history, the extensive air showers and the corresponding detection techniques. In the following chapter, Chapter 3 describes the scientific goals and the detectors R&D of the LHAASO experiment. These chapters establish the fundaments of our discussion.

In Chapter 4, the characteristics of the input signals of the telescope are studied through the simulation. In addition, a new photomultiplier model is presented to bridge the cosmic-ray simulation and electronic simulation design. The ideal behavior models of the front-end electronics based on classical and Application-Specific Integrated Circuit (ASIC) solutions are built and simulated in order to figure out a better solution for WFCTA telescope in Chapter 5. The design and the implementation of a PARISROC 2-based electronic system is presented in Chapter 6. Chapter 7 discusses the realization of a new user-defined prototype DAQ system for the front-end board. At last, the performance and the test results of the board are shown in Chapter 8.

Chapter 2

Principle of cosmic rays

2.1 The brief history of cosmic rays

The history of cosmic rays is a step-by-step progress that can be traced back to the end of the nineteenth century. In 1879, W. Crookes and his invention "Crookes tube" first opened us a window to study the conductivity of gases and radiations. With this powerful tool, in 1895, W. C. Röntgen accidentally discovered the X-rays. The picture of his wife's hand skeleton world-widely spreaded in few weeks and started a revolution in the medical diagnostics. After followed Röntgen, by studying the fluorescent materials such as uranium and radium, H. Becquerel and his student M. Curie discovered and defined the term "natural radioactivity". Almost at the same time, J. J. Thomson made a great experiment in modern science and successfully identified that the cathode rays were actually electrons in 1897, which was the first discovery of the sub-atomic particles in science history. Then, E. Rutherford and other scientists showed that the radiation consisted of three types of components, which are α-, β- and γ-radiations or rays. However, it took them more than ten years to identify which particles the radiations they were related to. From there on, the physical pedestal of cosmic rays was settled.

In the investigation of the ionization, it was found around 1900, by C. T. R. Wilson, that the gold-leaf electroscope kept discharging even if it was well isolated from natural radioactivity sources [Wilson, 1900]. It suggested that there were small quantities of radioactive substances embedded in the equipments or in the environment. Three years later, Rutherford and his colleagues did similar experiments to locate the origin of the penetrating radiation and to measure the relationship between the ionization and the absorber distance with a shielded electroscope [Rutherford and Cooke, 1903]. This concluded that the most

of the ionization was due to the natural radioactive substances existing everywhere in the crust of the Earth.

Therefore, if the ionization was coming from radiations from the surface of the Earth, it should be attenuated with the distance. Two years later, a German physicist and Jesuit priest, T. Wulf, started the investigation of the electricity of the atmosphere and radioactivity around 1905. He firstly invented and developed a new type of electroscope by replacing the golden leafs with two metal filaments which were fixed to a quartz string [Wulf, 1909]. Figure 2.1 shows the cross section of the Wulf's design and the picture of the real instrument, which was fabricated by a German company, Günther & Tegetmeyer [Fricke and Schlegel, 2012]. It was the same instrument that was used by V. F. Hess in his successful balloon experiments.

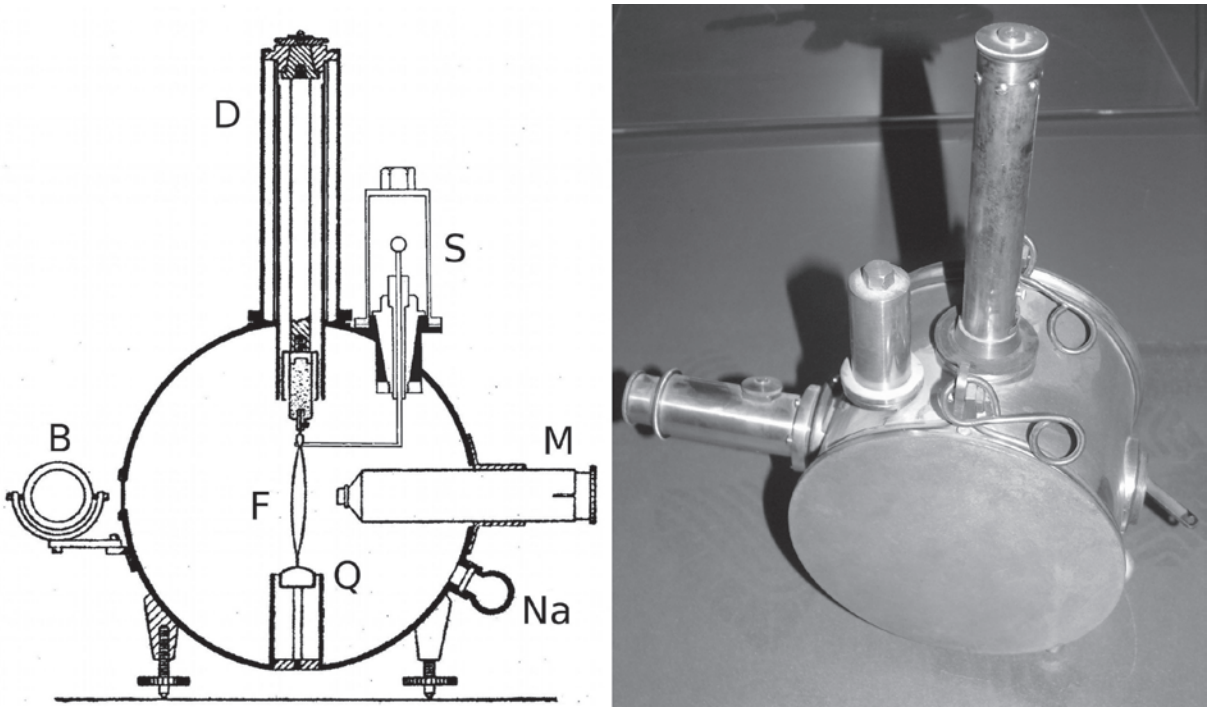


Figure 2.1: Left: the cross section of the Wulf's γ-ray electroscope. The lower end of the metal filament (F) was fixed to a quartz string (Q). The other end was attached to a rod extending outwards (D). The position of the filaments can be observed from a microscope (M). The charge was supplied via a movable electrode (S) that connected to the upper end of the filaments. The opening (Na) could be used to connect to a sodium-drying device. The filaments were illuminated with an attached movable mirror or lamp (B). Right: the real instrument fabricated by G&T, which the diameter is 17 cm and the width is 13 cm. The pictures are taken from [Fricke and Schlegel, 2012].

With this instrument, from 1908, Wulf begun his studies on the penetrating radiation in different environments and concluded that this sort of radiation should come from the upper Earth's layer [Walter, 2012]. In 1910, he performed several measurements on the

top of the Eiffel Tower (330 m) and realized that the ionization was not decreased as he expected at the top of the tower[Wulf, 1910]. It suggested that the radiation might come from the outside.

Figure 2.2: The picture of V. F. Hess and his balloon flight

The big breakthrough in the discovery of cosmic rays was in 1912 when V. F. Hess launched seven balloon flights to investigate the ionization rate at very high altitudes. Figure 2.2 shows a photograph of Hess after one of his famous balloon flights. As T. Wulf, Hess also further improved and calibrated the Wulf-type of electroscope. By the end of 1912, with three electroscopes, two were supposed to detect γ-radiation and the other one was supposed to measure β-radiation, he reached the maximum height of 5,350 m and recorded the ionization rate at different levels [Hess, 1912]. Figure 2.3 is a copy from Hess' original publication that shows the radiation decrease from ground to 1,000 m and then increase at the higher altitudes. This was the first definite evidence that showed that the source of the ionization or the "*Höhenstrahlung*" was from the upper atmosphere but not from the Earth.

During that time, this concept was not fully accepted by the scientific community until W. Kolhörster moved to a further step. From 1913 to 1914, he launched his own balloon flights to repeat the same measurements as Hess's did but at higher altitudes (9,300 m) with

Physik. Zeitschr. XIII, 1912. Hess, Durchdringende Strahlung bei sieben Freiballonfahrten. 1089

Tabelle der Mittelwerte.

Mittlere Höhe über dem Erdboden m	Beobachtete Strahlung in Ionen pro ccm und sec.			
	Apparat 1	Apparat 2	Apparat 3	
	Q_1	Q_2	Q_3 (reduziert)	Q_3 (nicht reduziert)
0	16,3 (18)	11,8 (20)	19,6 (9)	19,7 (9)
bis 200	15,4 (13)	11,1 (12)	19,1 (8)	18,5 (8)
200—500	15,5 (6)	10,4 (6)	18,8 (5)	17,7 (5)
500—1000	15,6 (3)	10,3 (4)	20,8 (2)	18,5 (2)
1000—2000	15,9 (7)	12,1 (8)	22,2 (4)	18,7 (4)
2000—3000	17,3 (1)	13,3 (1)	31,2 (1)	22,5 (1)
3000—4000	19,8 (1)	16,5 (1)	35,2 (1)	21,8 (1)
4000—5200	34,4 (2)	27,2 (2)	—	—

Figure 2.3: The table is taken from Hess' paper that shows the averaged ionization rate at different altitudes. The apparat 1 and 2 are supposed to the results of the γ-radiation. The apparat 3 is related to β-radiation.

a more stable and accurate detector, which was improved by himself and G&T company. These results confirmed Hess' conclusions and "undoubtedly" demonstrated that the source of the radiation was cosmic origin [Kolhörster, 1913, 1914].

In 1926, a debatable American scientist, R. A. Millikan and his colleagues reclaimed that they discovered that the source of the penetrating radiation was partially of cosmic origin by measuring the ionization at an extremely high altitude, which was up to 15,500 m. He also named this sort of radiation as "*cosmic rays*" or "*cosmic radiation*" that are widely used today [Milikan and Cameron, 1926].

After that, scientists struggled years to eliminate the interference of the background of the γ-radiation caused by the small amount of radioactive substances in the detector itself. It was not until 1929 that the invention of the "Geiger–Müller counter", finally freed them from this trap [Geiger and Müller, 1928]. The ability of the precise-time measurement of this instrument guaranteed that it can be used to measure the coincident events and isolated cosmic rays from the radioactive background. In the same year, W. Bothe and Kolhörster built a detector with two Geiger–Müller tubes one above the other and successfully demonstrated this concept [Bothe and Kolhörster, 1929]. This technique is now the most common technique in every particle-physics experiment.

The discovery of air showers is another big progress in the history of cosmic rays. In 1934, based on the experimental results with coincidences from high altitude to sea level, B. Rossi revealed the existence of the extensive groups of particles [Rossi, 1964]. Then, in 1938, it was P. V. Auger and his collaborators who systematically studied this phenomena.

With a high-resolution coincidence circuit (resolution: 5 μs) designed by R. Maze [Maze, 1938], Auger's group deployed detectors in the Swiss Alps. They noticed that two detectors separated by some distances, which was up to 300 m, would be triggered at the same time. They concluded that the showers or the "extensive air showers" were secondary particles that were due to the cascading reactions of the high-energy primary particles in the atmosphere. They estimated that a shower consisted of millions of secondary particles and the primary energy would reach 10^{15} eV [Auger et al., 1939].

Until 1950s, before the accelerators became practical and reached a reasonable energy level, investigating and measuring cosmic rays played a key role in particle physics. Important discoveries such as the discoveries of the Positron [Anderson, 1933], the Muon [Neddermeyer and Anderson, 1938], the Pion [Perkins, 1947] and so on were all related to the observation of cosmic rays. Even the accelerators continually evolved and achieved great success, studying and observing cosmic rays were still important for scientists. As an example, from the very beginning, the origin of cosmic rays is still a mystery for us after a century of pursuiting.

However, no matter how hard we have tried, it is impossible to cover all the aspects of the history of cosmic rays in a single section, we have to abbreviate it and skip many great discoveries. Reviewing the history of cosmic rays, one would finally recognize that every progress achieved in this field is following the development of the instrument. To build up a proper detector is alway the first and most important step of all experiments. Consequently, the principle of cosmic rays and the basic detection techniques of cosmic rays will be simply introduced and discussed in the following chapters.

2.2 The principle of cosmic rays

Since the primary cosmic rays are groups of high-energy particles emanated from the extraterrestrial sources, the researches on cosmic rays are usually focused on three interrelated aspects, which are the energy spectrum, the composition and the arrival direction. Basically, all of them reflect the properties of the origin of cosmic rays and how the cosmic rays propagate through the universe.

Among them, the most noticeable feature of cosmic rays is that their spectra cover a large range of energies, about 12 decades, from 10^9 eV to 10^{20} eV, and roughly follow a

power-law energy distribution with slight deviations at some special points. Conventionally, it can be written as:

$$N(E)dE \propto KE^{-\gamma}dE \text{ [particles m}^{-2}\text{s}^{-1}\text{sr}^{-1}\text{]} \tag{2.1}$$

where E is the particle's kinetic energy per nucleon in GeV. The exponent γ represents the spectral index of the flux and varies between 2.5 and 2.7 [Longair, 1992]. Figure 2.4 shows the "all-particle" differential energy spectrum as a function of energy. The flux is multiplied by $E^{2.6}$ to display the subtle changes in the slope [Olive et al., 2014]. This method was introduced by A. A. Watson in the 19th ICRC, in order to renormalize the distributions, which span many orders of magnitude [Watson, 1985].

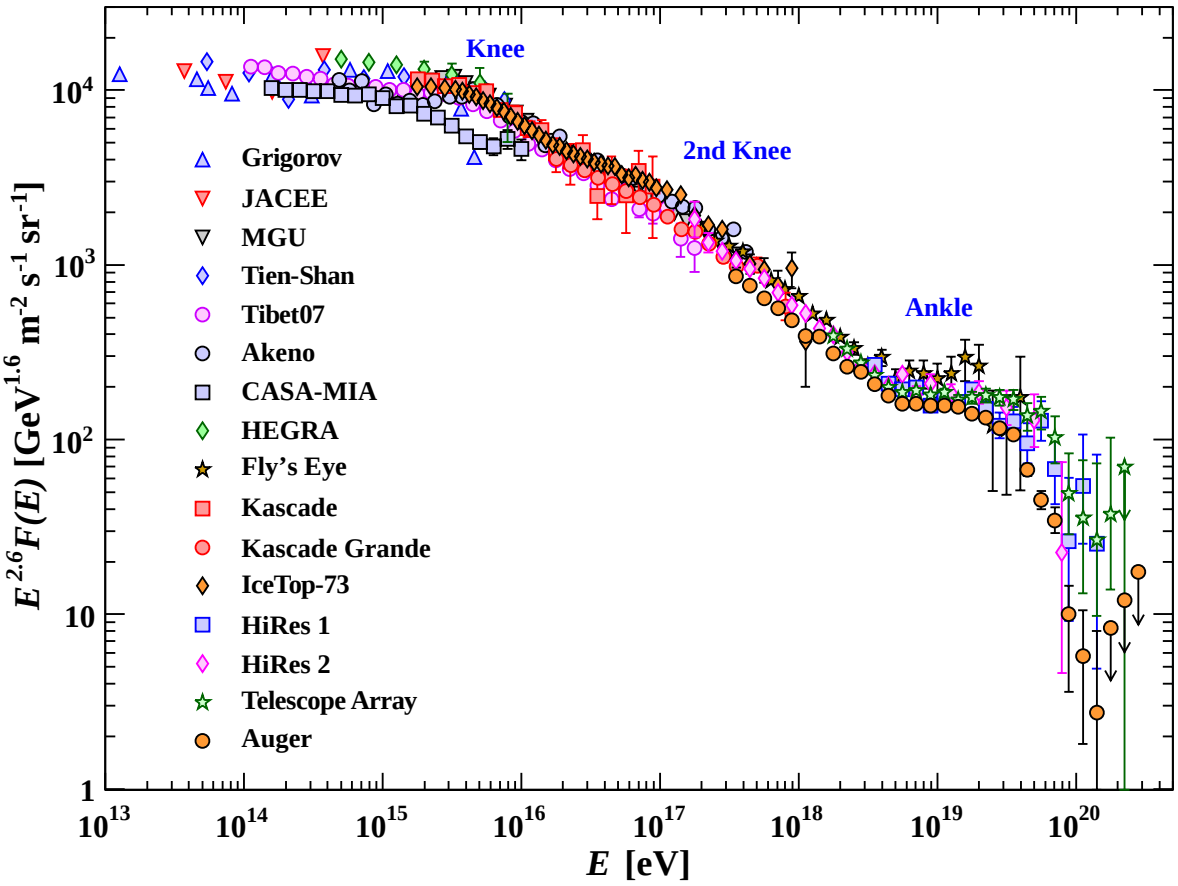


Figure 2.4: The all-particle energy spectra of cosmic rays as a function of E (energy per nucleus), which taken from [Olive et al., 2014]

The figure only presents the experimental results higher than 10^{14} eV which is the limit of the balloon/satellite type of direct measurements and the ground indirect measurements. Inspecting the figure, one can easily find out that there are three significant turns in the

curves. The first one happens somewhere in a range from 10^{15} eV to 10^{16} eV and is called as *"knee"*. At this point, the spectral index increases to around 3.1. The next one around 10^{17} eV is known as *"2nd knee"*. At this point, the index further increases to 3.3. Finally, at the *"ankle"*, which is around 10^{19} eV, the spectral index will come back to 2.7.

The flux of the cosmic rays is inversely proportional to the energies of the particles. According to [Olive et al., 2014], the flux is $\sim 1.8 \times 10^4$ $(E/1 \text{ GeV})^{-2.7}$ [particles m^{-2} s^{-1} sr^{-1}] from several GeV to 100 TeV, which means that a detector may capture 1 particle per square meter per second of cosmic rays with an energy about 37 GeV. Around the knee, it drops to 1 m^{-2} sr^{-1} year^{-1}. For those particles with energies higher than 10^{20} eV, the arrival rate is about 1 km^{-2} sr^{-1} century^{-1} [Longair, 1992]. The bends in cosmic-ray spectra may be due to its acceleration mechanisms and the ways of propagation. There are several theories can be used to explain these phenomena, such as the Fermi Mechanism for cosmic ray acceleration up to 10^{14} eV [Fermi, 1949], the UHE Mechanism for those at around 10^{18} eV [Sokolsky et al., 1992] and the GZK cut-off above 6×10^{19} eV [Greisen, 1966; Zatsepin and Kuz'min, 1966], which will not be discussed in this thesis.

The composition of cosmic rays at lower energy less than 10^{14} eV is carefully measured by direct measurements in space. Considering all cosmic-ray particles, there are about 98 % protons and 2 % electrons. Considering only protons and nuclei, for all energy scale, it is composed of about 87 % protons, 12 % helium and 1 % heavier nuclei as iron and so on. These ratios of primary nuclei are usually constant over all energy range, but change a little at the highest energies that is due to the acceleration mechanism and propagation of cosmic rays. For example, around the knee region, the composition is about 50 % protons, 25 % helium, 13 % CNO (Carbon-Nitrogen-Oxygen) and 13 % iron [Longair, 1992]. The accurate measurement of the fractions of nuclei at different energies is an important issue in the study of cosmic rays which would help to identify the origin of them.

Another topic about cosmic rays is isotropy or anisotropy in their arrival direction. Because the most compounds of cosmic rays are charged particles, the trajectories of them are easily disturbed by the terrestrial and the interstellar magnetic fields. Therefore, the directional information of cosmic rays may get lost before reaching the Earth. Based on the observation results, the particles with energies lower than 10^{14} eV distribute totally isotropically on the sky. Only the ultra high energy cosmic rays ($> 10^{18}$ eV) show an evidence of anisotropy [Hillas, 1984]. Therefore, if one wants to trace back to the origin of cosmic rays, the ultra high energy cosmic rays and the uncharged particles as neutrinos and photons are best probes. In 2007, the Auger collaboration reported that they observed

a correlation between the arrival direction of the high-energy cosmic rays ($\sim 6 \times 10^{19}$ eV) and the position of the nearby active galactic nuclei (AGN) [Pierre Auger Collaboration, 2007]. It might be a step towards the final answer of this open question.

2.3 Extensive air showers

When the energetic primary cosmic rays finally reach the Earth and hit the upper top of the atmosphere, collisions take place between the cosmic rays and the electrons, nuclei and molecules in the air, leading to the energy losses of the primary particles. If the particles are energetic enough, as a few GeV, the result of this strong interaction creates mesons and different types of secondary particles. The continued propagation of these primaries and the secondary particles in the atmosphere usually triggers the hadronic or electromagnetic cascades and produces more and more particles along their trajectories until the energy of particle drops below the critical energy E_c. Meanwhile, the unstable particles as pions and kaons easily decay into other particles as muons, neutrinos, gamma rays and electron-positron pairs. Therefore, a very high-energy primary particle creates countless secondaries along its path through the atmosphere to the ground and spreads out laterally from its incident axis due to the scattering processes. This cascade is well-known as Extensive Air Showers (EAS) and was discovered by P. Auger [Auger et al., 1939].

As a result of the different interaction processes, the components of cosmic rays in the atmosphere can be divided into three major groups: the hadronic component which is close to the shower core, the photon-electron component, which is caused by the electromagnetic cascade process and starts from the decay of neutral pions, and the muon component resulting from the charged pions or kaons decay [Grieder, 2001]. There is also a neutrino component which is originating from the decay of the charged pions and muons. 90 % of the primary energy is lost in the electromagnetic processes. Figure 2.5 gives an example of the development of an extensive air shower.

Traveling through the atmosphere, the number of secondaries in the air shower increases with the depth of atmosphere and reaches a maximum point, and then decrease due to energy loss, absorption and decay. This point is so-called “shower maximum” and the location of it is the “depth of maximum development” or X_{max}, which is measured from the top of the atmosphere. It can be also measured from the sea level, as the “height of maximum development”. This shower maximum depends on the energy and nature of the primary particle and the density of the atmosphere.

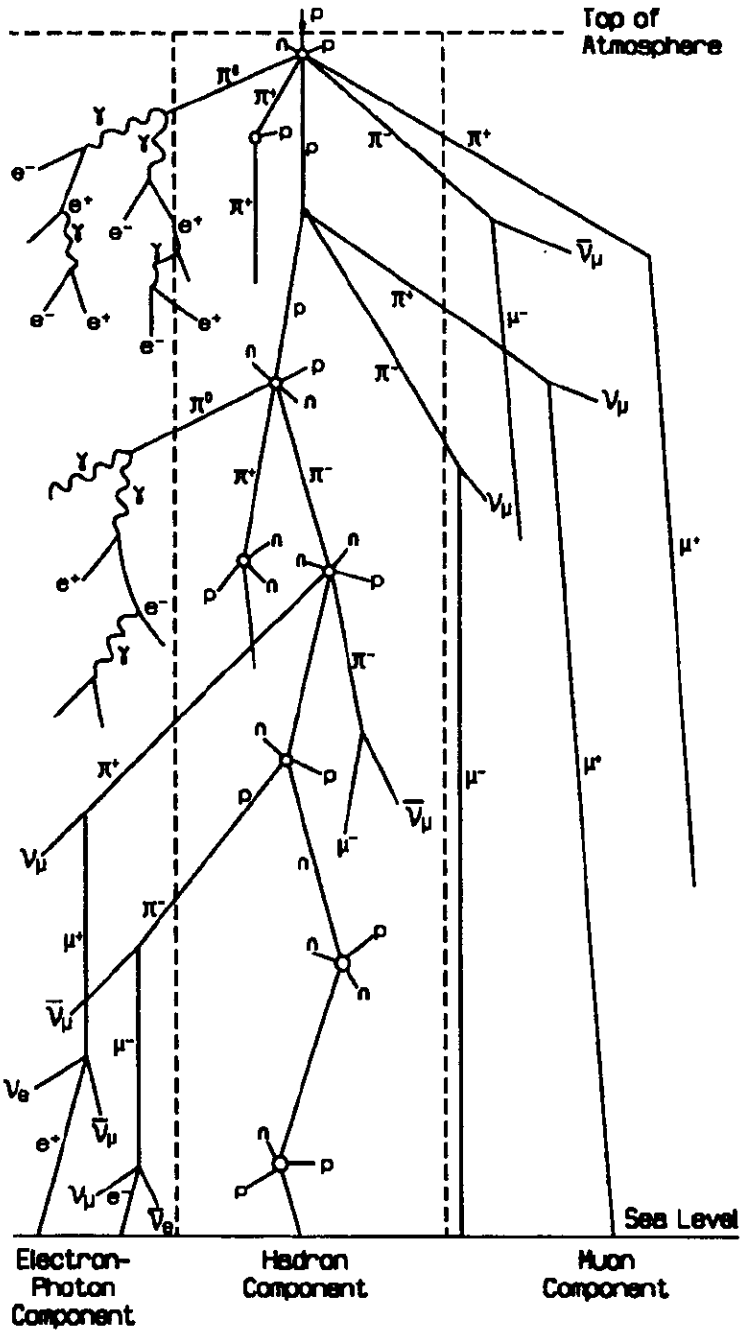


Figure 2.5: The schematic of the shower development: An energetic proton colliding the nucleus or molecule in the atmosphere initiates the cascade shower. The hadronic cascade, which is the core of the shower, continues producing secondaries until the energy drops below a specific value. The neutral pions decay into electrons, positrons and gamma rays in the electromagnetic process which is the biggest component in an air shower. The charge pions decay into muons or neutrinos. Even the muons produce electrons and neutrinos through decay. All these components construct a shower. This figure is taken from [Grieder, 2001]

The shower particles finally form a slightly curved disk-type of shower front with a thickness of $1 \sim 3$ m close to the axis and could extend to several hundred meters. However, with the increasing of the distance from the axis, due to increased scattering at lower energies and lower Lorentz factors of the parent particles, the shower shows a loose profile, which is presented in figure 2.6 (left) [Grieder, 2010]. Consequently, at the fringe of the shower disk, the arrival time could expand to more than one microsecond. The general time profile of the shower is also shown in figure 2.6 (right).

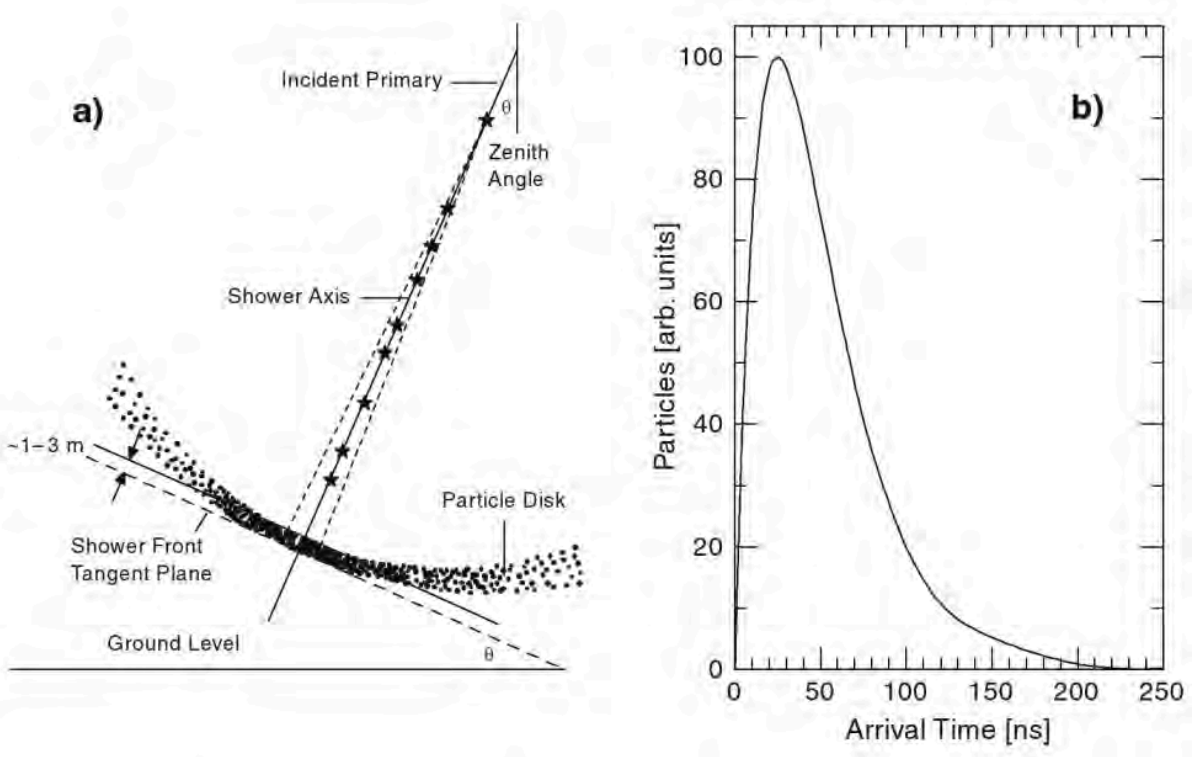


Figure 2.6: The shape and the time profile of a shower. Left: it shows a disk-type of shower front with a specific incident zenith angle before it impact the ground. Right: the approximate time profile of the shower, including all particle. These figures are taken from [Grieder, 2010].

As shown in the figure, the shower extends in two directions: longitudinal and lateral. The longitudinal development of a shower can be parameterized with the Gaisser-Hillas function [Gaisser and Hillas, 1977]:

$$N(X) = N_{max}(\frac{X - X_0}{X_{max} - X_0})^{\frac{X_{max}-X_0}{\lambda}} exp(\frac{X_{max} - X}{\lambda}) \tag{2.2}$$

Where $N(X)$ is the number of the particles at the depth of X, X_{max} is the depth of shower maximum as described in previous paragraph, X_0 is the depth of the first interaction point, which could be less than 0, λ is about 70 g/cm^{-2}.

The lateral development usually can be described with Nishimura-Kamata-Gresien (NKG) equation [Kamata and Nishimura, 1958; Greisen, 1960]:

$$\rho(r,N) = \frac{N}{r_M^2}\frac{\Gamma(4.5-s)}{2\pi\Gamma(s)\Gamma(4.5-2s)}(\frac{r}{r_M})^{s-2}(1+\frac{r}{r_M})^{s-4.5} \tag{2.3}$$

Where $\rho(r,N)$ is the particle density at the distance r from the axis, N is the total number of the shower secondaries, r_M is the Molière unit and s is the shower age.

In addition, if the energetic secondaries travel faster than the speed of light in the medium, air in this case, they will produce Cherenkov radiations. Furthermore, excited by the electromagnetic process, the nitrogen molecules in the air emit ultraviolet photons, which is called fluorescence or scintillation light. Theses two co-products are very important in the study of EAS, and will be discussed in Chapter 4.

2.4 Cosmic-ray detection techniques

As we mentioned above, the purpose of the study of cosmic rays is to determine the energies of the primaries, to identify the compositions and to record their arrival directions. One can identify two categories of experiments in this field: the balloon/satellite based direct detection and the ground based indirect detection. Both experiments have their advantages and can be the complementary to each other. Generally speaking, it is accurate that to identify and measure the primaries directly with the balloon flights or the satellites. However, limited by the payload of the carrier, the effective area of the detector and the flux of the primaries in the high-energy region, it is difficult to measure the particles with energies higher than 10^{14} eV. Those particle with energies higher than this value are usually measure on the ground with air showers.

In principle, independently, if the particles are charged or not, they can be detected through the interaction process of the particle with the matter or through the energy loss in the matter. Based on this, there are three typical techniques that are used in the modern particle detection: detection based on ionization in gases, detection based on electron-hole pair creation in semiconductors and detection based on scintillation or excitation in mate-

rials [Tavernier, 2010]. They are similar to the detection techniques, which are exploited in the accelerators.

2.4.1 Balloon/satellite based direct detection

In the very beginning, a balloon flight was the only way for scientists to reach the upper atmosphere and measure the cosmic rays directly until the satellite experiment was possible in 1957 (i.e., the launch of the Sputnik 1 by Soviet Union). In the first decades of 20th century, most detectors were combinations of the Wulf-type of electroscopes and cloud chambers. After that, the Geiger–Müller counters and the emulsion chambers gradually replaced the electroscopes and cloud chambers became the most widely used spectrometers and calorimeters in the cosmic-ray experiments. Because of their remarkable characteristics, some of them were still adopted in the modern cosmic-ray experiments. As an example, chambers based on the interleaved emulsion plates were used in the modern balloon experiments (e.g., JACEE [Asakimori et al., 1998] and RUNJOB [Derbina et al., 2005]) to study the chemical compositions of cosmic rays near the *knee* in the 1990s.

Figure 2.7 presents some basic structures of the recent balloon/satellite cosmic ray detectors. As shown in the figure, for the new generation detectors, most of them are combinations of multiple detection techniques. They can be roughly divided into four groups: tracking detectors, magnetic spectrometers, calorimeters and particle identification detectors such as time of flight detectors (TOF), Cherenkov detectors (CD) and transition radiation detectors (TRD). The detailed information can be find in the review [Baldini, 2014].

Tracking detectors

The purpose of the tracking detector is to record the paths or positions of the charged particles when they propagate through the medium (e.g., gases or solid states). It is usually a stack of interleaved position-sensitive plates as the emulsions which was mentioned above. Even though there are plenty of ways to build up a tracking detector in modern high-energy experiments, the fundamental of these detectors is that the drift of the ionization products which is induced by the electric field can be read out with the special patterns of electrodes, such as wire, strip and dot. Except the position information, usually in multiple dimensions, the sign and the amount of the charge can be also derived from the results. Compared with the gaseous detectors, the silicon detectors are preferable in the long-term space experiments. This is owing to its low average energy of creating electron-hole pairs

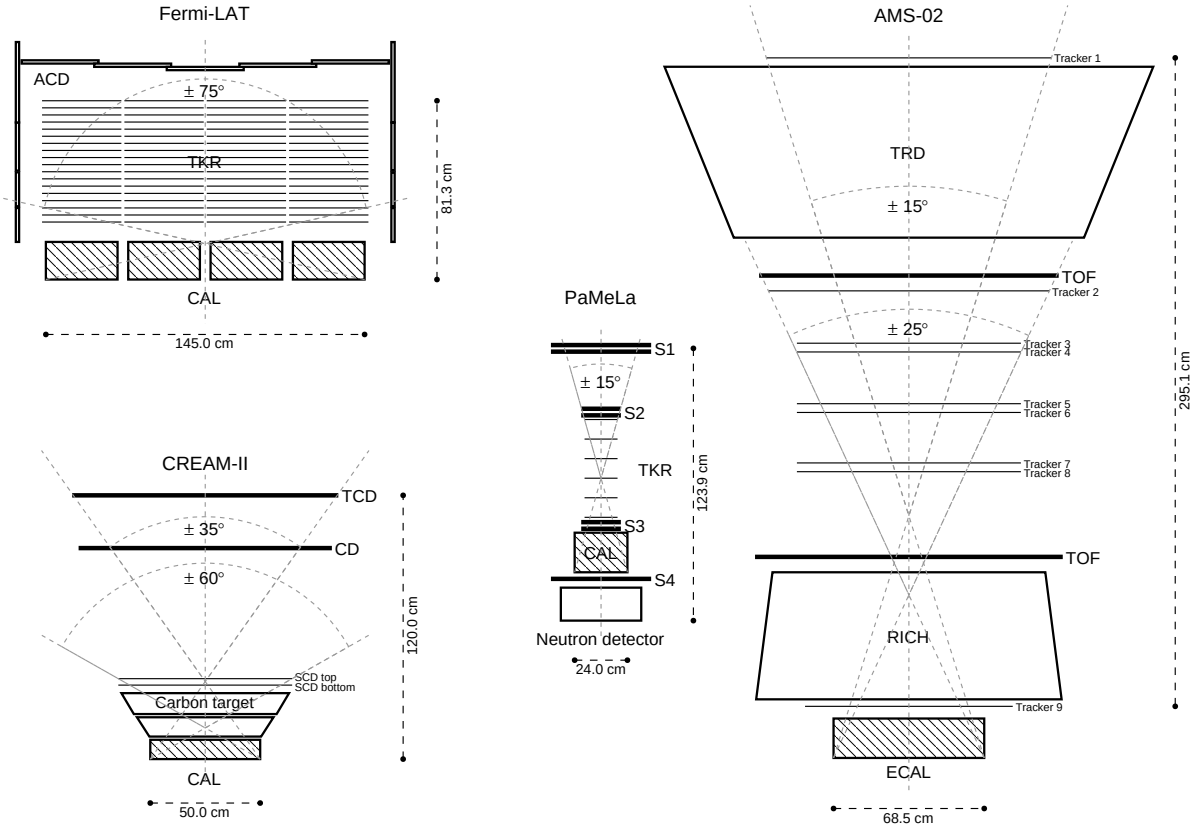


Figure 2.7: The brief diagrams of the recent balloon/satellite cosmic-ray detectors. Only the sketches of the detectors are presented here. For the Fermi-LAT, it consists of the anti-coincidence detector (ACD), the tracker (TKR) and the calorimeter (CAL). For the CREAM-II, it consists of the timing charge detector (TCD), the Cherenkov detector (CD), the silicon charge detector (SCD) and the calorimeter (CAL). For the PaMeLa, it is composed of the time of fight scintillators (S1–S3), the tracker (TKR), the calorimeter (CAL) and the neutron detector. For the AMS-02, it is made up of the transition radiation detector (TRD), the time of fight (TOF), the tracker layers, the electromagnetic calorimeter (ECAL) and the ring imaging Cherenkov detector (RICH). This figure is taken from [Baldini, 2014].

(a few eV) , the excellent intrinsic time response (several ns) and a large effective surface that can be easily fabricated (tens or hundreds of m^2).

Magnetic spectrometers

As for the magnetic spectrometers, they are designed to detect the momentum of the charged particle by measuring its deflection angle or the sagitta of the trajectory in the magnetic field. Therefore, placing the tracking detectors inside the magnets is a typical way of building magnetic spectrometers for space experiments. Because the magnet normally is a heavy passive component and limits the field of view of the instruments, this utilization must be carefully evaluated (e.g., superconducting magnet in AMS-02 [Aguilar et al., 2013] or permanent magnet in PAMELA [Picozza et al., 2007]).

Calorimeters

The calorimeter is another crucial part in a high-energy detection system. In fact, it is equivalent to an absorber where the particles partially or fully deposit their energy and convert them into measurable signals. It has triple advantages compared to the magnetic spectrometer. First, the energy resolution of the calorimeter improves as $1/\sqrt{E}$ at high energy, but that of the magnetic spectrometer decease with E. The second one is that shower depth in the calorimeter is nearly energy independent and only as a logarithmic function of E, which means the calorimeter design can be compact. In addition, these detectors are also sensitive to the neutral particles which cannot be detected in magnetic spectrometers (see figure 2.8).

According to the interactions, there are two basic calorimeters in modern high-energy experiments: electromagnetic calorimeters and hadronic calorimeters. As the name implies, the electromagnetic calorimeter aims to absorb the products of electromagnetic interactions. As a consequence, all of the particles lose their energy in this detector. Some of them as photons, electrons and positrons deposit all their energy in it except muons and neutrinos. Hadrons deposit most of their energy in the hadronic calorimeter and partly in electromagnetic one. Because of the mass of the high-density material in the hadronic detector, it is not a popular technique in space experiment.

Based on the internal structure of the detector, they can be classified into two categories: homogenous and sampling. The homogeneous calorimeter is a detector filled with high-density material which serves as an absorber and as a detection medium. The sampling

calorimeter consists of layers of passive absorber materials interleaved with active detector layers as scintillators or silicon detectors.

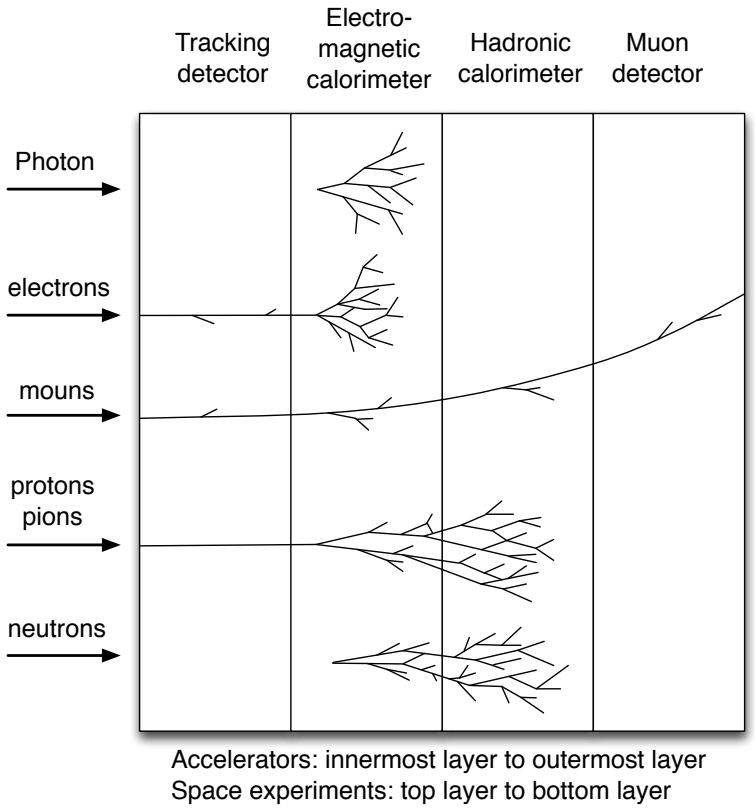


Figure 2.8: Diagram of the particle identification progress. For the accelerators, the tracks are from the innermost layer to the outermost layer. For the space detectors, they are from the top layer to the bottom layers [Lippmann, 2012].

Particle identification detectors

Since most particles simultaneously are absorbed in the calorimeters, it is difficult for these detectors to distinguish particles directly. Another type of particle identification detectors are necessary in this case. In order to identify stable particles, the charge and the mass of the particles must be determined. The sign and the amount of the charge of a particle are obtained from the path of the particle in the tracking system, but mass cannot be measured directly. Based on the Bethe-Bloch formula ($\beta\gamma = p/m$, $\beta = v/c$, here c is the speed of light in vacuum and γ is the relativistic Lorentz factor), the mass of the particle depends on the momentum and the velocity. Because the momentum can be obtained from the curvature of the path of the particle in the magnetic field (i.e., magnetic spectrometers), the velocity of the particle is the other variable which needs to be determined. There are

four methods to determine this variable: measuring the energy loss dE/dx, measuring the time of flight (TOF), detecting Cherenkov radiations or detecting transition radiations [Lippmann, 2012]. A diagram of the particle identification is shown in figure 2.8.

Table 2.1: The G_{eff} and T_{obs} of recent cosmic ray balloon/satellite detectors

Experiment	Eff. Geo. [m^2 sr]			T_{obs} [year]
	$e^{\pm}$	γ	*p/nuclei*	
Agile	–	0.1	–	> 7
AMS-02	–	0.05	–	20
ATIC	–	0.24	–	0.15
CREAM	–	–	0.43	0.5
Fermi LAT	2.8 @ 50 GeV	2.0 @ 10 GeV	–	10
PaMeLa	0.00215	–	0.00215	7
TRACER	–	–	4.73	0.05
CALET	–	0.12	–	5
DAMPE	0.3	0.2	0.2	3
HERD	> 3	> 3	> 2	10

Summary of the direct detection

In summary, using the similar techniques as the high-energy accelerators experiments, a correctly calibrated balloon/space detector offers an accurate way to measure primary cosmic rays directly above the atmosphere. Nevertheless, limited by the payload of the carrier (e.g., balloon or rocket), the bulk and the weight of these detectors are relative small values. This limits the effective geometric factor (G_{eff}) of the instrument, which mean that it is hard for the space detectors to measure the very high energy particles. Table 2.1 is a brief summary of the G_{eff} and the observation time (T_{obs}) of some recent space experiments [Baldini, 2014]. The typical number of the G_{eff} is unusually less than 1 m^2 sr (See table 2.1). Even the largest one, the TRACER experiment, this factor is only about 4.73 m^2 sr before the selection cuts. At the mean time, TRACER as a balloon experiment, the observing time of it was very short, only a couple of days. Therefore, even though the energy range of this detector could reach several hundred TeV, in fact, due to the short observing time, it cannot acquire enough high energy events for the statistical analysis. Besides, because the flux of the high energy primary decreases with the increasing energy, it aggravates this phenomena. For the high-energy particles (> 100 TeV), the direct detection based on the balloon/satellite experiments are difficult.

2.4.2 Ground based indirect detection

Since the secondaries in the air shower are similar as the ones produced in the space detector medium, the detectors on the ground could share almost the same detection techniques as the methods exploited in the space except that the atmosphere itself acts as the "gaseous chamber" of a calorimeter in this case. For a natural calorimeter, the accuracy of the measurements of the primary particles not only depends on the precise identification of the secondaries and monitoring of the development of the showers in the longitudinal and the lateral direction, but also relies on the models which are used to interpret the interactions in the atmosphere. The sophisticated effects of the atmosphere (e.g. absorption and scattering) and the complexity of the detection techniques adopted lead to large uncertainties in the ground experiments even in the same energy range which should be eliminated. The absolute calibration of the detector and the cross calibration among experiments are the key points of a successful cosmic-ray experiment.

Thus, in order to understand the complexity of the detectors, the ground based detection techniques are discussed in this section. According to the composition of the secondaries in showers, the detection techniques can be roughly divided into three categories: particle detectors, optical detectors and radio detectors. The schematic of these detectors are shown in figure 2.9.

Particle detectors

We learned previously that about 90 % of the energy of a primary particle is deposited by the electromagnetic processes and a large number of charged secondary particles such as electrons/positrons, photons and muons are created in the cascade. Hence, the particle detectors on the ground, which are also referred as the surface detectors or the ground arrays, are generally a group of arranged detectors separated with special distances. The detectors aim to distinguish the electromagnetic components in the air shower and measure the development of the shower on the lateral direction and record the arrival time of the shower front. With the lateral distribution and the arrival time, the incident directions and the energies of the primary cosmic events can be reconstructed.

The advantages of the ground array detectors are the large coverage area (Auger: $\sim 3000\text{km}^2$), the large field of view (full-sky), the long duty-cycle (> 90 %), and the lower cost compared to the telescope system with the same scale. However, the drawback of them is that they are only able to record the information of the shower front and hardly

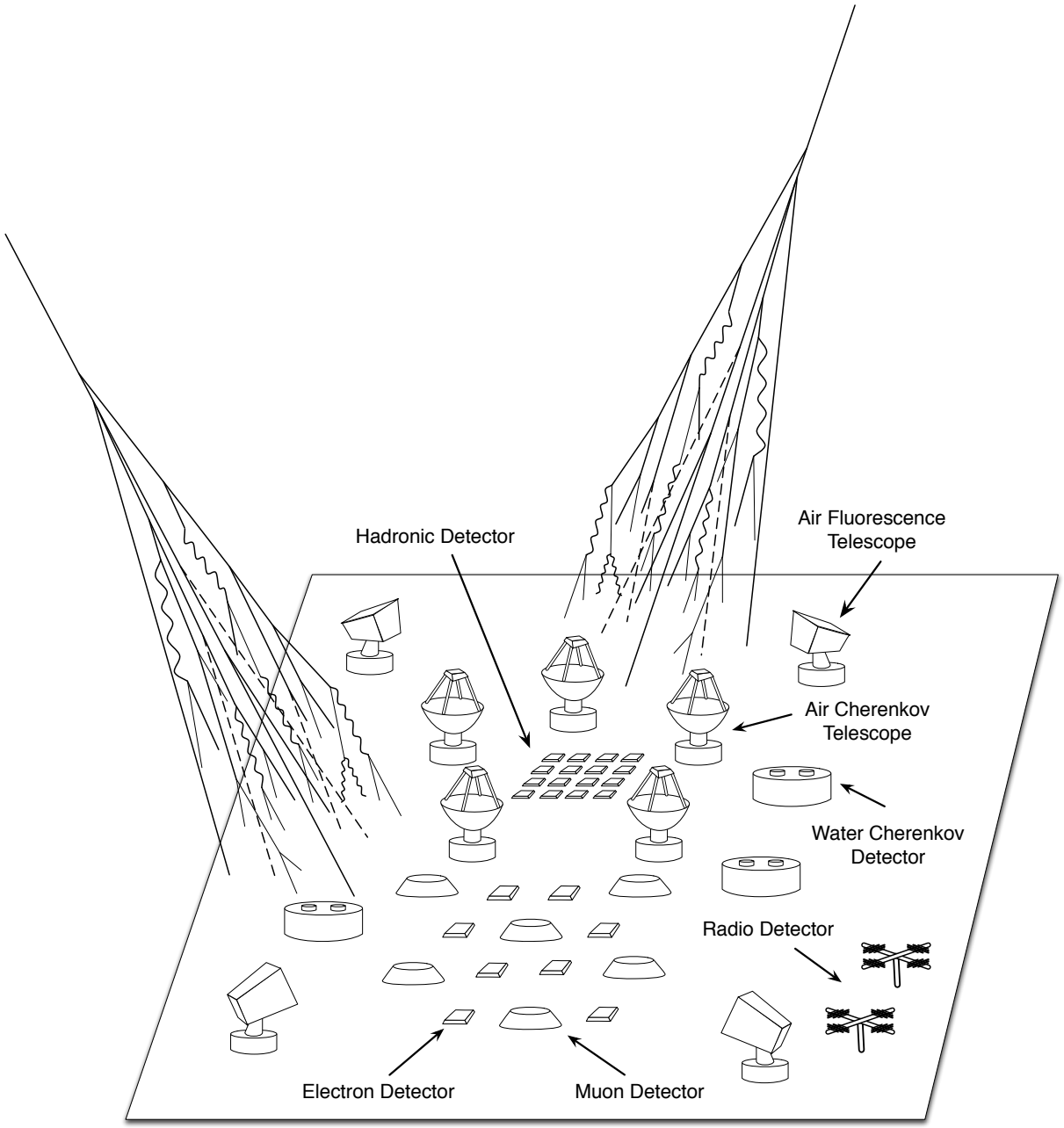


Figure 2.9: Schematic of the ground based detectors

distinguish the hadronic component and the muon component in a shower. This limits the capability of the ground detectors.

Therefore, in order to improve the accuracy of the reconstruction and to better discriminate the compositions of the primary cosmic rays, the muon component in a shower should be identified as well. As shown in figure 2.8, since muons barely produce the electromagnetic and hadronic showers, they can be easily distinguished by simply using a thick absorber to ensure all other charged particles dissipate their energies in the medium. As a result, the particles escaped from the absorber are muons. The typical medium can be lead, dirt or even water. It also can be done by using two scintillator detectors or RPC detectors with an absorber between them or by those specialized shielded muon detectors.

Based on the active materials used in the detector, the particle detector drops into three sub-detectors: scintillator detectors (e.g., AGASA [Takeda et al., 2003] and KASCADE-Grande [Apel et al., 2012]), ionization chamber detectors (e.g., RPC for ARGO-YBJ [Sciascio, 2014] and liquid for KASCADE-Grande) and water or ice Cherenkov detectors (e.g., Auger [Pierre Auger Collaboration, 2008], Milagro [Atkins et al., 2005] and IceCube [Abbasi et al., 2013]). Furthermore, the liquid ionization chambers of the KASCADE-Grande experiment can be used to detect the hadron components in the shower core.

Optical detectors

When the high-energy particles pass through the atmosphere, two types of radiations or lights are emitted: Cherenkov light and scintillation light or fluorescence light. The photon patterns can be collected by optical detectors on the ground and reflect the evolution of the air shower in the atmosphere. Basically, based on the infrastructures, there are two types of optical detectors in modern cosmic-ray measurements: the large aperture, wide-angle optical detector arrays and the narrow field of view (FOV), directional optical telescope systems. They can be also divided into the Cherenkov detectors and the fluorescence detectors based on their observing objects.

The wide-angle optical detector array, which is also known as Cherenkov counter array (e.g., TUNKA [Berezhnev et al., 2012]), is designed to record air Cherenkov photons in the shower when the air shower events cross its field of view. It is a non-imaging optical detector that operates as the surface detector array. The narrow-angle telescopes follow the same principle as the optical detector array, except that, in a telescope system, the photons will be collected by a large reflecting mirror or mirrors and focused onto a photon-sensivitve camera, which usually consists of photomultiplier tubes. Unlike the optical detector arrays,

the telescopes are camera-based imaging detectors with a high angular resolution. These telescopes are widely used in gamma-ray astronomy, such as H.E.S.S [Hinton, 2003] and CTA [Vercellone, 2014].

Similarly to the particle detector array, the Cherenkov optical detectors mainly observe those particles that emit toward the ground array, Cherenkov photons in this case. Because the propagation of these photons barely suffers the absorption and the scattering owing to the transparency of the atmosphere, the signals collected in the detector array or telescopes usually contain more development information of the shower from the first stage to the last one, along its trajectory. This technique reflects the whole picture of the air shower until it hits the ground. The results are always related to the shower maximum and the primary compositions and can be very useful in the event reconstruction [Gaisser et al., 2013].

The ultraviolet, isotropically emitted, fluorescence photons are also created in the interactions between the shower particles and the nitrogen molecules in the air. The isotropic feature suggests that these photons can be detected in all direction, which means that the fluorescence photons can be observed from the side of the shower by other optical detectors known as fluorescence optical detectors or telescopes. By observing the showers from the side, the detectors are able to record more detailed longitudinal profile of the shower and it is even possible to measure those showers where hit the ground far way from the detector array. Another advantage is that only a few fluorescence detectors are needed to get the stereo view of the shower which greatly decreases the uncertainty of measurement and can complement the particle detector array. The typical experiments are Fly's Eye [Baltrusaitis et al., 1985] and HiRes [Sokolsky, 2011] and Auger fluorescence telescopes [Pierre Auger Collaboration, 2010].

Generally speaking, both the fluorescence detector and the Cherenkov detector are designed to observe the optical emission of the air shower. This common feature makes them to share almost the same detection techniques and the infrastructures. Nevertheless, because of the different wavelengths of the photons, which are caused by the different excitation processes, and the different durations of the signals observed on the camera, which are cause by the different propagation paths in the atmosphere and the different locations of the detectors, the optical filters in the front of the camera and the front-end electronics are not exactly the same in these two detectors.

The performance of these detectors greatly depends on the quality of the atmosphere and they are sensitive to the environmental light or the night sky background. Therefore, these detectors can be only operated during the dry, clear and moonless nights. Due to the

weaker intensity of the fluorescence light and the larger distance from the shower trajectory, the accuracy of the fluorescence detection is more relied on the environmental parameters. Hence, the monitoring of the weather condition and the atmospheric parameters is a curial part in the event reconstruction of the optical detectors. Subjected to this, the duty-cycles of these detectors are only about 10 %.

The optical detectors, especially the camera-based imaging Cherenkov/fluorescence telescopes, are the detectors that is concerned in this thesis and will be discussed in detail in the Chapter 4.

Radio detectors

The principle of detecting the radio emission from the air shower was introduced by Askaryan in 1962 [Askaryan, 1962]. J. V. Jelley and his colleagues made the first detection of the radio frequency pulses produced by EAS in 1965 [Jelley et al., 1965]. However, it was very difficult to discriminate these signals from the radio background, which is caused by the human activities, (e.g., electric and electronic system) and natural sources, by using the technology at that time. Thanks to the rapid development of the modern detection techniques, in recent decade, the radio detection restarted again. The LOPES [Falcke et al., 2005], CODALEMA [Ardouin et al., 2005] and AERA [Kelley, 2011] are typical experiments in this field. Even though this technique grows very fast in these years, and has already presented some reconstruction results of the direction and the energy of the primary cosmic rays based on the observation data [Huege, 2014], basically, it is still in the R&D stage and needs to be matured.

Summary of the indirect detection

In summary, unlike the direct detection, the ground-based experiment measures the cascades of the secondaries initiated by the interactions of the primary cosmic rays in the atmosphere.

Due to the large spread distance of the shower disk, one usually needs a relatively large ground array, which depends on the energy of the primaries, to record the lateral information and to identify the particles. With the densities and the types of the particles and the arrival time of the shower front, it is possible to reconstruct and derive the arrival directions and the energies of the primary particles based on some special physical interaction models. The accuracy of the reconstruction mainly relies on these models.

Besides, the ground array only gives a two-dimensional picture about the lateral development of a shower that contains little information about the longitudinal cascade progress. It is not enough to describe the whole shower. As we mentioned above, the traveling of the charged particles in the atmosphere also creates the polarized Cherenkov light and the isotropic fluorescence light along their trajectories. These components can be observed by optical detectors or telescopes giving information of the longitudinal development.

Because each detection method used in the ground-based experiments has its own limitations and energy scales, so in today's high-energy cosmic ray experiments, in order to improve the performance of the experiment, the best solution is to build a hybrid system by combining these different detectors together, such as electron/muon detectors, hadronic calorimeters, water Cherenkov detectors, air Cherenkov/fluorescence telescope. Another detection method as radio detectors is still in the R&D stage and will be hopefully complement the air shower detection in future.

Chapter 3

LHAASO Experiment

In more than one hundred years since V. Hess discovered cosmic rays, numbers of experiments above the atmosphere, on the ground or even under the ground were designed, operated and aimed to answer the open questions about it, such as the cosmic ray origin and their propagation of cosmic rays. Basically, there are two methods that are widely used in today's cosmic ray experiments: space-based direct measurements and the ground-based indirect measurements. The applications of these detectors are determined by their characteristics which are described in previous chapter.

On one hand, even though it is always precise to study cosmic rays by balloons or satellites, limited by the low flux of cosmic rays in the high-energy region, the small geometric size of the detector and the short duty cycle of the experiment, it is difficult to measure the cosmic rays with energies higher than 10^{14} eV. On the other hand, in contrast, limited by the absorption of the atmosphere, the cascades of the primaries with energies below this threshold are hardly observed by the ground array at low altitude. Nevertheless, until we figure out how to build huge detector array in space, for the cosmic rays with energies above this value, the best and the only way to study them is through the ground-based indirect measurements.

However, for the ground detectors, different models and different detection techniques that are exploited in experiments usually lead to large uncertainties. A single detection method or detector is not enough to acquire all information for the event reconstruction. The accuracy of the reconstruction of the primaries are greatly related to the hadronic models, which are used to interpret the cascades of the showers. Thus, in order to compare the results from different experiments, the cross-calibration is necessary. Fortunately, there is still an overlap between direct and indirect measurements that can be used to compare the ground detectors with the data from balloons or satellites.

Generally speaking, the hybrid detection, which comprises a combination of different complementary techniques, is an reasonable solution to improve the performance of the experiment. Furthermore, a relative large energy range is necessary to bridge the space experiments and the ultra high energy ground experiment. Thus, hybrid detection with multiple techniques and the cross-calibration between detectors are two crucial points for the next generation ground experiment. The Large High Altitude Air Shower Observatory (LHAASO) is such a hybrid observatory tthat will be discussed in this chapter.

3.1 Scientific goals of LHAASO

The LHAASO experiment aims to study the primary cosmic rays by observing the secondaries in the extensive air showers, which are created from the interactions of the primaries and the atmosphere. The detection techniques are similar as other existing experiments, e.g., H.E.S.S [Hinton, 2003], Milagro [Atkins et al., 2005], Auger [Pierre Auger Collaboration, 2008], HiRes [Sokolsky, 2011], KASCADE-Grande [Apel et al., 2012]. It is focused on three main scientific topics: searching for the origins of cosmic rays, full-sky survey for new gamma ray sources and studying cosmic ray physics in a large energy range [Cao, 2010; Cao and Zha, 2013].

The first scientific goal of LHAASO is to search for the origins of cosmic rays by investigating the galactic gamma-ray sources in very high energy (VHE) region, which is from 30 TeV to 1 PeV. Observing and measuring the spectra of these known sources, such as the famous supernova remnant (SNR) RX J1713.7-3946 [Aharonian et al., 2007], especially at its high-end energy, with a high sensitivity and high energy resolution ground particle detector array, are supposed to provide us trustable evidences of the origins of cosmic-ray photons whether they are from the decays of π^0 which are produced by the accelerated hadrons or the inverse Compton scattering of high energy electrons [Grupen, 2005].

Since the first TeV gamma ray source, Crab Nebula, was discovered by an imaging atmospheric Cherenkov telescope (IACT) in 1989 [Weekes et al., 1989], more than 150 sources have been located in last twenty-five years [Hinton and Hofmann, 2009; Wakely and Horan, 2014] and most of them are extremely variable in a short period. The surveillance of the existing sources is a significant part of the multi-wavelength investigation of the gamma ray sources that might be helpful to answer several fundamental physics puzzles. Therefore, the second topic of LHAASO is the full-sky survey for new gamma ray sources above 300 GeV in the northern hemisphere as well as an important chain in the global monitoring of

the transient variation of the VHE sources. Figure 3.1 shows the sensitivity of LHAASO and the comparison among different experiments. In the figure, LHAASO should be one decade more sensitive than CTA above 10 TeV and would reach 0.07 Crab Units above 300 GeV.

Thirdly, owing to the advantages of hybrid observation and the high altitude of the site, LHAASO proposes to accurately measure the spectra and identify the compositions of the primary cosmic rays in a large energy range from 10 TeV up to several hundreds PeV that covers two interesting bends in the spectra, i.e., the "1st knee" and the "2nd knee". It also covers the region where the discontinuity between indirect detection and direct detection occurs. As a consequence, this large coverage guarantees that LHAASO could establish a connection between the balloon experiments as CREAM and the ultra high energy cosmic ray ground array as Auger.

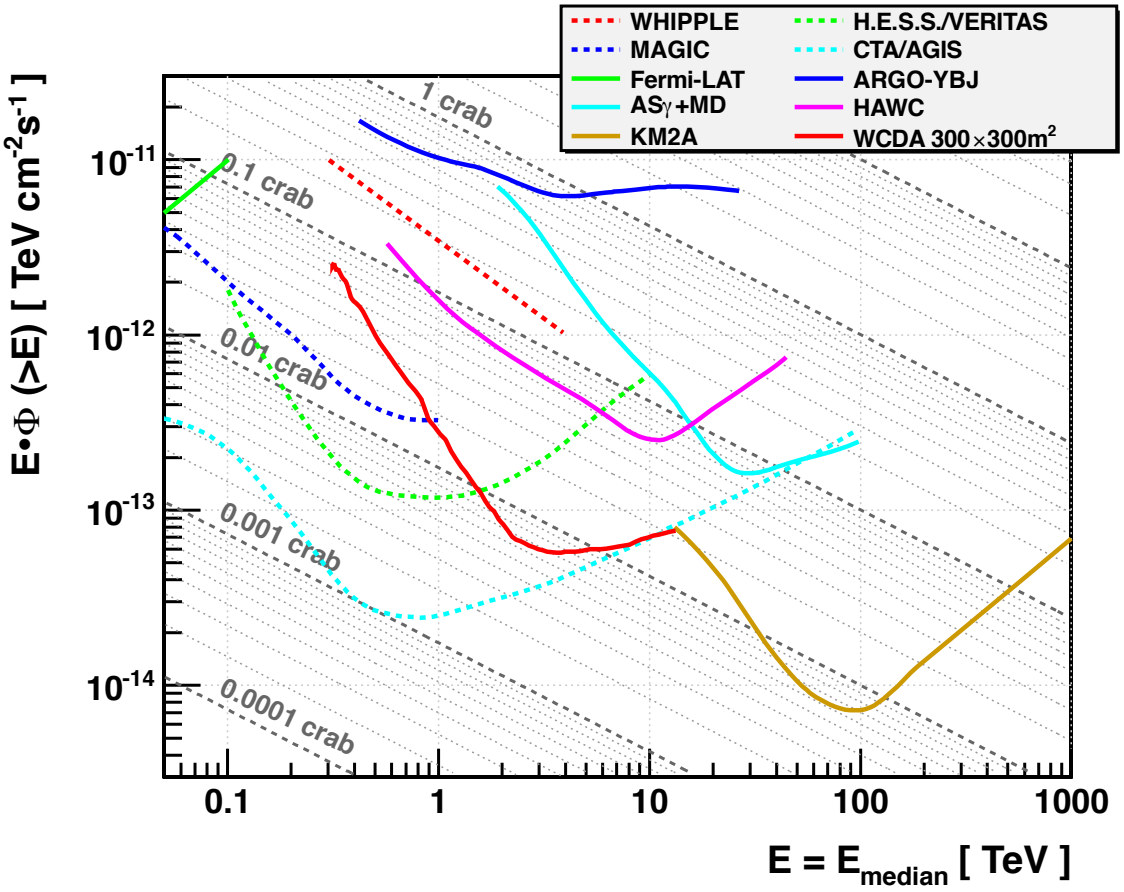


Figure 3.1: The sensitivity of LHAASO experiment for the gamma ray astronomy. The results of the other experiments are also drawn in for comparison. In the figure, LHAASO might be one decade more sensitive than CTA above 10 TeV and would reach 0.07 Crab Units above 300 GeV.

3.2 Detectors R&D for LHAASO

To achieve these goals listed above, four types of base-line detectors are proposed in the LHAASO experiment, which are the 1 km^2 extensive air shower array (KM2A), the water Cherenkov detector array (WCDA), the wide field of view Cherenkov telescope array (WFCTA) and shower core detector array (SCDA). The site of LHAASO will be located at around 29°21′30.7″ N and 100°08′14.65″ E in the Daocheng region of Sichuan province, southwest of China. The altitude of the site is about 4,400 m a.s.l. that is the height where cosmic rays with energies of few PeV reach their shower maximum. Figure 3.2 demonstrates the basic configuration of the LHAASO experiment and the relative locations of the detectors. The detailed views of detectors can be also found in this figure.

3.2.1 LHAASO-KM2A

In order to study gamma-ray astronomy above 30 TeV, the KM2A detector array, which consists of electromagnetic particle detectors (ED) and muon detectors (MD), is designed to discriminate the electromagnetic components and the muon components of the showers and to measure the lateral distributions of them.

The KM2A-ED is composed of 5,635 scintillator detectors that are placed in triangle with a spacing of 15 m (See figure 3.2). Figure 3.3 demonstrates the basic design of the KM2A-ED detector. Each detector is made up of 4×4 square plastic scintillation tiles with a size of 25 cm $\times$ 25 cm $\times$ 2 cm. Four wavelength-shift fibers are embedded in every scintillation tile to collect scintillation light produced by particles. In total, 128 ends of the fibers from 16 tiles will connect to a single photomultiplier to convert the light signals into electric signals finally [Cao and Zha, 2013]. Furthermore, a thin lead plate is used in the detector as the active material to improve the resolution of the detector. The whole detector including the electronic part will be packed into a iron box which size is 1 m $\times$ 1.2 m. Thus, whole sensitive area for KM2A-ED is about 5,635 m^2 and 1 m^2 each. The summarized specifications of both ED and MD in KM2A array are listed in table 3.1.

A 1 % engineering array of KM2A-ED was built by the side of the hall of the ARGO-YBJ in Tibet in 2010 to test and evaluate the performance of the prototype detector [Liu et al., 2011].

The muon detector, KM2A-MD, based on water Cherenkov detection consists of 1,221 cylindrical water tanks with a diameter of 6.8 m and a height of 1.2 m. The water tanks are buried in the ground with a layer of soil on it. The height of the soil layer is 2.5 m

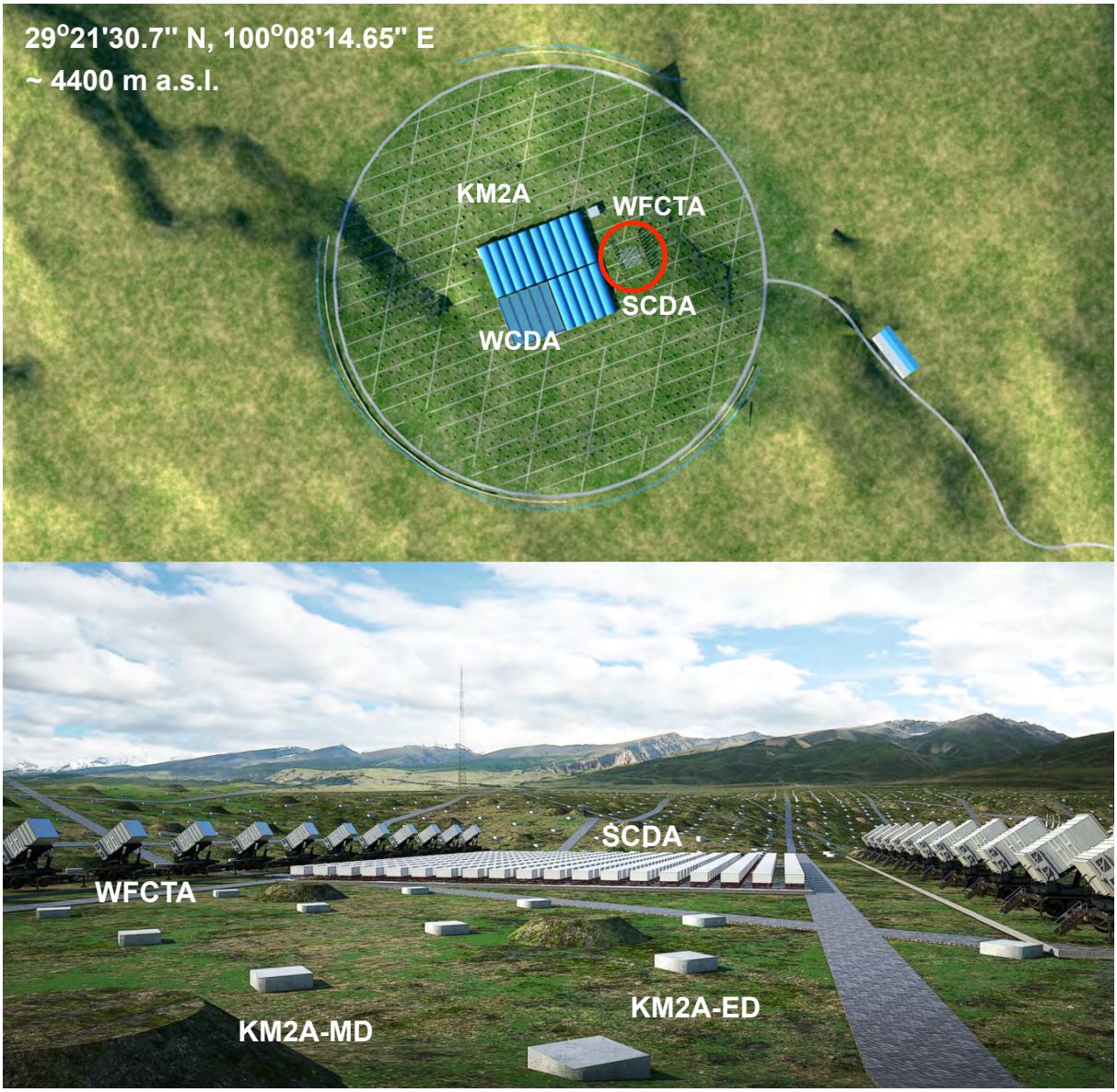


Figure 3.2: Imaginary top view and perspective view of LHAASO site. The relative locations of different detectors are presented in the upper figure. The WCDA detectors are in the middle of the layout and surrounded by KM2A array. The WFCTA and SCDA detectors are deployed by the side of WCDA where is marked with an red cycle. The detail information about the cycled area can be found in the lower figure that is the imaginary perspective view of the detectors.

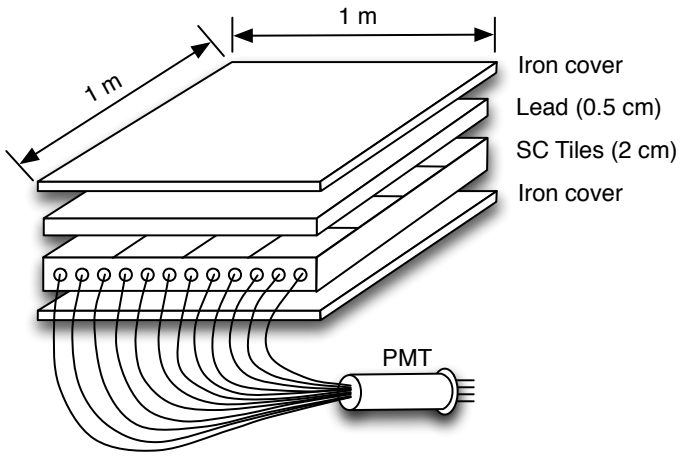


Figure 3.3: Basic layout of the KM2A-ED

above the ground, which is equivalent to an absorber with a radiation length of 12 can be used to stop other particles passing through except muons. As the KM2A-ED, the muon detectors are placed in triangle as well, but the distance increases to 30 m (See figure 3.2). The basic structure of the KM2A-MD is shown in figure 3.4. In practice, a photomultiplier looks downward into a bag, which is filled with pure water, to record the photons created by muons. The effective area of KM2A-MD is about 43,956 m^2 and 36 m^2 each (See table 3.1) [Ma et al., 2013]. A prototype detector is running at YBJ site to verify this design [Xiao et al., 2013].

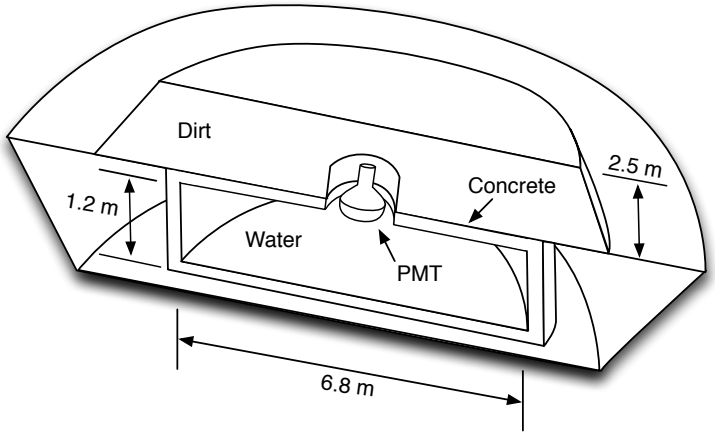


Figure 3.4: Basic structure of the KM2A-MD

Table 3.1: Summarized specifications of LHAASO-KM2A

KM2A-ED		KM2A-MD	
Property	Specification	Property	Specification
Effective area	1 m^2/detector 5,635 m^2/array	Effective area	36 m^2/detector 43,956 m^2/array
Thickness of tiles	2 cm	Water depth	1.2 m
Number of fibers	128	Mound height	2.5 m
		Water attenuation length	30 m (400 nm)
Detection efficiency ($>$ 5 MeV)	$>$ 95 %	Reflection coefficient	$>$ 95 %
Dynamic range	1 – 10,000 particles	Dynamic range	1 – 10,000 particles
Time resolution	$<$ 2 ns	Time resolution	$<$ 10 ns
Particle counting resolution	25 % @ 1 particle 5 % @ 10,000 particles	Particle counting resolution	25 % @ 1 particle 5 % @ 10,000 particles
Aging ($<$ 20 %)	$>$ 10 years	Aging ($<$ 20 %)	$>$ 10 years
Spacing	15 m	Spacing	30 m
Number of detectors	5,635	Number of detectors	1,221

3.2.2 LHAASO-WCDA

In last twenty-five years, IACTs contributed a lot to the discoveries of the gamma ray sources. However, suffering from the short duty cycle ($\sim 10\%$) and the small field of view ($\sim 5°$), the full-sky survey for them is still a time-consuming job. As a complementary technique, particle detector arrays as Milagro and ARGO-YBJ have already shown their unique abilities in this field with the advantages of a long duty cycle ($> 90\%$), a wide field of view (~ 1.5 sr) and good background rejection. Thus, in LHAASO, a water Cherenkov detector array (WCDA) is proposed to scan for gamma ray sources above 300 GeV in the northern sky. The LHAASO-WCDA consists of four rectangle water ponds with a size of 150 m $\times$ 150 m $\times$ 4.5 m for each of them as shown in figure 3.2. The total active area for this array is about 90,000 m^2 and the sensitive of it could reach 0.07 Crab Unit above 300 GeV (see figure 3.1).

Furthermore, each pond is divided into 900 cells (30 $\times$ 30), which size is 5 m $\times$ 5 m, by the black plastic curtains to prevent cross-interference light from the adjacent cells. The conceptual diagram of LHAASO-WCDA is shown in figure 3.5. The Cherenkov photons generated in the water are collected by a photomultiplier that is installed at the bottom of the pond and looking upward to record the arrival time and the number of the photons [Cao and Zha, 2013]. The detail information can be found in table 3.2.

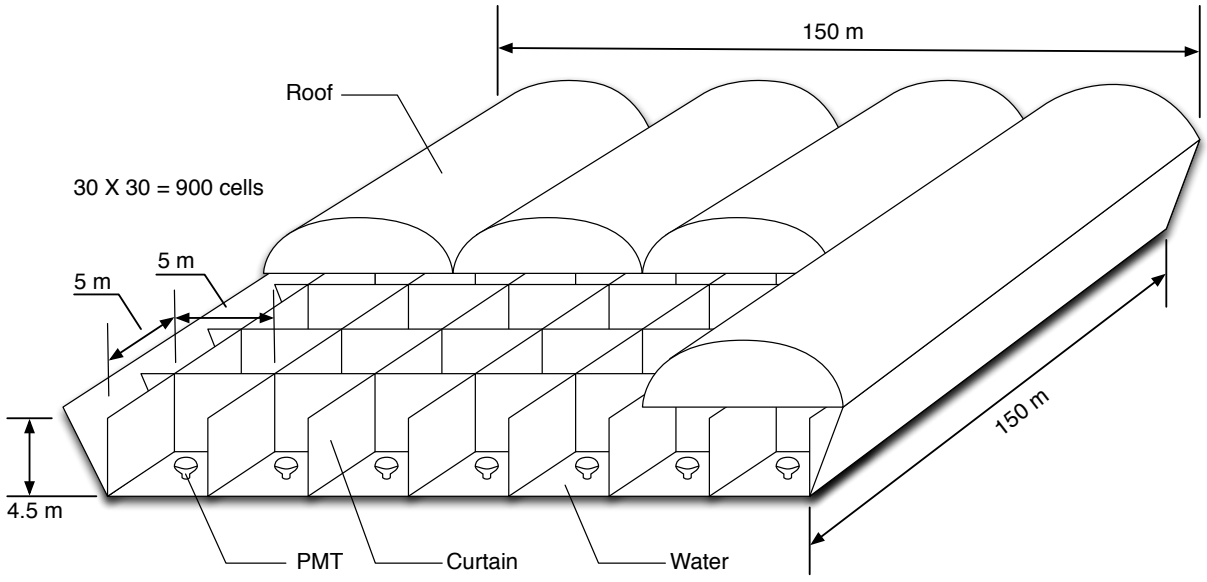


Figure 3.5: Conceptual diagram of LHAASO-WCDA

Table 3.2: Summarized specifications of LHAASO-WCDA

LHAASO-WCDA	
Property	Specification
Cell area	25 m^2
Effective water depth	4 m
Water attenuation length	$>$ 20 m (400 nm)
Precision of time	0.5 ns
Dynamic range	1– 4000 p.e.
Time resolution	$<$ 2 ns
Charge resolution	40 % @ 1 p.e. 5 % @ 4000 p.e.
Accuracy of charge calibration	$<$ 2 %
Accuracy of time calibration	$<$ 0.2 ns
Total area	90,000 m^2
Total cells	3600

In order to inspect and verify this design, a single unit prototype detector [An et al., 2011] and 1 % engineering array including 3×3 cells [An et al., 2013] with all auxiliary systems as DAQ, water purification system, slow control system and etc., have been constructed and operated next to the hall of ARGO-YBJ in Tibet since 2011.

3.2.3 LHAASO-SCDA

As shown in the figure 3.2, a shower core detector array (SCDA) is located by the side of LHAASO-WCDA, which consists of 20×20 detectors separated by a distance of 3.75 m. The total active area of the array is about 5,000 m^2. The detectors are built by a lead layer with a thickness of 3.5 cm (7 radiation length) above a plastic scintillation counter, each size is 50 cm $\times$ 80 cm $\times$ 1 cm. The basic design of this detector is following the design of the YAC (Yangbajing Air shower Core array) [Jiang, 2009; Amenomori, 2011] that is shown in figure 3.6. When the shower hits the detector array, the high energy electrons and gammas will be converted into electromagnetic showers by the lead cover and collected by the scintillators under it. Two photomultipliers, i.e., high-gain PMT and low-gain PMT, are attached to the scintillators with fibers to detect the light signals and cover a large dynamic range from 1 minimum ionization particle (MIP) to 10^6 MIPs. The purposes of this detector is to study the parameters of the shower core of cosmic rays, such as the number of the

particles, the extension of the lateral distribution and so on [Ma et al., 2013]. It is also used to provide a trigger source to select cosmic ray events in the hybrid detection.

The prototype detectors similar to the YAC-II have been constructed and operated together with ASγ detectors in Tibet since 2011[Zhai et al., 2013].

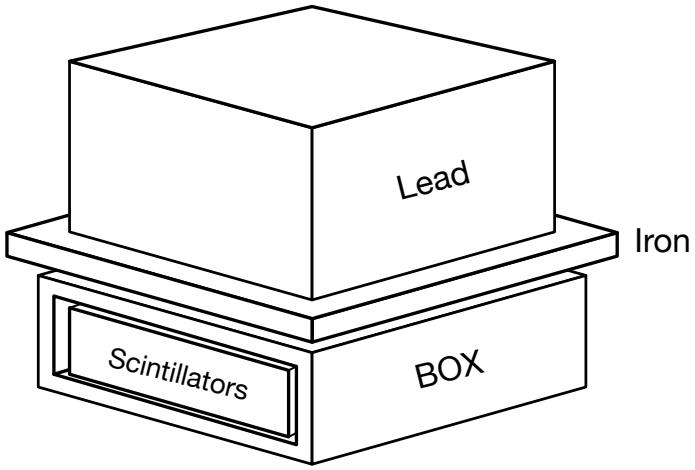


Figure 3.6: Basic design of the LHAASO-SCDA

3.2.4 LHAASO-WFCTA

To improve the particle identification of cosmic rays above 1 PeV region as well as to extent the energy scale to high energies even above 100 PeV, a wide field of view Cherenkov telescope array (WFCTA), is also designed for the experiment. According to the original plan, the LHAASO-WFCTA should be reconfigured into three modes. The first one is the "Cherenkov mode" that is focused on a low energy region from 30 TeV to 10 PeV. The second one is still the "Cherenkov mode" but it is focused on the middle energy scale from 10 PeV to 100 PeV. The last one is the "fluorescence mode" that allows the telescopes to measure the spectra and the compositions of cosmic rays above 100 PeV [Ma et al., 2013].

There will be 24 telescopes in the array. Each telescope is composed of 1,024 photomultipliers and covers a field of view (FOV) about $14^\circ \times 16^\circ$. To achieve the scientific goals, in the "Cherenkov mode", the telescopes will be combined into different groups and placed to cover the zenith angle from 0° to 30° and the azimuth angle from 0° to 360°. In the array, one of the telescopes will point to the zenith angle 0°; 8 of the telescopes will point to the zenith angle 77°; 12 of telescopes will point to the zenith angle 64°; the last 3 of the telescopes will be reserved for other observation. There should be overlaps between

the FOVs of the adjacent telescopes for the calibration purposes. Each telescope is 75 m away from SCDA to make sure the events observed by LHAASO-SCDA can be recorded and measured by LHAASO-WFCTA as well to form a hybrid observation[Cao and Zha, 2013].

In the second phase, the LHAASO-WFCTA array will be rearranged to reach higher energies with the "fluorescence mode". In this mode, the telescopes will be moved away from the ground array. They will be used to observe and monitor the fluorescence light of the showers from a distance of 4 to 5 kilometers by the side of the ground array. The 24 telescopes will be divided into three groups: 16 of the telescopes which covers the elevations from 3° to 59° and two other groups of the telescopes which covers the elevations from 3° to 31° perpendicularly. Each of these two groups of the telescopes consists of 4 telescopes. The schema of the "fluorescence mode" is shown in the figure 3.7. Under this configuration, the LHAASO-SCDA is replaced by the LHAASO-KM2A array. As a result of that, the showers with energies above 100 PeV can be detected and well measured by LHAASO-WFCTA and LHAASO-KM2A stereoscopically [Cao and Zha, 2013].

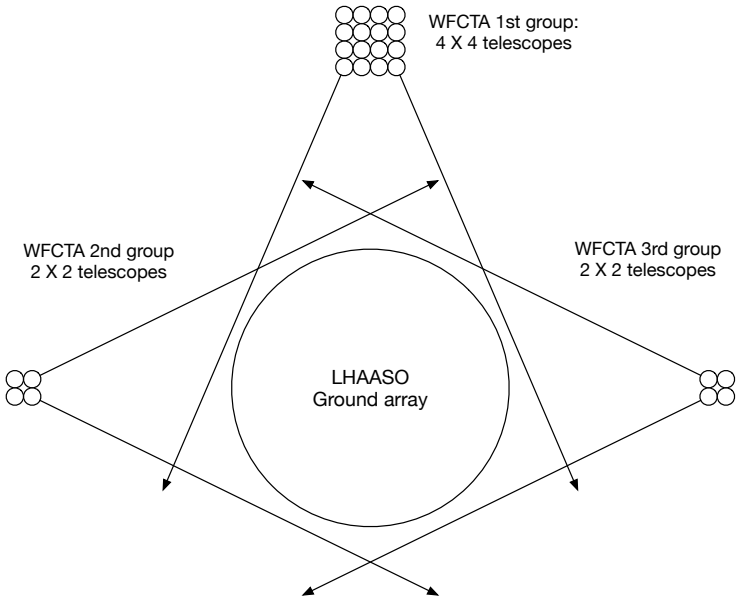


Figure 3.7: Schema of the "fluorescence mode" of the LHAASO-WFCTA

Two prototype telescopes of LHAASO-WFCTA were designed, fabricated and tested. Each of the telescope is composed of a 4.7 m^2 aluminized reflector and a camera of 256 hexagonal PMTs (16×16). They cover a FOV of $14° \times 16°$ and a single PMT is equals to 1° independently. The whole system, including the electronics, slow control and monitoring

system and etc., is assembled in a shipping container with a size of 2.5 m × 2.3 m × 3 m. The container and a hydraulic system are mounted on a truck frame to keep the flexibility of the telescope system [Zhang et al., 2011]. The picture of a prototype telescope is shown in figure 3.8. The detailed specification of LHAASO-WFCTA is shown in table 3.3.

Figure 3.8: Picture of the prototype of LHAASO-WFCTA

Table 3.3: Summarized specifications of LHAASO-WFCTA

LHAASO-WFCTA	
Property	Specification
Signal polarity	Negative (Anode)
Dynamic range	320 fC to 480 pC or 10 – 15,000 p.e. @ PMT Gain = 2×10^5
Charge resolution	20 % @ 10 p.e. 5 % @ 15,000 p.e.
Relative deviation	< 2 %
Time resolution	< 20 ns (RMS)
Adjustable threshold	5 p.e. to 100 p.e.
Single channel event rate	10 kHz/channel
Duration of signal	6 ns to 50 ns (Cherenkov mode) 10 ns to 3 μs (Fluorescence mode)
Pedestal monitoring	Electronics and Sky
Channel	1,024/telescope
Power consumption per telescope	260 W/telescope
Total telescopes	24

Int 2007, these two telescopes were deployed at Yangbajing in Tibet to verify the design of the WFCTA. The co-observation of the WFCTA prototypes and the ARGO-YBJ RPC carpet detectors already showed several inspiring results that proved the ability of the WFCTA prototype and the potential of the hybrid measurements. With the longitudinal development of the shower that was measured by the WFCTA prototypes and the lateral distribution that was measured by ARGO-YBJ RPC detectors, the hydrogen and helium nuclei were well separated from other cosmic ray components. The energy spectrum of these particles from 100 TeV to 700 TeV were also measured and compared with results from different experiments (e.g., ARGO and CREAM). Figure 3.9 shows the energy spectrum of protons and helium nuclei measured by the hybrid experiment of WFCTA prototype and the ARGO RPC carpet detectors. The measured spectral index γ is -2.63 ± 0.06. More information can be found in [Bartoli, 2014]. The additional information about this array will be discussed in the following chapters.

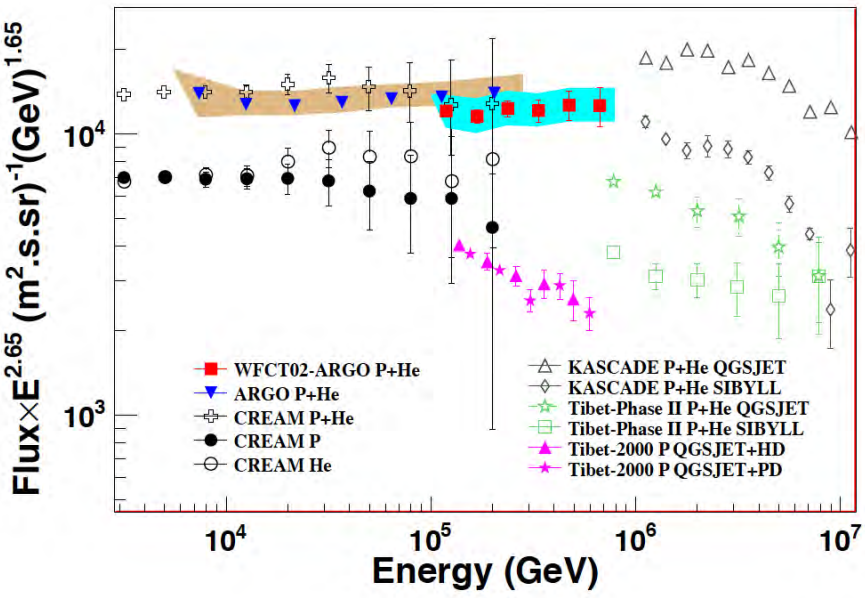


Figure 3.9: Spectrum of protons and helium nuclei from 100 TeV to 700 TeV measured by the hybrid experiment of WFCTA prototype and the ARGO RPC carpet detectors. The results are shown by filled red squares in a cyan shaded area. For the comparison, the results of other experiment are plotted as well. The figure is taken from [Bartoli, 2014].

Chapter 4

From cosmic rays to electronics

In the previous chapters, the brief history of the discovery of cosmic rays, the basic detection techniques and the proposal of LHAASO experiment were introduced and presented as the foundation of our discussion. Since the main purpose of this thesis is to study how to build an appropriate electronic system for LHAASO experiment, especially for the WFCTA telescopes, the bridge from the original cosmic rays to the electronics must be settled before we discuss the specific design of the electronics system. Prior to the design, the characteristics of the input signals of the telescope should be studied. As we know, the most common way to learn the behavior of the signals is through the simulations. Therefore, in this chapter, the additional information on the light production of cosmic rays and the cosmic ray simulation will be discussed at first. Then a new photomultiplier model for both physics and electronics will be introduced to link up with different simulation procedures and softwares. Finally, the connection between cosmic rays and electronics can be established.

4.1 Light production of cosmic rays

When the original cosmic rays hit the up top of the atmosphere, the energetic particles initiate a series of cascades and generates extensive air showers which contain millions of secondary particles. If these secondaries fulfill some conditions, two types of light or radiation are emitted when particles traverse through the atmosphere. They are the Cherenkov light and the fluorescence light. These photons correspond to the input signal of the IACT-type telescopes as the WFCTA that can be used to indicate the longitudinal development of the showers. In this section the basic characteristics of these two light emissions will be discussed.

4.1.1 Cherenkov light

Light or radiation is emitted when a relativistic charged particle travels through a transparent medium at the speed of v = βc, which is faster than the speed of light in the same medium. In this progress, the radiation emission is due to disturbance of the neutrality of the atoms along the trajectory of the charged particle. All the brief electromagnetic pulses radiated from each elements along the path are polarized and construct a wavefront that can be only observed in a small cone. This radiation is known as *"Cherenkov radiation"*, and the cone is called the *"Cherenkov cone"* [Jelley, 1958]. The progress of the Cherenkov light emission is demonstrated in figure 4.1. The opening angle or the Cherenkov angle θ can be explained by Huygen's principle (See figure 4.1).

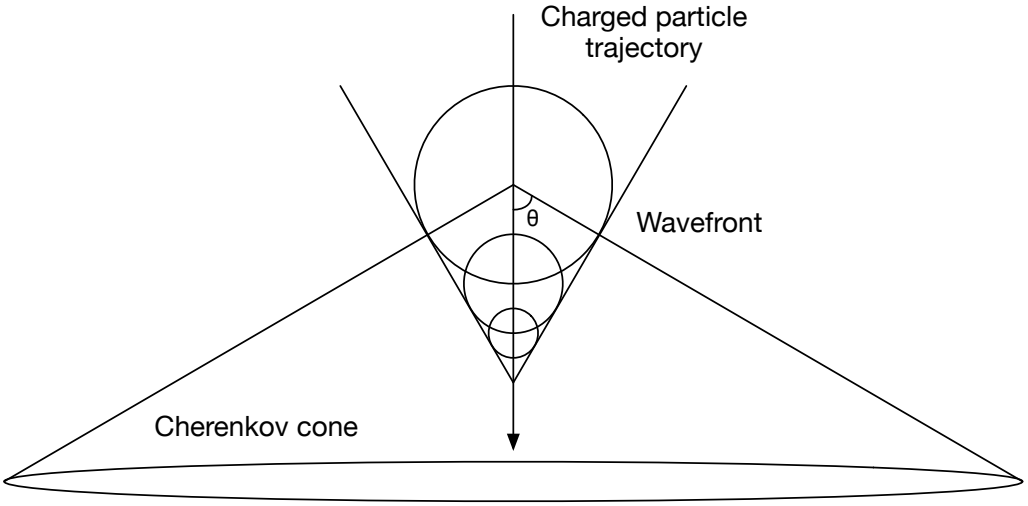


Figure 4.1: Diagram of Cherenkov light emission.

This angle depends on the velocity of the charged particles and the refractive index of the medium that is defined as

$$\theta_{ch} = acos(\frac{1}{n\beta}) \tag{4.1}$$

Where n is the refractive index of the given medium and $\beta = v/c$. There is a threshold velocity as

$$\beta_{min} = \frac{1}{n} \tag{4.2}$$

With the equation 4.2, the threshold energy for a particle to produce Cherenkov light can be described by

$$E_{min} = \frac{m_0 c^2}{\sqrt{1-\beta_{min}^2}} = \frac{m_0 c^2}{\sqrt{1-(1/n)^2}} \tag{4.3}$$

Where m_0 is the rest mass of the charged particle. Therefore, for the electrons and positrons, the minimum energy is about 21 MeV. For the ultra-relativistic particles ($\beta = 1$), there is a maximum emission angle for the Cherenkov light that is given by

$$\theta_{max} = acos(\frac{1}{n}) \tag{4.4}$$

Thus, the typical Cherenkov angle is about 1.3° in the atmosphere and depends on the refractive index of it. To calculate the production of the Cherenkov photons of an extensive air shower and to take into account the variation of the refractive index at different altitudes, a simple model can be used

$$n(h) = 1 + n_0 \cdot exp(-\frac{h}{h_0}) \tag{4.5}$$

Where $n_0 = 2.9 \times 10^{-4}$, $h_0 = 7,100$ m and h is the observation level. For example, when $h = 4,400$ m, which is the altitude of the LHAASO site, the minimum energy for electron to emit Cherenkov light is about 29 MeV.

Furthermore, the radius of the Cherenkov ring is derived from equation 4.4 and 4.5 and is given by

$$R_{cr} = h \cdot tan\theta \tag{4.6}$$

Based on the equations 4.3, 4.4, 4.5 and 4.6, the parameters of the Cherenkov light of a shower can be easily calculated. Figure 4.2 shows the calculation results of a γ-ray induced air shower. The minimum energy of electrons and positrons, the emission angle and the radius of the Cherenkov ring are all shown in the figure. In the figures, from the sea level to 20 km a.s.l., the minimum energy of electrons and positrons varies from $\sim$ 21 MeV to $\sim$ 86 MeV when the altitude increases. The Cherenkov emission angle θ decreases from $\sim 1.38°$ to $\sim 0.34°$ in the same altitude region. The radius of the Cherenkov ring increases with the altitude and reaches its maximum value at around 14 km a.s.l., then gradually decreases above this height. Thus, at the observation level, the lateral extension of the Cherenkov

light forms a circular distribution with a diameter of about 250 m, which is known as the *"Cherenkov light pool"* and shown in figure 4.3.

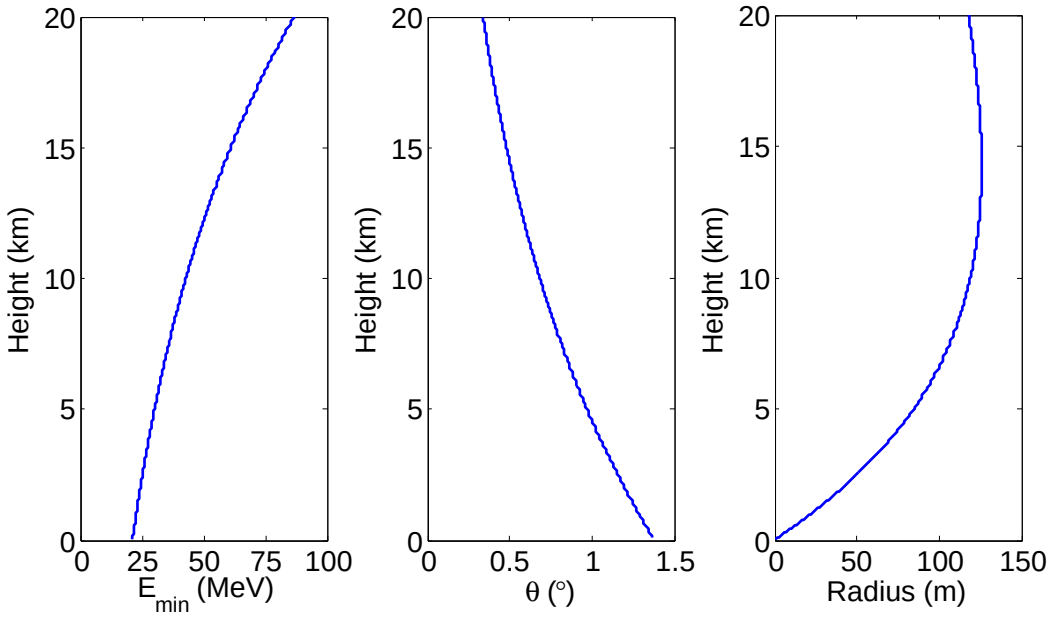


Figure 4.2: Parameters of the Cherenkov light of a shower. Left: the relationship between the minimum energy of electrons and positrons and the height of the shower maximum; Center: the relationship between the Cherenkov emission angle θ and the height of the shower maximum; Right: the radius of the Cherenkov ring against the height of the shower maximum.

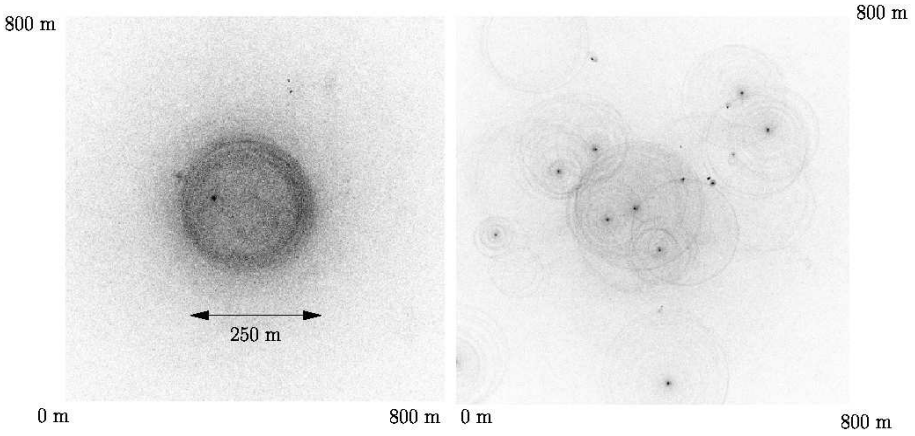


Figure 4.3: Distributions of Cherenkov light at different energies are seen on the ground. Left: γ-ray induced shower at 300 GeV; Right: proton induced shower at 1 TeV. The picture is taken from [Ergin, 2005].

Since the Cherenkov photons are highly polarized and travel with a speed of light, the arrival time of the signal is usually very short in duration about $3 \sim 5$ ns [Weekes,

2003; Cabot et al., 1998]. Moreover, the Cherenkov photons may be partially scattered and absorbed when they traverse through the atmosphere. There are three basic types of scattering and absorption processes: Rayleigh scattering, Mie scattering and Ozone absorption. More information can be found in [Ergin, 2005].

4.1.2 Fluorescence light

Unlike the Cherenkov radiation, when the energetic charged particles travels in the atmosphere, they will ionize and excite the nitrogen molecules. Nitrogen molecules will decay by emitting ultraviolet photons. These photons are called fluorescence or scintillation light. This isotropic light can be observed from aside at distances of several kilometers away. Considering this distance, it can be treated as a small diffuse light source which travels across the sky with a speed of light [Bunner, 1967]. The spectrum of the fluorescence spans from about 310 nm to 440 nm.

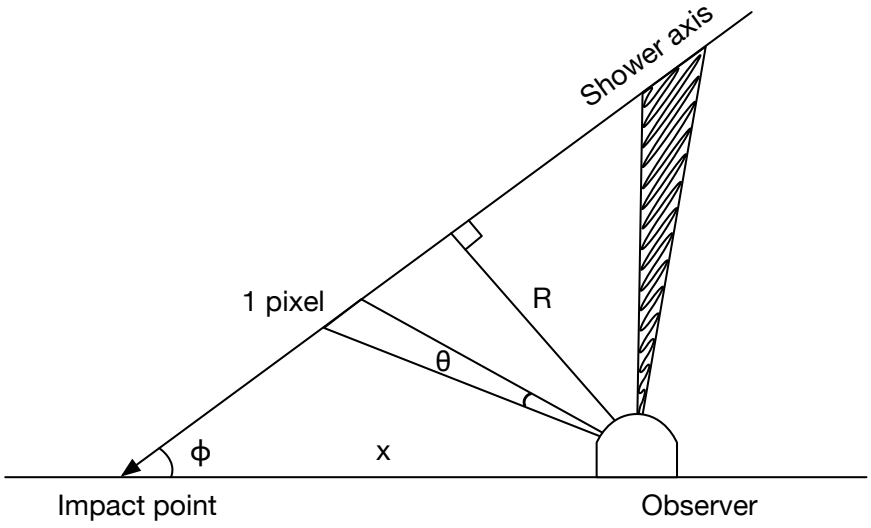


Figure 4.4: Demonstration of fluorescence light detection and parameters calculation

Figure 4.4 is a demonstration of how to detect fluorescence light caused by the air shower. As shown in the figure, by using basic trigonometric functions, one can easily estimate the duration of the fluorescence signal when it crosses a specific field of view[Sokolsky, 1989]. The duration of the signal approximates to

$$\Delta t_{PMT} = \frac{2R}{c \cdot cot(\theta/2)} \tag{4.7}$$

Where θ is the field of view of the detector. The distance of the closest path from the shower axis to the detector R is given by

$$R = x \cdot sin\phi \tag{4.8}$$

Where x is the distance from the impact point to the detector and ϕ is the incident angle from shower axis to the ground level.

As an example, in LHAASO experiment, the resolution of 1 pixel of the WFCTA is 1°. Hence, if the telescopes operate in the "fluorescence mode" and are placed at a distance of 5 km away from the ground array, and if the trajectory of the shower is vertical, for each pixel or a single PMT ($\theta = 1°$), according to equation 4.7 and 4.8, the duration of the signal is about 291 ns.

4.2 Cosmic ray simulations

Experiments must be carefully modeled and analyzed, not only to plan the experiment, but also to prepare the experimental data processing. Therefore, for a cosmic ray experiment as LHAASO, in order to guide the design of the detectors, the basic characteristics of the input signals must be simulated and understood. The most common way to do this is through a detailed Monte Carlo calculation that takes into account all the high energy physics processes. There are many computer simulation programs that can achieve this purpose, but the mostly used one is CORSIKA (Cosmic ray simulation for KASCADE).

CORSIKA is standard detailed Monte Carlo simulation program that is focused on studying of the evolution of EAS in the atmosphere that is initiated by photons, protons, nuclei or any other particles [Heck et al., 1998]. It is an assembly of several routines and was first developed for the KASCADE experiment at Karlsruhe in 1989. Since then this program has been continuously maintained and upgraded.

The program identifies about 50 elementary particles and allows to simulate the interactions and decays of these particles up to energies of 10^{20} eV. The type, energy, location, direction and arrival time of these particles can be also tracked down from the beginning to the end. It supports many options and models (e.g., QGSJET, GHEISHA and FLUKA), for different purposes. For more information, one could read the manual of the software [Heck and Pierog, 2011].

Thus, the first part of the cosmic ray simulation in this work is to generate the corresponding cosmic ray events by using the CORSIKA MC program. Because the purpose of

the simulation is to guide the design of the front-end electronics, but not to repeat all the physics simulation of WFCTA, only a few necessary events are produced to demonstrate the basic characteristics of the extensive air shower, as the maximum numbers of photons or photoelectrons induced by the showers in a specific energy range and the longest duration of the signal, which are the most important information for the electronics. In this work, CORSIKA v6990 is used to generated cosmic ray events. The quark-gluon-string model QGSJET-II-03 [Kalmykov et al., 1997] and FLUKA-2011.2b model [Ferrari et al., 2005] are selected to simulation high-energy and low-energy processes, respectively. For electromagnetic processes, the EGS4 electromagnetic model is used [W. R. Nelson and Rogers, 1985].

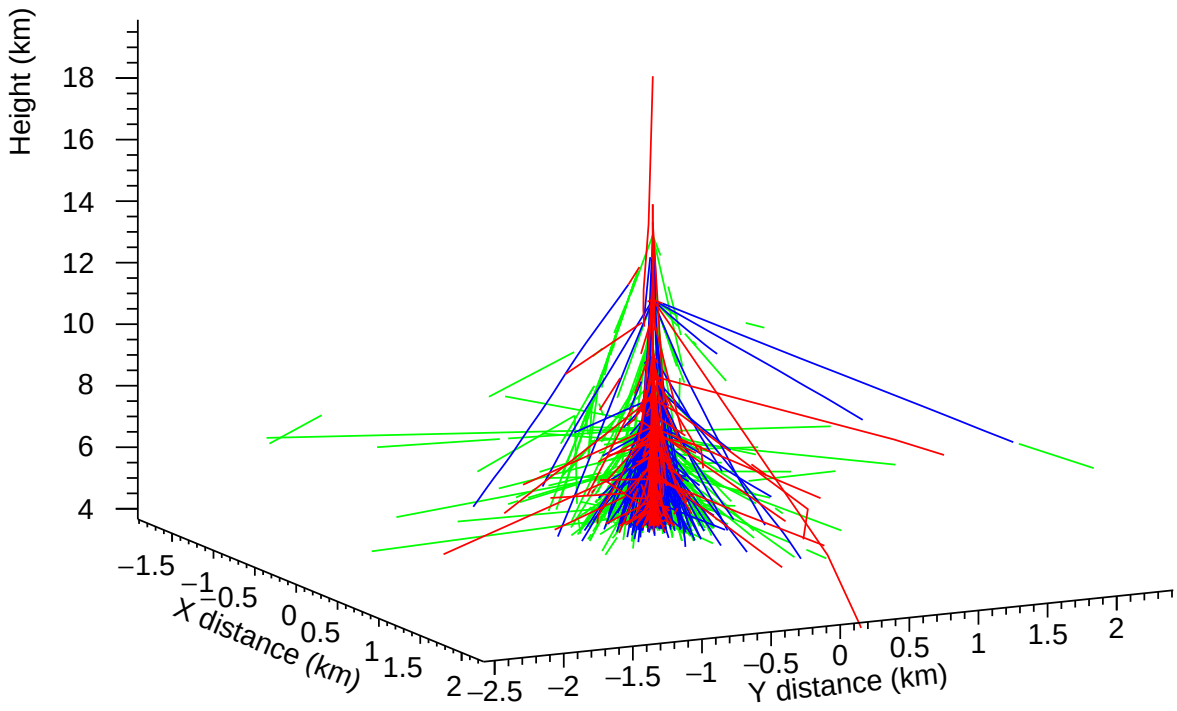


Figure 4.5: Example of cosmic-ray shower event in 3D vision generated by CORSIKA (1 PeV proton). In the figure, the green lines, the blue lines and red lines represent the electromagnetic components, the muon components and hadronic components respectively.

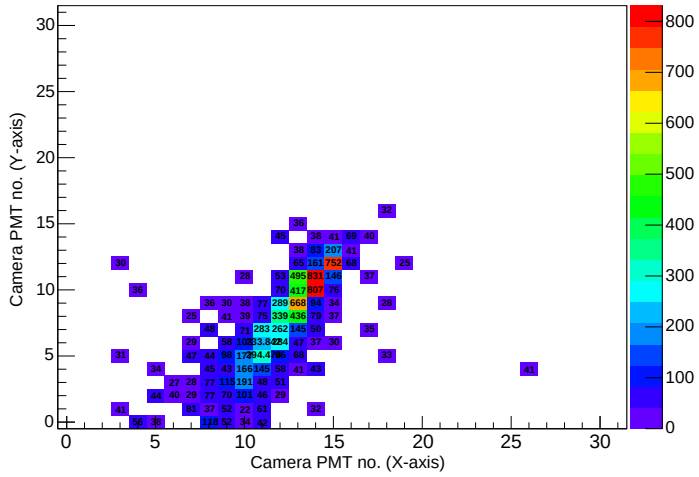
Figure 4.5 gives an example of extensive air shower event in 3D vision which is generated by CORSIKA at the LHAASO site. This means that the observation level is 4,400 m

a.s.l and the magnetic field parameter is set to Daocheng area (34.845, 35.396). It is a proton shower with an energy at 1 PeV. The zenith angle and azimuth angle are all 0°. In the figure, the green lines, the blue lines and red lines represent the electromagnetic components, the muon components and hadronic components, respectively. Because the photon-to-photoelectron conversion of the PMT is calculated in the program during the Cherenkov light simulation, the photoelectrons can be read out directly from the output files. However, since we still do not know which PMT will be used in WFCTA finally, in the simulation, the Hamamatsu R1398HA as the default tube of CORSIKA, has been exploited to evaluate our design.

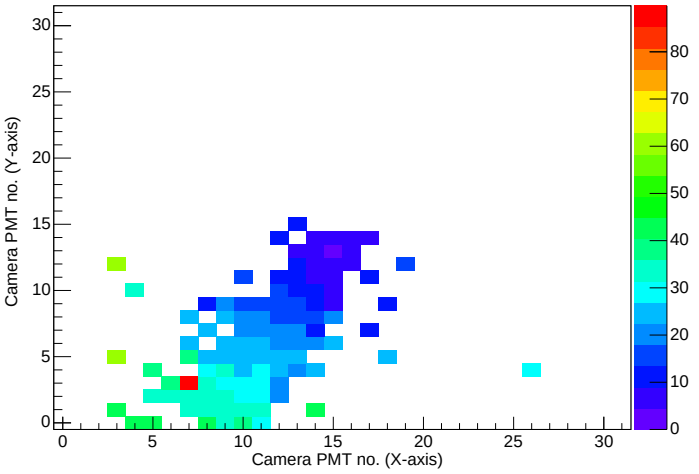
After events generation, the response of the telescope will be taken into account. A telescope simulation program, which name is "NewTel", written by the LHAASO group in the Institute of High Energy Physics (IHEP) China, is used to simulate the response of the reflectors, the behavior of the camera etc.. This program simulates the important values as the number of photoelectrons, the mean arrival time, the noise, the duration of signal captured by each tube in the camera array. Figure 4.6 shows the different type of possible images captured by WFCTA corresponding to the same event generated in the last step as the one shown in figure 4.5. Figure 4.6a shows the photoelectrons recorded by the camera. The maximum value is 831 p.e. including noise. This one not only shows the longitudinal development of the air shower, but can be used to evaluate the dynamic range of the PMT and the front-end electronics. Figure 4.6b presents the arrival time of the Cherenkov signal reaching the triggered tubes in the array. With it the time information of the shower, the direction of the cosmic ray can be reconstructed.

The duration of the signals is listed in the figure 4.6c. From the plot, it is clear that the average duration is about 10 ns for each tube. However, due to the design of the identification algorithm in "NewTel", it cannot recognize the multiple hits in the same sampling window for each tube. Hence, at the fringe of the image, there will be one or two of tubes who receive a "long" signal that may be over ~ 50 ns sometimes. Nevertheless, these sorts of plots are good enough for electronics. They suggest the possible dynamic range and the time profile of the input signal.

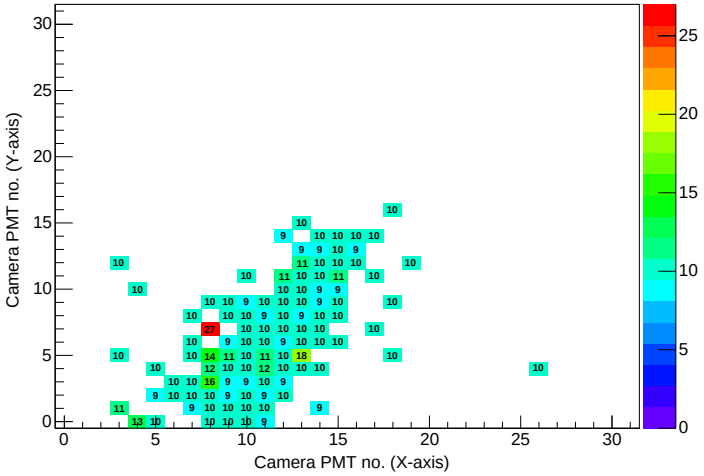
As described in the previous chapter, the energy range of WFCTA is from 30 TeV to 10 PeV. Based on this, several events in this scale are produced and passed to telescoped simulation program to verify the requirements of the telescope. Both proton induced showers and iron induced showers are simulated with different zenith angles (0°, 5°, 10°). Table 4.1 summarized all these results. First, the number of photoelectrons increases with increasing



(a) Number of photoelectrons on triggered tubes



(b) Arrival time of photoelectrons on triggered tubes



(c) FWHM of signals on triggered tubes

Figure 4.6: Example of a captured event by WFCTA camera (Proton: 1 PeV; zenith angle: 0°) (See text.)

energy. It reaches almost 40,000 p.e. when the energy of the shower increase to 20 PeV. Second, the number of photoelectrons induced by iron showers is larger than the one induced by proton showers. However, due to the fluctuations of the shower, in some cases, it may not exactly follow the rules. As shown in the table, the number of photoelectrons produced by a 5 PeV iron shower is smaller than the one generated by proton. For the low limit of the signal, it is about 30 p.e. when energy is down to 30 TeV.

Due to the inaccuracy of the computer simulation, it is safe to say that the dynamic range of the PMTs in the camera is from 20 to 12,000 p.e.. Furthermore considering the margin of the design, the range of the electronic system should be larger than this one. As a result of this, the requirement of the front-end electronics should reach 10 to 15,000 p.e. for WFCTA in the Cherenkov mode as we discussed in last chapter.

When showers hit the telescope un-vertically (e.g., zenith angle = 5° or 10°), the telescope continually records the events until they exceed the field of view of the telescope. It is obvious that, from the table 4.1, the air shower escapes the FOV when the zenith angle reaches 10°. The only difference of these events is the shape or the location of the image on the camera.

For the other important specification of the telescope, which is the duration of the signal, the mean value is about 11 ns in all cases. Most of the signals only last 9 to 10 ns, but some of them could sustain up to 50 ns that is due to the identification algorithm as we discussed above. Thus, the estimated length of time of the signal is from 6 to 50 ns with taking into account the design margin.

Table 4.1: Maximum photoelectrons and mean FWHM of the signals captured by WFCTA camera

Energy	Proton shower				Iron shower			
	Zenith angle			Mean	Zenith angle			Mean
	0°	5°	10°	FWHM (ns)	0°	5°	10°	FWHM (ns)
30 TeV	81	109	32	∼ 10	49	78	–	∼ 10
1 PeV	831	887	34	∼ 10	1,262	1,212	38	∼ 11
5 PeV	5,240	5,203	51	∼ 12	5,004.68	5,024.32	54	∼ 10
10 PeV	9,972.44	7,051.42	58	∼ 13	11,069.6	9,649	48	∼ 12
20 PeV	25,344.5	14,056.2	138	∼ 12	39,867.3	17,330.5	140	∼ 12

4.3 Photomultiplier simulation model

For now, two parameters of the input signal are extracted from the cosmic ray simulation, which are the dynamic range and the duration. The next step is to convert the light signals into electrical ones for the front-end system. As the most important devices used in LHAASO experiment, the behavior and the response of the photomultiplier must be carefully modeled for both physics and electronic purposes. However, before introducing of photomultiplier models, the basics of this sort of detector will be discussed. Then the common photomultiplier models as well as a new model for physics simulation and design of the electronics will be presented.

4.3.1 A brief introduction of photomultipliers

The photomultiplier is a vacuum tube, which is ultra sensitive to the light signal in ultraviolet, visible and near-infrared range of the electromagnetic spectrum. The role of the tube is to convert the faint light signal into electric one, and then amplify it to a detectable level. Two fundamental processes are involved in this progress that are the photoelectric effect and the emission of secondary electrons. The first document about photomultiplier was published in 1934 by RCA (Radio company of American) [Iams and Salzberg, 1943]. H. Iams and B. Salzberg firstly installed a photoelectric-effect cathode and a single secondary emission amplification stage into a vacuum tube that formed a phototube with a gain of 8. Then, this type of multiple dynodes tube was described in details in 1936 and was called as *"Photomultiplier"* later [Zworykin et al., 1936].

In more than seventy years, the photomultiplier continually developed and were widely used in many areas that spans from the medical diagnostic equipments to the aerospace instruments. However, it keeps three basic features: large sensing area, ultra-fast response and excellent timing performance, high gain and low noise. Consequently, the main structure of the tube is still more or less the same. Figure 4.7 shows the basic structure and the main elements of a photomultiplier based on Philips 56AVP, which is the world's first fast photomultiplier fabricated by Philips in 1956.

Most photomultipliers consist of four main components: a photocathode which converts the incident photons into electrons; an electron-optical system which focuses and accelerate the electrons; an electron multiplier which is composed of several stages of dynodes or secondary-emission electrodes; and an anode which collects the electrons amplified in the multiplier and output the electrical signal [Photonis, 2002]. A typical modern PMT has a

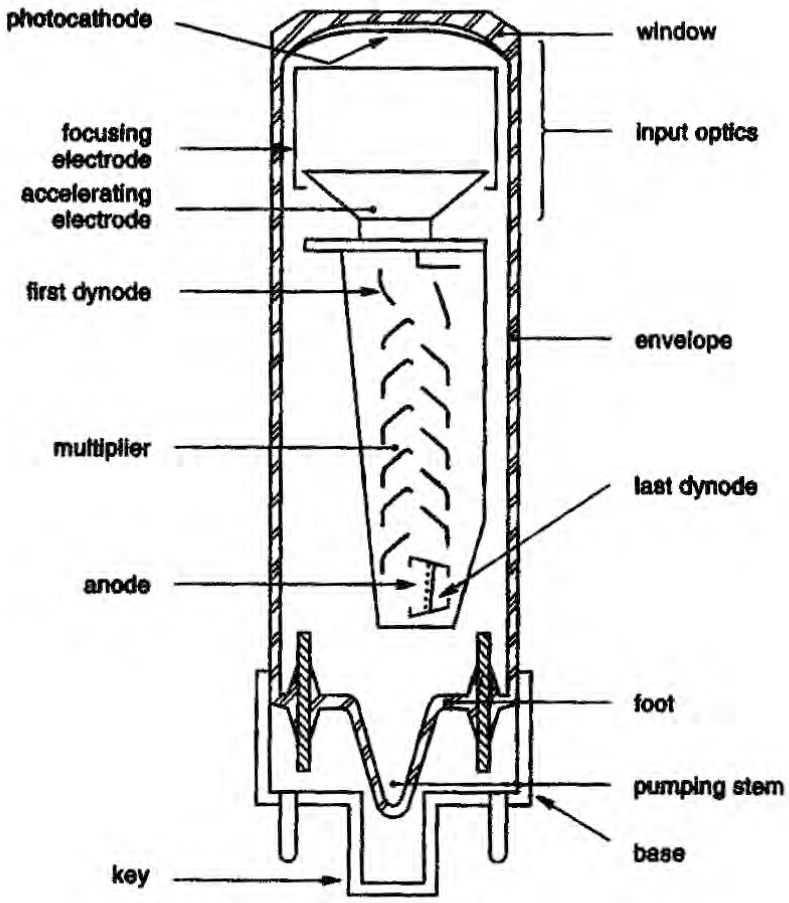


Figure 4.7: Basic structure and main elements of a photomultiplier based on Philips 56AVP. The figure is taken from[Photonis, 2002].

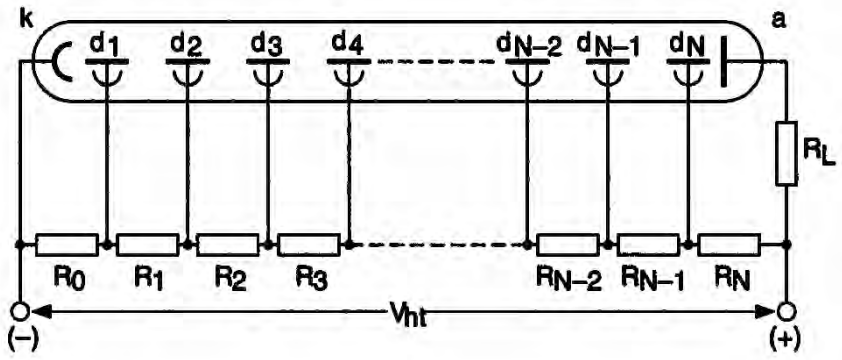


Figure 4.8: Basic structure of the high voltage divider or the base of a photomultiplier. The figure is taken from [Photonis, 2002].

gain larger than 10^6 and more than ten stages of multiplier. The acceleration and amplification of the secondary electrons mainly depends on the electric fields applied between the electrodes. It usually requires a gradient potential which is obtained from a resistive voltage divider across the electrodes of the PMT from the cathode to the anode. Increasing of the potential leads to higher gain of the PMT. This part of external circuits is known as the *"base"* of a PMT. Figure 4.8 shows the basic circuits of the base. The components used in a real base, such as capacitors, inductors, diodes and etc. are not shown in this figure.

4.3.2 Common photomultiplier models

Before any experiment and the design, this device must be carefully modelized. The purpose of the modelization is to find out the relation between the input signal and the output or the response of the system. Usually, in engineering and mechanical area, one can use a mathematical representation to fit or describe this relation or the response of a black box system. It is also well know as the *"transfer function"* or *"system function"*. Time is always a very important parameter in this description, since many of them should be used in time domain or frequency domain. Besides, as a mathematical function, it is a physical model in nature that can be exploited in experimental data analyzing and event reconstruction.

There are many ways to set up a model for PMT, but all of them start from the electric charge which is the basis of describing all electric phenomena. In the circuit theory, the separation of charge creates the electric force (i.e. voltage) and the movement of charge creates the electric fluid (i.e current) [Nilsson and Riedel, 2011]. As an electric device, from the operating principle of the photomultiplier, the tube is equivalent to a charge amplifier or a current source. Therefore, in the simulation, any PMT based detector can be replaced by a current source and its voltage-divider which is shown in figure 4.8. It is easy to say that the current source is the key point of the PMT modelization. Specifically, it is the shape of the signal that determines the charge of the signal. There are four common PMT models which are frequently used and listed below.

Trapezoid model

The simplest way to model a PMT is to treat its output as a trapezoid. Especially the isosceles trapezoid is the most commonly used model of PMT in computer simulation and real experiments. The algorithm and the function can be easily deployed in any program or even in a signal generator. Figure 4.9 shows an example of this output. It is a model

Table 4.2: PMT parameters be used by models in this section

Parameter	Value
Input signal	2.5 p.e.
Gain	10^6
Anode pulse rise time	3 ns
Electron transit time	20 ns
Transit time spread	3.3 ns

for a special PMT with the parameters that are shown in table 4.2. These parameters will be continuously used in the following models of this section. Due to the polarity of the electron, the output is negative.

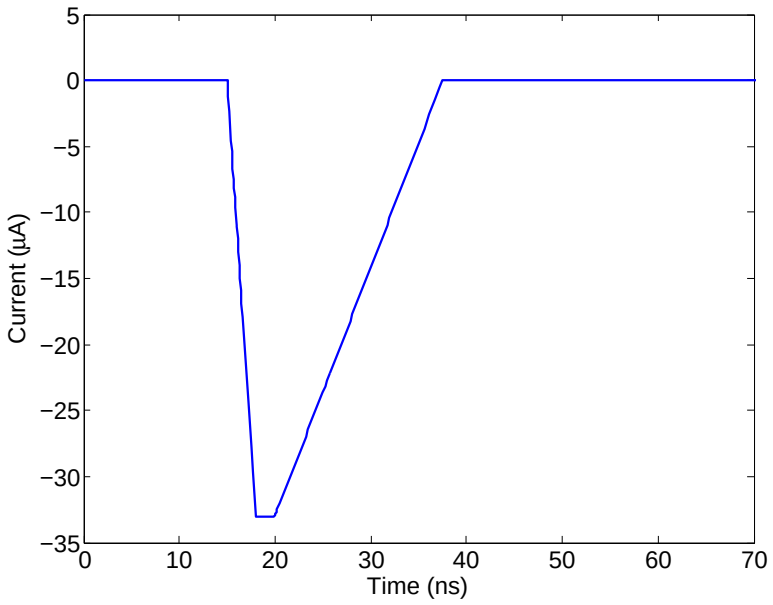


Figure 4.9: Output of trapezoid model for PMT (See table 4.2 and text for parameters.)

To create a similar signal as shown in table 4.2, a inverted trapezoid current output is used with parameters (amplitude: 33 μA; delay: 15 ns; rise time: 3 ns; fall time: 17.5 ns; on time: 2 ns). The area occupied by this trapezoid is the charge of the signal that equals to $\sim$ 404 fC or 2.5 p.e., when the gain of the PMT is 10^6.

Wave transformer model

Based on the circuit theory, the integrated circuit and the differential circuit can be used as the wave transformer to change the shape of a signal. The first order high-pass and low-pass RC filters are the simplest versions for these transformers that can be used in the PMT modelization. Figure 4.10 is a solution for the special PMT we want to model. By using a step response voltage source as the input, two high-pass RC filters with different time constants ($\tau = \mathrm{RC}$) as the transformers and a voltage-controlled current source (Gain = 1) as the output, the PMT model is settled. Carefully selecting the values of the components, the corresponding waveform is obtained and shown in figure 4.11. All the parameters of theses components are listed in the figure 4.10. The output of the trapezoid model is plotted to make a comparison. The charge of the signal is about $\sim$ 405 fC, slightly larger than the ideal value. This sort of model was used by Fermilab [Stancu et al., 2003].

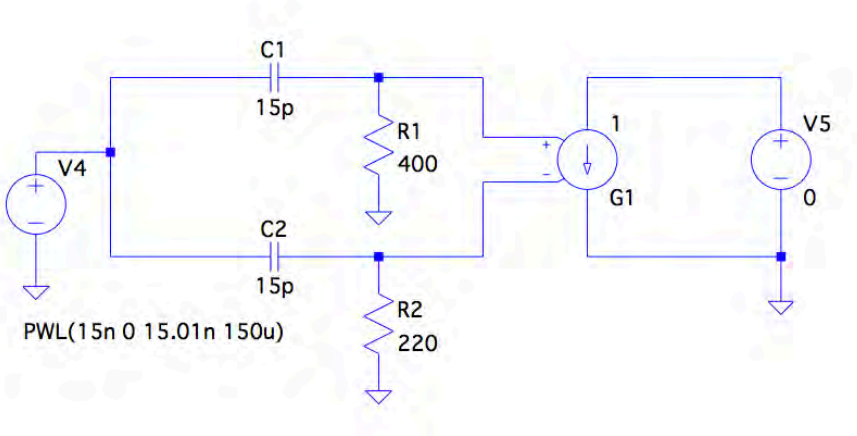


Figure 4.10: Schematic of a wave transformer model for PMT

Mathematical model

The mathematical expression is another common way in the device modelization. The response of the PMT can also be represented by some special functions. In fact, the fast rising edge and the long tail of the PMT output signal make it perfectly fit to the Landau distribution. Without considering the difficulties of the implementation in some simulation programs and the use of the model, an approximate Landau function as the Moyal function

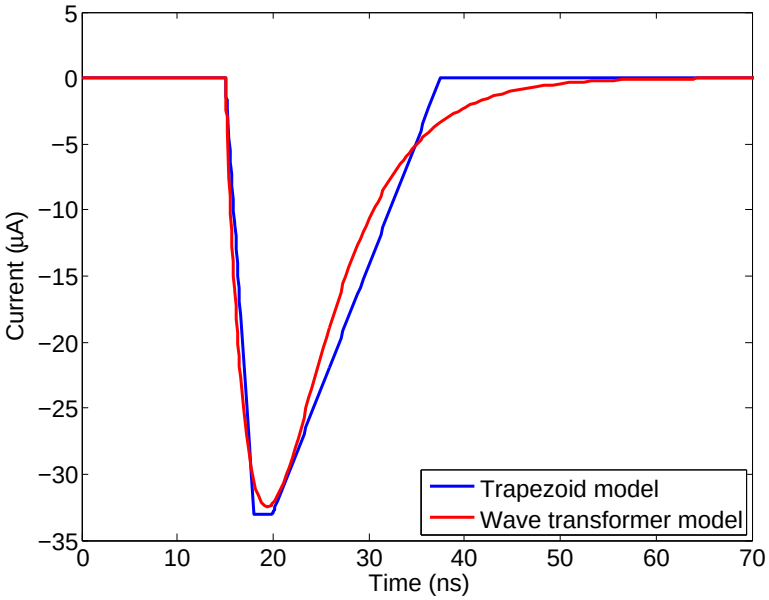


Figure 4.11: Output of wave transformer model

[Bäcker, 2005], is always the best solution of the PMT modelization. The Moyal function is given by

$$i_{Moyal}(t) = -A_{Moyal}\sqrt{\frac{exp(-\lambda_{Moyal}(t-t_0) - exp(-\lambda_{Moyal}(t-t_0)))}{2\pi}} \tag{4.9}$$

In this equation, the shape of the output of a PMT is decided by two free parameters which are A_{Moyal} and λ_{Moyal}. Moreover, there are some simplified solutions, if the simulation program does not support the arbitrary input function. The damped sine function is a substitution of Landau function that can be given by

$$i_{stim}(t) = \varepsilon(t) \cdot (-Ae^{-(t-t_0)\lambda} sin(2\pi f(t-t_0))) \tag{4.10}$$

Where the amplitude of the output is controlled by A and the shape of the signal is determined by λ, f and t_0. The $\varepsilon(t)$ is a unit step response, and can be described by

$$\varepsilon(t) = \begin{cases} 0, & \text{for } t < 0; \quad (4.11a) \\ 1, & \text{for } t \geq 0. \quad (4.11b) \end{cases}$$

This equation is adapted for the design of the FADC-based data acquisition system for KASCADE-Grande experiment [Bäcker, 2005]. However due to its four free parameters, this equation is quite difficult to manipulate. Figure 4.12 presents the outputs of three different models: the wave transformer model, approximated Landau function and damped sine function. The very similar outputs are achieved after a time-consuming parameters selection. The charges of the signal are ~ 400 fC for the Landau function and ~ 404 fC for the damped sine function.

There is a noticeable difference among these outputs in figure 4.12, where both damped sine function and wave transformer model give the outputs with a sharp transition at about 15 ns, that is owing to the contribution of the step response. It is the common drawback for the most existing PMT models except Landau function.

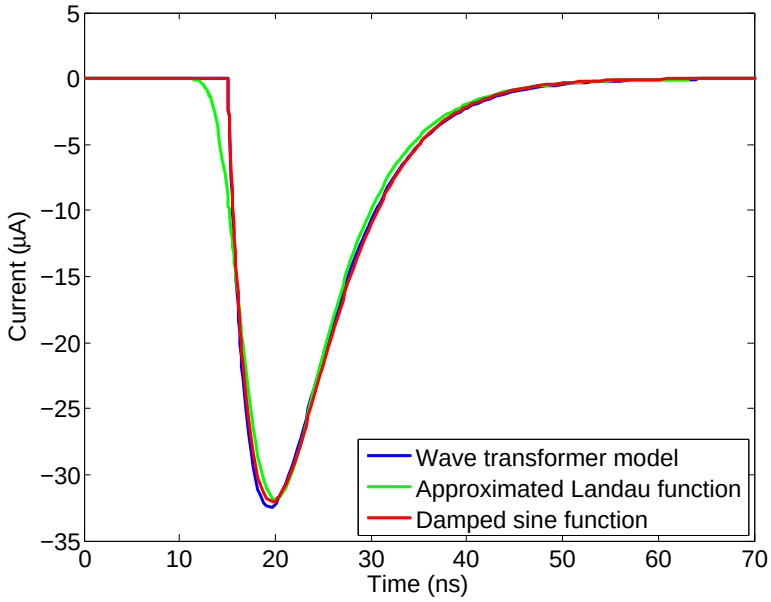


Figure 4.12: Output of the mathematical models. The Moyal function and the damped sine function are both drawn in the figure to compare with the output of the wave transformer model. The blue line represents the output of the wave transformer model. The red and green ones are the approximated Landau function or Moyal function and the damped sine function respectively.

Empirical model

The output can be also represented by an empirical function which is introduce by Philips Composants who was the former company of Photonis [Philips Composants, 1990]. It is given by [Photonis, 2002]

$$R_\delta(t) = \varepsilon(t) \cdot \frac{\sqrt{m+1}}{m!\sigma_R} \left(\frac{\sqrt{m+1}}{\sigma_R} t \right)^m exp \left(-\frac{\sqrt{m+1}}{\sigma_R} t \right) \tag{4.12}$$

Where $R_\delta(t)$ is the output response and depends on time when the input signal is a δ function. The shape of the output is related to two parameters: m and σ_R. It has a following property

$$\int_0^\infty R_\delta(t) = 1 \tag{4.13}$$

Since the integral of this equation is one, it can be use to simulate the output a PMT with a proper gain. However, the value of the parameter m is usually very large and could reach 50 in some cases [Cabot et al., 1998]. This greatly increases the order of function and the difficulty of the solution. Hence, the more popular deformations of this formula are the ones whit m = 1 [Guerra and Kontaxakis, 2006; Monzo et al., 2008], which is represented by

$$h(t) = \varepsilon(t) \cdot \frac{G}{t_p^2}(t - t_d) exp \left(-\frac{t - t_d}{t_p} \right) \tag{4.14}$$

Where G is the gain of the PMT, t_d is the transit time of the tube and

$$t_p^2 = t_r^2 + t_{jitter}^2 \tag{4.15}$$

Figure 4.13 shows the result of the equation 4.14 and 4.15. The parameters t_d, t_r and t_{jitter} are all taken from table 4.2. The approximated Landau function described above is also plotted in the same figure as a reference. The charge of the signal is $\sim$ 400 fC which is as accurate as the Landau distribution, but more easier to manipulate than the mathematical models. However, the sharp transition still exists that limits the application of this model in the design of electronics.

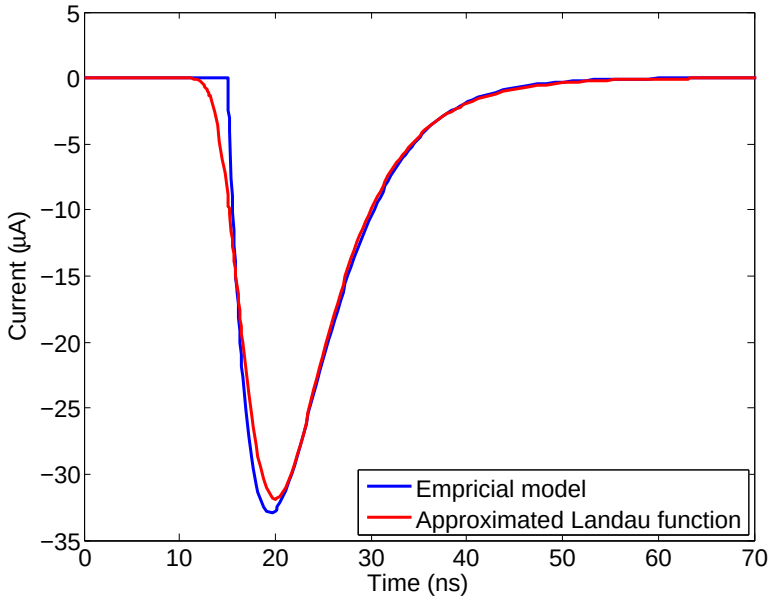


Figure 4.13: Output of the empirical function. The output of approximated Landau function is also shown in the figure as a reference. The red and blue lines are represent the empirical function and the approximated Landau function separately.

Summary of the existing PMT models

Figure 4.14 shows the outputs of all five different PMT models in time domain. It is clear that by carefully selecting the parameters for each model, the accurate output of PMT can be obtained. They all generate similar waveforms and charges and also can be easily integrated into physical or circuit simulation programs. However, due to their own properties, each of them has their advantages and disadvantages.

Trapezoid model: It is the simplest and the most widely used one among these models. This model can be easily implemented in any simulation program. However, the output of it is too rough to accurately characterize the PMT output and normally is used in the preliminary simulation and the instrumental test.

Wave transformer model: This model is circuit structure model which is usually exploited in electric circuit simulation. It is able to provide a good enough approximation of the PMT output signal but its circuit structure limits its application in physical simulation. The model is also easy to use but the selection of the parameters is a time-consuming job, since they are not related to the manual of the PMT. The efficiency of this model mostly depends on the user's experience.

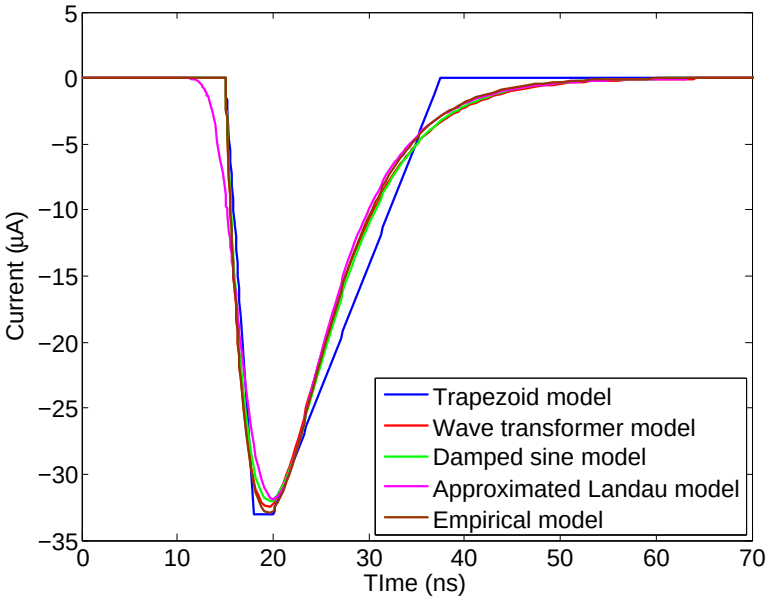


Figure 4.14: Outputs of all the PMT models in time domain. (See legend for the description of the lines)

Mathematical model: These models are usually accurate and efficient. For example, the Landau distribution is always the best way to describe the behavior of a PMT. However, they are only mathematical models. It is very difficult to link the parameters in the formula with the specifications of the PMT. The number of the parameters is another problem of these models. This makes that these models are not easy to play with, especially when one needs to study a complex detector system with several PMTs. The experience of the users is very important as well.

Empirical model: In fact, the empirical model is one sort of mathematical model. Some of them are really hard to manipulate or solve, but the simplified version, as the equation 4.14 and 4.15, is the second best choice in the detector design. It has limited number of parameters, and most of the parameters come from the manual of the PMT. It gives physical meaning to the function and makes it understandable.

At the same time, all these models except the Landau distribution share the same drawback. As shown in figure 4.14, at around 15 ns, the models have sudden transitions due to the step responses in the functions. There are no such signals in the real world. Electronic designer suffers a lot from these artificial signals when they are used in circuit simulation. By using the Fourier transform (FT) or the fast Fourier transform (FFT), these nonperiodic signals can be converted from time domain to frequency domain to obtain their

fundamental component and the harmonic components. For more information, one can read [Nilsson and Riedel, 2011].

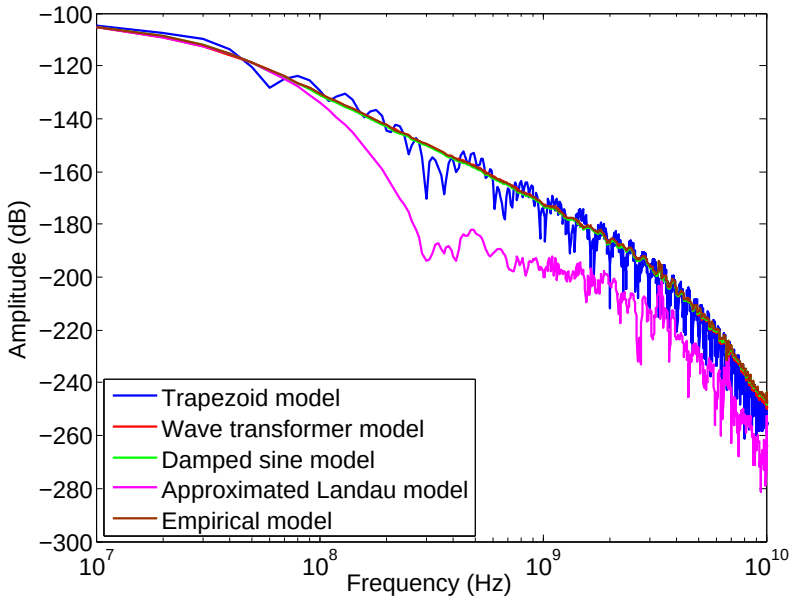


Figure 4.15: Outputs of all the PMT models in frequency domain. (See legend for the description of the lines)

Figure 4.15 gives the frequency-domain representations of these models. In this figure, the wave transformer model, the damped sine model and the empirical model show almost the same behavior owing to their similar outputs in time domain. The output of the trapezoid model is close to these three models but contains more harmonic components in the spectrum. Different from other models, the approximated Landau model presents a real-signal behavior. Compared to it, the other models all contain more high-frequency components in the whole spectrum. This difference is due to the sharp transitions in the outputs of these models.

Generally speaking, the sudden transitions in the output or the high-frequency components in the spectrum will not affect the accuracy of the physical simulation and data reconstruction but affects the design of the filters in the front-end electronics.

Thus, considering all these existing problems, a new simple and accurate PMT model is needed to analyze, verify and evaluate our new electronic design. It will be discussed in the next section.

4.3.3 New PMT model

In order to complement the imperfections of the existing PMT models, a new model is proposed. The purpose of the model is to achieve an accurate, simple and understandable solution for the PMT modelization that can be easily integrated in any simulation program. The function of the proposed model is given by

$$i_{PMT}(t) = n_{photon} \cdot QE \cdot CE \cdot G_{PMT} \cdot e \cdot h(t) \tag{4.16}$$

Where the $i_{PMT}(t)$ is the response of the PMT related to time. n_{photo} is the number of the incident photons. QE and CE represent the quantum efficiency and collective efficiency of the tube respectively. G_{PMT} is the gain and e is the electric charge which equals to 1.6022×10^{-19} C. Without considering the photoelectric effect and the collective efficiency, $n_{photon} \cdot QE \cdot CE$ can be replaced by $n_{photoelectron}$ directly, it also can be written as

$$i_{PMT}(t) = n_{photoelectron} \cdot G_{PMT} \cdot e \cdot h(t) \tag{4.17}$$

Where $h(t)$ describes the shape of the output signal and is given by

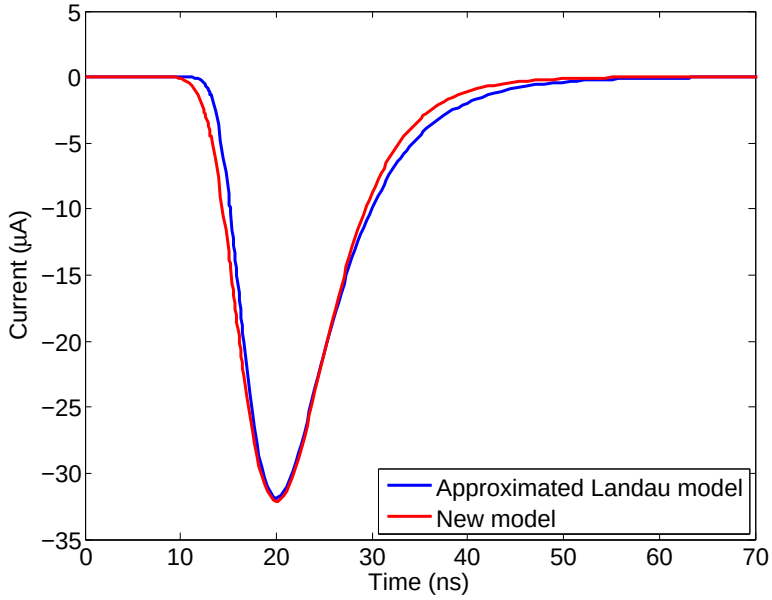
$$h(t) = \frac{1}{t_p} exp\left(-\frac{(t-t_t)}{t_p} - exp\left(-\frac{(t-t_t)}{t_p}\right)\right) \tag{4.18}$$

Where t_t is the electron transit time of the tube and t_p is the time characteristic of the tube that is given by

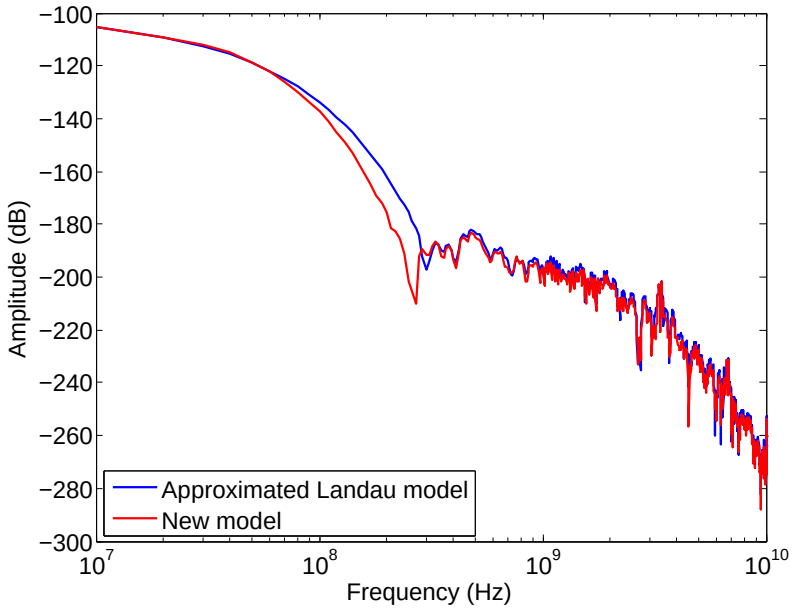
$$t_p^2 = t_r^2 + t_j^2 + t_l^2 \tag{4.19}$$

Where t_r, t_j and t_l are the rise time of the anode output, the spread of the transit time and the time spread of the input signal, respectively. All these parameters can be found in the manual of the tube and from experimental data. This makes that the proposed model has physical meaning and can be easily understood and manipulated.

With equations 4.16 or 4.17, 4.18 and 4.19, the output of the PMT is determined. Figure 4.16 gives an example of the result of the modelization of a special PMT which parameters are shown in table 4.2. Outputs of new PMT model in time domain and frequency domain are shown in figure 4.16a and figure 4.16b separately. It is obvious that this new model provides an accurate and efficient way to describe the behavior of a PMT in both time and frequency domain. Compared to the approximated Landau model, this



(a) Outputs of new PMT model in time domain



(b) Outputs of new PMT model in frequency domain

Figure 4.16: Outputs of new PMT model in time domain and frequency domain. The output of the approximated Landau model is also plotted for comparison.

one is comprehensible and convenient. Furthermore, due to the following property of the function $h(t)$

$$\int_0^\infty h(t) = 1 \tag{4.20}$$

This model also precisely presents the charge of the output signal. As shown in figure 4.16a, the charge measurement of the signal exactly equals to 400 fC which is 2.5 p.e. It can be perfectly integrated into a physical simulation program as well as the data reconstruction program.

However, if our purpose is to guide the circuit design, the complete PMT model is obtained by adding additional components as shown in figure 4.17. In the figure, B1 is an arbitrary current source for PMT model which is used to implement above equations from 4.16 to 4.17. C1 is the capacitance from anode to all electrodes. This value can be retrieved from device manual as well. B2 is a noise source to generate required background noise.

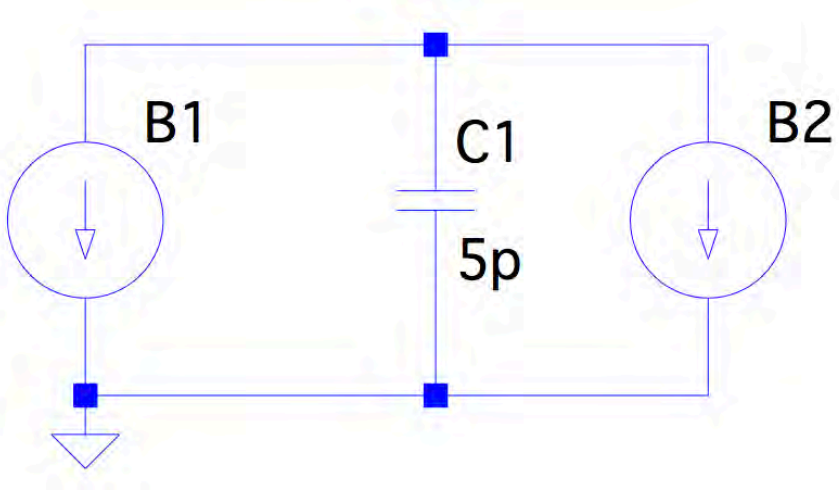
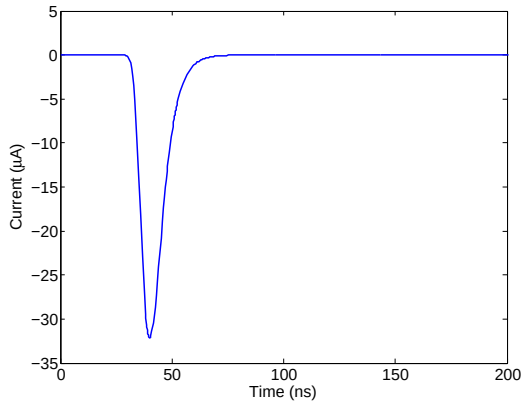
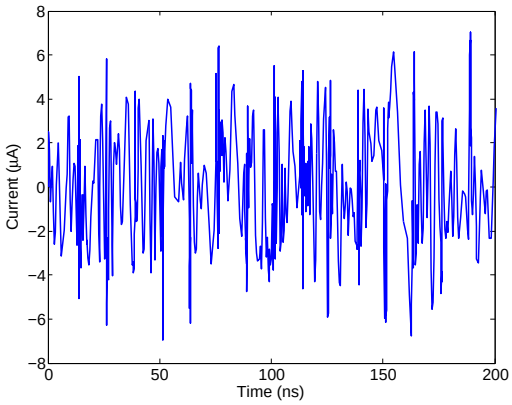


Figure 4.17: Complete PMT model for electric circuit simulation

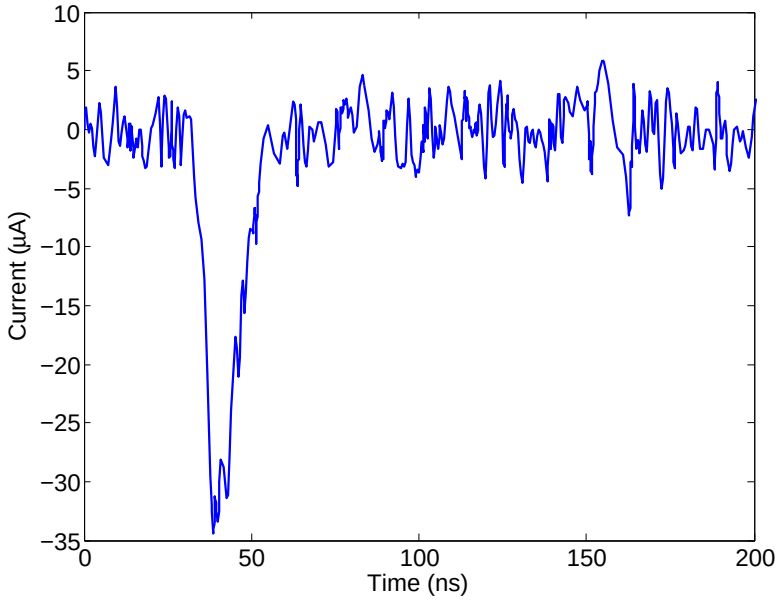
The output response of this complete PMT model is shown in figure 4.18. In this figure, the current components of the PMT model and background noise are also plotted respectively in figure 4.18a and 4.18b. The real output of the whole model is shown in figure 4.18c. The parameters of the tube still follow the table 4.2. It is comparable to other models except the noise components. Some examples are also provided to demonstrate the possibilities and the advantages of this model (See Appendix A).



(a) Current component of PMT model



(b) Current component of background noise



(c) Output of the complete PMT model

Figure 4.18: Output of complete PMT model for electric circuit simulation. The current components of PMT model and background noise are also plotted respectively in this figure

Chapter 5

Modelization of the front-end electronics

In last chapter, we presented a new photomultiplier model which can be used to bridge the cosmic ray and electronic simulations. With it, one can easily simulate any required PMT responses. The related examples are shown in Appendix A. It also established a solid fundament for us to study the behavior and response of the front-end electronics for WFCTA.

As an extreme sensitive photon-to-electron converter, photomultiplier has an ability to convert incident light into electric charges and amplify them to a detectable level. For example, typically, the quantum efficiency and collection efficiency of a tube are about 25 % and 80 %, respectively. It suggests that about 5 incident photons could generate a single photoelectron in the photoelectric conversion. Therefore, even with a gain of 10^6, the tube is only able to produce a output signal with a charge of 160 fC. Considering the distribution of the output current, the maximum output of a single photoelectron response of a tube is usually tens of μA. They are very weak signals for most electronics. On the other hand, sometimes, the input can be very large and reach thousands of photons as well. This rises the output of a tube to tens of mA. The demonstrations can be found in figures A.1 and A.2. Depending on the application, the output of a PMT may need to cover a dynamic range more than 3 orders of magnitude. It is not only a challenge for PMTs but also for the front-end electronics.

Generally speaking, the purpose of a front-end electronic system is to process the analogue input signal, convert it into the digital form and transfer it to another digital devices for the next step processing. The input signals are amplified, attenuated, filtered, digitized and finally transferred, collected and stored in a host computer. This circuit is the most important link in the chain of a detector system. The performance of the whole

system mostly depends on the performance of the front-end electronics. The electronics should be carefully studied and simulated before its implementation.

There are two types of designs that will be studied and discussed in this chapter, which are the design based on classical electronics and the one based on application-specific integrated circuit (ASIC). The advantages and disadvantages of these designs will be discovered through the electric simulations. All the ideal designs and behavior model in this chapter are evaluated and simulated with LTspice IV, which is a high performance SPICE (Simulation Program with Integrated Circuit Emphasis) simulator, schematic capture and waveform viewer with enhancements and models, provided by Linear Technology [Linear Technology, 2015]. Compared with other commercial SPICE simulators as HSPICE from Synopsys or Spectre from Cadence, LTspice is a well maintained fully-free software. It is accurate enough for most simulations, in this case the scale of the circuits is small and most of them are ideal and behavior models.

5.1 Design based on the classical electronics

Based on their purposes, most signal processing circuits or front-end electronics including classical ones can be divided into three main parts: analogue signal processing, digitalization and data transferring. Here we only discuss the first two parts. The data transferring will be introduced in Chapter 7.

Following this signal flow, the output signals of the PMT should be preprocessed and amplified before they are passed to the analog-to-digital converter (ADC). Moreover, due to the interferences of the noise, useful components of the signal also must be extracted out from the background in order to keep the performance and the accuracy. In this progress, at least, three main goals should be achieved to fulfill the requirements of the ADC. They are polarity adjusting, amplitude adjusting and bandwidth adjusting. This part of circuits is usually implemented with high order active filters.

Active filters can be classified into many types by different methods. For example, by its frequency response, it can be a low-pass filter or a high-pass filter; by its unique characteristics in response, it can be a Butterworth filter or a Bessel filter; by its circuit architecture; it can be a Sallen-Key type or a Multiple-Feedback (MFB) type [Zverev, 2005; Nilsson and Riedel, 2011]. Since there is no such ideal filter which could completely suppress the signals in its stopband and pass all signals in its passband, for the real filters, many trade-offs have to be made to get the best performance for a specific application.

The Bessel filter becomes the best choice of the preamplifier for a PMT based detector system, such as LHAASO-WFCTA and AUGER-FD, not only due to its linear phase response and excellent transient response of a pulse signal, but also because its transfer function has the same coefficients as Bessel polynomial which simplifies the design of the filter. The Bessel filters were adapted in both electronics of the WFCTA prototype [Zhang, 2010] and the AUGER-FD[Pierre Auger Collaboration, 2010]. As a result, the 4th order Bessel filter is used to evaluate the performance of the classical electronics in this chapter.

As the signal preprocessing circuit of an ADC, the design of the active filter relates to the characteristics of the input signal and the choice of the converter. In order to simplify the design, several definitions and assumptions are made and listed below:

a) The input signal of the front-end electronics is the anode output signal of the PMT. It suggests that the polarity of the signal is negative without considering the dynode readout. Signal inverting in the filter is necessary.

b) The model of the PMT is Hamamatsu R1924A in this section. The specification of this tube can be found in table A.1 in the Appendix A.

c) There are two types of PMT responses involved in (i.e., Cherenkov and fluorescence). It suggests that there should be at least two active filters with different cut-off frequencies for different responses.

d) Each event should be sampled at least 6 times to maintain the accuracy of the charge measurement.

e) For the Cherenkov mode, the specifications of the WFCTA prototype is taken as a reference [Zhang, 2010]. It suggests that the speed of the ADC should be faster than 40 MSPS (mega sample per second), and the cut-off frequency of the filter should be lower than 7.5 MHz.

f) The duration of the Cherenkov signal is 4 ns.

g) For the fluorescence mode, the specifications of AUGER FD is taken as a reference [Pierre Auger Collaboration, 2010]. It suggests that the speed of the ADC should be faster than 10 MSPS, and the cut-off frequency of the filter should be lower than 3.4 MHz.

h) The number of bit (NOB) of the ADC should be higher than 10 bits.

i) The full scale voltage of the ADC is 2 V.

5.1.1 Design for the Cherenkov mode

According to the definitions listed above, a 4th-order Bessel active filter with a cut-off frequency of 7.2 MHz and a gain of 12 dB (3.98×) is proposed to achieve this goal. The behavior of this filter can be described by a s-domain transfer function, which is given by

$$H(s) = \frac{8.75536e31}{s^4 + 2.14005e8s^3 + 2.06092e16s^2 + 1.02911e24s + 2.20235e31} \tag{5.1}$$

This formula suggests that the Bessel filter is an all pole filter and all these coefficients can be determined with a filter table in the design manual. Fortunately, the voltage-controlled voltage source (VCVS) in LTspice directly supports s-domain Laplace transform to define its behavior. This means that the equation 5.1 can be adapted into the simulation without any change. Consequently, a very simple behavior model of any active filter can be easily achieved with a single circuit element.

This circuit architecture can be also derived from this transfer function. In the real filter design, the high order filter usually is broken into several complex-conjugate-pole pairs which can be implemented by different circuit topologies, such as Sallen-Key or MFB. In this case, the filter consists of two 2nd-order filters, which are a 2nd-order MFB filter as the first stage and a 2nd-order Sallen-Key filter as the second stage.

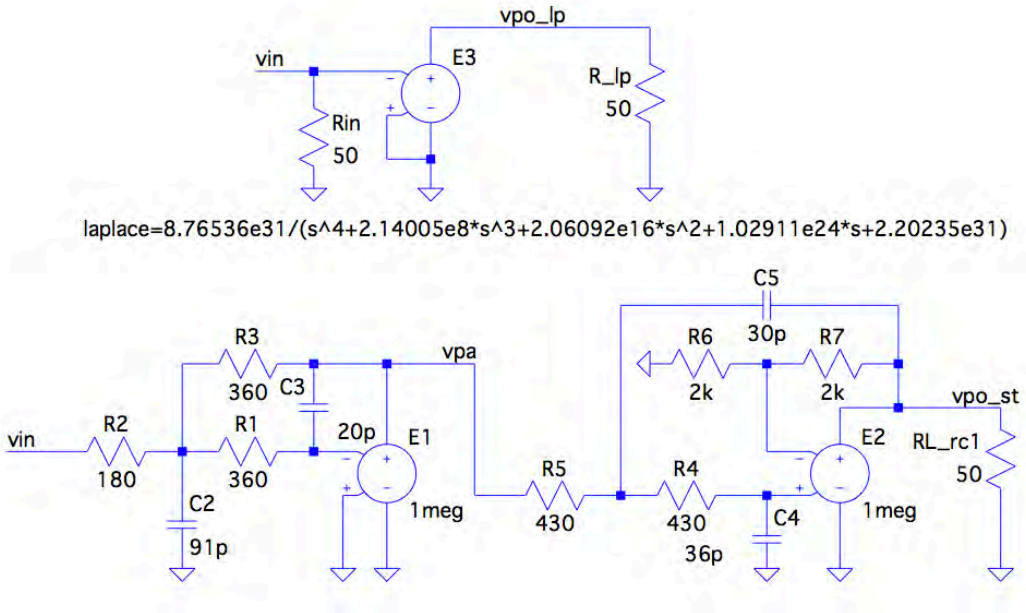


Figure 5.1: Schematic of transfer function model of the active filter and its ideal circuit implementation. The upper one is the transfer function model and the lower one is its ideal circuit implementation.

Both behavior models are shown in figure 5.1. The upper one is the mathematical behavior model which describes the active filter with its transfer function. The lower one is the ideal circuit implementation of the filter. In the schematic, the operational amplifier normally used in real filter is replaced by a VCVS with a gain of 10^6. The frequency responses of both models are shown in figure 5.2. It is clear that both responses are almost the same. The slight difference is due to the limited values of the real components.

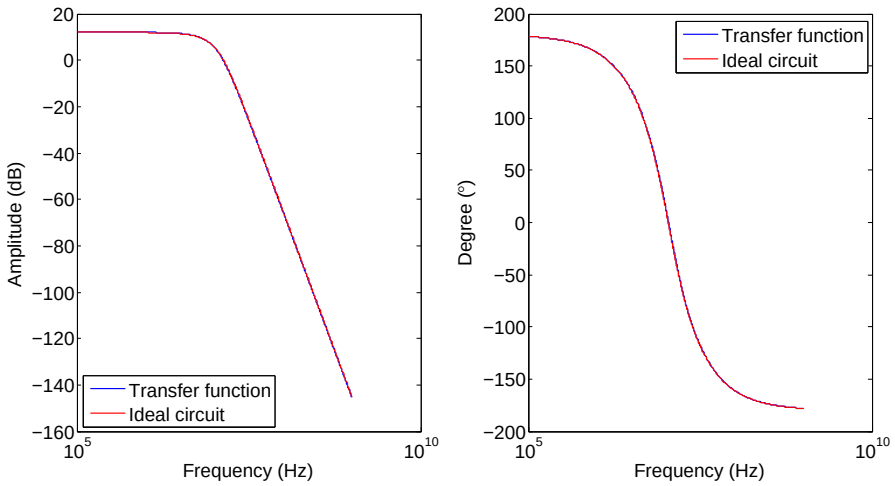


Figure 5.2: Frequency responses for the transfer function and the ideal circuit of the filter

Figure 5.3 presents the transient time responses of both models. The input signal is a single photoelectron response of the PMT with a FWHM of about 10 ns. According to the simulation results, the input charge is about 160.26 fC. The outputs of transfer function and ideal circuit are 641.03 fC and 640.80 fC, respectively. Therefore, the actual gain of active filter is about 3.99 or 12.02 dB, which is slightly larger than the expected value (12 dB or 3.98). Moreover, the signal is extended to more than 150 ns with counting the overshoot. It meets our requirement about the number of samples when a 40 MSPS ADC is used. The block diagram of this design is shown in figure 5.4.

The analogue output of the active filter will be digitalized following the signal flow. In this step, three ideal ADCs (i.e., 10-bit, 12-bit and 14-bit) are modeled to evaluate the performance of the ADCs. Three ideal digital-to-analog converters (DACs) are also modeled to convert the digital signal back to analog. The detailed modelization can be found in [Baker, 2009]. With the help of the DAC, the digital codes from ADC are reconstructed to calculate the charge of the output. Figure 5.5 shows an example of a full signal processing progress when a 14-bit ADC adapted in. In the figure, The blue, red and green

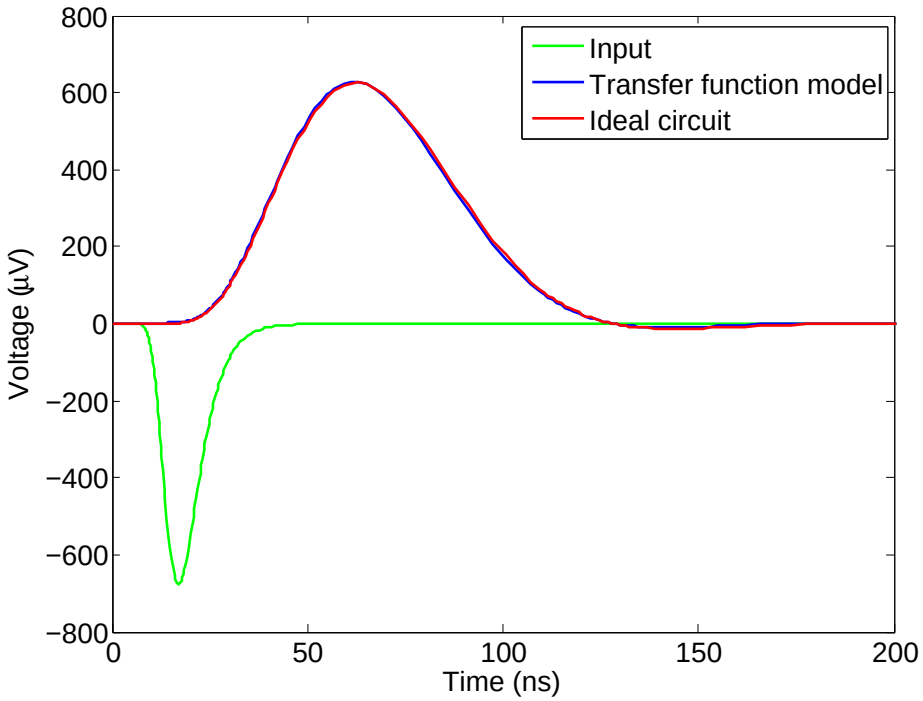


Figure 5.3: Transient time responses for the transfer function and the ideal circuit of the filter

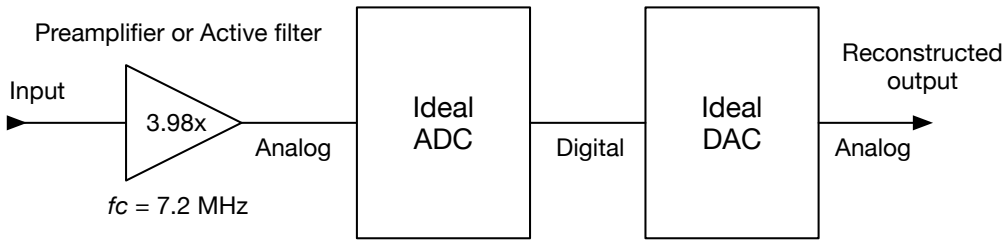


Figure 5.4: Block diagram of the design based on classical electronics

line represents the input, the output of the filter and the reconstructed output of front-end electronics, respectively. The input charge is about 320.36 fC (2 p.e.) and the charge of the reconstructed output is 322.05 fC. There is only 0.5 % deviation between these two values. It suggests that the front-end electronics based on this design is able to accurately measure the charge of the signal. In addition, it could easily measure large signals up to 560 pC. This corresponds to about 3,500 p.e. when the gain of the PMT is 10^6.

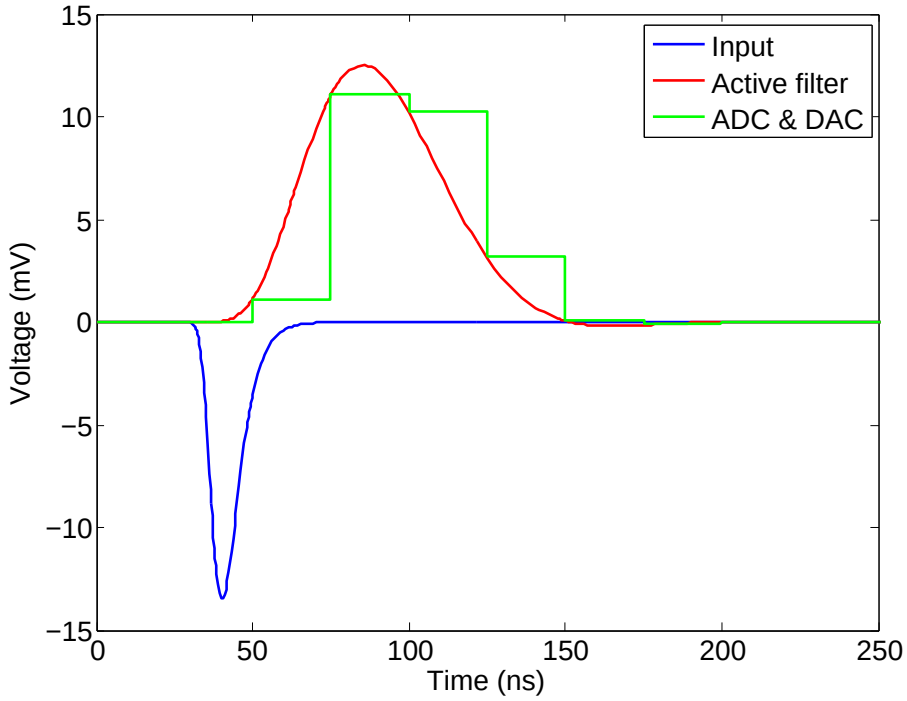


Figure 5.5: Example of the a full Cherenkov signal processing. The blue, red and green line represents the input, the output of the filter and the reconstructed output of front-end electronics respectively.

Due to the difference of the minimum charge which can be measured by the different ADCs, the accuracy of the charge measurements is limited by the resolution of the ADC. Table 5.1 shows the number of bits, the sampling rate and the minimum charge can be measured by different ADCs. The minimum measurable charge decreases with the increasing of the number of bits and the sampling rate of an ADC.

Figure 5.6 shows a more detailed simulation result. In the figure, the different deviations of the charge measurement of 10-bit, 12-bit and 14-bit ADC are compared. In this simulation, the gain of the PMT is set to 10^6. Two basic principles can be retrieved from this plot. The first is that, with a single stage preamplifier or active filter, the higher the

Table 5.1: Minimum charge can be measured by different ADCs

NOB	40 MSPS	80 MSPS	1 GSPS
10-bit	$\sim$ 245.4 fC	$\sim$ 122.7 fC	$\sim$ 9.8 fC
12-bit	$\sim$ 61.3 fC	$\sim$ 30.7 fC	$\sim$ 2.5 fC
14-bit	$\sim$ 15.3 fC	$\sim$ 7.7 fC	$\sim$ 0.6 fC

NOB of a ADC, the more accurate the charge measurement. In addition, it is common to every ADC that a larger input leads to a smaller the deviation. Furthermore, the effective number of bits (ENOB) of an ADC is usually one to two bits smaller than this ideal value. It will aggravate this situation in a real front-end electronic system. In the figure, the 14-bit ADC is the best candidate. It maintains a good linearity and keeps the fluctuations small. The only drawback is its price.

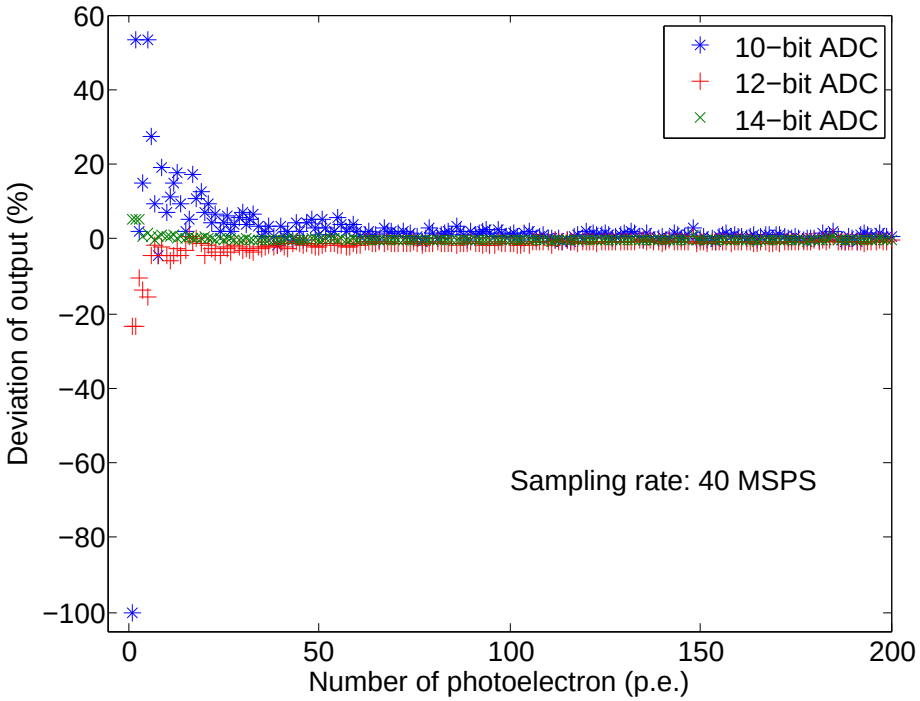


Figure 5.6: Deviations of the charge measurement of different number of bit of ADCs. The blue asterisk, red plus and green cross represent the deviations of 10-bit, 12-bit and 14-bit ADC separately.

The sampling rate of the ADC is another point that affects the accuracy of the charge measurement. Table 5.2 lists the deviations of the charge measurement of different ADCs

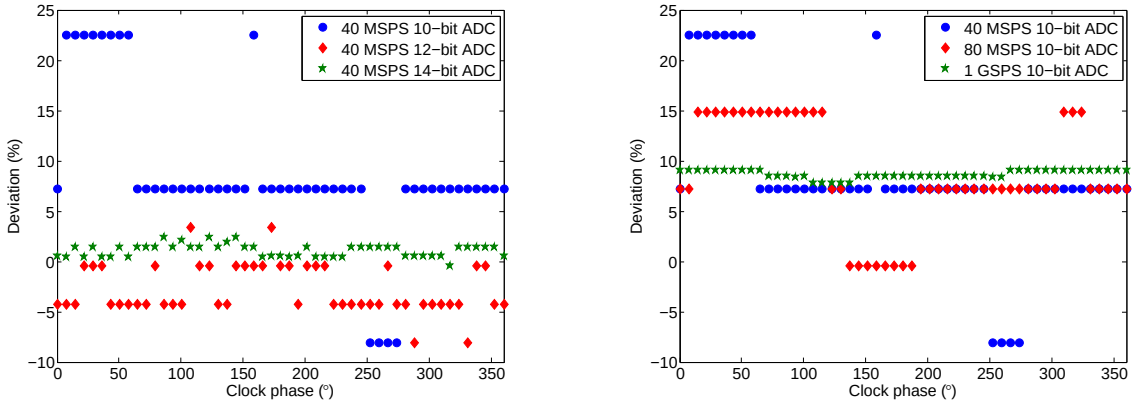
with considering both number of bits and the sample rate. However, in a real case, the accuracy of the measurement cannot be significantly improved by increasing the sampling rate as shown in the table. For the signals with a particular duration or frequency, the measurements are more sensitive to the least significant bit (LSB) than to the sampling rate.

Table 5.2: Deviations of the charge measurement of different ADCs with considering both the number of bits and the sampling rate

	40 MSPS			80 MSPS			1 GSPS		
Input (p.e.)	10-bit (%)	12-bit (%)	14-bit (%)	10-bit (%)	12-bit (%)	14-bit (%)	10-bit (%)	12-bit (%)	14-bit (%)
1	-100.00	-23.46	5.24	-23.46	-42.60	10.02	-2.21	-28.19	6.57
2	53.09	-23.46	5.25	91.37	-23.45	2.86	58.89	-19.79	3.70
3	2.07	-10.69	5.26	27.60	-4.30	3.67	28.34	-9.85	3.39
4	14.84	-13.87	0.49	14.85	-13.87	2.88	6.95	-6.80	2.94
5	53.13	-15.78	1.45	37.82	-11.95	1.45	24.68	-6.80	2.52
6	27.61	-4.29	0.50	14.86	-7.47	2.10	17.13	-6.29	1.98
7	9.39	-1.55	-0.19	-1.55	-1.55	1.19	8.26	-3.97	1.76
8	-4.29	-4.29	0.49	5.29	-1.89	1.70	16.11	-3.75	1.41
9	19.10	-2.17	1.02	19.10	-2.17	1.02	14.07	-3.75	1.04
10	7.19	-4.29	0.49	7.19	-2.38	0.49	8.78	-3.29	0.91
11	11.36	-6.04	0.71	11.37	-4.29	0.49	12.22	-2.22	0.66
12	14.84	-4.30	1.29	14.85	-2.70	0.89	11.01	-2.36	0.64
13	17.79	-2.83	0.12	11.90	-2.82	0.86	7.17	-2.35	0.59
14	9.38	-4.30	0.49	14.85	-2.92	0.84	9.55	-1.58	0.50
15	2.08	-3.02	0.17	7.20	-1.74	0.81	9.17	-2.33	0.39
16	5.27	0.49	0.49	10.06	-3.10	0.79	6.55	-2.71	0.39
17	17.09	-0.92	0.21	17.10	-0.92	0.49	7.47	-2.77	0.37
18	10.59	-0.04	-0.04	10.60	-0.04	0.76	7.95	-2.49	0.37
19	12.83	-1.28	0.24	8.81	-2.28	0.50	6.45	-2.72	0.42
20	7.19	-4.30	0.49	7.20	-3.33	0.97	6.93	-2.77	0.36

Moreover, this type of classical electronics also suffers from the clock phase error of the ADC. Figure 5.7 shows the simulation results in different conditions. In this case, the input signal is fixed to 10 p.e (PMT gain = 10^6). The results show that ADCs with less number of bits and slower sampling rate are more vulnerable to the variation of the ADC clock phase error.

It also can be concluded from table 5.2, figure 5.6 and 5.7 that the 10-bit ADC and the 14-bit ADC are inclined to overestimate the charge of input signal. As a contrary, the



(a) (b)

Figure 5.7: Deviations of the charge measurement of different ADCs due to clock phase error. Figure 5.7a shows the relation of same sampling rate and different number of bit. Figure 5.7b shows the relation of different sampling rate and the same number of bits.

12-bit ADC always underestimates the charge. This phenomenon is due to the minimum charge that can be measured by the particular ADC.

Based on the discussions above, it is clear that if one plans to use a single preamplifier or an active filter with a fixed gain in this front-end electronics, the 14-bit and very fast sampling ADC should be adapted into the system to maintain the performance and to reduce the fluctuations of the output. Nevertheless, due to the natural characteristics of the ADC, a multi-channel, very fast sampling ADC with a higher number of bit is quite difficult to implement in practice. Even there are some possible candidates, the prices are extremely high.

Since this phenomenon always happens at the low range of the input, as shown in figure 5.6 and table 5.2, the simplest way to solve this problem is to split the output of the preamplifier or active filter signal into two channels with different gains and then digitize them with two separated ADCs. The block diagram of this system is shown in figure 5.8. The gains of the HG and LG channel are set to about 32 and 8.

Figure 5.9 shows the comparison of the designs with and without the HG channel. In the figure, the red plus signs represent the deviations of the charge measurement of the HG channel. The blue asterisk signs, green cross and magenta circles represent the deviations of the charge measurements without HG channel as the design which is shown in figure 5.4. To present the details, the 1 p.e. and 2 p.e. data point of the blue asterisk are abandoned due to their large deviations which is shown in figure 5.6. This figure can be treated as

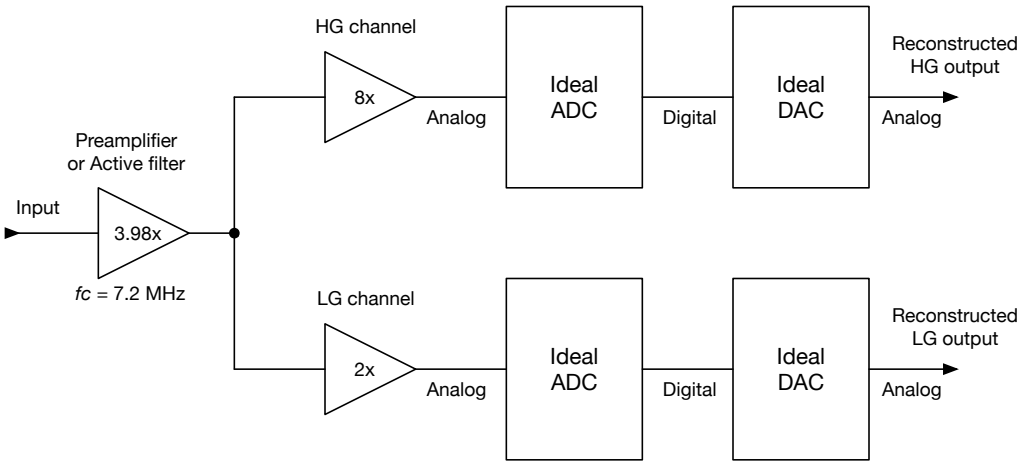


Figure 5.8: Block diagram of a dual-gain design

a zoom-out version of the figure 5.6. Compared with the previous design, it is clear that the performance of the system can be improved in both ways: by using of the dual-gain channels and the separated ADCs or by a single ADC with high number of bits. The first one is a cheaper and proper solution even it increases the complexity of the circuits. In this figure, the combination of two 10-bit ADCs obtains an even better result than the result of a 12-bit ADC without the HG channel. However, the 14-bit ADC is still the best choice.

One thing that should be mentioned here again is that all the discussions in this chapter are based on the ideal circuits and behavior models. The performance of the final system will degrade due to the limitations of the real components and devices.

5.1.2 Design for the fluorescence mode

The design for the fluorescence mode is more or less the same as for the Cherenkov mode. However, as a result of two different physical progress and propagations, the duration of a fluorescence signal is much longer than that of a Cherenkov signal. It usually reaches several μs depending on the distance of the telescope to the impact point. Thus, if we only consider the charge of the input signal, a signal preprocessing circuit with a low cut-off frequency and a lower speed ADC (10 MSPS) can be used in the design of the electronics. Hence, by using the specifications of AUGER-FD [Pierre Auger Collaboration, 2010] and the circuits discussed above, an ideal design for the fluorescence mode has been implemented to evaluate and verify the possible performance of the system. The block diagram is similar as the one shown in the figure 5.8.

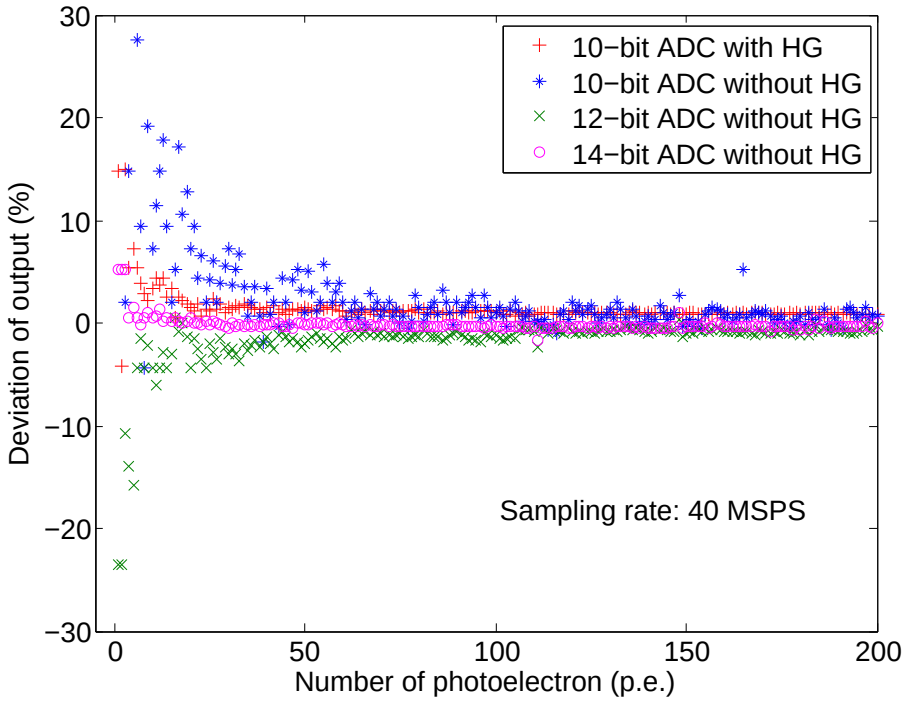


Figure 5.9: Deviations of the charge measurement with and without HG channel. The red plus signs represents the deviations of the charge measurement when HG channel plug in. The blue asterisk, green cross and magenta circle represent the deviations of the charge measurements without HG channel as the design which is shown in figure 5.4. The sampling rate of all ADCs is 40 MSPS.

To meet the requirement of the AUGER-FD, the cut-off frequency of the active filter is adjusted to 3.4 MHz, and the gain of the circuit is also adjusted to 1. The equation 5.1 is rewritten as

$$H(s) = \frac{1.09515e30}{s^4 + 1.01058e8s^3 + 4.59572e15s^2 + 1.08368e23s + 1.09515e30} \tag{5.2}$$

Figure 5.10 gives an example of a full fluorescence signal processing progress. The magenta line represents the fluorescence input signal from the PMT. The green and blue lines represent the output of the HG channel after the active filter and the reconstructed signal through ADC and DAC, separately. The cyan and red lines represent the output of the LG channel after the active filter and the reconstructed signal through ADC and DAC. The ADCs used in the example are two 10 MSPS 10-bit ADCs.

With an automatic signal generator, a fluorescence signal is produced with the total photoelectrons of 20,138.7 p.e. and the total charge of 3,222.19 pC. In the simulation results, the input charge is about 3,221.64 pC. The measured results of the HG and the LG channel are 3,247.35 pC and 3,261.72 pC respectively. Thus, the deviation from the input to the output is only 0.80 % (HG) and 1.24 % (LG). Therefore, a quite accurate charge measurement is obtained with two 10 MSPS 10-bit ADCs.

Figure 5.11 gives another example of the fluorescence signal processing with the same input signal as in figure 5.10. Differently from the previous design, two 40 MSPS 10-bit ADCs are exploited this time. According to the simulation results, the input charge is about 3,221.41 pC. The measured results of the HG and the LG channels are 3,234.87 pC and 3,261.72 pC respectively. Thus, the deviation from the input to the output is only 0.41 % (HG) and 1.25 % (LG). It is clear that replacing the slow ADCs with the fast ones will not significantly boost the performance of the system. Therefore, the fact is that, for a long duration signal as the fluorescence signal, 10 MSPS ADC is already accurate enough for most situations.

However, the 40 MSPS ADC is still a good choice, because not only the charge but also the shape of the signal can be recorded by the faster ADCs. Moreover, with this 40 MSPS ADC, the active filter with a cut-off frequency of 7.2 MHz still can be used, but may be not optimized for the dynamic range. The simulations also show the precise charge measurements with a Cherenkov configuration. Another advantage of using a 40 MSPS ADC is that it suffers less from the clock phase error.

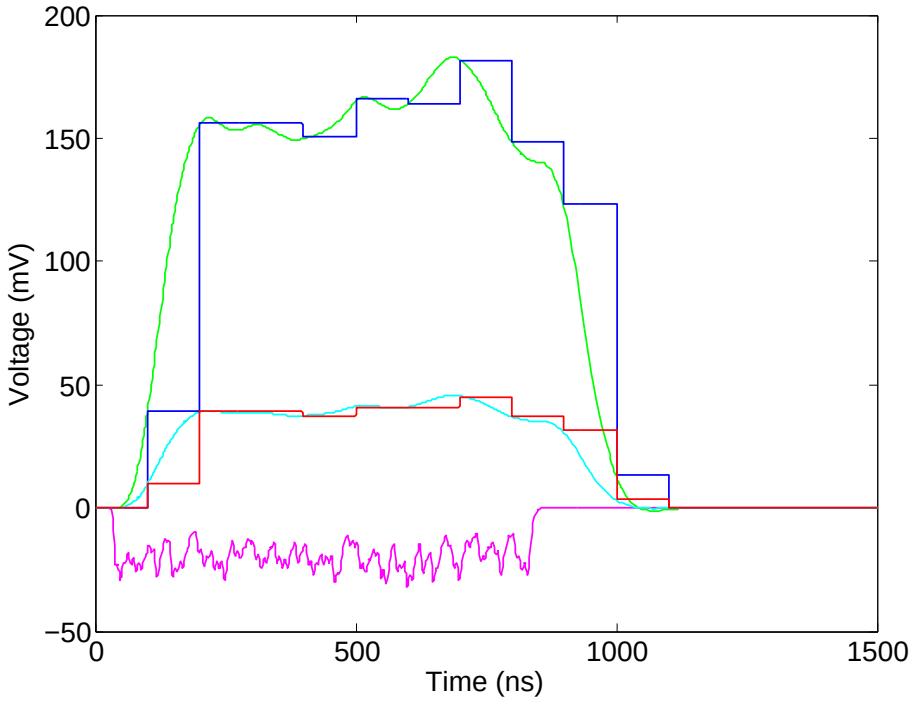


Figure 5.10: Example of a fluorescence signal processing with 10 MSPS 10-bit ADC. The magenta line represents the fluorescence input signal from PMT. The green and blue lines represent the output of HG channel after the active filter and the reconstructed signal through ADC and DAC. The cyan and red lines represent the output of LG channel after the active filter and the reconstructed signal through ADC and DAC.

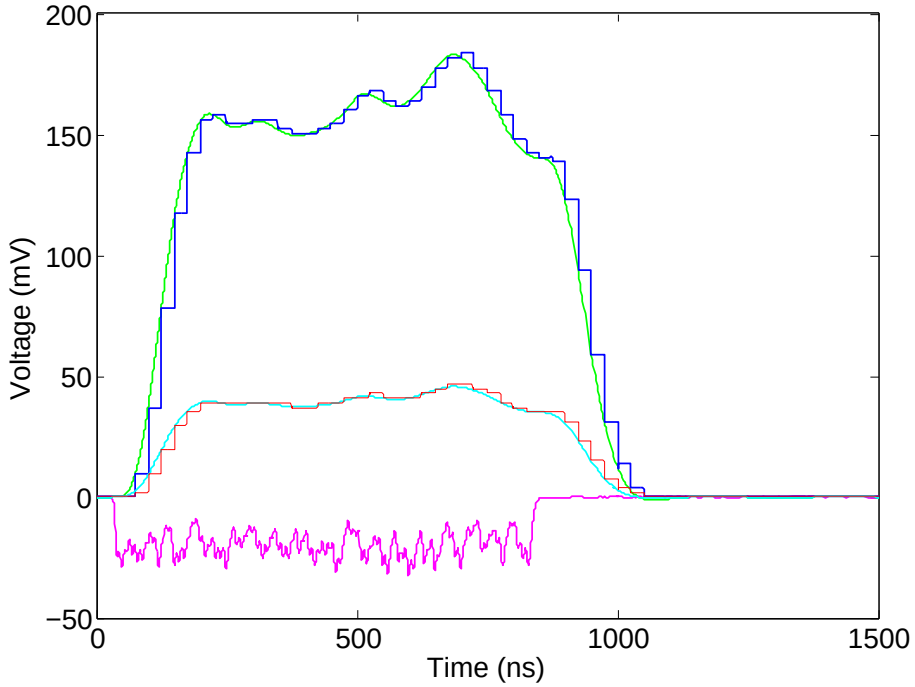


Figure 5.11: Example of a full fluorescence signal processing progress with 40 MSPS 10-bit ADC. The magenta line represents the fluorescence input signal from the PMT. The green and blue lines represent the output of HG channel after the active filter and the reconstructed signal through ADC and DAC. The cyan and red lines represent the output of LG channel after the active filter and the reconstructed signal through ADC and DAC.

5.1.3 Brief summary of the design based on the classical electronics

In this section, we studied and discussed the designs of the front-end electronics based on classical electronics for the new WFCTA telescopes. As this is the traditional way to design an electronic system, it is not necessary to emphasize that classical electronics could meet the most requirements of a detector, if they are reasonable. The simulation results show that the designs introduced in this section fulfill all the specifications of WFCTA in both Cherenkov and fluorescence mode, which is not surprising.

However, one thing that has to be highlighted here is that designing a circuit is a progress of compromising and balancing between different factors, such as gain, noise, bandwidth, input scale, power, price, etc., since they cannot be fully satisfied in a single design. Compromise is the key point of a design. Therefore, it also means that the goal can be achieved in different ways. An electronic system can be implemented with a simple circuit with expensive, hight power consumption components and devices or a complex circuit with moderate components. As shown in this section, one could achieve a precise charge measurement of a small signal with a single channel preamplifier and a 40 MSPS 12-bit ADC or with a dual-gain channels design and two 40 MSPS 10-bit ADCs to obtain a similar precision at a cost of increasing the complexity of the circuit.

Furthermore, in the real case, the electronic system also suffers many challenges from the harsh environmental conditions. Sometimes, a classical electronic system may not be the best choice.

5.2 Design based on the ASIC

A large hybrid cosmic ray experiment such as LHAASO, which is proposed to be built at a high altitude of 4,400 m a.s.l and consists of several different detectors, has to overcome several challenges for the design and for the construction. On one hand, at such high altitude, the air pressure is only about 60 % of that of the sea level. This decreases the efficiency of the heat dissipation. On the other hand, the large number of channels increase the density and the complexity of the electronics as well as the power consumption, especially for the telescopes such as WFCTA. Furthermore, the stability, the reliability and the maintainability of the system are crucial points for the detectors at harsh environmental conditions and remote locations.

Unlike the classical electronics, which is composed of serval discrete components such as resistors, capacitors, inductors and different devices as integrated circuit (IC) chips, the application-specific integrated circuit (ASIC) is a special IC chip. It is a group of electronic circuits including transistors, resistors, capacitors and inductors which are integrated and fabricated on a small "die" which is made by semiconductor materials such as silicon or germanium. This type of IC is also different from the general purpose IC and is always customized and focused on a particular purpose with some special designs and requirements. It usually integrates both analogue and digital circuits in it.

Comparing with the traditional discrete circuits, ASICs have three main advantages: integration, cost and performance. With today's IC technology, billions of semiconductor devices can be implemented on a tiny plate. This high integration gives a possibility for the designers to build a complicated electronic system, a mechanical system and even a mixture of them on a single chip. The small area of the chip saves the precious space of the circuits and greatly reduces the cost. The high performance is due to the fast switching of devices, small power consumption and short paths between the components on a small die. As a result, a high density, stable, reliable and high performance design can be obtained by using ASICs.

Considering all these factors, a customized ASIC would be a well-suited solution for LHAASO. Integrating all the analogue and digital components into a single chip will simplify the design of the system, decrease the power consumption and increase the reliability, especially for the WFCTA telescopes, which have high density of electronics. In fact, nowadays, in the design of electronics, it is not a question to use ASICs or not, it is a question which one should be used. Fortunately, we have found one that is PARISROC 2 (Photomultiplier ArRay Integrated in SiGe ReadOut Chip)[S. Conforti Di Lorenzo et al., 2012].

5.2.1 General description of the PARISROC 2

The PARISROC chip [S. Conforti Di Lorenzo et al., 2012] is a complex system on chip (SoC) IC that processes analog signals up to the digitization. It is designed for multiple-purpose use by the OMEGA microelectronics group (Palaiseau, France) and fabricated in 0.35 μm SiGe technology by Austria Micro Systems (AMS). The PARISROC chip provides several functionalities. It can auto-trigger asynchronously and provide digitized time and charge measurements. It has 16 independent channels and a common digital part. Typically, it covers a dynamic range from 50 fC to 100 pC and the time tagging is better than 1 ns.

It is a low-power consumption chip requiring only 15 mW per channel. The event rate of the chip could reach 20 kHz in the best case. The die size of the chip is around 5 mm × 3.4 mm. It usually is sealed in the typical CQFP-160 (Ceramic Quad Flat Pack) or TQFP-160 (Thin Quad Flat Pack) package which size is about 33 mm × 33 mm (1089 mm^2). The basic characteristics of the PARISROC 2 chip are summarized in table 5.3.

Table 5.3: Basic characteristics of the PARISROC 2

Property	Specification
Technology	AMS 0.35 μm SiGe
Channels	16
Power supply	3.3 V
Power consumption	15 mW/channel
Die dimension	5.034 mm × 3.42 mm
Die area	17.21 mm^2
Package	CQFP-160/TQFP-160
Package dimension	33 mm × 33 mm
Package area	1089 mm^2

The main architecture of the PARISROC 2 is shown in figure 5.12. It is composed of three main parts: trigger, charge and time measurements. The charge measurement is obtained by two gain paths (high and low) for small and large input signals in order to maintain a good charge resolution over a large range. The gain of each channel can be set and adjusted individually but the ratio of the gains between high-gain and low-gain channel is locked to 10 to 1. This adjustable gain of the preamplifier has been implemented to slightly compensate the gain dispersion of the photomultipliers operated at a common high voltage. The preamplifiers are followed by a slow shaper with variable shaping time and variable gain. Both shaper signals are stored in two analog memories with a depth of two to minimize the dead time during digitization. A discriminator allows to select the non saturated charge signals for analog-to-digital conversion.

Figure 5.13 and 5.14 presents the principle chronogram and the schematic of the analog TDC of PARISROC 2, respectively. The time measurement is obtained by two time units [S. Conforti Di Lorenzo et al., 2011; Dulucq et al., 2010]. The coarse time (time stamp) is performed by a 24-bit gray counter at 10 MHz. It suggests that the coarse timer has a dynamic range of 1.67 s and a step of 100 ns. The fine time is obtained by time-to-amplitude converter (TAC) and stored in two analog memories, in parallel with the charge measurement. When a trigger is generated, the valid stored value is converted into digital

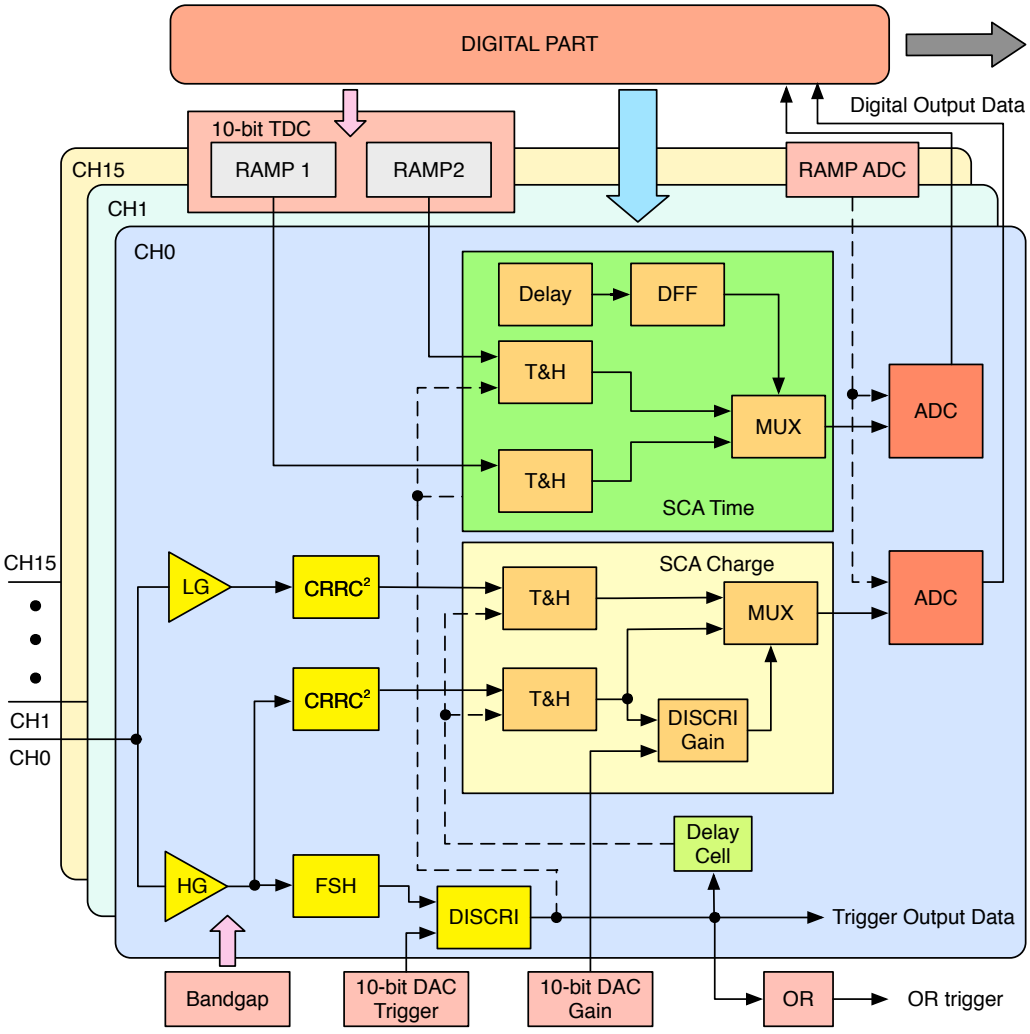


Figure 5.12: Block diagram of PARISROC 2

by using the same internal ADC. The total duration of each ramp is 140 ns. The linear zone of each ramp is 100 ns and 1 V in voltage. It suggests that the fine timer has a dynamic range of 100 ns and a step of 220 ps (1 ADC count). The absolute real time of each event can be recovered by the sum of the coarse and the fine time with a special algorithm to achieve a resolution better than 1 ns.

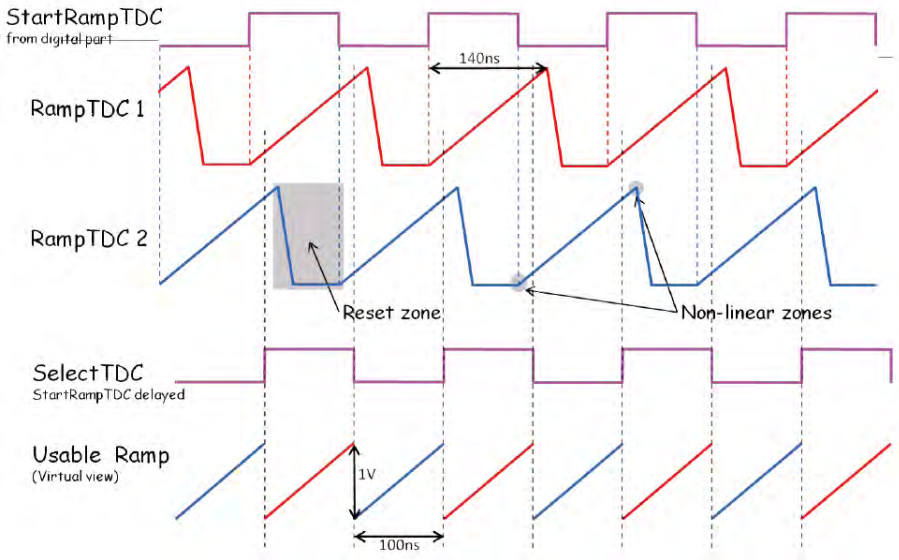


Figure 5.13: Principle chronogram of the analog TDC of PARISROC 2. The figure is taken from [S. Conforti Di Lorenzo et al., 2011].

The high-gain preamplifier followed by a fast shaper is used to produce a trigger. An adjustable low offset discriminator is used as the trigger threshold. All channels are handled independently by the digital part and only channels that created triggers are digitized and transferred to the internal memory and then sent out. The digitized results of the charge measurements and the time measurements are combined into a PARISROC output data frame which has a length of 51 bits and is synchronized to a 40 MHz clock. The 16 trigger lines and 1 "OR" signal of all trigger lines are sent out for the extra time measurements.

Moreover, the PARISROC 2 chip has 278 slow control parameters and 260 probe parameters which cover full aspects of the chip control. However, based on the application, the number can be typically reduced to 5, such as the discriminator of DAC 0 (DD0), the discriminator gain of DAC (DDG), the trigger delay (TD), the slow shaper gain (SSG) and the slow shaper time constant (SSTC). These slow control parameters are selected prior testing and adapting. Since these registers are synchronized to a 10 MHz clock, the reconfiguration of the ASIC lasts about 27.8 μs for slow control parameters and 26 μs for probes parameters.

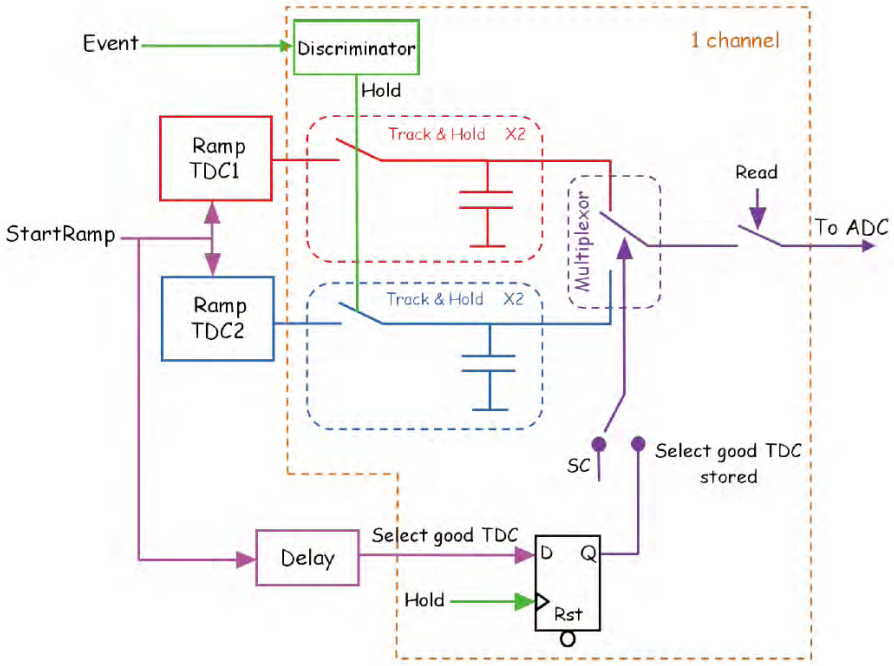


Figure 5.14: Schematic of the analog TDC of PARISROC 2. The figure is taken from [S. Conforti Di Lorenzo et al., 2011].

Table 5.4: Summary of the most important parameters of the PARISROC 2

Slow control parameters	Purpose
Discriminator of DAC 0	Setting threshold and adjustable step
Discriminator gain of DAC	Setting the switch point of HG & LG
Trigger delay	Point to measure the charge
Slow shaper gain	Setting the gain of slow shaper
Slow shaper time constant	Setting the time of shaper

5.2.2 Ideal behavior and response of the PARISROC 2

In order to understand the ideal behavior and response of the PARISROC 2 chip, a SPICE-based behavior model has been implemented for the simulation. As shown in figure 5.12, the PARISROC 2 consists of three main parts: trigger, charge and time measurement. Since it is difficult to describe the behavior of a pure digital circuit in a SPICE program, the circuits of the time measurement in PARISROC 2 are not integrated in the model. The time measurements can be obtained by using the output trigger and additional data analyzing program. The behavior model for this ASIC is based on [S. Conforti Di Lorenzo, 2010].

For the same reason as the classical electronics, in order to increase the dynamic range of the chip and to reduce the number of bits of the ADC, the input signal of PARISROC 2 is split into two parts and amplified separately by two preamplifiers with different gains. Based on this principle, a behavior model of the dual-gain preamplifiers of a single channel in PARISROC 2 has been built and is shown in figure 5.15. The input capacitances of the HG and the LG preamplifier are 5 pF and 0.5 pF, respectively. The feedback capacitance of these preamplifiers is variable and controlled by a common 8-bit register with a default value of 0.25 pF. Therefore, the default gain of the HG and LG preamplifiers are 20 and 2, respectively. The ratio of these two gains is locked to 10 to 1, due to the common control register. Moreover, the matching resistor R1 is not integrated in the chip.

Figure 5.16 gives the ideal responses of the HG and LG preamplifiers of the ASIC with an input signal of 160 fC (1 p.e. @ PMT gain = 10^6). The maximum amplitude of the input is about 0.67 mV. The corresponding outputs of the HG and the LG channel are 1.34 mV and 13.40 mV, respectively.

The amplified HG output signal is sent to a fast shaper (FSH) and to a discriminator which follows it to generate the trigger signals. The fast sharper is implemented by a CRRC filter with a gain of 8 and a time constant of 15 ns. The ideal model of it is shown in figure 5.16. The baseline of the shaper can be set by a reference voltage (vref_fsh in figure 5.16). It is about 2 V in practice. The ideal responses of the fast shaper and the output of HG channel are both presented in figure 5.17. The fast shaper gives an output of 107.20 mV for a signal of 160 fC. This ensures that the chip can be triggered by a signal of about 50 fC.

At the same time, both HG and LG channels are sent to two slow shapers (SSH) for further signal processing. In this stage, the outputs of the preamplifiers are amplified again and shaped for the charge measurement. The signal-to-noise ratio (SNR) is optimized due

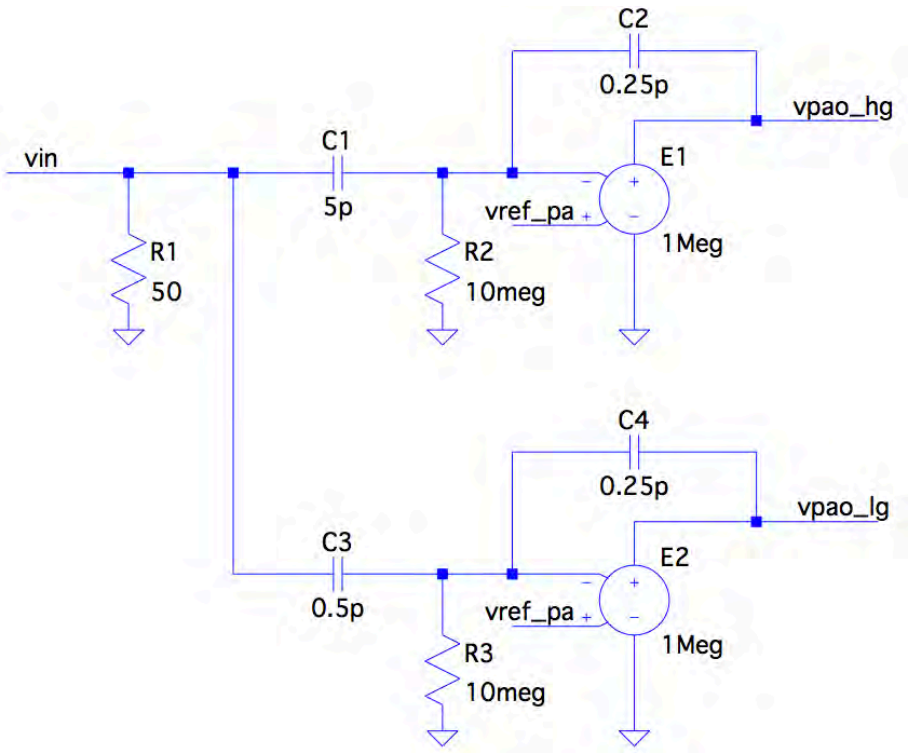


Figure 5.15: Behavior model of the dual-gain preamplifiers of a single channel

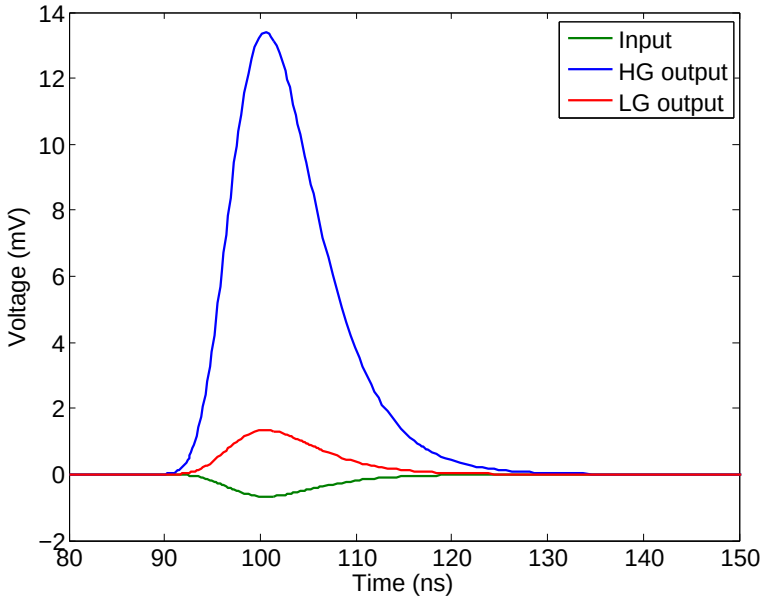


Figure 5.16: Ideal responses of the HG and LG preamplifiers with a signal of 160 fC.

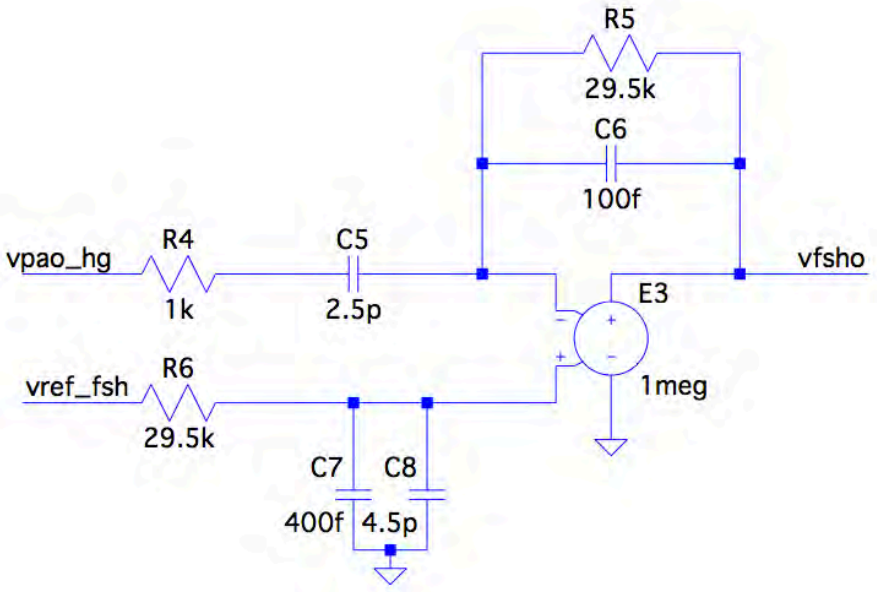


Figure 5.17: Behavior model of the fast shaper.

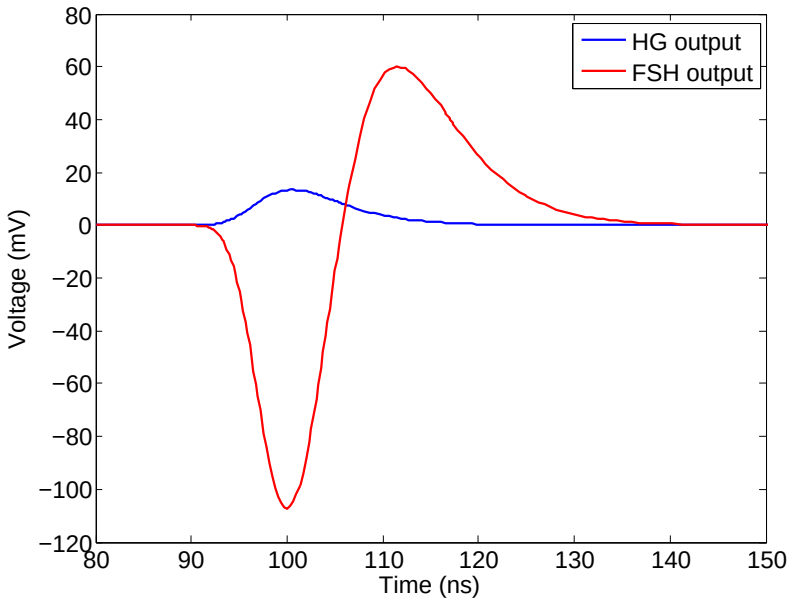


Figure 5.18: Ideal responses of the fast shaper and the output of HG channel

Table 5.5: Slow shaper parameters of the PARISROC 2

Time constant (ns)	Rf1 (Ω), Cf1 (pF)	R1 (Ω), C1 (pF)	Rf2 (Ω), Cf2 (pF)	Gain of shaper
25	16K, 1.5625	16K, 1.5625	48K, 0.5208	0.90
50	16K, 3.1250	16K, 3.1250	48K, 1.0416	0.50
	32K, 1.5625			1.00
100	16K, 6.2500	16K, 6.2500	48K, 2.0830	0.25
	64K, 1.5625			1.00

to the use of the CRRC^2 band-pass filter in the ASIC. The structure of the slow shaper is shown in figure 5.19 and the parameters of it are listed in table 5.5. Since we only discuss the ideal model of the slow shaper, the reference voltages are taken from the table. The more detailed information is shown in [S. Conforti Di Lorenzo, 2010].

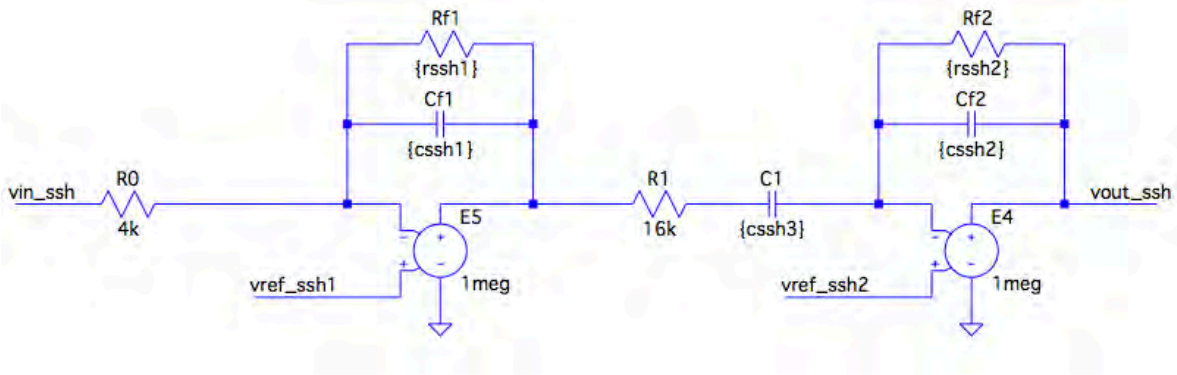


Figure 5.19: General structure and the behavior model of the slow shaper

Figure 5.20 gives an example of the outputs of both HG slow shaper and LG slow shaper. The injected charge, the shaping time and the gain are 160 fC, 100 ns and 0.25, respectively. The maximum outputs of the HG slow shaper and LG slow shaper are about 4.41 mV and 441 μV, respectively.

Based on the electrical theory, the charge of the input is not only proportional to the charge of the output, but also proportional to the amplitude of the output, if the duration of the input signal is the same. Therefore, unlike the classical ADC-type of design as described in last section, in the PARISROC 2, the ADC unit only samples a specific point of the output of the slow shaper. The location of the sample point is determined by the delayed trigger signal. The sampled amplitude of the slow shaper is used to represent the

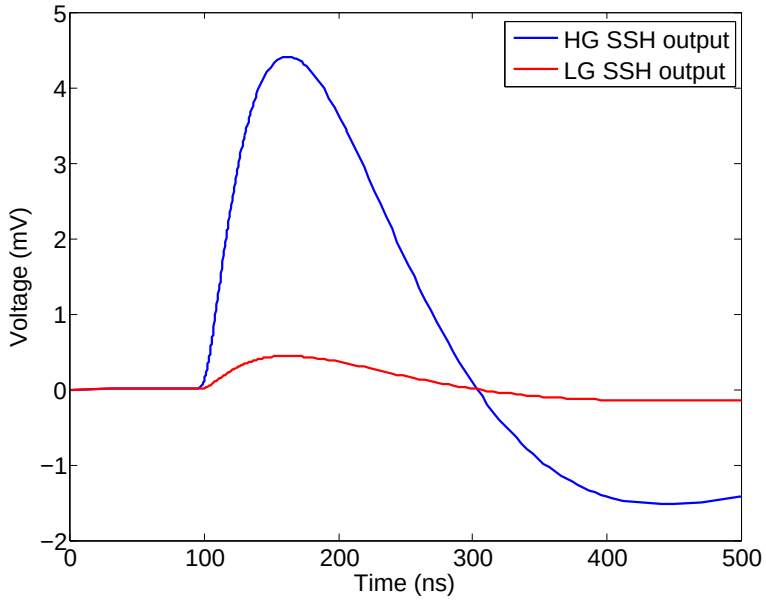


Figure 5.20: Ideal responses of the slow shapers with a shaping time of 100 ns and a gain of 0.25

charge of the input signal. To achieve this purpose, track and hold (T&H) units are needed and follow the slow shapers.

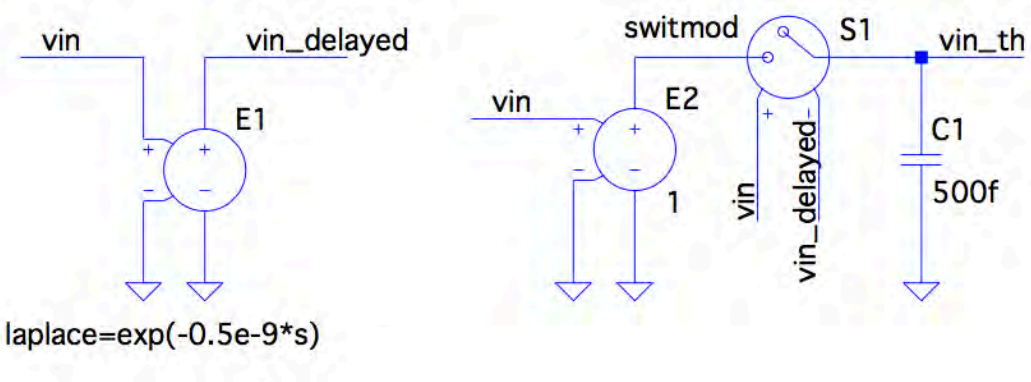


Figure 5.21: General structure of the ideal track and hold circuit

The general structure of the track and hold circuit is shown in figure 5.21. To simplify the design, in this behavior model, an ideal delay and an ideal voltage controlled switch are used to replace the amplifier. The basic idea of the design is simple. The input and the delayed input are used to control the switch. When the input is larger than the delayed input, the circuit will track and store the maximum value of the input signal. When

the input is smaller than the delayed input, the circuit will hold the input signal at the maximum. The delay time can be easily set by the transfer function, which is given by

$$H(s) = exp(-t_{delay} \cdot s), \tag{5.3}$$

where t_{delay} represents the delay time. Thus, the formula in the schematic implies the delay of the circuit is 0.5 ns. The responses of the HG slow shaper and the T&H of it are shown in figure 5.22. Simply by sampling the output of the T&H with an ideal ADC, the charge of the input is obtained. The 10-bit 40 MSPS ADC used in PARISROC 2 simulation is the same ADC as the one which is used in the classical electronic modelization.

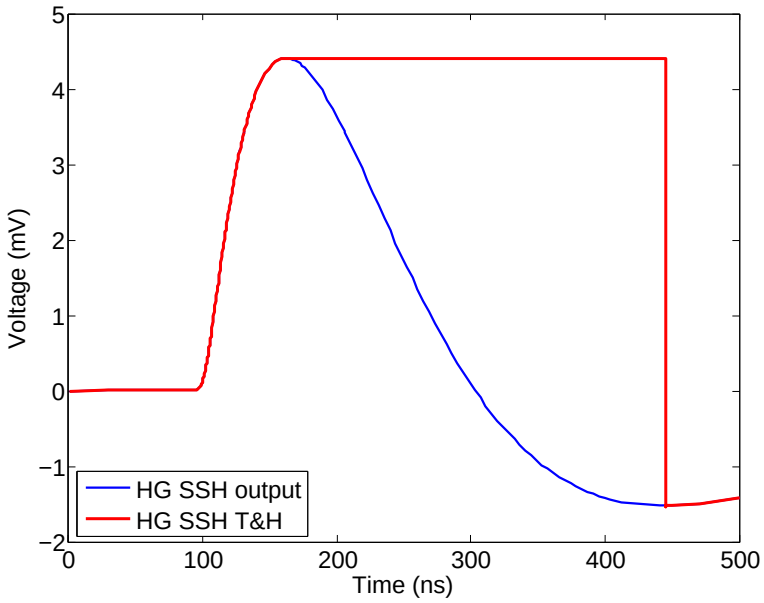


Figure 5.22: Ideal responses of the HG slow shaper and its T&H circuit

By combining all these behavior models together, the ideal response of the PARISROC 2 can be evaluated with a set of input signals which have a fixed duration (Cherenkov: 4 ns) and varied amplitudes (1 to 2,000 p.e.). The linearity of the chip has been simulated and is shown in figure 5.23. The HG channel covers a dynamic range from 1 p.e. to 453 p.e. and the LG channel covers a dynamic range from 3 p.e. to 2,000 p.e..

Figure 5.24 shows the residuals of both digitized outputs. The blue circles and the red circles represent the residuals of the digitized outputs of the HG and the LG channels, respectively. As the result of an ideal ADC, the residuals of the outputs should be less than

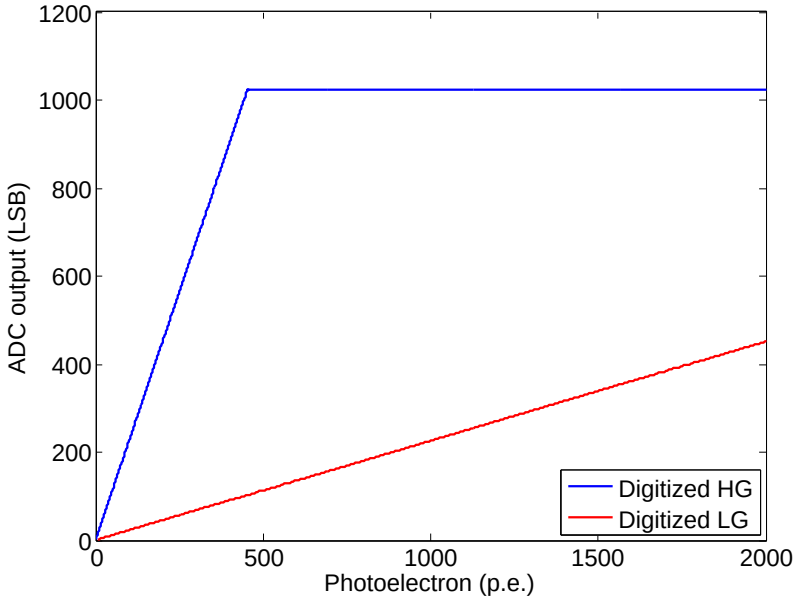


Figure 5.23: Digitized outputs of the PARISROC 2 for both the HG and the LG channels

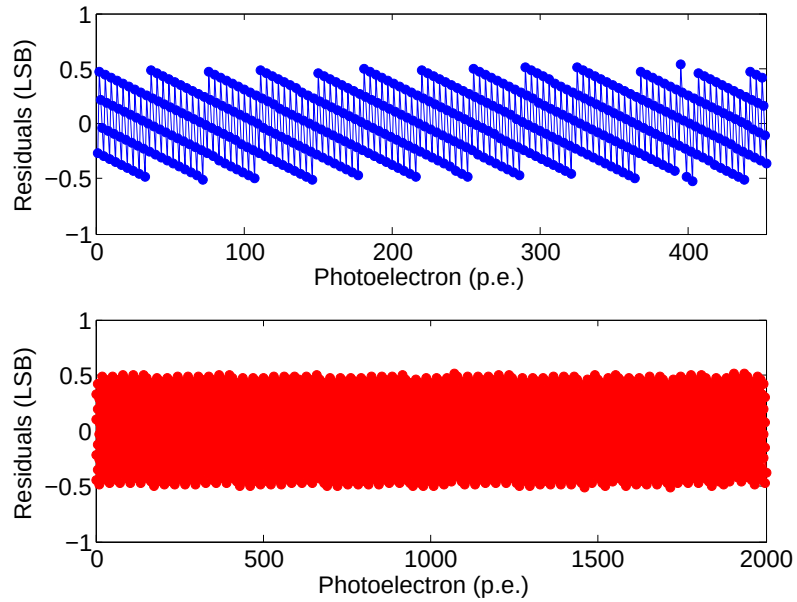


Figure 5.24: Residuals of the digitized outputs of the PARISROC 2 including the HG and the LG channel. The blue circles and the red circles represent the residuals of the digitized outputs of the HG and the LG channel, respectively.

± 0.5 LSB. It is obvious that the behavior model of PARISROC 2 fulfills this requirement. It also implies that this chip could achieve a very precise charge measurement over a large dynamic range.

Compared with the classical ADC-type electronics, this structure has at least two advantages. First, sampling the output of the slow shaper at a specific point decreases the requirement of the sample rate of an ADC. In this configuration, even a low speed ADC (10 MSPS) could achieve a precise charge measurement, affecting only the dead time and the event rate of the chip. A high speed ADC could improve the event rate and decrease the dead time. Second, sampling the maximum output or the approximated maximum output of the slow shaper could avoid the deviations which are introduced by the minimum charge that can be measured by a specific ADC in a classical electronics. This phenomenon has been discussed in the last section. Even if the ideal units are used in the behavior model, the classical electronics still suffers a lot from the minimum charge of the ADC. Unlike the previous design, the precision of the PARISROC 2 mostly depends on the linearity of the preamplifiers and the slow shapers. It is possible to achieve the highest performance of an ADC, if the signal preprocessing units are fully linear.

However, this assumption has one limitation: the duration of the input signal must be fixed, due to its $CRRC^2$-type of filter in the slow shaper. The use of a band-pass filter not only cuts off the unwanted noises, but it also limits the bandwidth of the input signal. Figure 5.25 shows the frequency response of the slow shaper of PARISROC 2. It can be explained with the figure 5.25. The duration of the signal can be easily represented by the frequency of the signal. It is easy to find out from this figure, when the duration of the input signal is changed, the gain of the slow shaper is changed as well. Consequently, the ASIC cannot maintain the linearity of the charge measurement.

Figure 5.26 shows the relation between the signal duration and the deviations of the HG output of the PARISROC 2. The input signal is fixed to 100 p.e. and the duration of the input signal varies from 1 to 20 ns. The signal with a duration of 1 ns has been used as the baseline to calculate the deviations of the output. The HG output of the PARISROC 2 decreases with the increasing the width of the input signals. When the FWHM of the input signal of the PMT reaches about 8 ns, the HG output will be -2.2 % less than the baseline value. At this point, the FWHM and the top width of the corresponding PMT output are 20.09 ns and 47 ns, respectively. When the duration of the input is about 20 ns, the HG output will be -11 % less than the baseline. Therefore, it is obvious that the PARISROC 2 is not suitable to measure those signals with large variation of the durations.

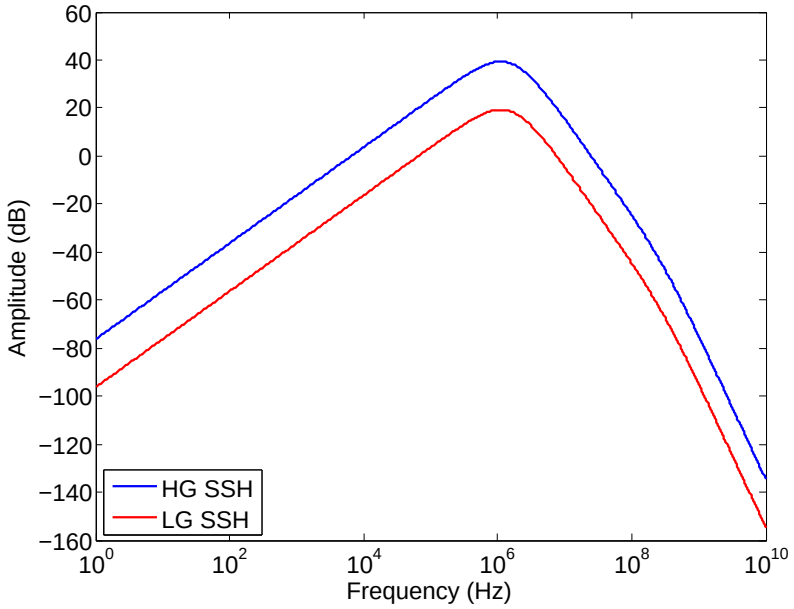


Figure 5.25: Frequency responses of the HG SSH and LG SSH

Due to the limitation of the shaping time (< 100 ns), it is also not suitable for signals with long durations. Based on the simulation results, the PARISROC 2 chip cannot be directly used in the fluorescence mode of the WFCTA without any upgrades. The simplest way to make it compatible with the fluorescence mode is to output the slow shapers and sample these signals with external ADCs.

5.2.3 Brief summary of the design based on the ASIC

Compared with the classical electronics, the design based on the ASIC has several advantages. The low cost, low power consumption, high performance makes it an attractive solution for detectors requiring stability, reliability and maintainability of the system at harsh environmental conditions and remote locations. As a result of that, in this section, we simply discussed and studied the possibilities of using the ASIC in the design of the front-end electronics of the WFCTA. The PARISROC 2 ASIC chip has been chosen as a candidate of our design. By establishing a whole behavior model of this chip, we carefully simulate the behavior of the chip and evaluate its performance. According to the results, it is clear that, in principle, a design based on the PARISROC 2 could easily achieve a very large dynamic range and accurate charge measurement. It is very suitable for signals with

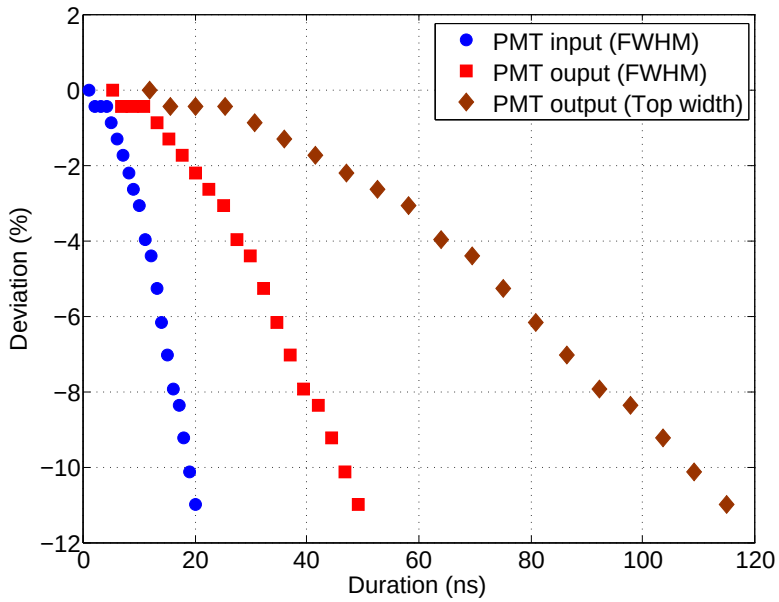


Figure 5.26: Relation between the signal duration and the deviations of HG output of the PARISROC 2

a fixed duration or little variation in duration as the Cherenkov light signals. However, due to the limitation of the shaping time (< 100 ns) and the architecture of the slow shaper ($CRRC^2$ filter), it is not optimum for signals with long durations or variable durations as the fluorescence light signals. Therefore, it can be hardly adapted in the fluorescence mode of the WFCTA without any modifications. The simplest way to make it compatible with the fluorescence mode is to output the slow shapers and sample these signals with external ADCs. In the next chapter, the design and the implementation of the front-end electronics based on PARISROC 2 will be presented.

Chapter 6

Design and implementation of the FEE based on PARISROC 2

For the camera of the WFCTA, the density of pixels is the most important specification. Small pixel size will improve the quality of the picture of the shower but increase significantly the complexity of the electronic system. Due to the characteristics of the Cherenkov light signals, the telescope requires a high-performance front-end electronics which can deal with hundreds of channels and be implemented into a small space with the specifications of accurate charge measurement (linearity better than 1 or 2 %), high dynamic range (three orders of magnitude) and short readout time (few microseconds). Moreover, the operation of the telescope at high altitude has to face the challenges of low power consumption, stability, reliability and maintainability of the system. Compared with the traditional FADC-type of design, the integration on all of analog and digital components into a single chip will simplify the design of the system, decrease the power consumption and increase the reliability of the system. Based on the specifications and the requirements of the telescope, simulations and studies have been performed with the behavior models of the PMT and two types of the front-end electronics, which are shown in the last chapter. All results suggest that a customized ASIC as PARISROC 2 is naturally an excellent candidate of the front-end electronics for WFCTA considering all aspects.

Accordingly, a new front-end electronics based on PARISROC 2 has been proposed to fulfill the specifications of WFCTA in electronics and mechanics. In this chapter, the design and the implementation of the FEE will be introduced and discussed. However, the performance of the real chip should be evaluated against the requirements of the telescope before the application of the ASIC. The preliminary test results of the PARISROC 2 will be shown in this chapter as well. These include different groups of tests such as the dynamic

range and linearity, the duration of the signal, the pedestal monitoring and the event rate. The performance is also evaluated with a candidate PMT of WFCTA, which is CR303 manufactured by Beijing Hamamatsu.

6.1 Preliminary test results of the PARISROC 2

The PARISROC chip was originally designed for the PMT readout in PMm^2 (square meter PhotoMultiplier) project [Campagne et al., 2011]. A prototype of the front-end electronics with PARISROC 2 fulfilling the requirements of PMm^2, was successfully designed and tested by the SEP group of the IPN-Orsay. This specific prototype is used as a test bench to evaluate the PARISROC 2 chip for the requirements of the WFCTA in the first phase. The preliminary test results of the ASIC with this application board, including the general electronics tests and the PMT tests will be presented in this section.

6.1.1 Test bench and configuration of the chip

The picture of the test bench is shown in figure 6.1. The system is composed with a PMm^2 application board, a signal generator, a 40 V power supply, an oscilloscope, a multimeter, an attenuator, a signal splitter and a light-tight box for PMT.

As we mentioned in the Chapter 5, the PARISROC 2 chip has 278 slow control parameters (SCPs) that are used to control the internal registers and the functional blocks in the chip. According to the operating mode of the ASIC, the quantity of the charge is measured by the dual-gain channels and the slow shapers in order to achieve a good charge resolution ($\sim$ 30 fC). Depending on these functional blocks, the input signal is amplified and shaped. At the same time, the trigger signal, which is generated from the high-gain channel based on the threshold, after being delayed, will be sent to execute a pseudo-track-and-hold progress. It means that the charge track & hold unit will only keep the charge value at an exact point, which is related to the trigger delay, but not track and hold the whole curve. Therefore, based on the application, the SCP number can be typically reduced to 5, which are shown in table 5.4. These slow control parameters should be selected prior testing. In the evaluation of the ASIC, the values and the ranges of the parameters which are used in the tests are listed in table 6.1.

To choose an appropriate threshold (DD0) is the first step. This parameter will affect the performance of the chip. Theoretically, this threshold should fulfill the requirements from detecting small signals with single photoelectron to large signals with thousands of

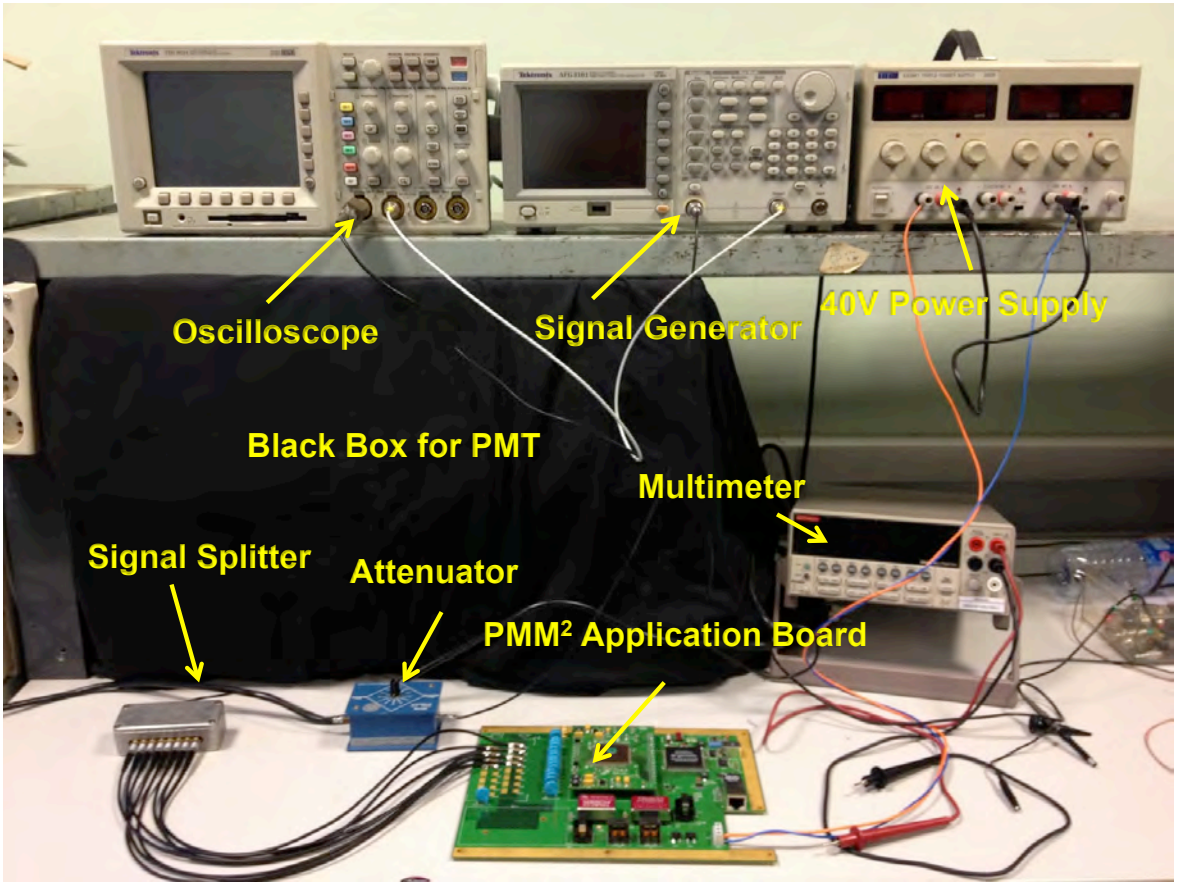


Figure 6.1: Picture of the test bench based on the PMm^2 application board

Table 6.1: Values of the most important parameters of the PARISROC 2

Slow control parameters	Values
Discriminator of DAC 0 (DD0)	790 (0 to 1023)
Discriminator gain of DAC (DDG)	550 (0 to 1023)
Trigger delay (TD)	8 (0 to 63)
Slow shaper gain (SSG)	16K (16K to 64K)
Slow shaper time constant (SSTC)	50 ns (0 to 175 ns)

photoelectrons. According to the datasheet of the ASIC [OMEGA microelectronics, 2012], the threshold is around 800 by default, depending on the noise level of the system. In our tests, it has been set to around 790. The rest of these parameters are all default values of the chip for a shaping time (SSTC) of 50 ns. The preliminary tests of the ASIC were performed with this configuration.

6.1.2 Dynamic range and linearity

A typical structure of dual-gain amplifiers is adopted in the PARISROC 2 in order to measure the charge. Generally, the input signal will be amplified by two preamplifiers with the gain of 20 and 2 by default. Then data from both channels will be shaped to certain time such as 50 ns by default and digitized by using a 10-bit 40 MSPS Wilkinson ADC. Figure 6.2 and 6.3 show the dynamic range and the linearity of the charge measurement of the PARISROC 2 with the PMm^2 application board.

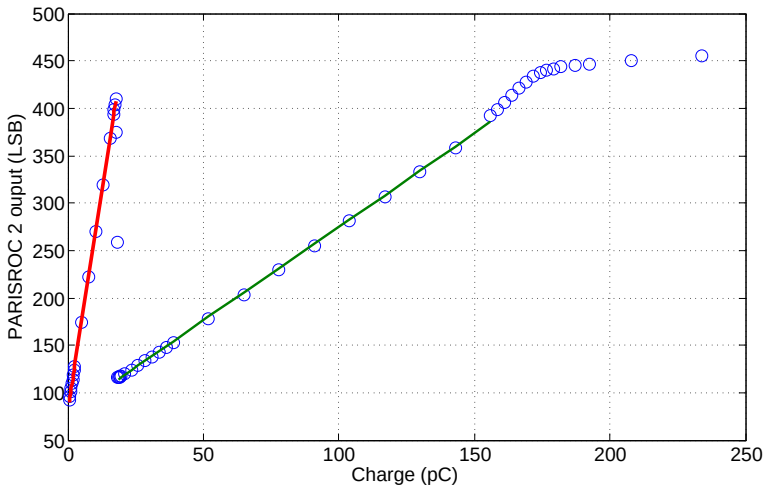


Figure 6.2: Dynamic range of a single channel of PARISROC 2. The blue circles represent the output of a single channel of PARISROC 2. The red lines and the green lines are the results of linear fits of the HG and the LG channel, respectively.

Since the PARISROC 2 cannot deliver the HG and the LG channel simultaneously, in the figure 6.2, it is clear that the output of the PARISROC 2 is discontinued. The output is switched automatically at the specific point controlled by the DDG. The transformation happens at around 18.2 pC for the DDG of 550. It will take about 1 pC to stabilize the output because of the SCA capacitors and noises. There will be a drop of the linearity when

signal occasionally locates in this range. It is an intrinsic problem of the PARISROC 2 and should be fixed in the next version of the chip.

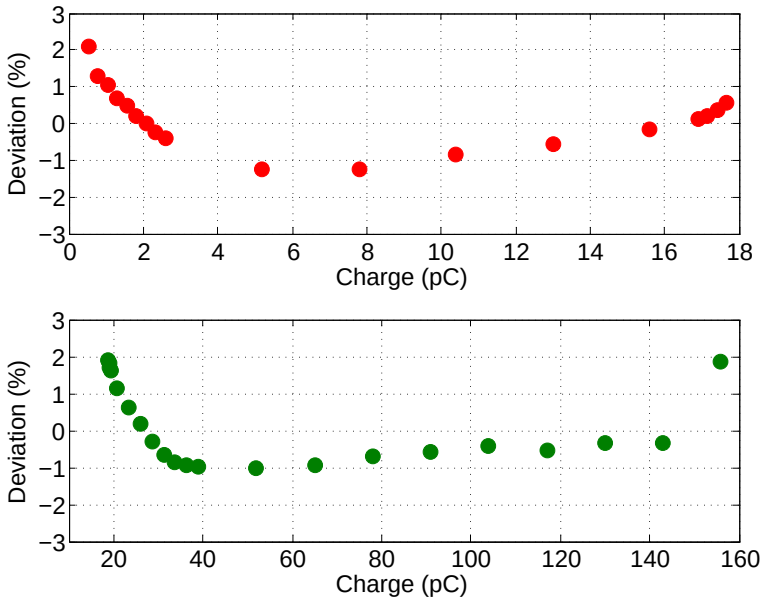


Figure 6.3: Linearity of the HG and LG channel. The red dots and the green dots represent the deviations of the HG and LG channel, respectively.

The measurement can be divided into two parts: the HG channel and the LG channel measurement. From the figure 6.2 and 6.3, the dynamic range of the HG channel is from 520 fC to 17.68 pC with a linearity better than 2 %. The LG channel is able to cover a dynamic range from 18.72 pC to 156 pC with a linearity better than 2 %. Above 156 pC, the output of the preamplifier will saturate very quickly and indicate a large deviation from the expected values. Even without considering the discontinuity between the HG and the LG channels, the whole dynamic range for a single PARISROC 2 channel is roughly from 10 to 3,000 p.e. (PMT gain = 10^5). Due to the nonlinearity and the noise of the real circuits, it is not surprising that this range is smaller than the simulation results which were presented in the Chapter 5. However, this range is not enough to cover the requirement of the WFCTA (10 to 15,000 p.e. at PMT gain = 10^5). Although increasing the shaping time and decreasing the gain of the slow shaper could improve the performance of the charge measurement, a single PARISROC 2 channel still cannot cover the required dynamic range. These results also suggests that the PMm^2 application board is not optimized for this application. A new design for the FEE of the WFCTA is necessary.

6.1.3 Signal duration

Even though, in principle, the Cherenkov light signal produced by the high-energy particles usually lasts a few nanoseconds ($\sim$ 4 ns), it is still wise to design an electronics system that supports longer duration times due to the uncertainty of the location of the telescope. The specifications of WFCTA which is shown in table 3.3 in the Chapter 3, demand that the electronics could deal with signals whose width is spread from 6 ns to 50 ns in the Cherenkov mode. Therefore, the performance of the charge measurement of PARISROC 2 has also been evaluated with the signals with variable duration. The result is presented in figure 6.4. The upper plot shows the result of the charge measurement when the signals with variable duration are injected into chip. The deviation of the measurement is shown in the bottom plot. In this test, the amplitude of the input signal is fixed to 20 mV. The width of the signal is varied from 8 ns to 60 ns.

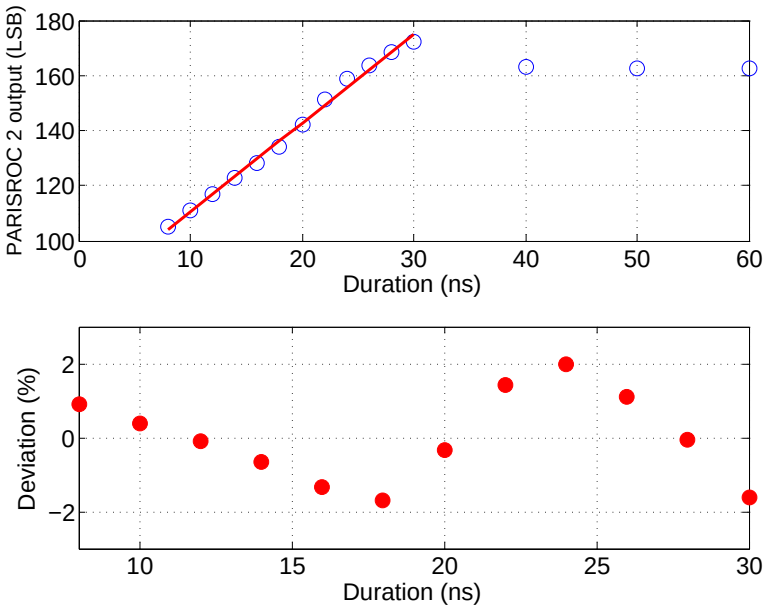


Figure 6.4: Linearity of the charge measurement with the signals with variable duration. The upper plot shows the result of the charge measurement when the signals with varied duration are injected in PARISROC 2. The deviation of the measurement is shown in the bottom plot.

By the default setting, the shaping time of the PARISROC 2 is only 50 ns. As a result of that, the output of the system will be saturated at around 30 ns, if linearity better than 2 % is required. This suggests that the default SSTC is not able to meet this characteristic of the telescope. A large SSTC is needed for this requirement. However, due to the interference

from the HG, a large TD is necessary to avoid the nonlinearity. Therefore, series of tests on the relations between the different SSTCs and the TDs, including 50 ns, 75 ns and 100 ns of the SSTC and the TD from 1 to 64, have been performed and studied. Based on the result, the SSTC = 100 ns and the TD = 39 ns is an appropriate option for WFCTA.

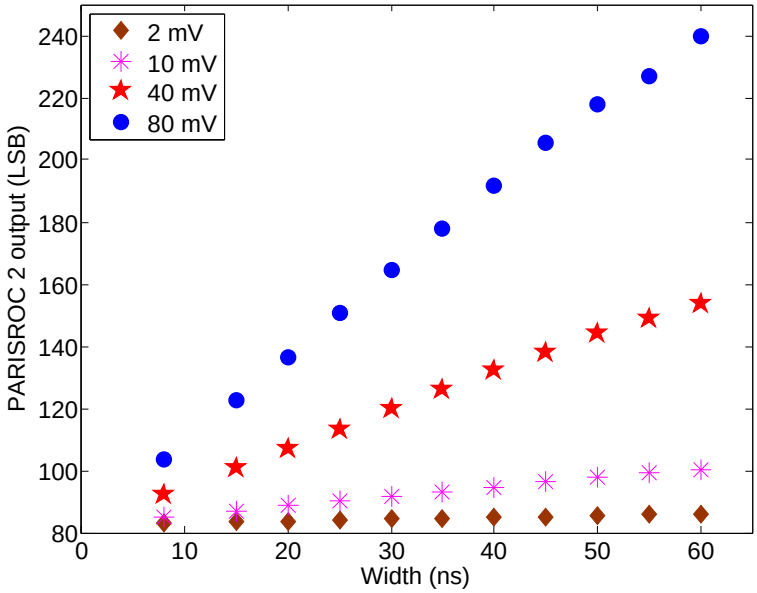


Figure 6.5: Output of PARISROC 2 vs. signal duration. The brown diamond, red star, magenta asterisk and blue dot represent the amplitudes of the signals which are fixed at 2 mV, 10 mV, 40 mV and 80 mV, respectively.

By using this new configuration, the linearity test of the duration-varied signal has been repreformed. Figure 6.5 shows that the different results obtained for amplitude 2 mV to 80 mV and duration times from 8 ns to 50 ns. They all show linearity which is better than 0.4 % [Chen, 2013]. This indicates that the PARISROC 2 can deal with duration-varied signals by properly selecting the slow control parameters. Moreover, it fulfills the requirement of WFCTA on the pulse width from 6 ns to 50 ns for the Cherenkov mode.

6.1.4 Event rate and pedestal monitoring

The event rate of the ASIC chip has been studied with different groups of tests to understand the relation between the event rate and the configuration of the chip. In these tests, a fixed input signal has been used. The event rate is calculated at the host computer.

The results show that the event rate for a single channel is mostly affected by the TDC unit. The SSTC and the TD have little influence on the event rate. The maximum single channel event rate (SCER) is around 60 kHz when the TDC is on and 130 kHz when the TDC is off. The maximum SCER can reach around 135 kHz when only one channel is triggered and around 8.4 kHz when all 16 channels are triggered simultaneously. The SCER is slightly affected by the amplitude, the width of the signal and the gain of the channels. Nevertheless, the number of triggered channels is the key point of the SCER. When the number of the triggered channels is increasing, the SCER will drop very fast.

However, based on the design of the PARISROC 2, due to the of the Wilkinson ADC in the digital unit, the ASIC needs more time to convert large analogue signals. Therefore, the random signals with different amplitudes and durations will aggravate the burden of the ADC and increase the conversion time. According to the datasheet, the event rate of the chip should be above 20 kHz for the fixed-amplitude signals to cover the worst situation and to achieve an average event rate of 5 kHz.

The phenomenon of the event loss has also been found in these tests. After several studies on this, the reason of this problem was finally found. It is due to the performance of the FPGA and the FTDI USB (universal serial bus) communication interface which are used on the PMm^2 application board. An example of this phenomena is shown in figure 6.6. In the oscilloscope screens, the green curve is the trigger signal from signal generator, the yellow one is the output of the fast shaper and the blue one is the not-delayed trigger signal generated by chip itself. If there is no trigger missing, for example, when only one channel has been triggered, the curve is shown in the left picture of figure 6.6. On the contrary, when 7 or 8 channels have been triggered, one can observe missing triggers (presented in the right picture of the figure). From this point, the FPGA and the interface should be different in the new design to improve the performance of the event rate and eliminate the missing trigger phenomenon.

For the pedestal monitoring, because the capacitor in series installed at the input port of the chip stops the DC component of the input signal, the only pedestal that can be observed is an artificial pedestal from the ADC conversion. The pedestal of input signal cannot be obtained from the output directly. One solution for this is to use an external trigger to monitor the pedestal variation caused by the night sky background. However, due to the lack of this port, the function is not supported by the PMm^2 application board. This will be implemented for the new electronics.

Figure 6.6: Comparison of the output of the non-delayed trigger with and without trigger missing. The left picture is the output of the non-delayed trigger without trigger missing. The right picture is the output of the non-delayed trigger with trigger missing. The green curve is the trigger signal from the signal generator. The yellow one is the output of the fast shaper. The blue one is the non-delayed trigger signal generated by chip itself.

6.1.5 PMT measurements

The performance of the PARISROC 2 chip was also evaluated with signals from the candidate PMT of the WFCTA telescopes. The model of the PMT is CR303, which is manufactured by Beijing Hamamatsu. Two prototype bases have been designed and fabricated for this PMT. The tests were performed by a standard NIM system and the PARISROC 2 test bench. As a preliminary test, the single-photoelectron response (SPR) and the PMT gain have been measured.

Figure 6.7 shows the single-photoelectron response measured by the standard NIM system as well as by the PARISROC 2 test bench. The blue-dash line and the red-solid line represent the results obtained by the standard NIM system and by PARISROC 2, respectively. To obtain these results, a high voltage of -1250 V was applied to the PMT. As shown in this figure, the two SPR distributions are very similar but have different location and height. This is due to two factors. The first one is the different gains of preamplifiers between the NIM system and the PARISROC 2. This affects the location of the pedestal and the peak of the single photoelectron. The second one is that the PARISROC 2 uses a threshold to trigger acquisition instead of a synchronized external trigger. Therefore, it is not easy to control the ratio of single photoelectron events to total events. This affects the number of the effective events. These two points can explain the slight differences seen in the spectrum measured by the standard NIM system and by the PARISROC 2 test bench.

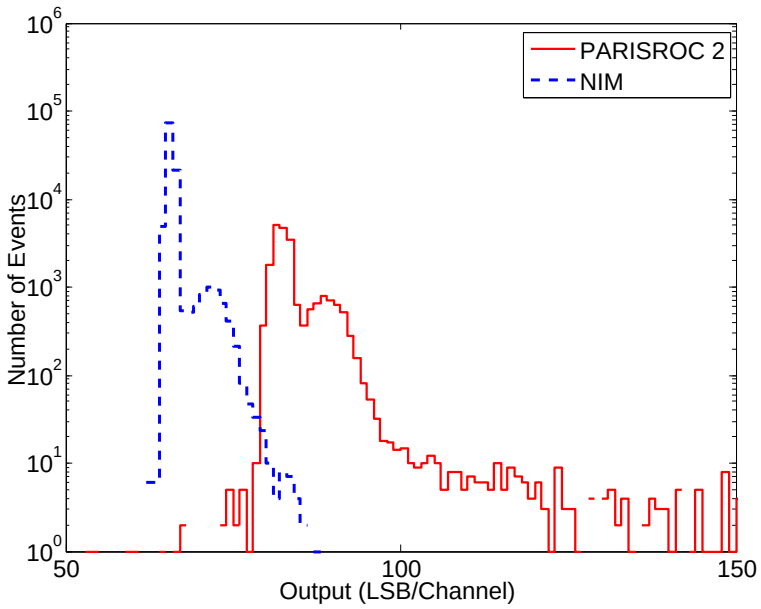


Figure 6.7: Single photoelectron response measured by PARISROC 2 and NIM. The blue-dash line and the red-solid line represent the results obtained by a standard NIM system and by PARISROC 2, respectively.

According to these results, the SPE peak-to-valley (P/V) ratio of CR303 is around 1.87 with the NIM system and around 1.35 with PARISROC 2 [Chen, 2013]. The P/V ratio measured by PARISROC 2 is smaller than the result of the NIM system, which is due to a slightly larger pedestal distribution caused by noise. There are also some high-energy events forming a small tail of the distribution obtained by PARISROC 2. It is clear that the PARISROC 2 has ability to distinguish the single photoelectron from the background noise confirming its good performance in terms of resolution.

6.1.6 Brief summary of the preliminary test results

Even though the PMm^2 application board is not designed and optimized for the WFCTA, it is still a good beginning for the designers who want to be familiar with the chip and to understand the basic principles of it. Different types of tests and studies on PARISROC 2 have been performed with this board and compared to the WFCTA telescope. According to the preliminary results, this chip only partially fulfills the requirement of WFCTA with this existing board by carefully choosing the slow control parameters. However, due to the limitation of the application board, the full performance and all the characteristics of the ASIC is still unclear. In order to improve the performance of the elec-

tronics and to further understand the characteristics of the chip, a new front-end electronics dedicated to WFCTA is necessary.

6.2 Design and implementation of the new FEE

To overcome the limitations of the existing board and to meet the requirements of the new prototype telescope, a new front-end electronics system is necessary. This readout system must be suitable for testing and should be easily installed in a telescope. In another words, it must meet the electrical and the mechanical requirements at the same time. The application information of PARISROC 2, the conceptual design and the implementation of the new front-end board will be presented and discussed in this section.

6.2.1 Application information of PARISROC 2

The structure and the description of the PARISROC 2 have been already introduced in Chapter 5. In this section, we only focus on the application information of the chip, including the basic characteristics, the pin-out, the data structure of shift registers and the frame structure of the output of the ASIC. More information can be found in [OMEGA microelectronics, 2012].

Basic characteristics of the PARISROC 2

The basic characteristics of the PARISROC 2 are presented in table 5.3. As shown in the table, the typical package of this chip is CQFP-160 (Ceramic Quad Flat Pack) or TQFP-160 (Thin Quad Flat Pack) package, whose dimensions are both 33 mm $\times$ 33 mm (1089 mm^2) (See figure 6.8). The QFP-type package is usually used in the test of the ASIC, but its dimension is too large for a compact design. In future, it will be replaced by the BGA (Ball Grid Array) package to reduce the occupied area.

Pin-out of PARISROC 2

As a mixed-signal integrated circuit, the analog parts of this chip are very sensitive to noise. All the power supply pins should be isolated from each other. To suppress the noises on the power line, the ferrite chip beads can be used as high efficiency EMI (Electro magnetic interference) suppression filters (EMIFIL) to isolate different power lines and to decrease noises on them. On an application board based on PARISROC 2, the analog power supplies are divided into 6 different parts. At the same time, at least one kind of decoupling

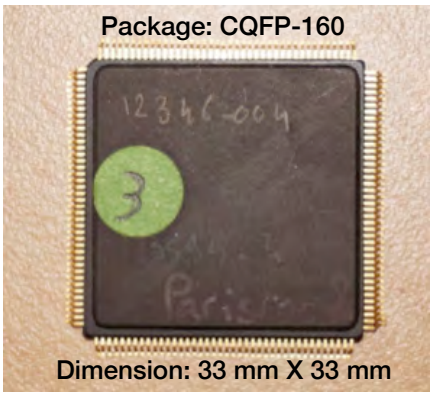


Figure 6.8: Picture of a PARISROC 2 chip with CQFP-160 package

capacitor with correct value is needed to lower the impedance of the power delivery system (PDS). Generally, the value of these capacitors is 0.1 μF. All of them must be placed to the pins as close as possible. The analog and digital power planes should be separated from each other.

The figure 6.9 shows a schema of the pin-out of the chip. It also shows the proportion between the die and the package. As shown in the figure, the PARISROC 2 has 160 pins, which can be divided into 4 different types. The types and the numbers of pins are listed in table 6.2.

Table 6.2: Pin types of PARISROC 2

Pin type	Sub type	Pin number
Power supply (55)	Substrate GND	13
	Analog GND	15
	Digital GND	3
	Analog VDD	21
	Digital VDD	3
Analog Bias (41)	Voltage Bias	17
	Current Bias	24
Analog I/O (21)	Input	18
	Output	3
Digital I/O (41)	Input	13
	Output	23
	LVDS Clock	4
NC	Not connect	2

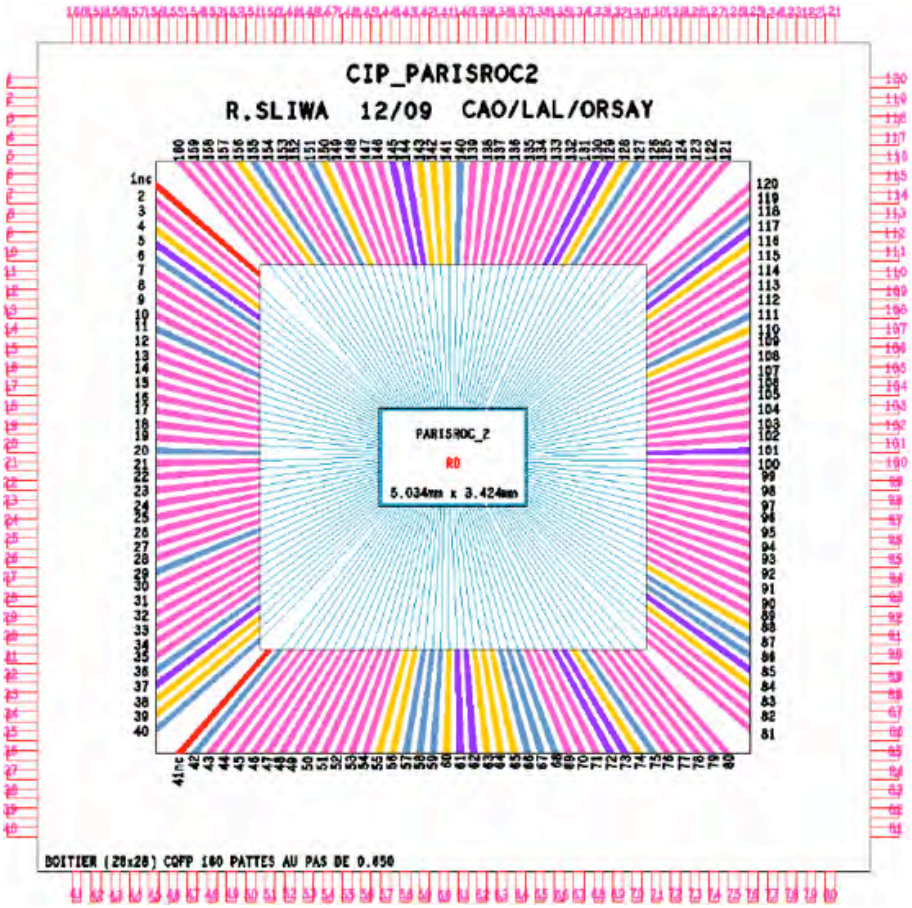


Figure 6.9: Schema of pin-out of PARISROC 2

There are 16 analog inputs in PARISROC 2, which are used to connect the external signals or the PMTs. Another 5 pins of them are special pins for different purposes, such as calibration signal input, external input for ADC and so on. The impedance of the inputs and the routing metal layers must be matched to reduce the signal reflection.

The bias pins of the chip have to be treated carefully as well. According to the table, the chip has 41 analog bias pins. Some of these pins are only designed for testing and used as observing ports to help designer monitor the chip. In fact, there are only 13 pins to be used to compensate the chip. The other pins are useless and have to be connected to the bypass capacitors to keep the chip stable.

The power supply of PARISROC 2 is +3.3 V. It demands that the FPGA must support the LVTTL-3.3 (Low-Voltage TTL) or LVCMOS-3.3 (Low-Voltage CMOS) single-ended I/O standards. The LVDS-3.3 (Low-Voltage Differential signaling) standard is also necessary for the clock signals.

There are 2 internal shift registers in the chip, which store the parameters of the SCU (Slow control unit) and the PCU (Probe control unit). They are controlled by 4 digital I/Os individually. Due to the lack of the enable pins for these registers, in a multi-PARISROC application, the control lines of different chips should be separated.

Two pairs of LVDS clocks, which are 40 MHz and 10 MHz, are connected to the ASIC for different purposes. The 10 MHz clock is used for data transmission, especially for the two internal control registers mentioned above. It is also used for the time measurement. The 40 MHz clock is used by the internal Wilkinson ADC and for the output of acquired data. These LVDS clocks must be accurate and matched. Otherwise, they will degrade the performance of the data transfer and the precision of the time measurement.

For the digital pins, due to the design of the ASIC, 18 digital outputs related to the trigger are designed for monitoring and debugging. The trigger information of each channel is already included in the digital serials output data. Therefore, these pins can be ignored in an application design. Generally speaking, a single PARISROC 2 chip requests at most 62 I/Os or at least 37 I/Os. The selection of the FPGA will depend on this.

Data structure of shift registers of PARISROC 2

As descried above, 2 internal shift registers are included in PARISROC 2 chip. They are very important registers that store the parameters of different control units. For example, the slow control parameters are stored in one of the shift registers. Their values directly

determine the performance and the behavior of the chip. Therefore, understanding the structure of this register is an essential part of the design.

The probe control register is designed to select the internal signals to analog or digital output pins. It can be used to help designers to monitor or debug the chip. The length of this register is 260 bits and can be divided into 9 groups. Normally, the values of this register are all logic zero. The structure of the probe control register is shown in figure 6.10.

Bit 259	TDC Ramp	Bit 258	
Bit 257	TDC Start Ramp	Bit 256	
Bit 255	Preamp HG & LG Output	Bit 224	CH15HG + CH15LG + ... + CH00HG + CH00LG
Bit 223	Slow Shaper & Fast Shaper Output	Bit 176	SSH_HG_CH15 + FSH_CH15 + SSH_LG_CH15 + ...
Bit 175	5 Digital Signals for SCA	Bit 096	
Bit 095	2 Digital Signals for TAC	Bit 064	
Bit 063	Trigger Delayed & Not Delayed Output	Bit 032	
Bit 031	Read TAC Register to Read Time	Bit 016	
Bit 015	Read SCA Register to Read Charge	Bit 000	

Figure 6.10: Data structure of the probe control register of PARISROC 2

The structure of the slow control register is shown in figure 6.11. The length of the register is 278 bits. Each of them represents a slow control parameter. The parameters can be divided into 29 different groups. These groups are used to control all the aspects of the chip from setting thresholds to enabling or disabling functional units. Choosing the right values and setting them should be done prior to any other operations of the chip.

All these registers are synchronized to a 10 MHz clock. It implies that it will cost 26 μs to shift 260 bits parameters into the probe register or 27.8 μs to shift 278 bits parameters to the slow control register. It also means that there is a 27.8 μs dead time after the chip has been reconfigured.

Frame structure of the digital output of PARISROC 2

The PARISROC 2 chip is designed to send out the charge and the time measurements by only using two lines, which are the digital output (d_out) and the flag signal for data sending (TransmitOn). The logic one on the TransmitOn pin indicates the sending data procedure on. The effective data is coming out from d_out port simultaneously. Every 51

Bit 277	10 bits DAC threshold Discri 1	Bit 268	MSB --> LSB
Bit 267	10 bits DAC threshold Discri 0	Bit 258	MSB --> LSB
Bit 257	10 bits DAC threshold Discri Gain	Bit 248	MSB --> LSB
Bit 247	DACs Power Pulsing	Bit 244	SW_DAC, EN_DAC2, EN_DAC1, EN_DAC0
Bit 243	Bandgap Power Pulsing	Bit 242	EN_BG, SW_BG
Bit 241	Ramp TDC Power Pulsing	Bit 240	EN_INTEGTDC, SW_INTEGTDC
Bit 239	ADC Precision Choice	Bit 238	
Bit 237	Mask Discriminators	Bit 206	D0CH0 + D1CH0 + … + D0CH15 + D1CH15
Bit 205	Disable Output Buffers	Bit 202	EN_CLK10, EN_CLK40, ENB_TRIG, ENB_OR
Bit 201	Delay for the trigger	Bit 196	MSB --> LSB
	Trigger Polarity Choice	Bit 195	
	Trigger Input Choice	Bit 194	
	Trigger Output Choice	Bit 193	
Bit 192	Discri Power Pulsing	Bit 190	EN_GAINDISCRI, EN_DISCRI01, SW_DISCRI
	ADC Discri Polarity Choice	Bit 189	
Bit 188	ADC Discri Power Pulsing	Bit 187	EN_DICRIADC, SW_DISCRIADC
	ADC Input Choice	Bit 186	
Bit 185	Ramp Choice	Bit 184	
Bit 183	Gain Choice	Bit 182	
Bit 181	TAC Power Pulsing	Bit 180	EN_TAC, SW_TAC
Bit 179	SCA Power Pulsing	Bit 178	EN_SCA, SW_SCA
Bit 177	OTAS Power Pulsing	Bit 175	SW_OTAS, EN_OTAS, EN_OTAS_PRB
Bit 174	Fast Shaper Power Pulsing	Bit 173	EN_FSH, SW_FSH
Bit 172	Slow Shaper Power Pulsing	Bit 169	EN_SSH_LG, SW_SSH_LG, EN_SSH_HG, SW_SSH_HG
Bit 168	Slow Shaper Gain	Bit 167	
Bit 166	Slow Shaper Time Constant	Bit 164	
Bit 163	Preamp Power Pulsing	Bit 160	EN_PA_HG, SW_PA_HG, EN_PA_LG, SW_PA_LG
Bit 159	Gain Preamp Compensation	Bit 032	CH15SW_CFB7 to CH15SW_CFB0 … CH00SW_CFB7 to CH00SW_CFB0
Bit 031	Enable Input Test	Bit 000	CH15HG + CH15LG +… + CH00HG + CH00LG

Figure 6.11: Data structure of the slow control register of PARISROC 2

bits can be treated as a PARISROC frame and contain all the information generated by the ASIC . The structure of the digital output frame is shown in figure 6.12.

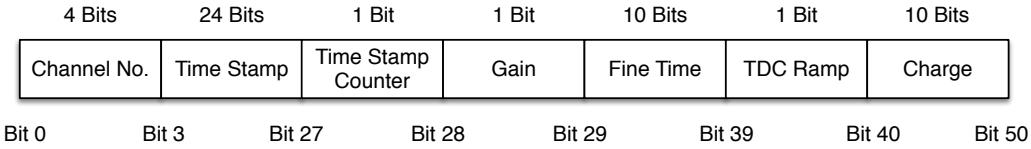


Figure 6.12: Frame structure of the digital output of PARISROC 2

Each frame contains 4-bits trigger channel number in gray code, 24-bits time stamp in gray code, 1-bit time stamp counter symbol, 1-bit gain channel symbol, 10-bits fine time in gray code, 1-bit TDC ramp symbol and 10-bits charge in gray code. A single frame is equivalent to about 7 bytes.

The output is synchronized to a 40 MHz clock signal. Therefore sending a frame will take 51 clock periods or 1.275 μs. Transferring all 16 channels data will consume at least 20.4 μs without considering the dead time between each frame. The maximum data output rate of PARISROC 2 will not exceed 50 kHz even if the dead time is zero, when 16 channels are triggered.

Theoretically, the single channel event rate of the PARISROC 2 chip is from 5 kHz (worst case) to 20 kHz (best case). Hence, if all 16 channels are triggered simultaneously, the data output rate of the ASIC will vary from 0.51 Mbyte/s (4.08 Mbit/s) to 2.04 Mbyte/s (16.32 Mbit/s). For the PMm^2 application board, the data output rate is from 0.56 Mbyte/s (4.48 Mbit/s) to 2.24 Mbyte/s (17.92 Mbit/s), due to its specific data structure which is longer than the default one.

6.2.2 Conceptual design of the front-end electronics

For a purpose of simplifying the system, decreasing the power consumption and increasing the stability, the reliability as well as the maintainability, the new FEE is designed as an autonomous or semi-autonomous module (subcluster) of multiple pixels. Based on the requirement, the proposed electronics is designed as a subcluster module of 16 pixels, each pixel corresponding to a PMT output.

Figure 6.13 shows a sketch of a modular subcluster. It consists of five main parts: photomultipliers, high-voltage module, front-end electronics, backplane board and the frame to sustain and fix all these components. The basic idea of the design is that the front-end electronics can be attached directly to the PMT array and pass the preprocessed or

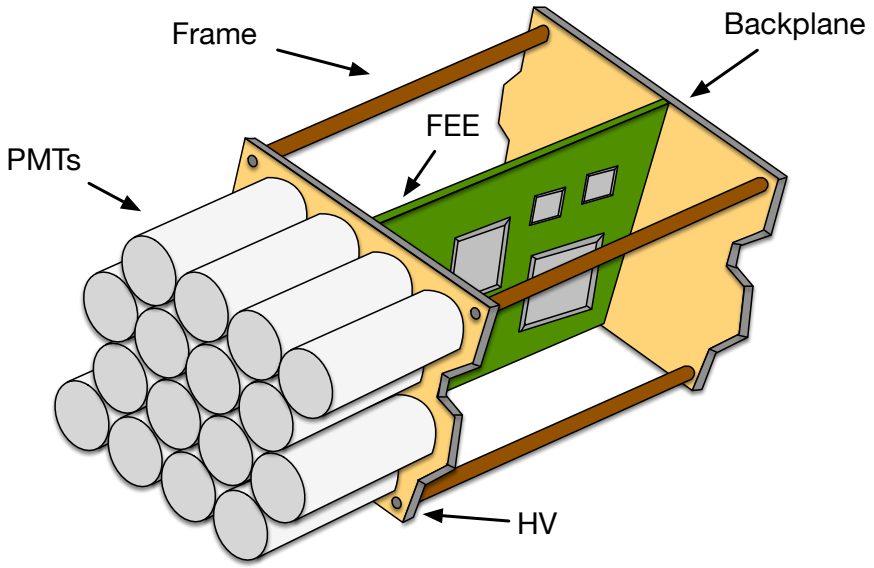


Figure 6.13: Sketch of a modular subcluster FEE

processed data to the motherboard through the backplane or to the host computer through the Ethernet.

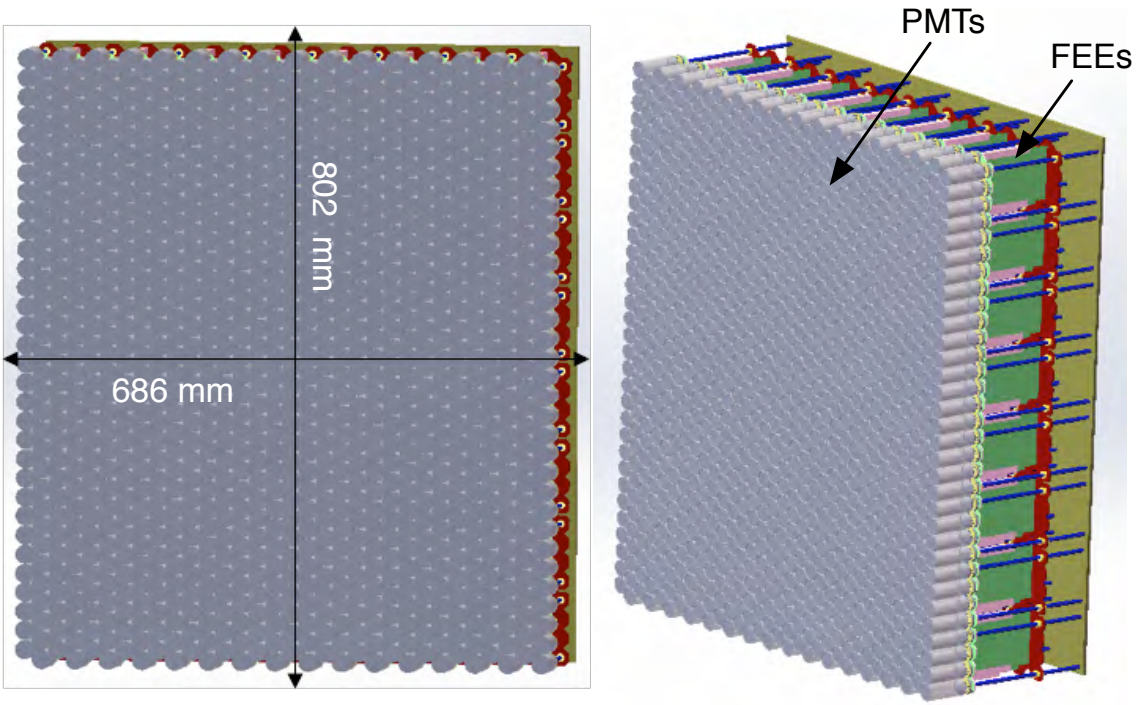


Figure 6.14: Sketch of the imagining system of WFCTA including PMTs and FEEs

Thus, the combination of several subclusters build the camera of the telescope. According to the requirement, the camera will be constructed with 8 × 8 modular subclusters. The sketch of the imagining system of WFCTA including PMTs and FEEs is presented in figure 6.14. The dimension of the camera is 802 mm × 686 mm which is estimated with the diameter of the PMT (25.4 mm). The width of each front-end board can be also derived and should be less than 80 mm.

According to the previous test results, the upper limit of the dynamic range of a single channel of PARISROC 2 is smaller than the requirements of WFCTA.To reach the required dynamic range, two PARISROC channels have been connected by replacing the 50 Ω matching resistor with a voltage divider to change the voltage distribution between these two channels (See figure 6.15). This extends the dynamic range of the second channel while keeping good linearity. As an example, the sum of the value of RX and RY must be 50 Ω and if the value of each resistor is 25 Ω, the upper limit of the dynamic range of the second channel would be twice of the first one. The lower limit would also increase accordingly. It is obvious that by using this configuration, PARISROC 2 can easily obtain the required dynamic range (three orders of magnitude). The other advantage of this configuration is that it could avoid the output discontinuity when it switches from the high-gain to the low-gain channel. Two ASICs are required on the board to satisfy the requirement of the number of the channels.

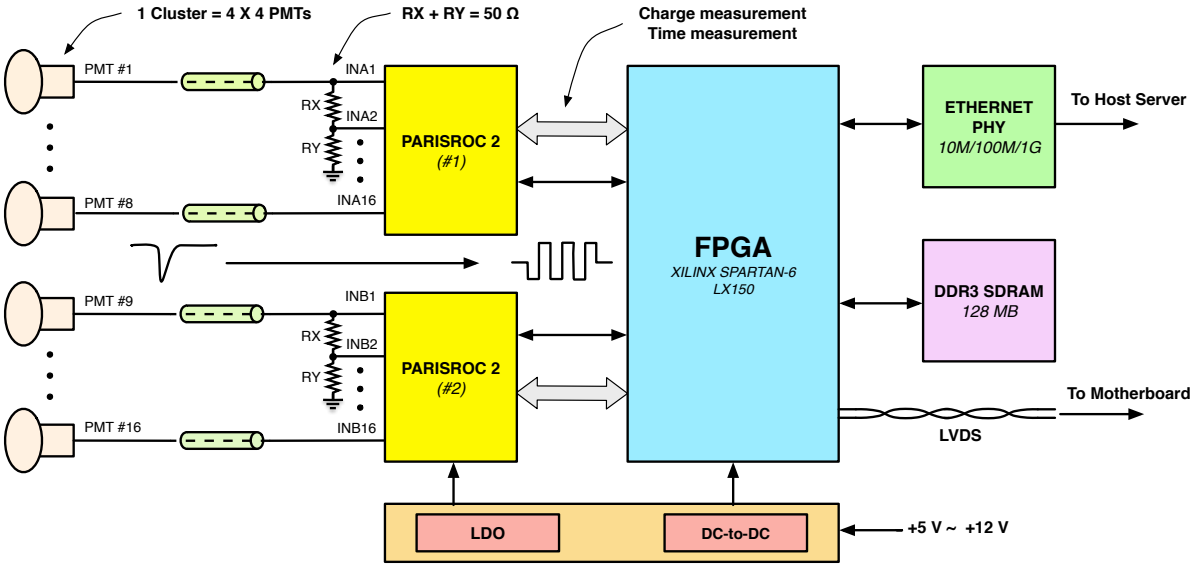


Figure 6.15: System block diagram of the front-end electronics based on PARISROC 2

A FPGA is exploited in the FEE to control the two chips and handle with the data processing. The digitized charge and time measurements are acquired and processed by the FPGA and stored in an on-board high-speed memory. Considering the requirement of the bandwidth for the data transmission and for the future additional extensions, a gigabit Ethernet transceiver is integrated on board to transfer data packets and control commands though Ethernet. Multiple pairs of low voltage differential signaling (LVDS) connections are reserved to exchange data through the backplane. They can be used to transmit data, to distribute clock signals and to send control commands. The low dropout regulators and the DC-to-DC converters are integrated on board to match the voltage requirements and to satisfy the power consumption limits. The system block diagram of the front-end electronics based on PARISROC 2 is shown in figure 6.15. Moreover, in order to achieve high performance and to reduce the power consumption as much as possible, the software in the FPGA should be described with VHDL (VHSIC Hardware Description Language).

6.2.3 Hardware implementation of the front-end electronics

Following the conceptual design, the front-end board has been designed, implemented and fabricated. The board is designed for a subcluster with 16 inputs which correspond to each output of the PMTs. The SMA connectors are used to provide high-quality and reliable connections for PMTs. In the the front-end board, the signals are divided into two groups which are processed by two PARISROC 2 chips separately in order to achieve the requested dynamic range and to improve the event rate. The final dimension of the board is 140 mm $\times$ 80 mm which meets the requirement of WFCTA. The detailed information about the hardware and software implementation of the board, including the selection of the FPGA, the DC regulators and the communication interface, is presented in this subsection.

Selection of FPGA

As the control unit of the system, the FPGA is the key point. The choice of it will greatly affect the performance of the whole system. Normally, the selection is limited by the area, I/O requirements, the power consumption and the cost. Considering that this prototype is designed for the subclusters of WFCTA telescopes, the high-end FPGAs like Virtex from Xilinx or Stratix from Altera are out of option. Making compromise between all the facts, Spartan-6 series FPGA could be the optimum choice.

Furthermore, the possibility of revising the PCB board multiple times in the prototype phase forces us to reduce the cost. A mezzanine board integrating all necessary chips

would save us time and money. After several investigations, a board named TE0600 [Trenz electronic, 2012] and designed by Trenz electronic was chosen. Figure 6.16 shows the top and bottom view of the mezzanine board. The most important advantages of this board are its size and integrity. It only occupies an area of 20 cm^2. It also integrates DC regulators, Ethernet PHY controller and DDR3 SDRAM on it. Due to these characteristics, it can be easily implanted into our new front-end electronics system.

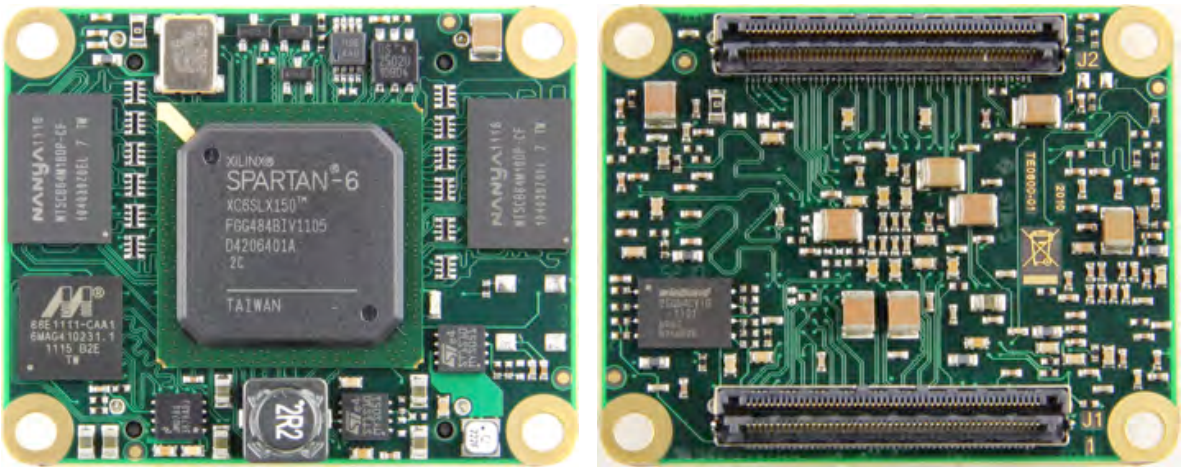


Figure 6.16: Top and bottom view of GigaBee XC6SLX (TE0600)

Selection of DC regulators and estimation of power consumption

The option of regulators mainly depends on two points: the input voltage scale and the power requirement of the chips. According to the datasheet [OMEGA microelectronics, 2012], the power consumption of each channel of PARISROC 2 is about 15 mW. Therefore, all 32 channels of two chips will consume 480 mW and the maximum current will be around 146 mA. The digital parts of the chip almost consume nothing compared with the analogue parts. Therefore, the key point is how to provide power to these sensitive analogue components and to decrease the noise levels.

However, ASICs are not the most power consuming components on the board. The power consumption of a FPGA is composed by three parts. The core, the I/Os and the auxiliaries. Each of them has its own different requirement. In the extreme condition, the power consumption of the XC6SLX150 could exceed 20 W for the 3.3 V I/O standards. Its maximum current is about 6 A in this case. The more accurate power consumption can be estimated after the design of the software by using the Xilinx power estimator (XPE) [Xilinx, 2012] which is provided by Xilinx.

However, even it is impossible to achieve such high power consumption in our design, to be on the safe side, TPS54620 [Texas Instruments, 2009], a 4.5V to 17V input, 6A DC/DC converter provided by Texas Instruments is applied in this system to meet the electrical requirement and placement. The power solution for the ASICs is also from Texas Instruments. An 800 mA, low noise micro-power adjustable regulator, LP3878 [Texas Instruments, 2005], has been selected. Two of them are used to provide current to the analog parts and to the digital parts separately.

All these chips support a wide input voltage scale from 4.5 V to 16 V. It suggests that this board can easily adapt the same input voltage scale, which fulfills the requirement of WFCTA.

Selection of communication interface

The selection of the communication interface mostly depends on the bandwidth requirement and the cost of the application. Normally, the serial communication will be the first option for most electronics system. Although there are dozens of serial communication architectures in modern electronic designs, the USB and the Ethernet are the most popular ones. They can be easily developed and cheaply implemented. For example, one can always find these ports from a PC or a Server. Considering short-distance data transferring (only centimeters or meters), USB interface has its advantages. The Ethernet will be more reliable when this distance extends to kilometers.

On the LAL test board [S. Conforti Di Lorenzo et al., 2012] and the PMm^2 [Campagne et al., 2011] application board, the designers used the FT245X series chip from FTDI Ltd. for communication and debugging. The FT245X series chips are USB to parallel FIFO interfaces. Usually, these chips are used in system debugging, monitoring and a small amount of data transmission. The FTDI Ltd. claims these chips are USB 1.1 or USB 2.0 compatible. However, even the latest chip in this family, FT245R [FTDI, 2010] only supports USB Full Speed mode. It means that the maximum data transfer rate of this chip is only 12 Mbit/s or about 1.5 Mbyte/s. According to the reference manual, the actual rate of this chip will not exceed 1 Mbyte/s with D2XX Direct Drivers and 300 Kbyte/s with VCP Drivers.

As described in the previous section, the data output rate of PARISROC 2 is from 0.51 Mbyte/s at 5 kHz event rate to 2.04 Mbyte/s at 20 kHz event rate. Hence, if the ASIC only works at 5 kHz, the interface is able to deal with them. At the same time, if the event rate increases to 10 kHz, the output data channel will be blocked. The FPGA has to stop the

acquisition and to wait until the communication interface clears the cache. It is the reason why the PMm^2 application boards and the LAL test board cannot achieve the expected event rate.

Considering all these points and in order to be compatible with the communication system of WFCTA telescopes, an interface based on 1000 M Ethernet is proposed and integrated in the electronics. The theoretical bandwidth of the interface is 1000 Mbit/s. Generally, 90 % of the bandwidth can be easily achieved. Even for a telescope, this bandwidth is absolutely large enough. The Ethernet transceiver is integrated on the mezzanine board with the FPGA.

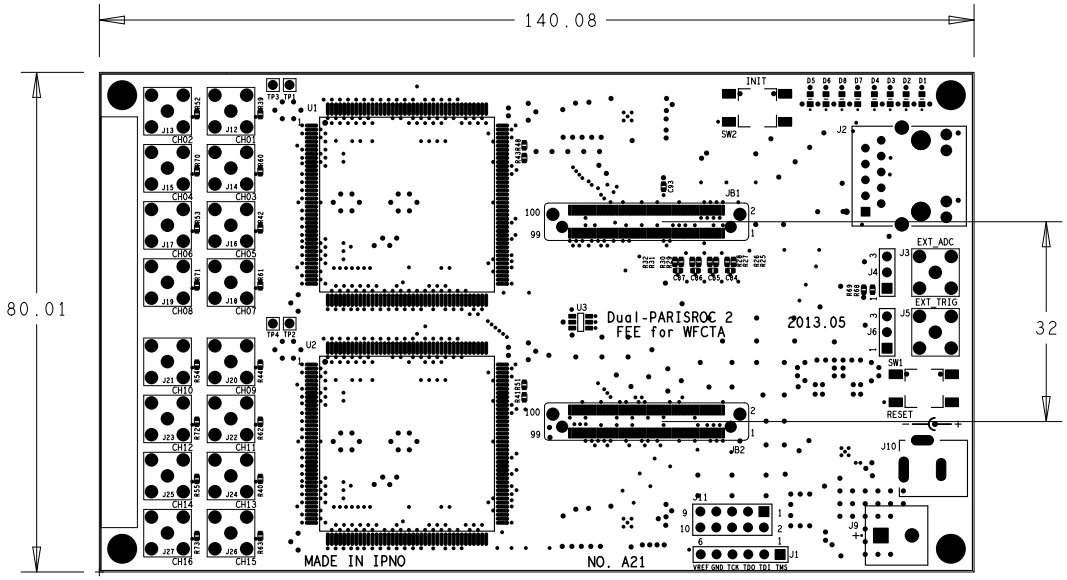
Furthermore, the possibility of using white rabbit (WR) protocol [Jansweijer, 2013] is another motivation for adopting Ethernet interface. The WR is developed to synchronize nodes in a packet-based network with sub-ns accuracy. The protocol results from the combination of IEEE 1588-2008 (Precision Time Protocol, PTP) [IEEE, 2008] with two further extensions: automatic precise measurement of the link delay and clock synchronization over the physical layer with synchronous Ethernet (SyncE).

The Ethernet is a high-level data transfer interface between systems like telescopes and host computer. It is usually too complicated for a subcluster. On the other hand, the data transfer mode of PARISROC 2 is serial data transfer. Hence, the first option of a subcluster is still to transmit data across a backplane by using multiple differential pairs. For a Spartan-6 FPGA, by using SERDES unit [Xilinx, 2013], which is included in normal IOB blocks, the data transfer rate can be easily up to 500 Mbit/s. This value is already 20 times of the maximum data output rate of the ASIC. It fully satisfies the requirement of the telescope.

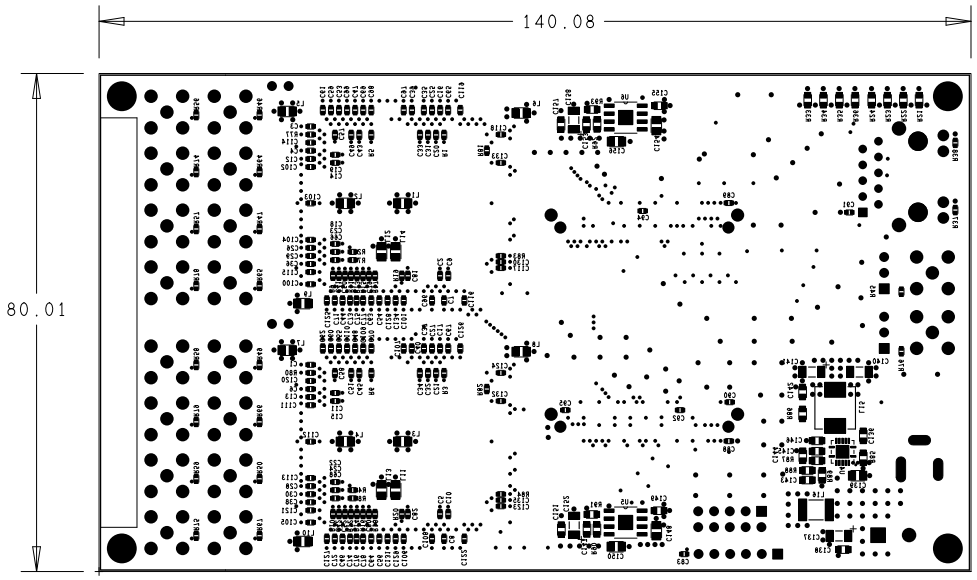
6.2.4 Final assembled board

With the help of the SEP of IPNO and the OMEGA group, two prototypes of the new front-end electronics were designed, fabricated and assembled in France. The PCB layout of the new front-end electronics is shown in figure 6.17.

The board is a six-layer PCB board with 4 internal layers. It contains three signal layers including top layer, bottom layer and one internal layer, two ground planes and one power plane. The impedances of the single micro-strips or the differential micro-strips on the signal layers have been adjusted to 50 Ω and 100 Ω to satisfy the requirements. The main connectors as the SMA, Ethernet port, power jack, pin headers as well as the ASICs and the FPGA mezzanine board are assembled and installed on the top side. All the DC



(a) Top view of PCB board



(b) Bottom view of PCB board

Figure 6.17: PCB layout of the new front-end electronics. The top view and bottom view are shown in figure 6.17a and 6.17b.

regulators and corresponding components are assemble at the bottom side to increase the distance to the sensitive analog signal and reduce the noise. From the figure 6.17a, it is clear that the ASICs occupy the largest space on the board, due to their TQFP packages. This package should be replaced by the BGA package in the future. Figure 6.18 presents the picture of the assembled board.

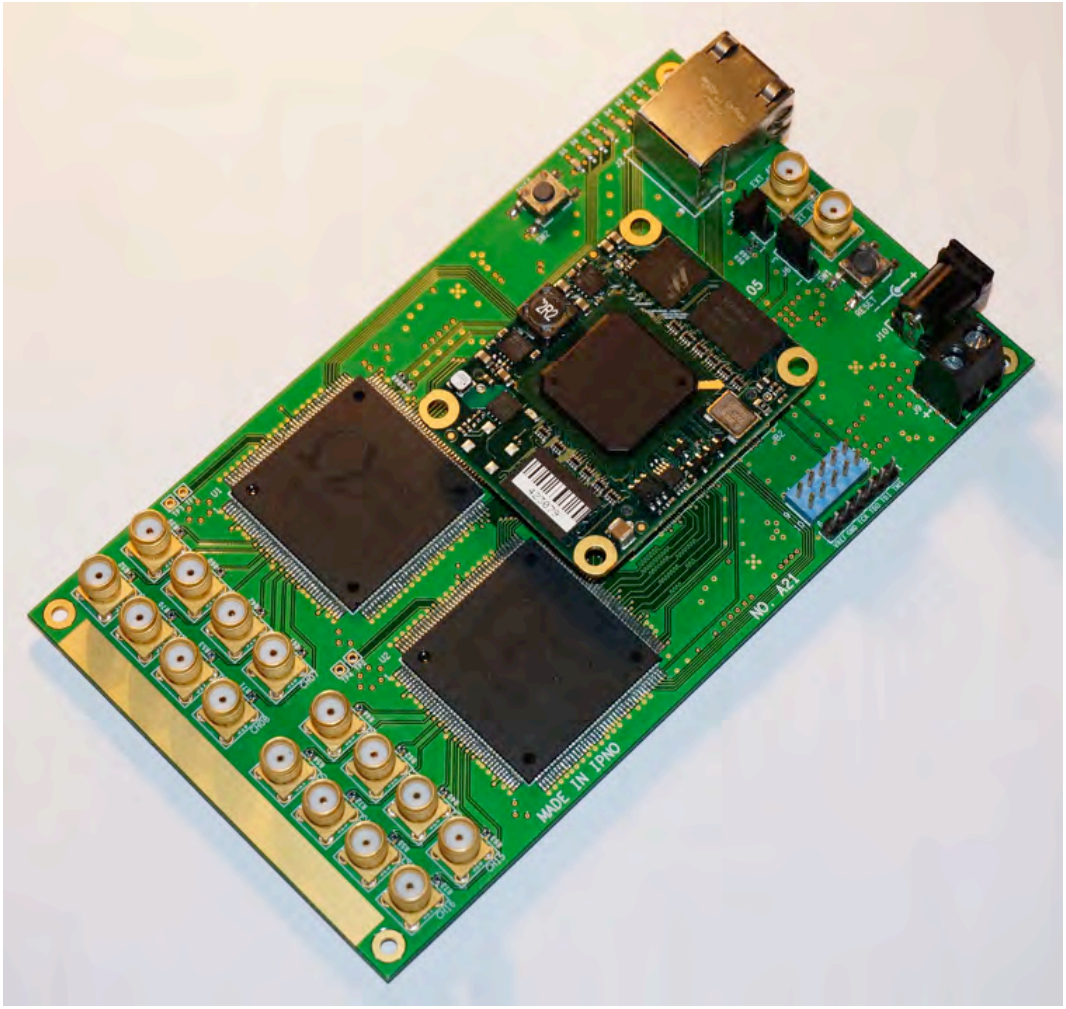


Figure 6.18: Picture of the final assembled board

6.2.5 Brief summary of the design and implementation of the new FEE

To conquer the imperfections and the shortcomings of the existing application board, to reveal all characteristics of the ASIC and to fulfill the requirements of WFCTA, a new front-end electronics based on two PARISROC 2 chips has been successfully designed, imple-

mented and fabricated. The detailed design information about the hardware and software implementation has also been discussed in this section, including the application information of the ASIC chip and the selection criterion of different components. To achieve high performance, the original communication system based on the USB interface is fully replaced by a new structure with a 1000 M Ethernet interface and two new transferring protocols. The discussion on the software implementation and the new communication system will be presented in the next chapter.

Chapter 7
DAQ system of the FEE

In principle, the data acquisition is a process of measuring real physical signals, converting them into digital forms and transferring them to a digital device for further data processing. Therefore, a data acquisition system (DAQ) usually consists of three main parts: sensors that are used to convert the physical signals (e.g., photons, sound) into the electrical signals (e.g., current and voltage), signal processing circuits that are used to amplify, filter and convert the analogue electrical signals into digital ones and a communication unit including an interface and a special protocol that controls the data exchange between the front-end circuits and the host computer. It usually contains both hardware and software implementations.

In the DAQ system which is proposed for front-end electronics, the PMT plays the role of the sensor. The front-end electronics is the hardware implementation of the system. The conceptual design and the hardware implementation of the DAQ system have been fully described in the Chapter 6. This chapter is focused on the corresponding communication system and the software implementation of the system. Based on this, the communication based on USB (universal serial bus) and Ethernet as well as the design and the implementation of the software of the system will be presented in this chapter. It will be mainly focused on the super light TCP/IP protocol suite that we developed and the protocols which are covered by this protocol suite.

7.1 Communication system and protocols

Generally speaking, there are several ways to build a communication system to exchange data between infrastructures, with a specific medium, such as light, copper and radio. A communication system is composed of a necessary hardware infrastructure and

the protocols. When the data is transmitted between electronic devices, it must follow some preexisting agreements and rules. The agreements and rules are the protocols in computer science. The protocol is a set of digital rules that regulates how the message should be constructed, sent, received and secured. Without a proper protocol, the communication cannot be established.

The performance of a DAQ system usually depends on the quality of the communication and is limited by the interface bandwidth and the characteristics of the protocol. In a modern electronic system, the most widely used communication systems are based on the USB and the Ethernet. This is due to their cheap prices, easy implementation and popularity. In this section, a communication system based on USB and network will be discussed.

7.1.1 Communication based on USB

The universal serial bus, USB, is an industry serial bus standard that defines the connection and the communication between computers and peripherals. The first release, USB 1.0 was developed and officially published in 1996. Nowadays, it has already evolved to its latest version which is USB 3.1 [USB Organization, 2013]. This new standard guarantees a data transmission rate of 10 Gbit/s, and was released in 2013. In the last twenty years, USB successfully replaced the earlier interfaces (i.e., serial and parallel ports) and became primary wire connection for the peripherals on computers. It has also been used as a power supply for the portable devices such as the cellphone and the DAQ system. Depending on the application, it supports different standard protocols, such as the bulk-only transport (BOT) protocol [USB Organization, 1999] and the USB attached SCSI protocol (UASP) [C. E. Stevens, 2010]. Besides, it also supports the user-defined protocols for special applications.

The application boards that were mentioned in the last chapter, the PMm^2 application board and the LAL test board, share almost the same hardware implementations (FT245X series USB interface) but adapt their own communication protocols in each design. The common points of these protocols will be discussed below.

LAL USB protocol

For the LAL test board [S. Conforti Di Lorenzo et al., 2012], which was used in the evaluation of PARISROC 1 and PARISROC 2, a user-defined USB protocol, which name is LALUsb [D. Breton, 2007], was used in the communication system to establish the con-

nection between the board and the computer. This protocol was developed by the LAL electronics department. It is an extension of FTDI library and provides a simplified error handling mechanism, a data encapsulation and the interrupts management complying with the specifications of the USB interface. It contains a full solution of the USB based communication from the design of the hardware to the program of the DAQ application. With it, a designer can easily realize a prototype DAQ system just following documentation.

Header:	0XAA
Control 1:	8-bit command
Control 2:	8-bit command
Data N:	0 < N < 65536
Trailer:	0X55

Figure 7.1: Basic data structure of the LALUsb frame

However, it is a very light protocol, which only supports the basic read and write operations. The error processing and the interrupts control are achieved by identifying the unique byte of the header, the tailer and special user data. The basic data structure of the LALUsb frame is shown in figure 7.1. It is a typical packet communication protocol. The header and the trailer with fixed values are used to identify a correctly transferred packet. The first control byte is used to store the number of data bytes for transferring, and the second one indicates the type of the operation (i.e., read or write) and the subaddress. For the writing operation, the length of the data is limited to 256 bytes. For the reading operation, the length of the data is up to 65,536 16-bit word. The detailed information can be found in [D. Breton, 2007].

The first version of this protocol based on FT245B supports the USB 2.0 full-speed standard, whose data rate is 12 Mbit/s. Even though LAL claims that the second version of this protocol, which is based on FT2232/FT4232 could benefit from the advantages of the USB 2.0 high-speed standard ($\sim$ 50 Mbit/s), the real performance of it is very limit. According to the experience on the test board, it could only achieve a data transfer rate of several kbyte/s, probably due to the FPGA implementation.

PMm^2 USB protocol

Compared with the LAL test board, the hardware implementation of the communication system in PMm^2 application board is similar. They both adopt the FT245X series FTDI USB controllers (FT245R for PMm^2 application board). The only difference between them are the communication protocols that are used.

The PMm^2 USB protocol is designed to control the PMm^2 application board and transfer the acquisition data to the computer. It is based on a protocol distributed by LAPP (Laboratorie d'Annecy-le-Vieux de Physique des Particules) [SEP, 2011]. The basic data structure of the PMm^2 USB protocol is shown in figure 7.2.

Start:	0X553A553A
PMm^2 Box control	32-bit command
Submarine control	32-bit command
Data N:	0 < N < 372
End:	0XA355A355

Figure 7.2: Basic data structure of the PMm^2 frame

The structure of this protocol is also simple expect that the width of the data is extended to 32-bit word. It starts with a special header and ends with a special footer. The PMm^2 box control command defines the type of the request, number of the 32-bit data word and the address of the application board. The submarine control command determines the operations and the number of the data word related to the submarine board. The upper limit of the length of the data sector is not clearly defined in [SEP, 2011], but it can reach at least up to 372 32-bit words. All the data is encoded in Manchester code format.

The real performance of this protocol is much higher than that of the LAL USB protocol, even if they share almost the same hardware infrastructure. In our tests, the data transfer rate of the PMm^2 USB protocol is close to its theoretical value, which is about 1.5 Mbyte/s. This improvement of the data rate is probably due to its FPGA software implementation and the acquisition software at the computer side.

By simply comparing the frame structures of these protocols, one can easily find out the common points of the communication protocols. A special protocol must start with a special header and end with a footer. These two components are the identifications of the protocol. The control commands and the data sector are located between the header and the

footer, but the number and the length of them can be defined by user for different purposes. Furthermore, in order to ensure the reliability and the security of the transmission, some protocols contain the checksum sectors. The checksum sector is located between the header and the footer as well, but the calculation of it should consider the values of the header and the footer. The most communication protocols follow these rules including the Ethernet protocols which will be presented in the following.

7.1.2 Communication based on network

Exchanging information on network is popular in modern electronic system. There two terms in this field: networking and internetworking. The networking is the process and the methodology of connecting different computers to exchange information among them, whereas the internetworking is the process and the methodology of connecting different networks, in despite of their infrastructures and distances [Syngress Media, 2001].

The embryo of the network and interwork appeared in late 1960s and was proposed by United States Department of Defense (DoD) to distribute, control and process military information over a large scale based on a packet-switched wide area network (WAN). The study on Advanced Research Projects Agency Network (ARPANET) eventually formed the cornerstone of today's Internet. The network was not widespread until the development of the personal computer (PC) in 1980s. Companies realized that sharing data and cooperating works by connecting PCs could greatly promote the productivity. As a result of that, the local area network (LAN) which is applied to connect local computers and the WAN, which is applied to connect LANs, were created and implemented.

OSI reference model

There are countless ways to send and receive data over the network. However, due to the requirement of interconnectivity and interoperability of the communication, the standards for defining and regulating data on the network are necessary. The well-known protocols are the Open System Interconnection (OSI) reference model and the Transmission Control Protocol/Internet Protocol (TCP/IP).

The OSI reference model is a conceptual model which was created by International Organization for Standardization (ISO) in 1984 [Syngress Media, 2001]. It divides, defines and reorganizes the communication into a seven-layer model that describes the behaviors and the functions of the different layers and the communications between them. The basic architecture of the OSI seven-layer model is shown by the left plot of figure 7.3.

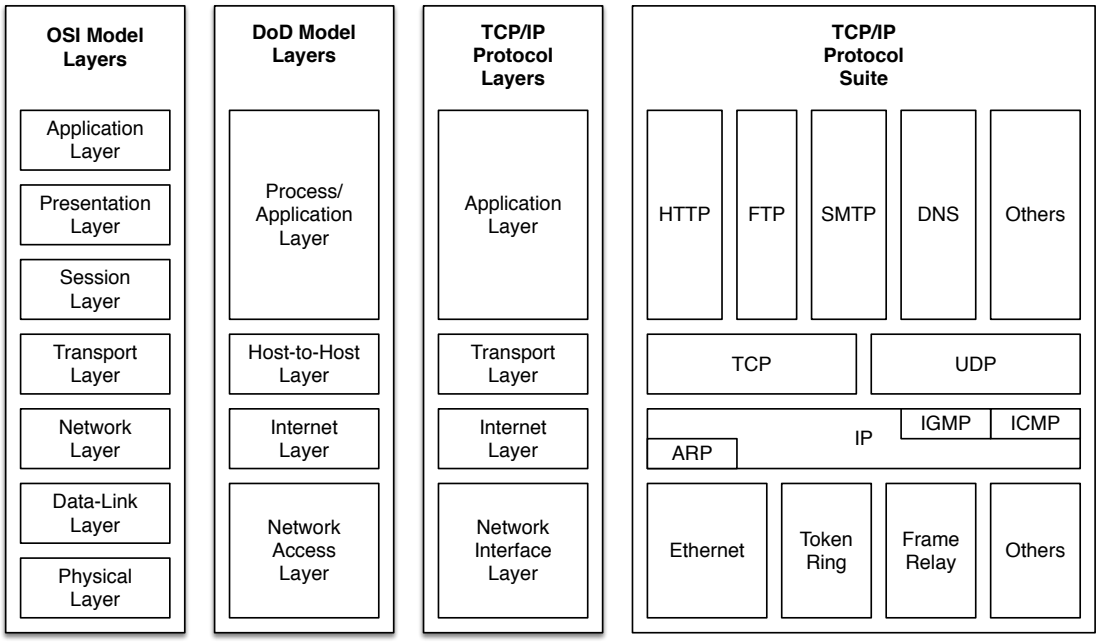


Figure 7.3: Basic architecture of different network models. The OSI model is presents in the left plot. The two plots in the middle are the basic structures of the DoD model and the TCP/IP model. The right one is the detail structure of the TCP/IP protocol suite and the the typical protocols included in.

In this layer structure, each upper layer is data source of the lower layer. The lower layer adds its own header and footer to the data received from the upper layer. Here are two very important concepts revealed in data transmission that are the *encapsulation* and the decapsulation. The encapsulation is a process of adding a header or a footer to the data. It is also called as *wrapping* the data. The header is usually used to indicate the beginning of the data section and represents the features of a special protocol and a special layer. The footer is normally used for error checking. The decapsulation is a reversed process of removing a header or a footer from the data. Within them, the sending and receiving process can be described as belows:

The application layer is the entry and the exit of all communication, where the user data is broken into small pieces and delivered to presentation layer. In the presentation layer, data is translated, manipulated and encrypted to form a special data format. Then, different headers which represents each layer are added repeatedly from layer to layer until the final data (including all headers) reaches the hardware where it is transmitted to different hosts. In this process, the packed data has its own name. For example, it is called as *segments* in the transport layer, as *datagrams* in the network layer and as *frames* in the datalink layer. The final data in *raw bitstream* is handled by the physical layer.

When the bitstream has been delivered to its destination, the data is reassembled and reorganized in each layer from the bottom to the uppermost. The headers and the footers of each layer are discarded in this process until the readable data reaches the application.

TCP/IP model and its protocol suite

Except the OSI model, there are also many different network communication models and protocols suites. All of them follow the principles that have been presented above. The only difference among them is how to divide layers and to organize data. Since the OSI model is a reference model which only defines the methodology of the communication, it is originally designed to understand the networking technology. In practice, the more precise description of the model and the technical details on implementation of the communication are needed. In today's communication framework, the DoD model and the TCP/IP protocol suite are the most famous and widely used model and protocol suite. The basic structures of these models are shown in the middle plots of figure 7.3.

As illustrated in the figure, the TCP/IP model has a four-layer structure, which can be roughly compared to the OSI model. It has an application layer that maps to the three upper layers in the OSI model (i.e., application, presentation and session). The responsibility of this layer is to provide application an ability to access the network and defines the protocols can be used. The network interface layer of the TCP/IP model also contains the datalink layer and the physical layer of the OSI model, since they both related to the hardware implementation and the physical infrastructure of the system [Syngress Media, 2001].

The transport layer and the Internet layer are very important layers. They determine the transportation of the user data between two systems and how to delivery the data to its destination over a large distance through different networks. Generally, it provides a robust, scalable, cross-platform, end-to-end connection for dissimilar systems and also specifies how the data should be formatted, addressed, transmitted, routed and received [Microsoft, 2000].

The detailed architecture of the TCP/IP protocol suite is shown in the right plot of figure 7.3. It is clear that the TCP/IP protocol suite is a collection of different protocols which is not static. The typical protocols in this stack are HTTP (Hypertext Transfer Protocol), TCP (Transmission Control Protocol), UDP (User Datagram Protocol), IP (Internet Protocol), ARP (Address Resolution Protocol) and so on.

Figure 7.4 shows the concept of the data encapsulation, decapsulation and the communication based on TCP/IP protocol suite between two hosts. The user data is encapsulated

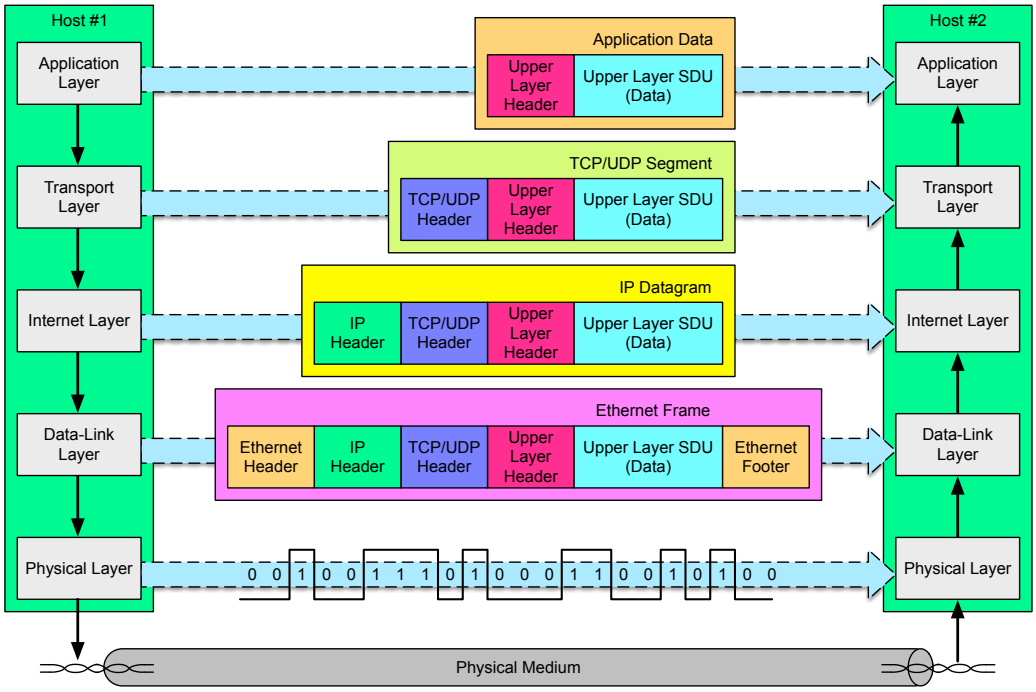


Figure 7.4: Communication between two hosts with TCP/IP protocol suite

layer by layer until the frame reaches the physical medium. Each time a specific header or footer is added to the data to reflect the characteristics of the layer. For example, a header, which is used to indicate where the Service data unit (SDU) comes from, is added to it at the application layer. This message is passed to the layer below as a Protocol data unit (PDU). In the transport layer, the PDU from the upper layer is wrapped again. A TCP header is added to determine how to transport it. In the next layer, the TCP segment is passed to the Internet layer to encapsulate the IP header and form an IP datagram. With the IP header, the data can be routed to a host thousands kilometers away through different physical networks. The IP datagram is packed into specific frame according to the physical communication interface, such as Ethernet frame or Token Ring frame. When the packet or the frame reaches the physical interface, it will be sent out through the physical interface.

Receiving a frame is a decapsulation process. When a frame has been received, the operating system or the specific application inspects and decapsulates the frame layer by layer. Only those headers that match the conditions will be passed to the higher layer. Otherwise, the frame is dropped or retransmitted depending on the protocol used in the transport layer. After the decapsulation progress, the readable data finally reach application layer. The transmission is finished in this phase.

In this process, the protocols used in the transport layer greatly affects the communication. The transport layer has two core protocols that control how the data is delivered. There are TCP and UDP [Microsoft, 2000].

Transmission Control Protocol (TCP)

TCP provides a reliable, connection-oriented data delivery service between only two computers. The one-to-one feature of the protocol is well-known as *unicast*. This means that the connection must be established prior to the data transmission between the two computers. As a connection-oriented communication, TCP is considered as reliable communication, because the data transmission of this protocol is in sequence and has to be acknowledged. The unreached packets will be retransmitted again after a special period of time.

User Datagram Protocol (UDP)

UDP provides an unreliable, connectionless but the best performance delivery service for multiple computers by using *broadcast* or *multicast*. It is suitable for small amount of random data requiring fast data exchanging. Since the data delivery in UDP does not require the acknowledgement, it is treated as an unreliable communication. It does not retransmit the unreached and corrupt packets and does not guarantee the sequencing of the packets. UDP is used when one does not want to suffer from the overhead of establishing a TCP connection, or when the applications or upper-layer protocols provide reliable delivery.

Comparing the two protocols, TCP has a lot of advantages, but these features make it very complicated and hard to be described and implemented with HDL (Hardware description language). Whereas, UDP is simple and efficient and is widely used in the Internet communications and the physics experiments (e.g., CTA [Hoffmann and Houles, 2012]). It can also be implemented with HDL and put into a moderate FPGA without the support of an operating system. More information on the two protocols can be found in [Kozierok, 2005]

7.2 Design of a super light TCP/IP protocol suite for FPGA application

As we learnt that a full-feature TCP/IP protocol suite is large, complicated and can be hardly deployed in a FPGA. A light, and user-defined communication protocols should be

implemented for embedded applications. For this purpose and also to simplify the design and improve the performance of system, a new IP hardcore of a super light TCP/IP protocol suite is proposed for the new DAQ system of the front-end electronics in this section.

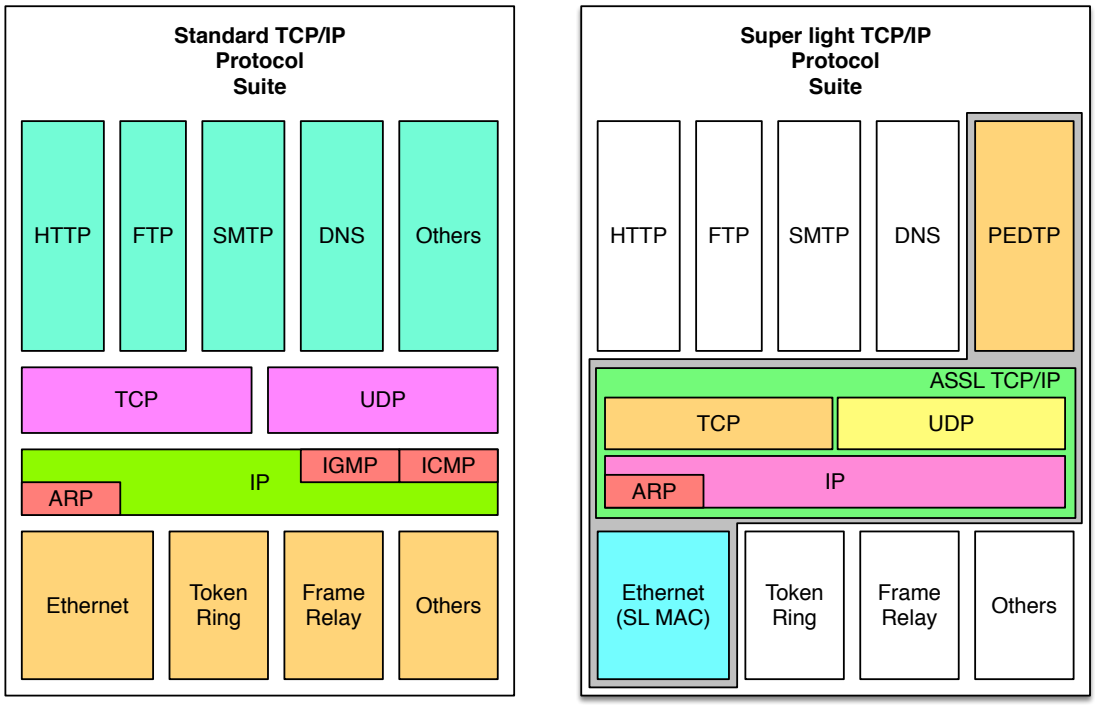


Figure 7.5: General structures of the super light TCP/IP and standard TCP/IP

Figure 7.5 compares the general structure of this new super light protocol suite to the standard TCP/IP protocol suite. The super light TCP/IP protocol suite consists of three main components: an application specific super light TCP/IP protocol (ASSL TCP/IP), a physics experiment data transfer protocol (PEDTP) and a super light Media Access Control hardcore (SL MAC) for the Ethernet application. In figure 7.5, the protocols are marked with different colors. The detailed information about the design and the implementation of these IP cores will be presented following.

7.2.1 Super light Media Access Control hardcore (SL MAC)

The communication must be established over a specific network with a physical medium. The Institute for Electrical and Electronics Engineers (IEEE) developed a group of standards for the physical network labeled 802 series [IEEE, 2014b]. There are serval standards in this series, such as 802.3 (Ethernet), 802.5 (Token Ring) and 802.11 (Wireless LANs).

Based on the previous design of the front-end electronics, the physical network is Ethernet in this application. To fulfill the requirement of the data transmission on Ethernet, a super light MAC hardcore controller is designed and implemented to connect the physical interface (PHY) on the application board.

Ethernet is a broadcast system which means that the data frames are received by every nodes in the same network segment. In this environment, the frame with the special header address is passed to upper-level protocols, others are discarded without specifying. The hardware address is used to decide whether the frame is handled or dropped. The typical Ethernet frame or IEEE 802.3 frame is shown in figure 7.6.

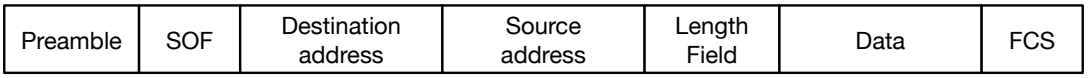


Figure 7.6: IEEE 802.3 frame format

An Ethernet frame starts with a 7-byte preamble with a value of 0x55 that indicates the beginning of a new frame. The next byte is a start-of-frame (SOF) delimited with a value of 0xD5 which ends the preamble and starts the real frame. The next part is the hardware address part that consists of two 6-byte MAC addresses (i.e., destination and source address). After the address section, there is a length field that shows the number of byte of data contains in this frame. The user data or payload follows the length field. The minimum user data is 64 bytes. If it is shorter than this value, it must be padding with extra bytes. The maximum of the data is 1,500 bytes in a typical Ethernet frame. The frame is finished with a 4-byte frame check sequence (FCS) field. It includes a cyclic redundancy check (CRC) value to ensure the integrity of the frame in case of the damage that happened during the transmission [Syngress Media, 2001]. Furthermore, after each data transmission, the devices must hold a minimum idle period which is known as interframe gap (IFG). The typical IFG is 96 “bit time”, which is about 96 ns for a gigabit Ethernet.

Based on these principles and referred to the standard 802.3-2014 [IEEE, 2014a], the SL MAC controller is designed to achieve the following functionalities:

a) Detect, receive and transmit the legal frames.
b) Add and check the FCS.
c) Discard the illegal frames.
d) Attach and detach the preamble, the SOF and the padding.
e) Hold minimum IFG between two transmissions.

Since this hardcore is a super light MAC controller and only designed for the gigabit Ethernet which works in the full-duplex mode, the half-duplex mode and the Carrier Sense Multiple Access/Collision Detection (CSMA/CD) method are not supported by this core.

7.2.2 Application specific super light TCP/IP protocol (ASSL TCP/IP)

The ASSL TCP/IP consists of four main protocols in this super light protocol suite, which are Internet Protocol (IP) and Address Resolution Protocol (ARP) maps to the Internet layer of the TCP/IP model, and TCP and UDP maps to the transport layer. For the protocols in the Internet layer, the main purposes are addressing packets and routing the data to its destination. The transport-layer protocols are responsible for transporting and guaranteeing the data transmission between computers and connecting the upper-level application layer and the low-level Internet layer.

Super light Internet Protocol (IP)

As an Internet layer protocol, IP is a protocol where the node addresses are set. It is defined in the RFC 791 standard [IETF, 1981a] and designed to help to distinguish the computers in the network communication. IP does not only provide an addressing mechanism but also be used in data delivery. It provides a connectionless, unreliable delivery service which means that this protocol delivers the packets without acknowledging them. Checking the integrity and requesting retransmission is the task of the upper-level protocol, such as TCP and application itself. Except the addressing, the IP protocol has another very important feature that is the routability [Syngress Media, 2001]. The routers use IP protocol to route the packet to its destination across different networks.

There are two popular IP protocols in today's network communication: IP version 4 (RFC 791) and IP version 6 (RFC 2460 [IETF, 1998]). The ASSL TCP/IP only supports IPv4 standard.

The basic format of a IPv4 packet is shown is figure 7.7 [IETF, 1981a]. A typical IPv4 packet is composed of two sections: a header section and a data section. It does not contain a data checksum section or any footer. It is because that the designer of the IPv4 thought that the CRC checksum in Network layer is good enough to the integrity of the packet. The length of the header is 192 bits or 24 bytes. According to the previous discussion, the whole length of a IP packet should no exceed 1,500 bytes, if it will be transmitted on

Ethernet. The header is divided into several subsections which are defined by different RFC specifications (e.g., RFC 790, RFC 1071, RFC 6864). As a result, the full description of the IP protocol is absolutely beyond the scope of this thesis. For more information, one could read [Syngress Media, 2001; Microsoft, 2000] and all related RFC documents.

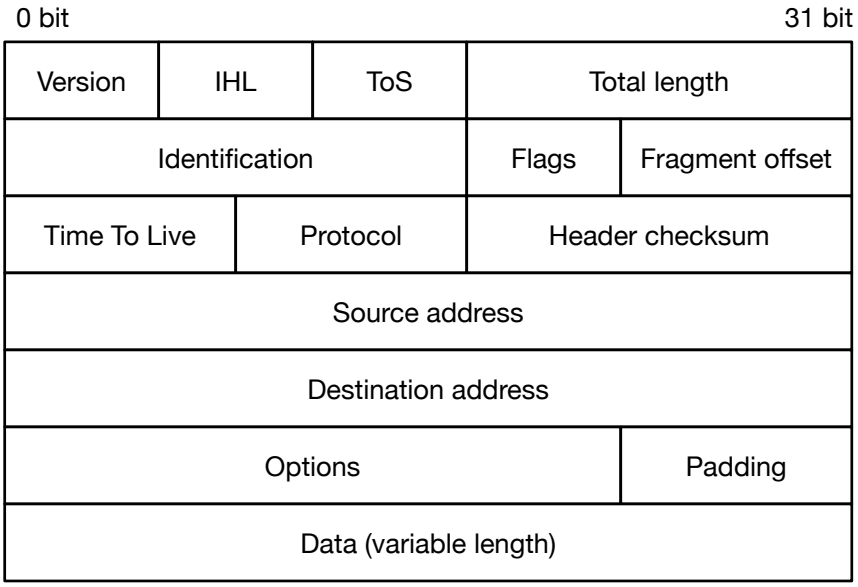


Figure 7.7: Basic format of a IPv4 packet

The hardcore of ASSL TCP/IP supports most features of the IPv4 standard, including the IP address setting, packet assembling, IP header checking and packet delivery. The packet fragmentation and reassembly are not used in this version of ASSL TCP/IP, since, in a physics experiment, the most data transmission only happens in a local network and does not need to cross the network boundaries. The extension of the length of the packet can improve the performance of the transmission. This makes the packet fragmentation become an unnecessary service in these applications.

Super light Address Resolution Protocol (ARP)

Based on the structure of an Ethernet frame, the computers in the same physical network cannot communicate without knowing each other's MAC addresses, which are the addresses defined in the Network layer. As an Internet layer protocol as well, the ARP protocol is defined in RFC 826 [IETF, 1982] and provides an IP-to-MAC address resolution service. It maintains a table that is stored in a cache including a set of IP addresses and their corresponding MAC addresses.

When the upper-level protocol starts a data sending request with an IP address, it always checks the ARP cache at first to retrieve the physical address of the specific IP address that it wants to send to. If the physical address is not stored in the cache, the ARP will update the cache by using broadcast packets to inquire which computer has this MAC address. Normally, the data in the table will expire after a certain period of time. Broadcasting data is expensive and noisy for a network. Misusing of the ARP protocol will cause server security problems for the communication system, and therefore it must be treated carefully.

The basic packet format of ARP protocol based on IPv4 over Ethernet is shown in figure 7.8. An ARP packet size is 30 bytes including the Ethertype which indicates the type of the packet (0x0806 for ARP). To fulfill the requirement of the Ethernet transmission, the packet must be complemented to 64 bytes to meet the minimum frame size. In the ASSL TCP/IP, the super light ARP supports all basic features of the standard ARP protocol. For the detailed information about ARP protocol, one could review RFC 826[IETF, 1982].

Super light User Datagram Protocol (UDP)

As described above, UDP offers a fast but unreliable data delivery service which is in the transport layer. Compared with the IP protocol, it has no big difference in natural except that it attaches an UDP header to the packet when it is called by a user program from the application layer. The basic behavior of this protocol is defined in RFC 768 [IETF, 1980].

To use UDP, the UDP port numbers must be provided by both terminals in the communication progress, including the source port and the destination port. These port numbers are the only ways to identify data streams and pass them to the right application. Each UDP-based application must bound to a distinct computer network port.

The basic format of an UDP datagram is simple and is shown in figure 7.9. The UDP header only consists of four 2-byte fields, which are a source port, a destination port, the length of the datagram including this header and the data, and a 16-bit checksum. This header will be attached to the data from the application layer and passed to the Internet layer to encapsulate an IP packet in the sending process. On contrary, the datagram from the lower layer will be verified and the header will be removed. Based on the source and the destination port, the user data will be passed to corresponding software in the application layer. According to this description, it is easy to implement this protocol in ASSL TCP/IP. More information can be obtained from [Kozierok, 2005].

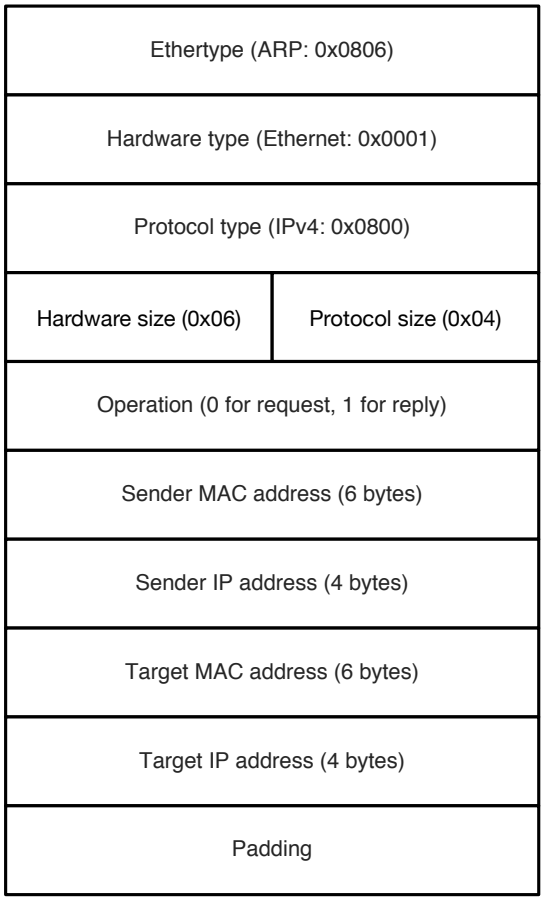


Figure 7.8: Basic packet format of ARP protocol based on IPv4 over Ethernet

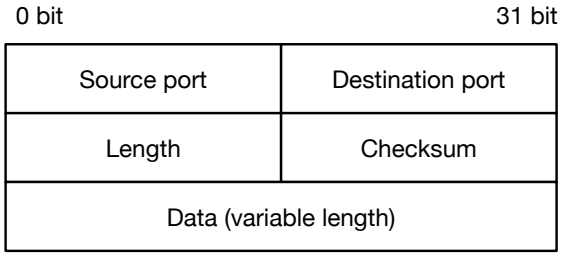


Figure 7.9: Basic format of an UDP datagram

Super light Transmission Control Protocol (TCP)

Since the TCP, which is defined in RFC 793 [IETF, 1981b], provides a reliable, connection-oriented data delivery service only between two nodes in the network, the operation and the application of this protocol is very complicated and usually needs the support of an operating system. The connection establishing process and the data exchanging process are both very complex in this protocol. To fully cover and describe all aspects of the TCP in this thesis is obviously impossible. In the following, only the fundamentals of this protocol are revealed. The technical details can be found in [Kozierok, 2005]

The basic format of a TCP segment is illustrated in figure 7.10. It contains a 11-field header and a variable-length data field. Similarly to the UDP, the TCP also uses the ports to identify the corresponding applications. The first two fields of the header are the source port and the destination port. The next two sections are the sequence number and the acknowledgement number. These values are initialized and synchronized in the connection establishing stage. There is a 4-bit data offset in the header that indicates the start pointer of the user data. After the data offset, there are 3-bit reserved bits and 9-bit flags. The flags are very important. They determine the behavior of the protocol and how the data should be processed. The window in the header represents the size of the receiving buffer. The checksum field provides a similar function as the one used in the UDP. The urgent pointer is next and must work with URG flag. Except the basic communication functions, TCP also supports extra ones. These special functions are defined in the options field just following the urgent pointer sector. The last field of a TCP segment is a variable-length data. .

TCP is a reliable and connection-oriented protocol and in the communication, the connection between two computers must be established prior to the data exchanging. The connection must also be reliably terminated after the communication. The figure 7.11 presents the state diagram of the TCP connection and termination. This connection is well-know as a *session*.

TCP provides three ways to establish the connection or the session: active open, passive open and simultaneous open. They all open the session through a process which is a three-way handshake. For example, in the active open mode, when the source computer starts a session, it will send a packet with a random sequence number and a set “SYN” flag. When the destination computer receives the “SYN” flag and is ready to response, it will send a packet with an acknowledge number and a set “SYN+ACK” flag. If the source

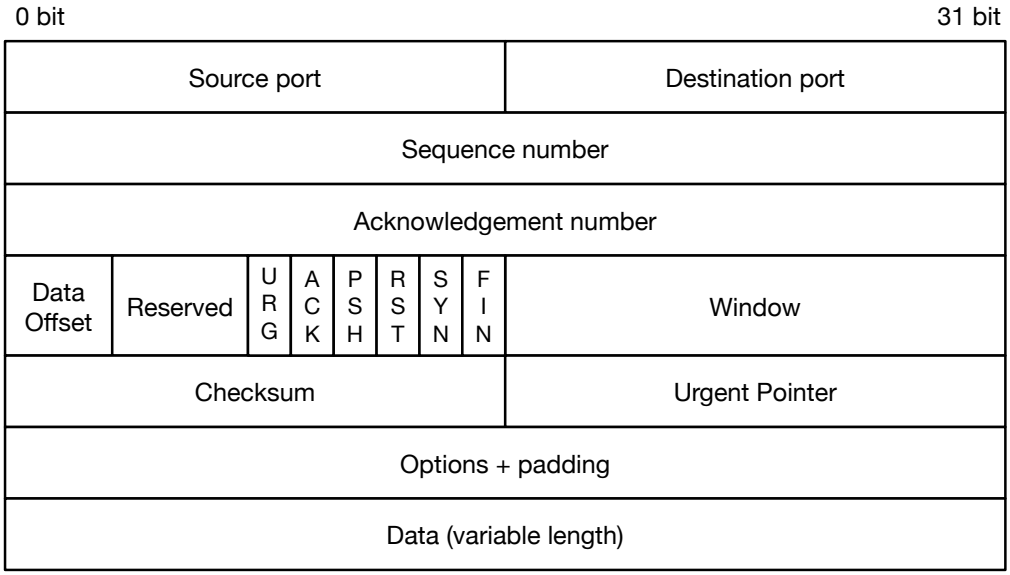


Figure 7.10: Basic format of a TCP segment

computer agree with the response, it will send a packet with a set "ACK" flag to establish the connection. At this moment, the session is successfully opened. It allows the data exchange in this reliable pipe.

The termination of the session must be reliable as well. TCP also supplies three similar ways to close the connection between two computers. They follow the similar rules of the three-way handshake process, but only add an additional step to send a packet with a set "FIN" flag. Due to this characteristic, the process is a pair of two-way handshakes that is called as four-wave termination.

The data exchanging with TCP is far more complicated than the opening and the closing of the session. The packets are identified, verified and reordered with the sequence number and the acknowledge number to guarantee the reliable transferring. Only the packets that match the those values without errors will be stored in the buffer. The duplicated packets will be rejected and the unacknowledged packets will be retransmitted by the protocol. The size of the buffer is checked in each data exchanging. TCP exploits a sliding window mechanism to achieve the flow control. It implies that the receiver continually reminds the sender how much data can be received. If the receive buffer is full, the transmission will be stopped automatically until enough space is released.

For the ASSL TCP/IP protocol, we developed a super light TCP that supports all basic communication functions and compatible to the standard TCP which is defined in

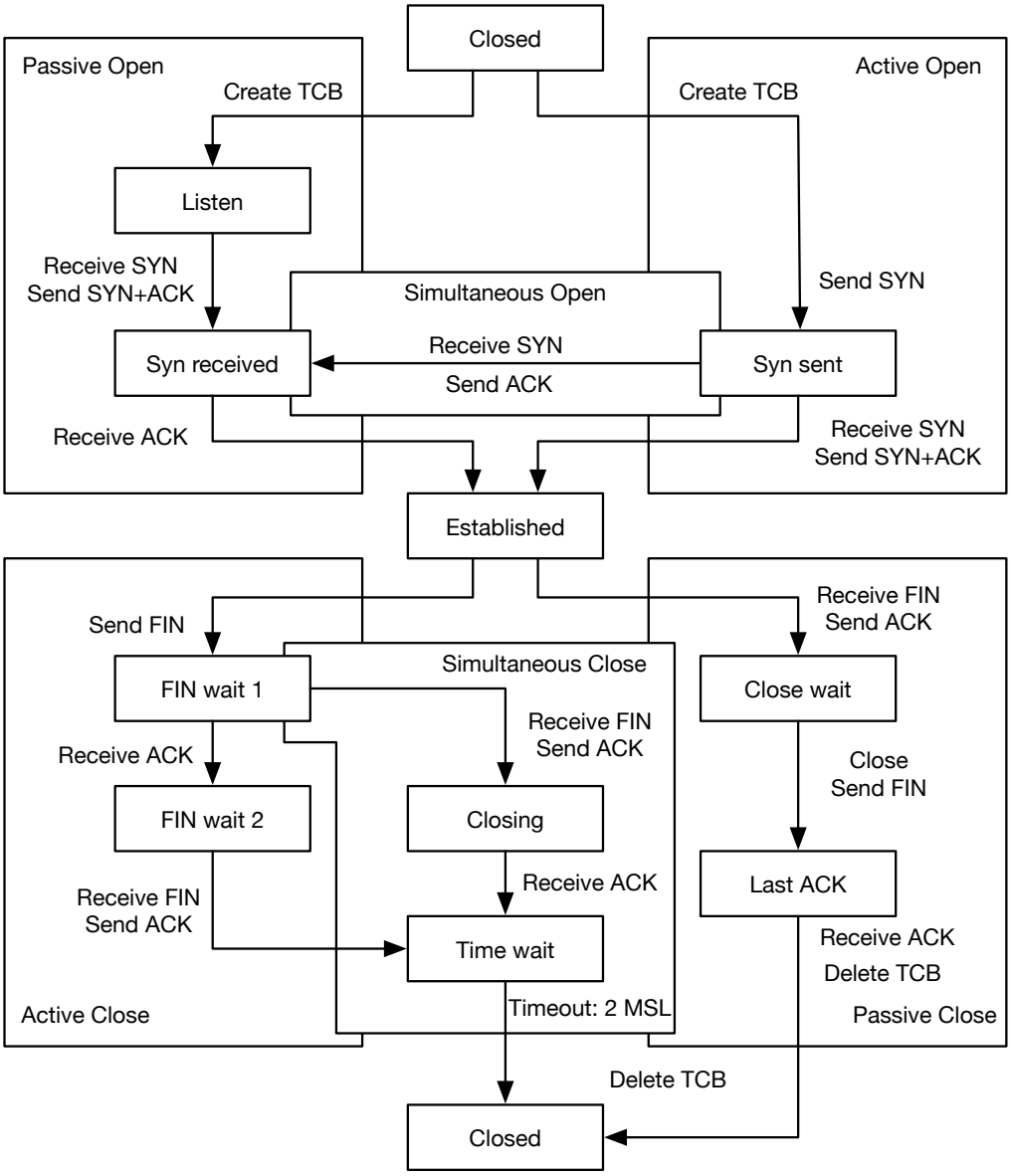


Figure 7.11: State diagram of the TCP connection and termination

RFC 793 [IETF, 1981b]. It also partially supports the maximum segment size (MSS) and the window scaling (WS) which are defined in the RFC 1323 [IETF, 1992].

Brief summary of the ASSL TCP/IP

In order to fulfill the requirements of the new front-end electronic and achieve the data transmission over the network, the ASSL TCP/IP is designed and implemented. It consists of four major super light protocols which are SL IP, SL ARP, SL UDP, SL TCP and located in the Internet layer and transport layer of the TCP/IP model. These protocols that developed by us fully cover all the necessary functions for a network communication and are compatible to the standard protocols in the modern communication system. The ASSL TCP/IP is also a fully user-defined protocol suite that can be adapted for different applications. The usage of the protocol suite is simple and convenient. Due to its small size, these protocols can be easily integrated in a FPGA application.

7.2.3 Physics experiment data transfer protocol (PEDTP)

PEDTP is a fully user-defined higher-level protocol, which maps to the application layer in the TCP/IP model. The purpose of this protocol is to provide an easy-implementation method to control and manage the DAQ system in a physics experiment. It is a message-based protocol which is similar as HTTP (Hypertext transfer protocol) used in the webpage accessing.

The PEDTP defines a set of human-language-based methods or commands to manage the system and indicates the desired operations which should be performed. The basic message structure of PEDTP is shown in figure 7.12.

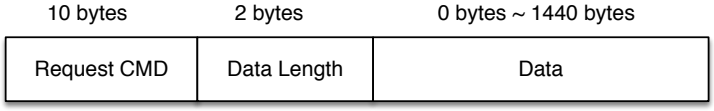


Figure 7.12: Basic structure of a PEDTP message

The PEDTP message is composed of a 12-byte header and variable-length data section which is from 0 bytes to 1,440 bytes for a normal Ethernet application. The header contains a request command sector and a data length sector following it. The commands or the methods in this protocol are defined as verbs. In a specific version of the PEDTP which is designed for the ASICs from OMEGA, there are five basic commands that are defined

to fulfill the requirements. The commands, theirs functions and the examples are listed in table 7.1.

Table 7.1: PEDTP commands for ROCs from OMEGA

Commands	Functions	Example
"SET"	Set parameters	"/SET SLC /": set the slow control parameters.
"GET"	Get parameters	"/GET TEMP/": get the temperature sensor data.
"STA"	Start operation	"/STA ACQU/": start data acquisition.
"STP"	Stop operation	"/STP ACQU/": stop data acquisition.
"SND"	Send data to host	"/SND TEMP/": send temperature data to host.

In the data transmission, the commands are encoded in ASCII code, which makes that they can be recognized directly by the designers and engineers. With this application layer protocol, the management of the DAQ system can be easily achieved. Moreover, the design of the DAQ application is simple and efficiency and can be implemented by using any programing language which supports the TCP/IP, such as C, C#, Java and so on.

7.3 Software Implementation of the DAQ

To achieve high performance, the software control system is fully described in VHDL (VHSIC Hardware Description Language). The block diagram of the new front-end electronics is shown in figure 7.13.

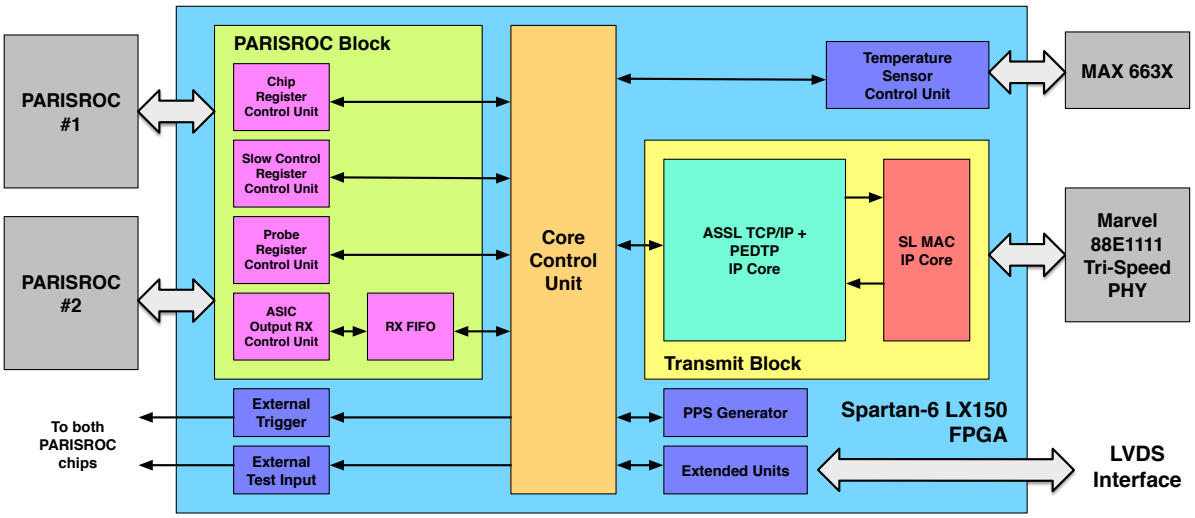


Figure 7.13: Block diagram of the new front-end electronics

The core control unit based on finite state machine (FSM) is designed to manage and control the two ASICs, the communication system and the peripherals. The different registers in the ASICs can be controlled by the core unit through their independent internal buses. When the PARISROC 2 chips generate a data transmission request, the data will be automatically stored in a "Ping-Pong" buffer. When the number of the buffered data exceeds the user-defined waterline, they will be sent out into the transmit buffer to construct a specific frame.

As described in previous chapter, the length of a PARISROC frame is 51 bits, which is shorter than 7 bytes. Therefore, a chip header of 5 bits will be added to the frame to complement it and to extend it to 7 bytes. At the same time, a one-byte chip footer will also be added to align the frame to 8 bytes due to the requirements of the data transmission. Therefore the frames coming from the chip No. 1 will start with a hexadecimal character "A" and end with two hexadecimal characters "99" . They are similarly "5" and "77" for the chip No. 2. The structure of the encapsulated PARISROC frame is shown in figure 7.14.

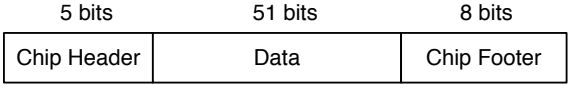


Figure 7.14: Structure of the encapsulated PARISROC frame

The frame will be passed to the ASSL TCP/IP protocol engine and then to the SL MAC core. Depending on the protocol which is used in the hardcore engine, it will be encapsulated into different types. If the UDP of the ASSL TCP/IP is used, a UDP datagram will be constructed. The total length of a UDP packet is 555 bytes. It can be divided into two parts. One is the header of the protocol which is 42 bytes, the other one is the payload with a length of 513 bytes. Within it, there are 1 byte control code and 512 bytes acquisition data. For the application of the TCP of the ASSL TCP/IP, the TCP message is built with the structure shown in figure 7.12. The total length of a TCP message is 1,506 bytes by taking into account all the headers and footers.

Finally, the frame will be delivered to an appointed destination through Ethernet. The receiving procedure shares similar steps. When a packet is received, it is decapsulated and filtered. The core unit produces the corresponding write or read requests and distributes received data to specific registers. The system also supports data transmission through the LVDS interface by other user-defined protocols.

The software including the FPGA program at the front-end board side and the DAQ application at the computer are all successfully implemented.

The whole DAQ system and the control part of the ASIC at the FPGA side only consumes about 10 % of resources of a Spartan-6 LX 150 FPGA. Therefore, this user-defined ASSL TCP/IP hardcore engine can be easily embedded into a typical commercial FPGA as the Spartan-6 (Xilinx), Cyclone-V (Altera) or any other FPGAs with similar or better performance than these two. The top performance of the engine is usually determined by the model of the FPGA.

The DAQ software at the host side is written in C# and supports five basic functions, including the connection and control registers setting, the slow control register setting, the probe register setting, the data acquisition and the data analysis. The five main interfaces of the software are given in Appendix B.

The test results and the performance of the whole electronics will be presented in the next chapter.

Chapter 8

Performance and test results of the FEE

In order to fulfill the requirements of the Cherenkov telescopes in LHAASO experiment, a WFCTA oriented front-end board has been designed, implemented and fabricated, including the hardware and the software, following the previously described design framework. The next step is to verify and evaluate the performance of the ASIC and the new application board. For this purpose, a series of tests have been performed, including charge measurements, time measurements, single channel event rate, pedestal monitoring, performance of the prototype DAQ that was developed in this thesis and described in chapter 7, PMT measurement and evaluation of the power consumption of board.

The test bench that has been used here is similar to the one which was used to evaluate the PMm^2 board and is shown in the Chapter 6. Only the PMm^2 application board is replaced by the new FEE. The slow control parameters (SCPs) are adjusted a little to meet the requirements and are listed in table 8.1. The tests were performed by using input signals produced by a standard signal generator. The new front-end electronics was also evaluated with a candidate PMT (CR303) of WFCTA.

Table 8.1: Values of the most important parameters of the PARISROC 2 for the new design

Slow control parameters	Values
Discriminator of DAC 0 (DD0)	835 (0 to 1023)
Discriminator gain of DAC (DDG)	350 (0 to 1023)
Trigger delay (TD)	39 (0 to 63)
Slow shaper gain (SSG)	16K (16K to 64K)
Slow shaper time constant (SSTC)	100 ns (0 to 175 ns)

8.1 Charge measurement

The typical dynamic range for an IACT usually covers a large range from a single photoelectron to thousands of photoelectrons. For the WFCTA, the required range is from 320 fC to 480 pC with relative deviation better than 2 %, which is equivalent to a range from 10 to 15,000 p.e. at PMT Gain = 2×10^5. The relative deviation is defined as the maximum deviation between the ideal output (linear fitted line) and the actual output (measured value) after the offset has been removed.

Firstly, the dynamic range and nonlinearity of a single PARISROC 2 channel were evaluated with the new broad. The results of the dynamic range and the linearity are presented in figure 8.1 and 8.2, respectively.

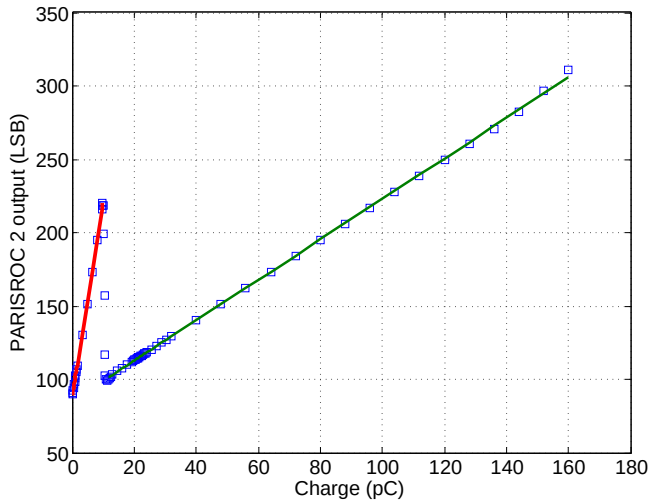
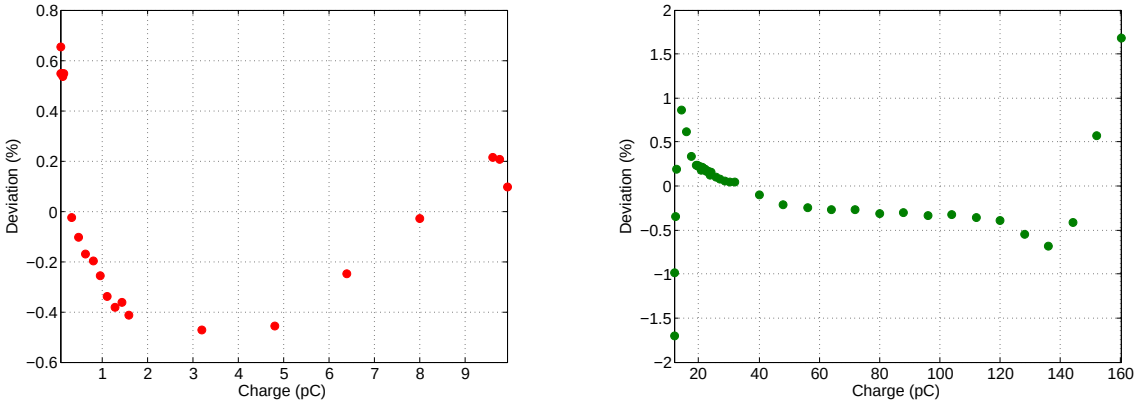


Figure 8.1: Dynamic range of a single channel of PARISROC 2 (new design). The blue squares represent the output of a single channel of PARISROC 2. The red line and the green line are the linear fitted lines of the HG and the LG channel, respectively.

Compared with the previous result shown in figure 6.2, it is clear that, by simply increasing the slow shaper time of the ASIC, even a single channel could achieve a larger dynamic range. The whole dynamic range in this case is from 80 fC to 160 pC. In figure 8.2a, the nonlinearity of the HG channel is better than 1 % and the nonlinearity of the LG channel is better than 2 % (see figure 8.2b). The nonlinearity is defined as the maximum deviation between the ideal output (linear fitted line) and the actual output (measured value) without removing the offset of the actual output.



(a) (b)

Figure 8.2: Nonlinearities of the HG and LG channel (new design). The red dots in figure 8.2a and the green dots in figure 8.2a represent the deviations of the HG and LG channel, respectively.

The gain difference between the HG and the LG channel can be calibrated by multiplying LG data by the actual gain ratio. The result is shown in figure 8.3. The actual gain ratio is about 9.65 (HG/LG) which is slightly smaller than the theoretical one (10) from the datasheet of the ASIC.

Figure 8.4a and 8.4b present the whole scale of the calibrated charge measurement of a single PARISROC 2 channel and its deviation. Due to the imperfection of the auto-gain controller in PARISROC 2, the output of the chip is still discontinuous when the input reaches the set threshold. In the figure 8.4b, the largest deviation in the switching region exceeds 8 %. These measurements suggest that dynamic range of a single PARISROC 2 channel still cannot fulfill the requirements of the WFCTA.

Therefore, in the new design, as shown in figure 6.15, by replacing the 50 Ω matching resistor with a voltage divider to change the voltage distribution between these two channels, the dynamic range can be extended with good linearity. Figure 8.5a and 8.5b show the results of the charge measurements performed with the FEE. Figure 8.5a shows that the FEE achieves a dynamic range from 80 fC to 160 pC or 320 fC to 640 pC with the nonlinearity better than 1 %. This is equivalent to a range from 10 to 20,000 p.e. (PMT gain $= 2 \times 10^5$). The gain ratio of these two channels is 2. In fact, the dynamic range of the new design can be even larger due to the use of the second channel but has not yet been tested. The dynamic range is similar to what we had achieved (160 fC to 260 pC) with the PMm^2 application board [Chen, 2013].

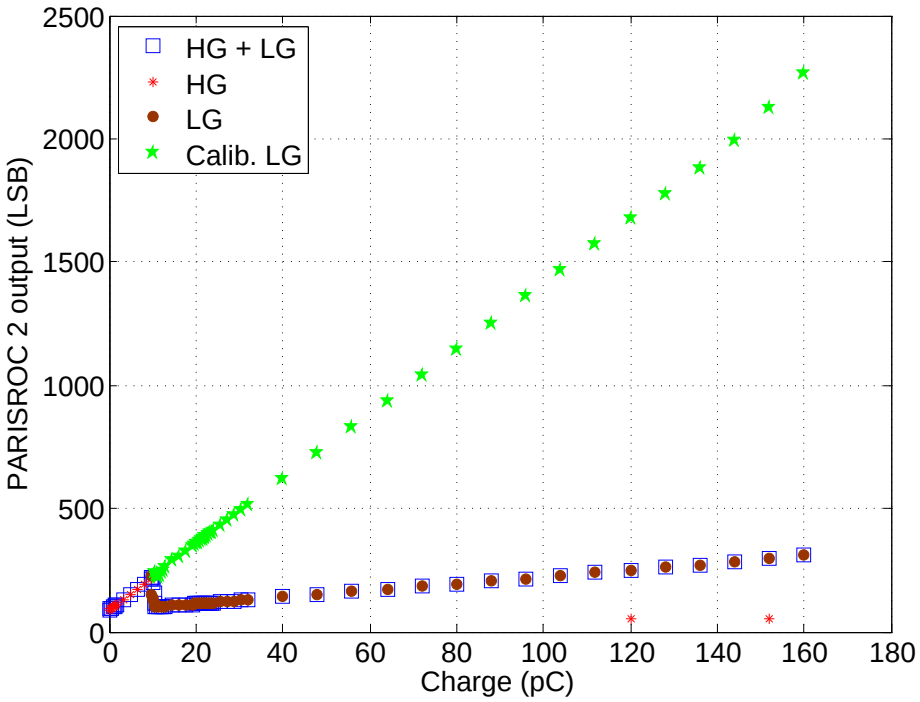
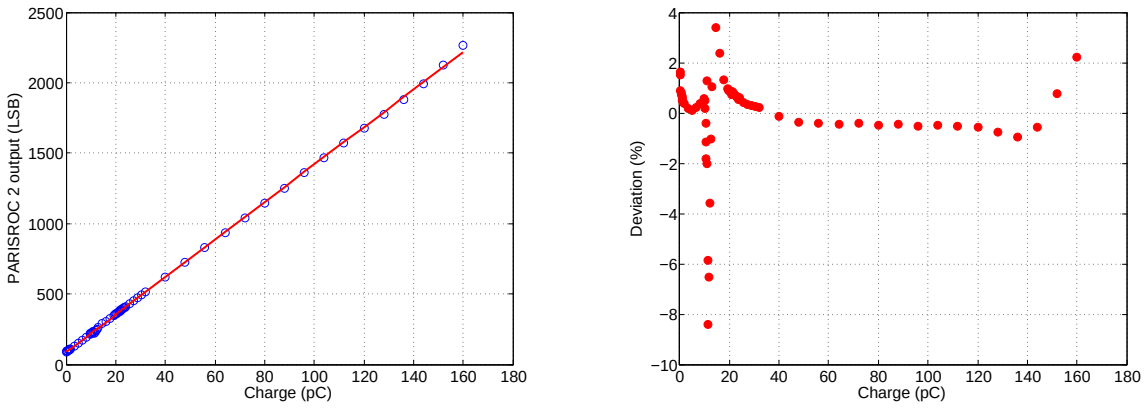
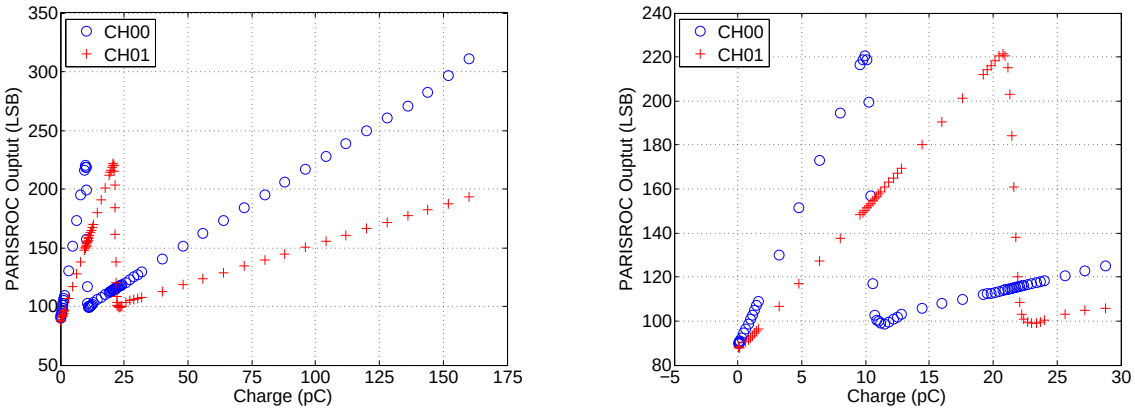


Figure 8.3: Charge measurement with the calibrated LG data. The figure shows a similar output as shown in figure 8.1 which is marked with blue squares, the HG channel marked with red asterisks, the LG channel marked with brown dots and the calibrated LG channel marked with green stars.



(a) (b)

Figure 8.4: Calibrated charge measurement of a single PARISROC 2 channel. Figure 8.4a shows the whole scale of the calibrated charge measurement (blue circle) and its linear fitted line (red line). Figure 8.4a presents the nonlinearity of the output.

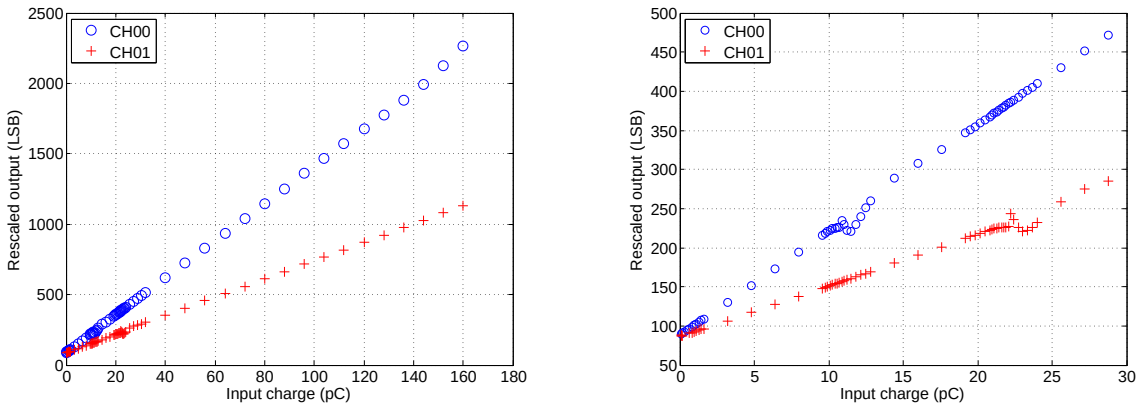


(a) (b)

Figure 8.5: Charge measurements of the new front-end electronics. The symbols of circle and plus represent the outputs of the first channel and the second one, respectively. Figure 8.5a shows the dynamic range of the front-end electronics. Figure 8.5b shows the zoom-out plot focused on the region of the HG to LG switching.

Moreover, figure 8.5b shows a zoom-out plot of the figure 8.5a, which is focused on the region of HG to LG switching. The discontinued output can be observed in this region, when the output switches from the HG channel to the LG channel at about 3.4 pC. This bug will be fixed in the PARISROC 3 currently under development. Before that the discontinuity between the HG and the LG channel can be avoided by alternatively using the different PARISROC 2 channels in the data processing, but it increases the difficulty of the data processing (four channels). For example, when CH00 meets its discontinuity, the HG data from the CH01 can be used to complement the nonlinear region, whereas, the LG data from the CH00 can be used to replace the discontinued region of the CH01.

The gain differences between the HG and the LG channel in CH00 and CH01 are calibrated by multiplying LG data by the actual gain ratio and shown in figure 8.6a and 8.6b. The figure 8.6a shows the whole scale of the dynamic range and the figure 8.6b shows the zoom-out plot the region of the HG to LG switching. In the figure 8.6b, it is clear that the discontinuity greatly affects the linearity of the system and should be corrected in PARISROC 3. It also shows that the electronics provides a full overlap of the different PARISROC 2 channels, which are used as the HG and the LG channel in the system. The gain difference for CH00 is about 9.65 (HG/LG) and about 9.69 for CH01. The gain difference between the CH00 and the CH01 is about 2.03. They all match the



(a) (b)

Figure 8.6: Calibrated charge measurement of the new front-end electronics. Figure 8.6a shows the whole scale of the dynamic range. Figure 8.6b shows the zoom-out plot focused on the region of the HG to LG switching.

expected values which are 10 for the gain difference the HG and the LG channel in a single PARISROC 2 channel and 2 for two PARISROC 2 channels.

However, after removing the offset (Y-intercept) and calculating the relative deviation of the system, the dynamic range of the HG channel of the CH00 is from 320 fC to 9.92 pC and the one of the LG channel is from 16 pC to 152 pC. In this range the relative deviations of both channels are better than 2 %. For the CH01, the dynamic range of the HG channel is from 3.2 pC to 20.8 pC and the dynamic range of the LG channel is from 25.6 pC to 160 pC. The upper-limit of the dynamic range of the CH01 has not been tested yet due to the limitation of the signal generator used in the test. The relative deviations of both channels of CH01 are better than 2 % as well. These values roughly fulfills the requirement of WFCTA (320 fC to 480 pC with relative deviation better than 2 %). In the PARISROC 3, the intrinsic dynamic range of the ASIC will increase to a range from 160 fC to 320 pC with the nonlinearity better than 1 %. With a similar design, the new chip should fully cover the required dynamic range of the WFCTA telescope in future.

8.2 Time measurement

As explained in Chapter 5, in case of the PARISROC 2 chip, the real time of an event can be calculated based on two time units which are a 24-bit gray counter for the coarse time and a 10-bit TAC for the fine time. The high-precision time measurement of the TAC

is achieved by two phase-reversed ramps which are designed to eliminate the dead zone of the ramp switching. The real time can be recovered from the sum of the coarse time and the fine time with a special method [Dulucq et al., 2010], which is shown in the algorithm 8.1.

Algorithm 8.1 Recover the real time from the PARISROC 2 output

if $DO_{TAC} \times TU_{TAC} > 90\ ns$ **then**
  if $LSB(BIN(CNT_{TS})) = CNT_{1-bit}$ **then**
    $T_{real} = CNT_{TS} \times TU_{TS} + DO_{TAC} \times TU_{TAC}$
  else
    $T_{real} = (CNT_{TS} - 1) \times TU_{TS} + DO_{TAC} \times TU_{TAC}$
  end if
else
  $T_{real} = CNT_{TS} \times TU_{TS} + DO_{TAC} \times TU_{TAC}$
end if

In the algorithm 8.1, DO_{TAC} and TU_{TAC} represent the digital output of the TAC and its time step. CNT_{TS} and the TU_{TS} represent the digital output of the coarse-time counter and its time step which is 100 ns. CNT_{1-bit} is used to mark the falling edge of the clock signal as well as a symbol of how to select the right ramp. The DO_{TAC}, CNT_{TS} and CNT_{1-bit} can be retrieved from the PARISROC 2 output frame shown in figure 6.12. The only unknown parameter in this algorithm is the time step of the TAC (TU_{TAC}).

The common method to find out this time step of the TAC is to synchronize an external signal with the internal signal "start ramp", and to inject a synchronized input signal with a special delay (i.e. 1 ns) to reconstruct the TAC ramps[S. Conforti Di Lorenzo et al., 2012]. With the TAC outputs of the start and the end point of the ramp, the time step can be calculated by $100ns/TAC_{range}$. Figure 8.7 shows an example of the reconstructed TAC ramps. In the figure, the mean time dynamic range of the two ramps is about 587 ADC count, which leads to a time step of 170 ps. However, this common method is a time-consuming task, which is not optimized for the mass verification. In this thesis, another fast and effective calibration method is proposed to find out the TU_{TAC}. The new calibration method is described in the following.

To calibrate the time tagging system, an asynchronous external signal is injected into the ASIC to trigger the chip. After this, the data acquisition is activated to accumulate enough events (tens of seconds) in order to record the highest and the lowest outputs of the TAC. An example of the recorded TAC output range is shown in figure 8.8. Since there are

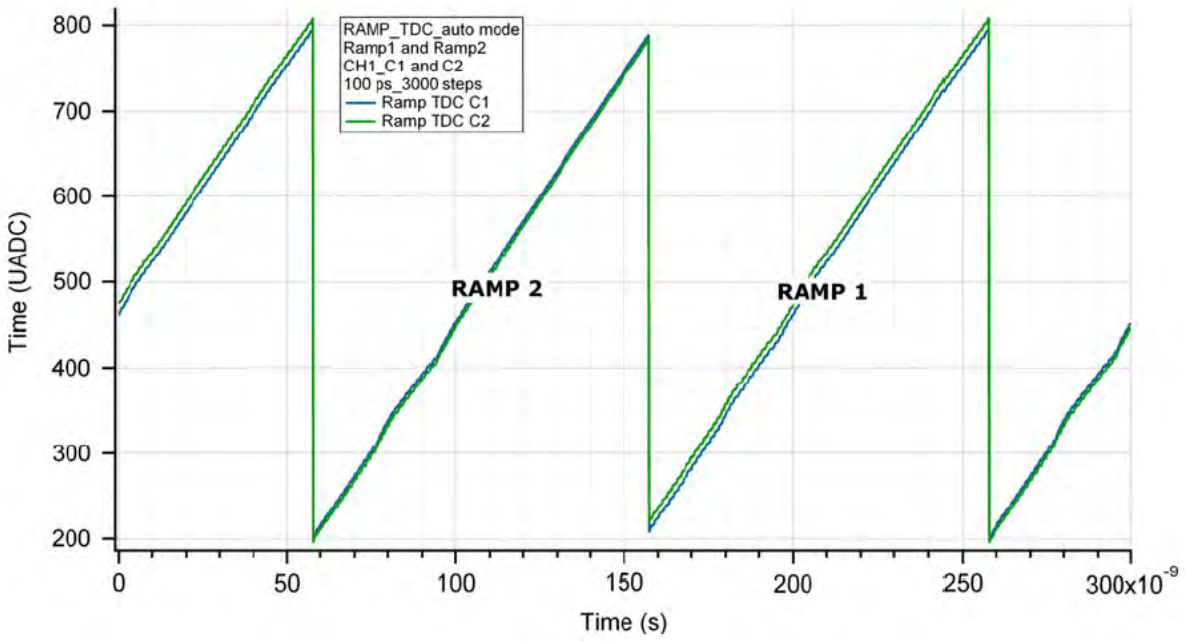


Figure 8.7: Reconstructed TAC ramp by using common method. The figure is taken from [S. Conforti Di Lorenzo et al., 2012]

two ramps and two capacitors are used in the TAC system, four groups of fine time data are recoded.

Table 8.2: TAC output ranges and the TU_{TAC} for different combinations

Combination		Range (LSB)	TU_{TAC} (ps)
Ramp 0	Capacitor 0	602	166.113
	Capacitor 1	601	166.389
Ramp 1	Capacitor 0	602	166.113
	Capacitor 1	605	165.289

The TAC output ranges and the and the TU_{TAC} are listed in table 8.2. It gives a mean range of about 602 LSB and leads to a mean time step of 166 ps. Based on the tests result, the output range of the TAC is stable and usually around 600 LSB. The absolute real time can be retrieved with this time step.

Figure 8.9 shows the result of the recovered absolute time of the events. The number of recorded events is 320,000 and the recording lasts 16 s. There is no discontinuity in figure 8.9 which indicates that all desired events are captured. The figure8.10 shows the time interval of the adjacent events without calibration. The distribution is centered to zero by subtracting the mean time interval of the two adjacent events. The RMS of the distribution

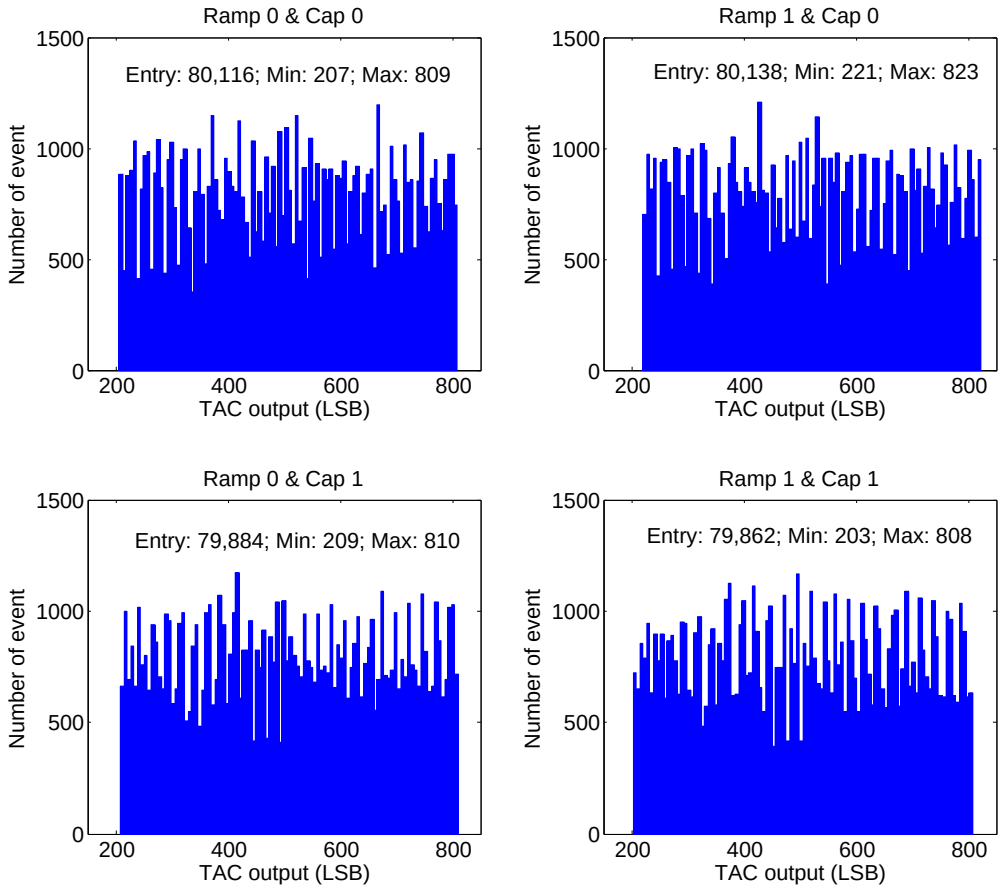


Figure 8.8: Recorded TAC output range. The upper-left one is the TAC output of the results from Ramp 0 and stored on Capacitor 0. The upper-right one is the TAC output of the results from Ramp 1 and stored on Capacitor 0. The down-left one and the down-right one are the TAC output of the results from Ramp 0 and stored on Capacitor 1 and the TAC output of the results from Ramp 1 and stored on Capacitor 1 respectively

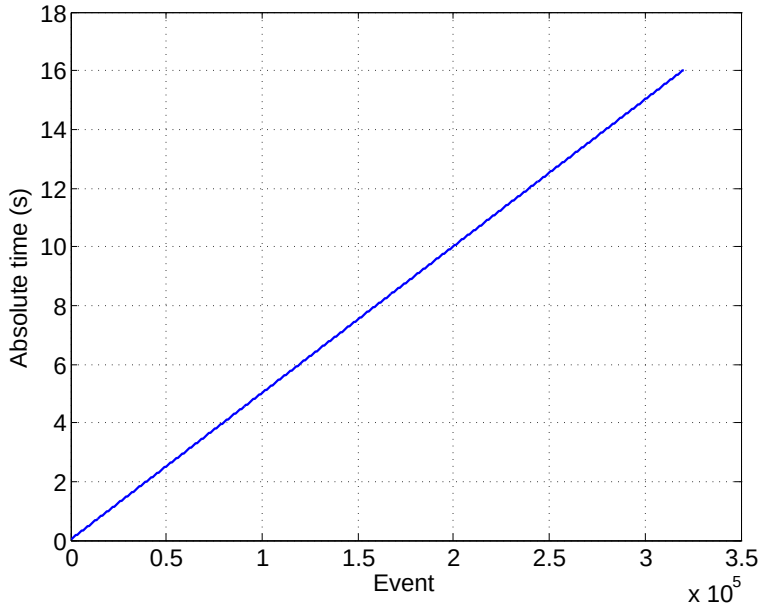


Figure 8.9: Recovered absolute time of the events

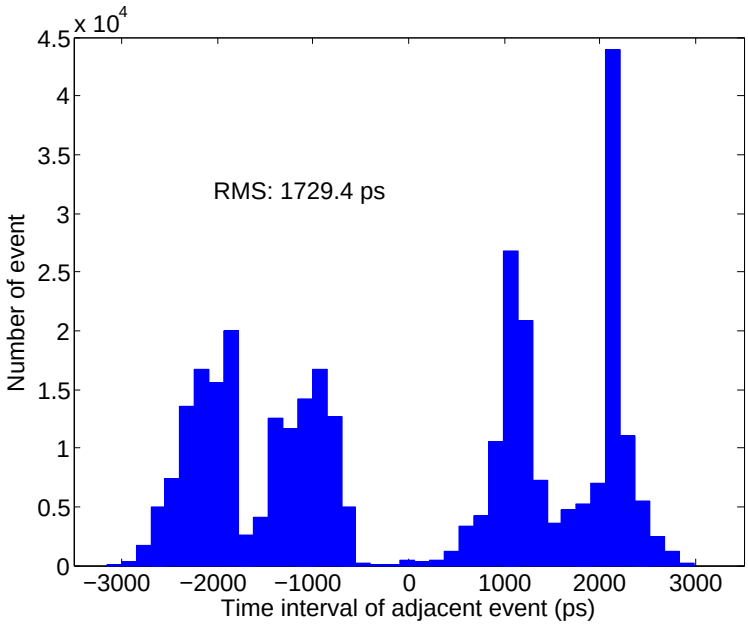


Figure 8.10: Time interval of the adjacent events without calibration

is about 1,729.4 ps which suggests that the time resolution without calibration of the ASIC is about 2 ns and is worse than the expected value (1 ns). Inspecting the figure 8.10, it is also clear that the distribution presents a four-peak structure. Each peak represents a set of time outputs corresponding to a combination of the two ramps and two capacitors.

Table 8.3: Coefficients for the time measurement calibration

Combination		Mean (LSB)	Coefficient (LSB)
Ramp 0	Capacitor 0	509	0
	Capacitor 1	522	-13
Ramp 1	Capacitor 0	511	-2
	Capacitor 1	504	+5

Thanks to the new design, the on-board FPGA can be used as a synchronized external trigger source of the ASIC chip. The differences in the time measurements are due to the process variations in the fabrication of the integrated circuit and can be calibrated with the FPGA time measurement. The calibration coefficients can be determined with the statistical mean values of the TAC outputs and are listing in table 8.3.

By using table 8.2 and 8.3, the time measurement of the ASIC can be easily calibrated. The figure 8.11 presents the calibrated result of the same time measurement which is shown in figure 8.10. After calibration, the RMS of the distribution decreases to 263.19 ps. This new result is much better than 1 ns. The resolution of the time measurement is affected by the frequency of the input signal. Even in the worst case, the RMS value is always better than 450 ps. These results are also better than the previous result ($\pm$ 450 ps) [S. Conforti Di Lorenzo et al., 2012], showing the efficiency of the new calibration method. However, the common method is still necessary to study the behavior of the TAC and to measure the nonlinearity of the time measurement unit. The best application of the new calibration method is for the mass verification.

8.3 Single channel event rate and pedestal monitoring

By using the FPGA as a trigger source, the event rate of the FEE can be tested and verified by the time measurements as well. Theoretically, since the output of the PARISROC 2 chip is synchronized to a 40 MHz clock signal, transferring a 51-bit frame will take 1.275 μs and at least 20.4 μs for 16 channels without considering the dead time between each frame. Thus, the maximum data output rate of PARISROC 2 will not exceed 50 kHz even if the

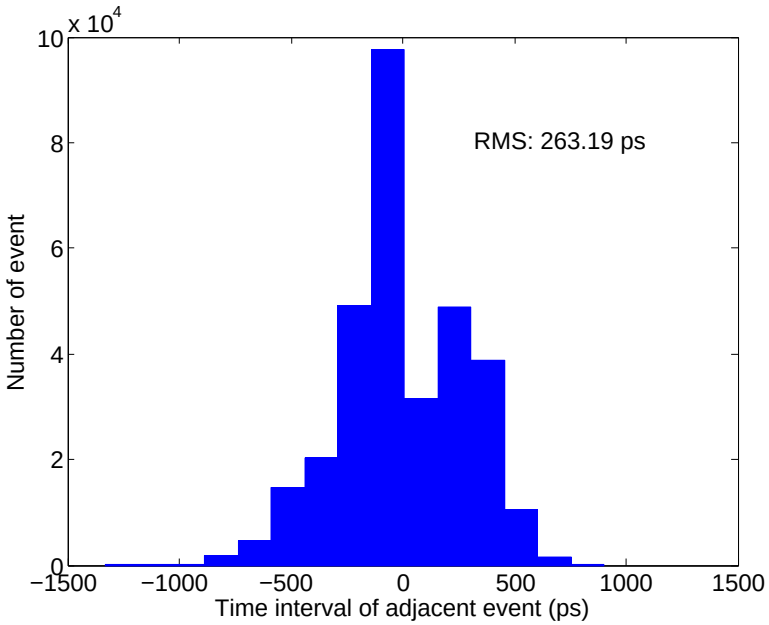


Figure 8.11: Time interval of the adjacent events with calibration

dead time is zero. According to the test results, for a single channel with frequency-fixed and amplitude-fixed inputs, the event rate can be up to 49.5 kHz without losing any events. For all 32 channels on the board, this value will drop to about 24.3 kHz. If one shuts down the TAC unit, the single channel event rate could even reach around 37 kHz. Thanks to the new DAQ system, this value is about 4.4 times higher than the previous result (8.4 kHz) [Chen, 2013].

However, the real signals are random signals with variable frequency and amplitude, due to the characteristics of the Wilkinson ADC embedded in the PARISROC 2 that takes longer time to convert larger signals, the event rate of the system should be smaller than this one. Based on the datasheet of the chip [OMEGA microelectronics, 2012], by taking into account the influence of the amplitude and the frequency, the event rate for the ASIC should be around 5 kHz. As an autonomous, trigger-less ASIC, the setting of the threshold also affects the effective event rate. A suitable threshold is a key point for a PARISROC 2 application.

Due to the architecture of the preamplifier of the PARISROC 2 chip, the DC component of the input signal is stopped by the series capacitor installed at the input of the chip. For now, the pedestal monitoring of the new design can be achieved with an external trigger and by monitoring the variation of the event rate. Another improvement in the future for

PARISROC 3 is to add an external input which bypasses the series capacitor and connects to the input of the preamplifier allowing to monitor the pedestal directly.

8.4 PMT measurement

The performance of the new electronics has also been evaluated with the CR303 photomultiplier which is a candidate PMT for the WFCTA and fabricated by Beijing Hamamatsu. The test bench was built at the IPNO. It consists of a light-tight box, and two NIM modules which are the High-Voltage (HV) generator and the Light-Emitting Diode (LED) driver. The HV generator is used to provide the power supply of the PMT. The LED driver is the signal source of the diode. It also generates the external trigger to synchronize the whole system.

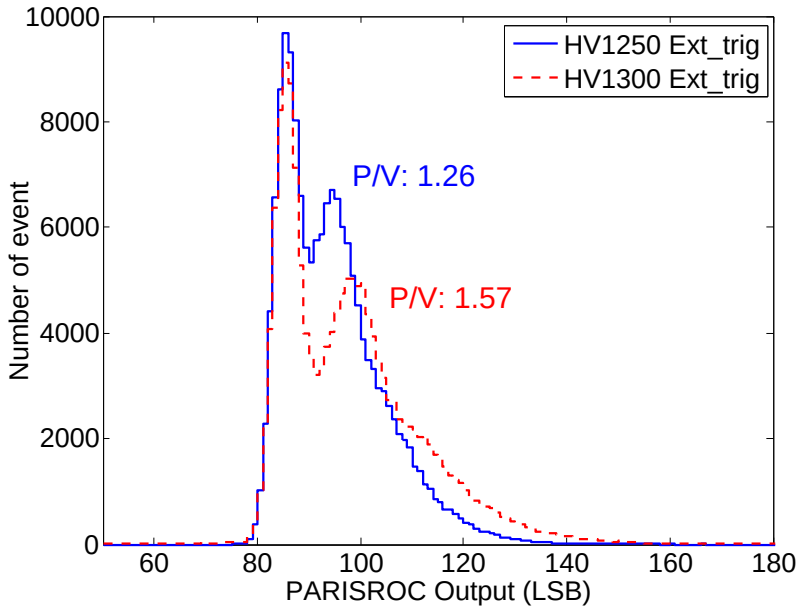


Figure 8.12: Single photoelectron responses of the CR303 measured with the new front-end electronics with external trigger at different high voltages

Figure 8.12 shows the single photoelectron responses (SPR) under different high voltages with an external trigger. In this condition, the SPR of the tube can easily be extracted with a good peak-to-valley (P/V) ratio. For the voltage of -1,250 V, the P/V ratio is about 1.26 (blue solid line) and 1.57 for the voltage of -1,300 V (red dash line). The secondary electron can be observed as well directly in the figure. The result implies that the front-end

electronics and the ASIC works well and has a very good resolution at high voltages. The single photon electron response of a PMT can be clearly measured.

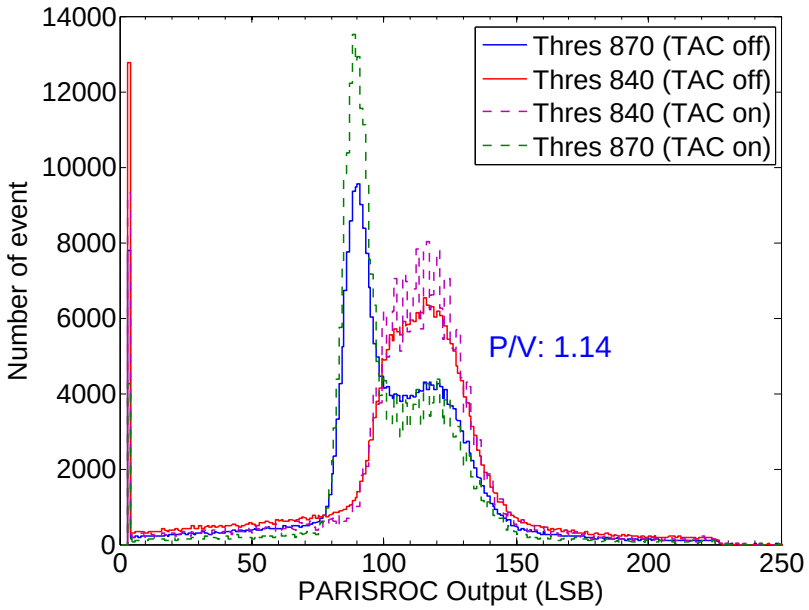


Figure 8.13: Single photoelectron responses of the CR303 measured with the new front-end electronics with internal trigger at different thresholds

Figure 8.13 shows the results obtained with an internal trigger. For the threshold of 840, the pedestal of the SPR cannot be observed, only the location of the peak can be observed (red solid line for TAC off, purple dash line for TAC on). The pedestal is suppressed by the relatively high threshold. The power-on and the power-off states of the TAC unit also affect the charge measurement of the ASIC. The periodical crosstalk from the TAC, which repeats every 4 LSB (purple dash line) [S. Conforti Di Lorenzo, 2010], affects the accuracy of the charge measurement when the internal trigger is used.

The similar tests are repeated at the threshold of 870 (blue solid line for TAC off and green dash line for TAC on). Under this condition, both the pedestal and the SPR peak can be observed. The P/V ratio drops to 1.14 in this case due to the influence of the coupling noise. However, the threshold will not affect the location of the pedestal and the peak. Increasing the gain of the slow shaper in the ASIC could improve the performance and yield better results. The coupling noise from the digital units in the chip should be reduced in the next version of PARISROC.

8.5 Data transmission performance and power consumption

Several tests were also performed to study the data transmission performance of the electronics by using the FPGA as an external trigger source and packet generator. According to the test results, the Ethernet interface on the board provides a maximum average data output rate up to 972 Mbit/s which almost achieves the full bandwidth of a 1 G Ethernet (1000 Mbit/s). This ensures that the performance of the ASIC will not be slowed down by the data transmission system.

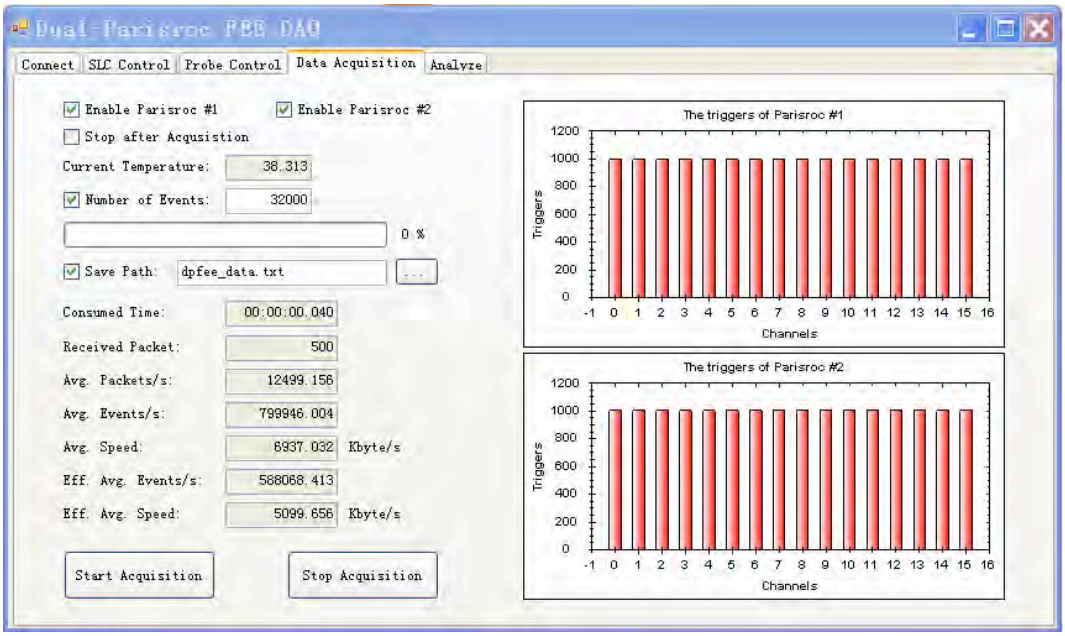


Figure 8.14: Maximum data output rate measured with the DAQ software

The maximum data output rate can be measured with the DAQ software. Figure 8.14 shows an example of the data output measurement. In this case, the result was measured by setting the frequency of the FPGA external trigger to 100 kHz. To acquire 32,000 events only costs about 40 ms. The measured average data rate is about 6.94 Mbyte/s ($\sim$ 55.52 Mbit/s). Each chip produces 400 Kbytes data per second. This also suggests that the effective data rate is around 25 kHz. This result is verified by the time measurement that was discussed previously. The precise value is 24.3 kHz. This test was made with the TAC unit power-on. If one shuts down the TAC, the new DAQ system could process a data

output rate up to 10.27 Mbyte/s ($\sim$ 82.14Mbit/s) without losing any events, when all 32 channels are triggered at an event rate of 37 kHz.

Table 8.4: Measured power consumption of the front-end electronic board

Unit	Power consumption
PARISROC 2 $\times$ 2	$\sim$ 1.0 W
Ethernet interface	$\sim$ 1.1 W
FPGA & Peripherals	$\sim$ 0.88 W
Summary	$\sim$ 2.98 W

The measured power consumption of each unit and the whole board are shown in table 8.4. Based on the measurement, the whole board only consumes about 2.98 W when ethernet interface starts up. It suggests a power consumption of 128 W (Ethernet off) or 196 W (Ethernet on) for a WFCTA telescope (64 sub-clusters) that is smaller than the power budget (260 W per telescope).

8.6 Summary of the test results of the FEE

In order to verify and evaluate the design and the implementation of the new electronics, a series of tests have been performed, including charge measurements, time measurements, single channel event rate, pedestal monitoring, performance of the prototype DAQ that was developed in this thesis and described in chapter 7, PMT measurement and evaluation of the power consumption of board.

According to the charge measurement, thanks to the use of the second channel for extending the dynamic range, the new FEE could cover a dynamic range from 80 fC to 160 pC with the nonlinearity better than 1 %. After changing the criterion from the nonlinearity to the relative deviation which is defined by IHEP, the FEE could roughly cover a dynamic range from 320 fC to 160 pC with the relative deviation better than 2 %. However, the upper-limit output of the second channel has not been tested yet, due to the limitation of the used signal generator. The further tests are needed to find out the final dynamic range of the system.

Moreover, due to the imperfection of the auto-gain controller in PARISROC 2, a discontinuity existing in the output can be observed. Even though this discontinuity can be avoided by alternatively using the different PARISROC 2 channels in the data processing, this bug should be fixed in the next version of the PARISROC chip.

For the time measurement, by using a new proposed time calibration method, a very high-precision has been achieved. With this new method, the best result of the RMS of the distribution of the time interval of the adjacent events is about 263.19 ps and 450 ps for the worst case. The common method is still useful to study the behavior of the TAC and to measure the nonlinearity of the time measurement unit. The best application of the new calibration method is for the mass verification.

For the signals with a fixed frequency and a fixed amplitude, the single channel event rate of the ASIC could reach 37 kHz, when the TAC is shutdown. However, for the random signals, the event rate drops to around 5 kHz, according to the datasheet of the chip, due to the working principle of the Wilkinson ADC embedded in the PARISROC 2.

Due to the architecture of the preamplifier of the PARISROC 2 chip, the pedestal monitoring can be done by monitoring the variation of the event rate or by using an external trigger.

The electronics has been evaluated with a candidate PMT of the WFCTA, which is CR303. The results show that the ASIC has a good charge resolution and is able to distinguish the single photoelectron and measure the SPR of the PMT. The periodical crosstalk from the TAC was observed to affect the accuracy of charge measurement when the internal trigger is used. The interference appears every 4 LSB repeatedly. This should also be improved in the next PARISROC chip.

Based on the test result, the maximum average data output rate of the on-board Ethernet interface is up to 972 Mbit/s. For the new DAQ system, the highest recorded data rate is about 10.27 Mbyte/s or 82.14 Mbit/s, which implies an event rate of 37 kHz. This event rate was cross-checked with the time measurement.

One of the most notable advantages for an ASIC-based design is its low power consumption. The measured power consumption of the board is only about 2.98 W when the Ethernet interface is powered. Without considering the influence of the communication system, the power consumption of the rest of the components on the board is about 1.88 W.

Chapter 9
Conclusion and perspective

In the history of cosmic ray studies, the development of instrument has always played a very important role. After physicists determine the scientific goals of an experiment, the first-priority task is to design, implement and operate a prototype detector in order to prove the technical feasibility of the experiment. This is also the case for the LHAASO experiment, which is a large, hybrid-detection observatory, aiming to answer the puzzle of cosmic rays.

However, the modern scientific instruments are no longer as simple as the ones that were used by V. F. Hess. To plan and implement a real detector is a very complex project that includes many steps and efforts of different people. It is obvious that the discussion of the design of the whole detector is fully beyond the scope of this thesis. Hence, this thesis is only focused on the study of the front-end electronics for one of the LHAASO detectors, namely WFCTA. The purpose of the thesis is to design a prototype electronic system for the Cherenkov telescopes. In order to realize this goal, six topics from the physical simulation to the DAQ system have been discussed and presented in this thesis. These topics are concluded in the following:

1) Prior to the electronic design, physics simulations were made to understand the propagation of cosmic rays in the atmosphere and to figure out the characteristics of the input signal of the electronics. In this process, a simulation program, which name is CORSIKA, was exploited to generate cosmic ray events and trace all the particles produced during the propagation. Based on these events from CORSIKA, another program from IHEP was used to simulate the optical behavior of the WFCTA telescope and to record the input signals of each tube in the camera array. Two important parameters of the input signal were retrieved, which are the number of photons or photoelectrons and their arrival times. The number of photons or photoelectrons determines the charge of the

input signal, and the arrival time defines the shape of it. These simulations also helped to deepen the understanding of the specifications of the telescope and to cross-check them.

2) A sensor is used to convert the natural physical signals such as light into electronics one such as current. In this case, the sensor is a photomultiplier. A high-efficiency and high-accurate PMT model was successfully built to fit both physical and electronic simulations with the parameters. The parameters of this model directly source from the manual of the tube, which makes the use of the model very simple. This new model and another four different PMT models were compared and discussed in details to reveal their advantages and disadvantages.

3) A behavior model for the design based on the classical electronics was built and studied by using the new PMT model as the input source. For comparison, a behavior model of an ASIC solution based on PARISROC 2 was also studied. According to the results, in theory, both solutions all fit the requirements of the telescope. Following the rapid development of the micro-electronics, the natural choice for the electronics of the future, high-density, low power dissipation and high-performance telescopes is based on the ASICs. In particular, an ASIC based solution would be well-suited for the WFCTA telescopes of LHAASO.

4) The ASIC was evaluated by using the existing application boards such as the PMm^2. The results show that the existing designs cannot fully demonstrate the real performance of the chip. Therefore, a new LHAASO-oriented front-end electronic board that is based on two PARISROC 2 was developed and implemented. The board was successfully designed and fabricated with the help of the OMEGA microelectronics group and the SEP of the IPNO.

5) The reason of the limited performance of the existing boards such as the PMm^2 board and the LAL board is due to their USB-based communication systems. In order to improve the performance, three fully user-defined FPGA-embedded IP hardcores were implemented to manage the communication through network. There are a PEDTP high-level protocol which maps to the application layer, an ASSL TCP/IP protocol suite corresponding to the transport layer protocols which includes a IP core, an ARP core, a UDP core and a TCP core, and a MAC controller core which maps to the network interface layer and actually is used to encapsulate and decapsulate the Ethernet packets

from the separated hardware PHY chip. Based on these IP cores, the related software and hardware of the DAQ system on the host computer side and on the FPGA side were both finished and verified.

6) A series of tests have been performed to verify the concept of the design and to evaluate the performance of the application board, including the charge measurement, the time measurement, the single channel event rate, the pedestal monitoring, the performance of the DAQ, the PMT measurement and the power consumption of board. The preliminary results show the good general performance of the PARISROC 2 and that this design nearly meets the specifications of the WFCTA.

As a prototype electronics, the tests and the modifications of it are not finished. The future studies and works will be focused on the improvement of the FEE and the evaluation of this board as a subcluster of a prototype telescope. For the purpose of efficiency, the communication system of this front-end electronics is based on the UDP protocol now. However, due to the limitations of the UDP, the connection between the client and the server is still unreliable. The TCP protocol will be induced to balance the performance and the reliability of the communication and to avoid event loses in the next step. Furthermore, the software application at the host side will continually evolve to provide a friendly interface for those who are not familiar with the complex ASIC chips as PARISROC 2.

However, it is fair to say that there are still some specifications of the telescope that are not perfectly fulfilled. The most concerning parameters are the dynamic range of the charge measurement and the single channel event rate. For the next version of the ASIC, it appears necessary to increase the dynamic range of a single PARISROC channel to a larger scale and to boost the maximum signal input rate from the present 20 kHz/channel to at least 100 kHz. Moreover, the tests also reveal some imperfections and deficiencies of the ASIC, mostly related to the signal integrity. They should be improved and fixed in the next version of the ASIC. Some extra functions and more detailed control commands will be added as well. All these modifications will make the new PARISROC 3 ASIC a good candidate for the WFCTA of LHAASO.

At the same time of the writing of the thesis, the new ASIC is under design and will be finished soon. The future plan also includes the design of a new front-end board based on the PARISROC 3.

Appendix A

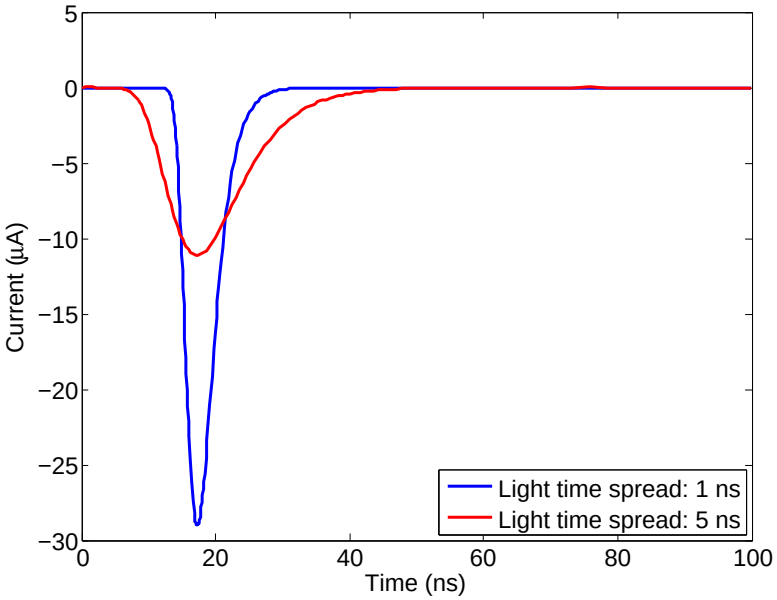
Examples of the proposed PMT model

A.1 Models for real PMT

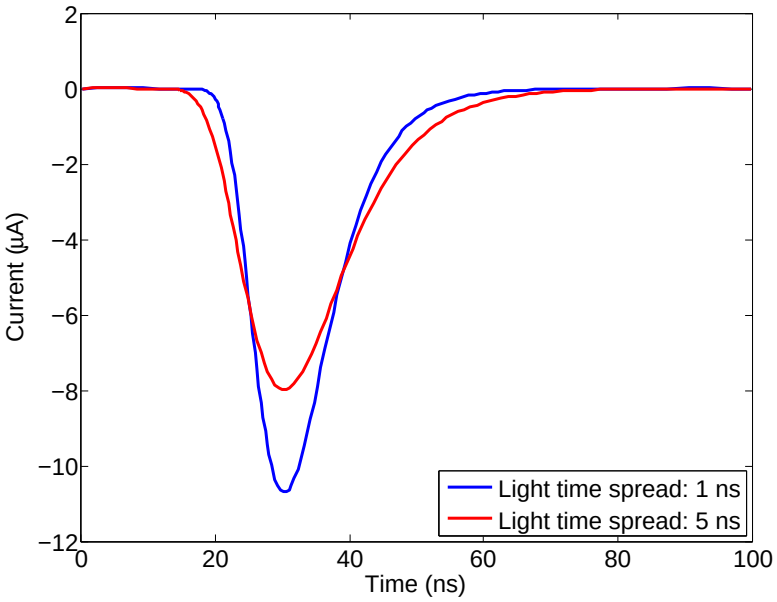
Two PMTs which are Hamamatsu R1924A [Hamamatsu, 2003] and HZC Photonics XP3062 [HZC Photonics, 2011] are modelized with the model presented in Chapter 4. Their specifications are listed in table A.1.The single photoelectron responses of different light time spreads for both models are shown in figures A.1. Usually, a long duration of input signal leads to a long-duration but small-amplitude signal. In spite of the different shape of the output, the charge of the signal remains the same. It gives us a possibility to generate different types of signal with this model.

Table A.1: PMT specifications for Hamamatsu R1924A and HZC Photonics XP3062

Specification	Hamamatsu R1924A	HZC Photonics XP3062
Input signal	1 p.e	1 p.e
Light time spread	1 ns and 5 ns	1 ns and 5 ns
Gain	10^6	10^6
Anode pulse rise time	1.5 ns	3 ns
Electron transit time	0.9 ns	4.5 ns
Transit time spread	17 ns	30 ns
Capacitance to all electrodes	–	5 pF



(a) Single photoelectron response of Hamamatsu R1924A



(b) Single photoelectron response of HZC Photonics XP3062

Figure A.1: Single photoelectron response of different PMTs with different light time spread

A.2 Model for Cherenkov response

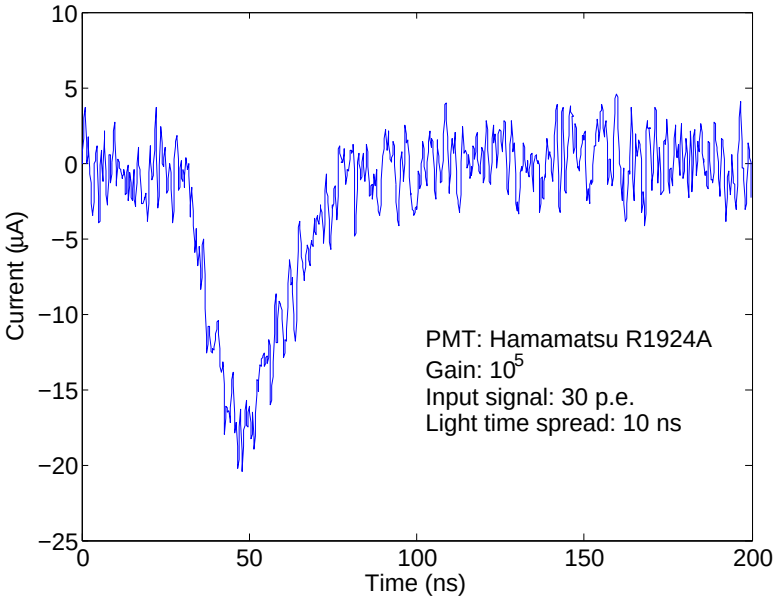
The most important motivation of creating this model is to simulate the Cherenkov response of the PMT. As an extremely short flash light, the Cherenkov response of a PMT has no difference from the one that is shown in figure A.1 except the duration of the input light and the number of the injected photons. These two parameters can be retrieved from the cosmic ray simulation which is introduced in Chapter 4. To simulate the response of the WFCTA, the PMT Hamamatsu R1924A is selected and the gain of the tube is adjusted to 10^5. The rest of the parameters are listed in table A.1. With the results from the physical simulation, the Cherenkov responses of a single tube in the camera array can be plotted and are shown in figure A.2. The showers are induced by a proton shower (energy: 30 TeV, zenith angle: 0°) and an iron shower (energy: 20 PeV, zenith angle: 0°).

The Cherenkov response of a tube with night sky background (NSB) can be also created with this model. Figure A.3 gives an example of this kind of output. In the figure, the input signal is about 50 p.e., and the noise level of the tube is about 3 to 4 p.e.. The NSB is from 5 to 20 p.e.. The input signal can be easily extracted from the background with an appropriate threshold.

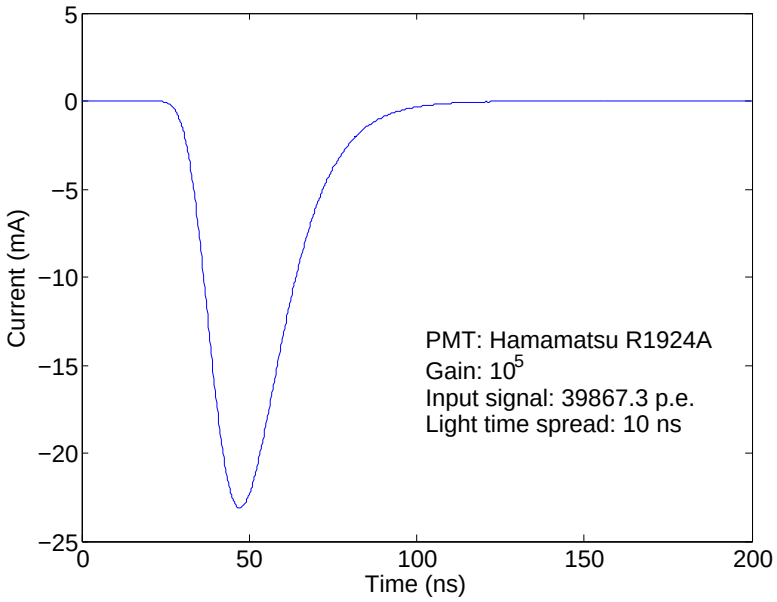
A.3 Model for Fluorescence response

The fluorescence type of long duration signal can be produced with this model as well. Figure A.4 presents an example of the fluorescence response of Hamamatsu R1924A. The signal lasts about 794 ns and the charge of it is around 500 pC.

A software model generator was designed and implemented to automatically produce responses for Cherenkov and fluorescence signals for the evaluation.



(a) Cherenkov response of a tube induced by a proton shower (30 TeV, 0°)



(b) Cherenkov response of a tube induced by an iron shower (20 PeV, 0°)

Figure A.2: Cherenkov responses of a tube induced by different extensive air showers

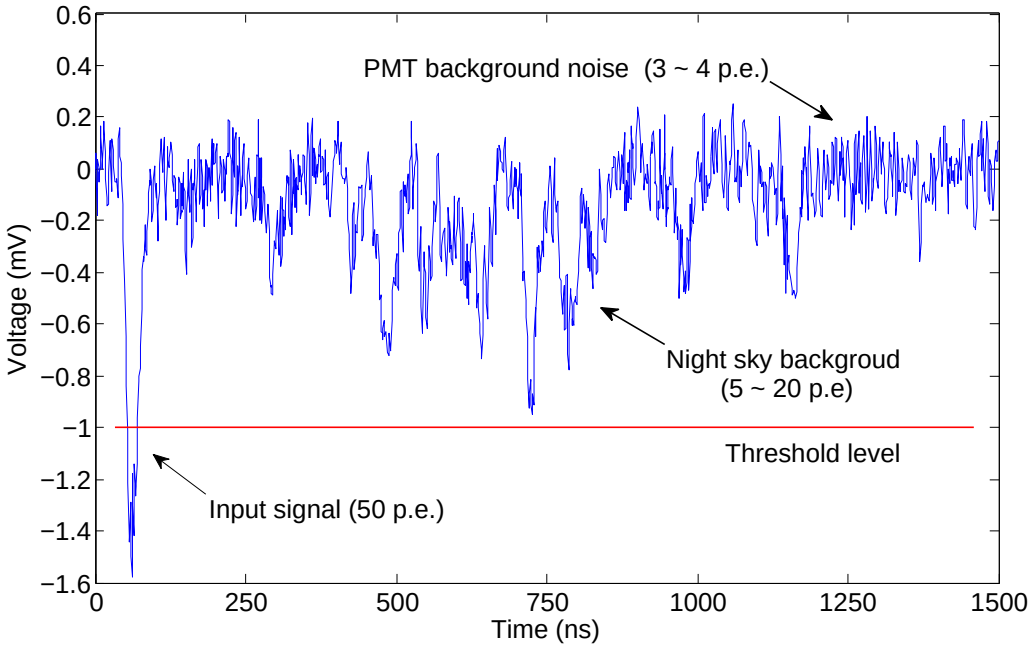


Figure A.3: Cherenkov response with night sky background

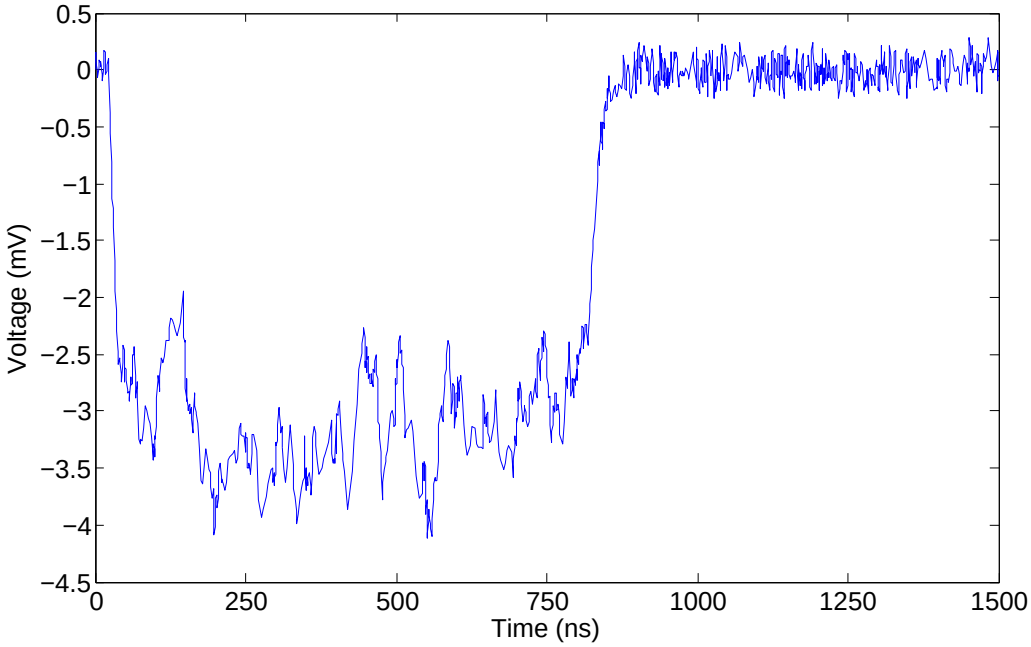


Figure A.4: Fluorescence response of Hamamatsu R1924A

Appendix B

Interface of the DAQ software

The DAQ software is written in C# and supports five basic functions, including the connection and control registers setting, the slow control register setting, the probe register setting, the data acquisition and the data analysis. The five main interfaces of the software are shown in figure B.1, B.2, B.3, B.4 and B.5, respectively.

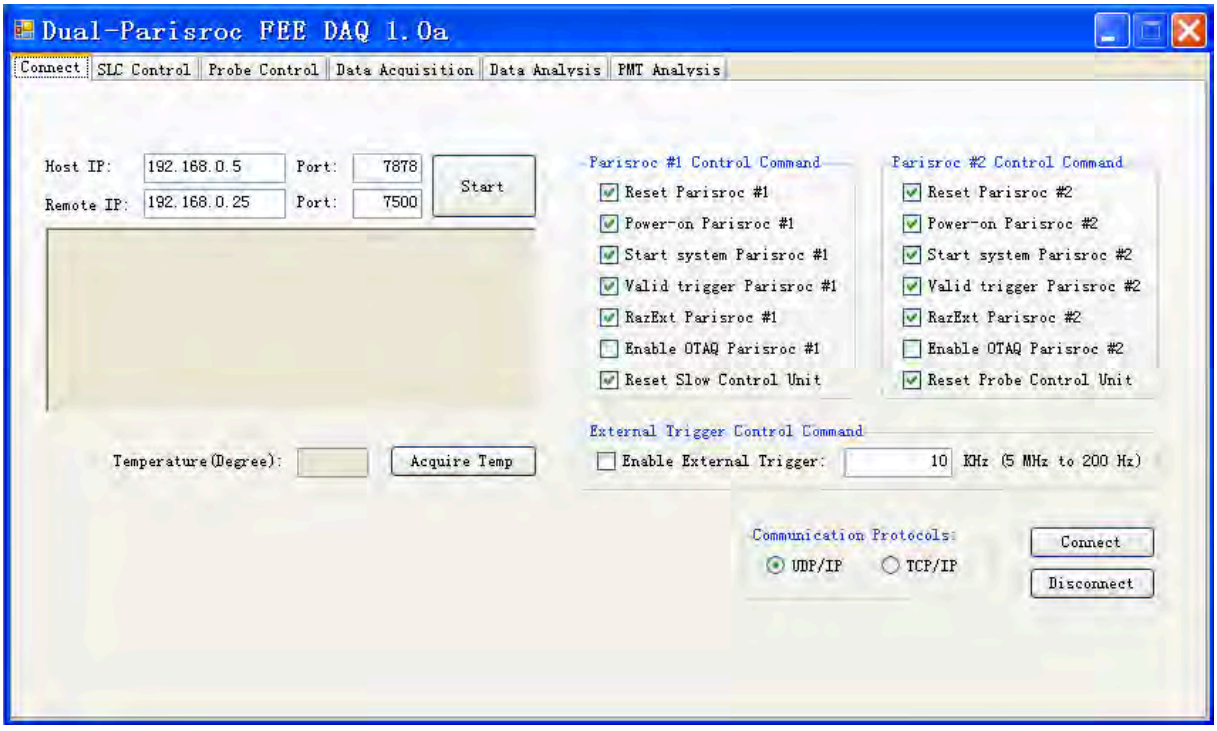


Figure B.1: Connection and chip register control interface

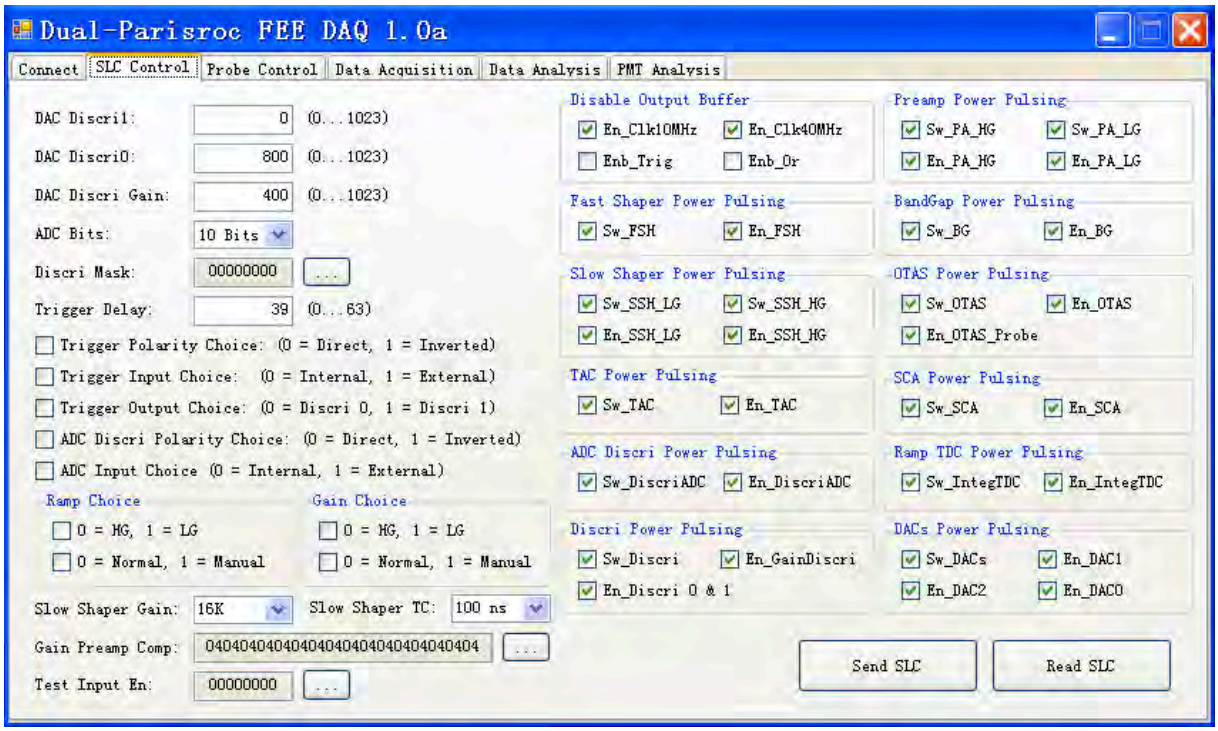


Figure B.2: Slow control register of the ASIC setting interface

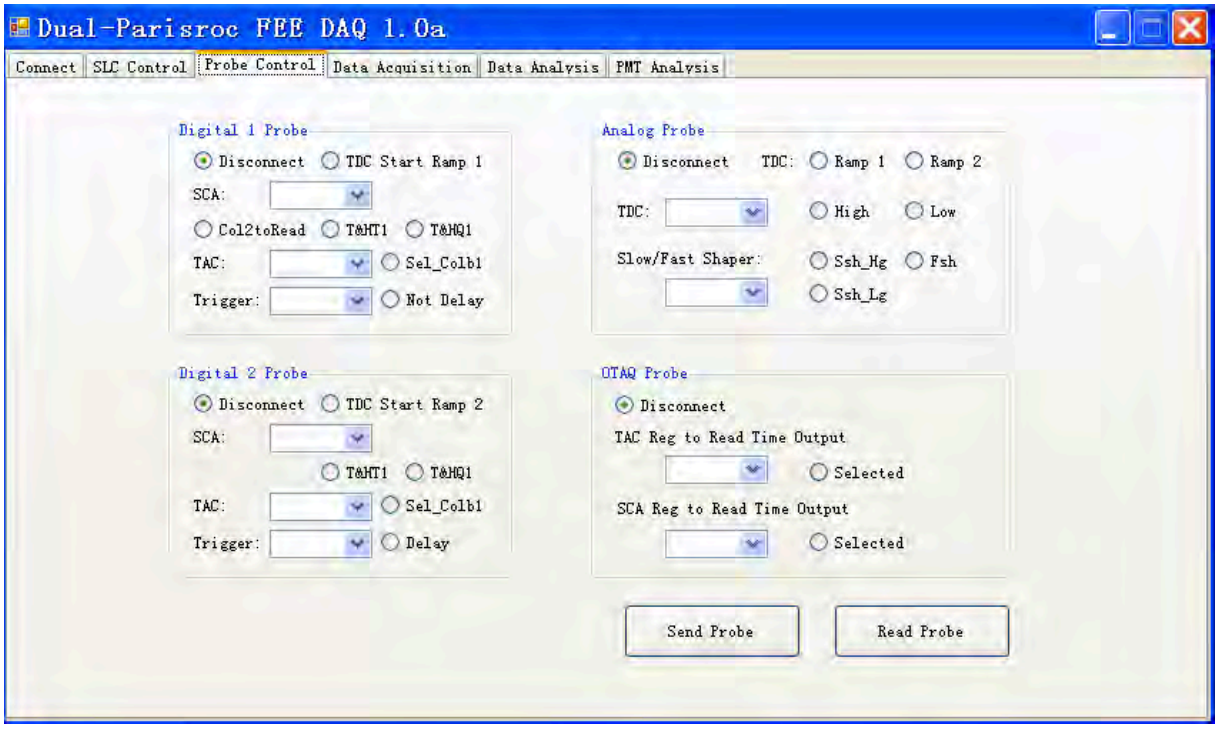


Figure B.3: Probe register of the ASIC setting interface

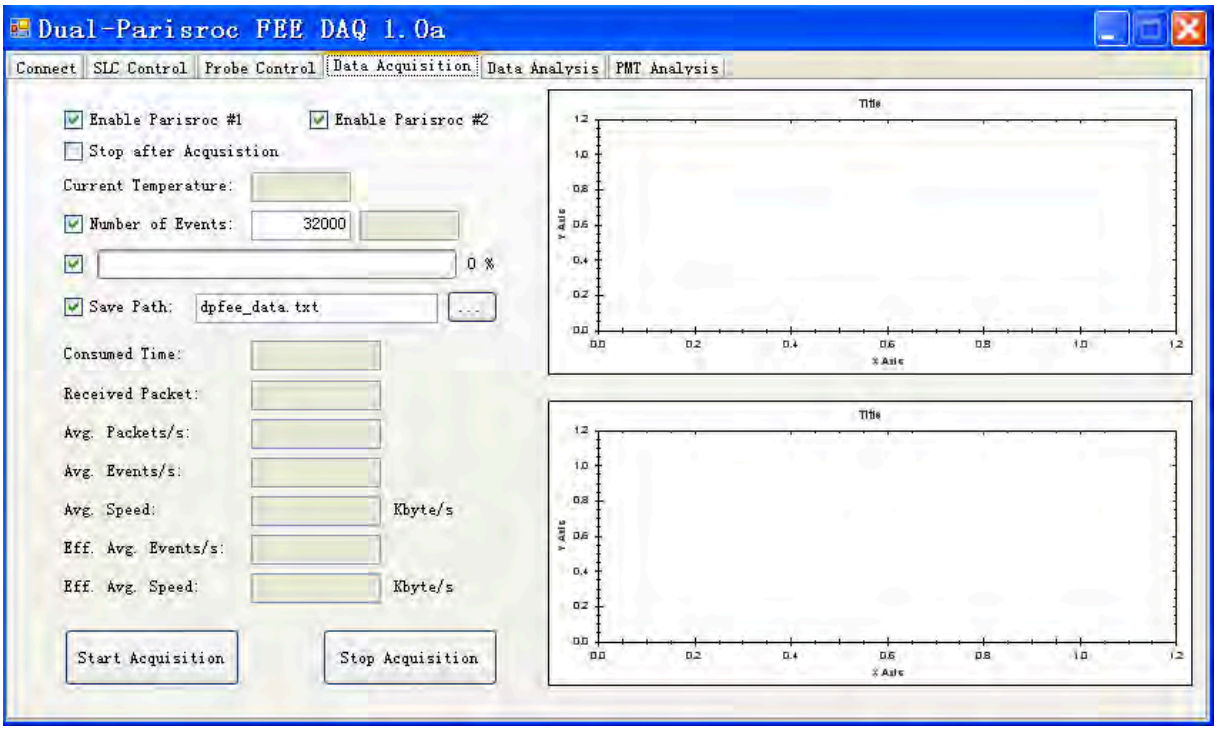


Figure B.4: Data acquisition Interface

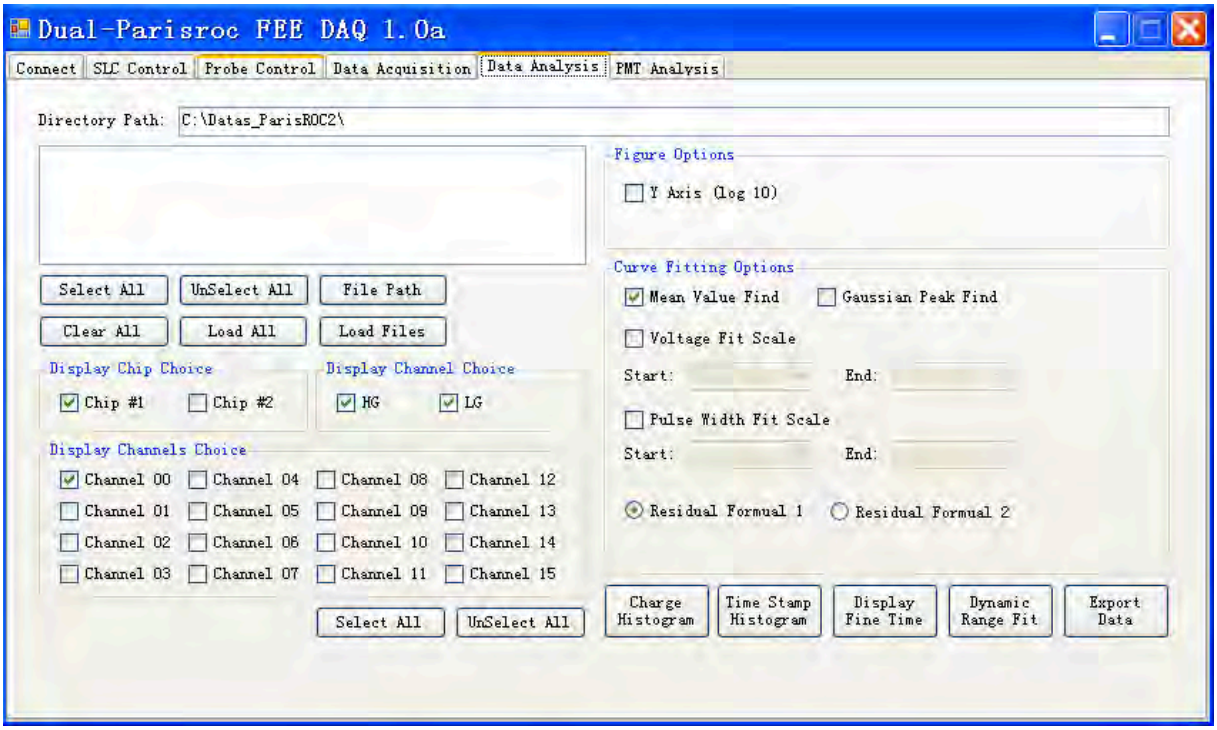


Figure B.5: Data analysis Interface

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