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# Belle II Vertex Detector: Run Performance (PXD + SVD) and Upgrade Developments (VTX)

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The Belle II experiment at SuperKEKB continues to pursue high-precision measurements in Standard Model studies and in searches for physics beyond the Standard Model, with a target dataset of 50 $\mathrm{ab}^{-1}$ and peak luminosities of $6 \times 10^{35}$ $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The current Vertex Detector (VXD), composed of the DEpleted P-channel Field Effect Transistor (DEPFET)-based Pixel Detector (PXD) and double-sided strip-based Silicon Vertex Detector (SVD), has achieved excellent tracking and vertexing performance through Run 1 and Run 2. To address future challenges from increased luminosity and background, a new all-pixel Vertex Detector (VTX) is under development, utilizing radiation-hard DMAPS technology based on the OBELIX sensor. In this contribution, we present the performance of the current VXD system, highlight operational challenges, and present the validation and integration status of the upcoming VTX upgrade.

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## 1. Introduction

The Belle II experiment, a high-precision B-factory at the SuperKEKB collider in Tsukuba, Japan, is intended to explore for possible new physics beyond the Standard Model by functioning as an intensity frontier in one of the highest luminosity environments. SuperKEKB achieved a new world record in December 2024 with an instantaneous luminosity of $5.1 \times 10^{34}$ cm$^{-2}$s$^{-1}$, adding to a total data set that has surpassed 575 fb$^{-1}$ since 2019 and aiming towards 50 ab$^{-1}$ of data in the next decade [1, 2]. This operational scale enables Belle II to probe rare processes, time-dependent measurements, and phenomena beyond established physics.

The Vertex Detector (VXD) is the central component of Belle II's tracking and vertexing capabilities (see Figure 1). It combines compact advanced sensors to optimise efficiency and spatial resolution closest to the interaction point. Built on the DEpleted P-channel Field Effect Transistor (DEPFET) active pixel sensors, the innermost Pixel Detector (PXD) has 40 modules organised in two circular layers. The PXD is fully surrounded by the Silicon Vertex Detector (SVD), which consisted of four layers of double-sided silicon strip sensors which provide excellent and stable over time hit efficiency irrespective of high background conditions.

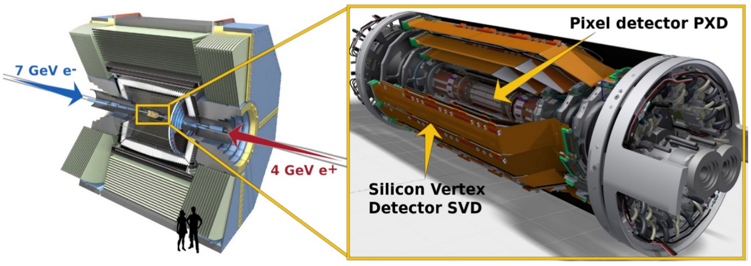


**Figure 1:** Schematic view of the Belle II detector. The inset shows the position of the VXD, consisting of the PXD and SVD.

The first Belle II data-taking period (Run 1, 2019–2022) started with the full SVD configuration and a reduced PXD configuration, which included a complete inner layer (eight ladders) and only two of the twelve outer-layer ladders. Each ladder consists of two pixel modules. After the long shutdown (LS1), the second Belle II data-taking period (Run 2) started in 2024 with the full two-layer PXD (PXD2) installed, while maintaining the stable SVD configuration [3]. With these improvements, VXD maintained stable performance and ensured the system's resilience, even under increasing luminosity and high beam-background conditions.

While the existing VXD operates efficiently under the current background conditions, future increases in luminosity will lead to significantly higher background levels, which would challenge the long-term tracking and vertexing performance. Therefore, a new pixel-based Vertex Detector (VTX) is being developed to ensure stable operation under these future conditions. The VTX utilizes depleted monolithic active pixel sensors (DMAPS), primarily the OBELIX chip, to enhance tracking and vertexing capabilities. This new VTX aims for higher radiation tolerance and vertex resolution, supporting Belle II's goals of 50 ab$^{-1}$ integrated luminosity and operation at $6 \times 10^{35}$ cm$^{-2}$s$^{-1}$.

## 2. PXD: Pixel Vertex Detector

### 2.1 The Pixel Vertex Detector

In this section, we discuss the innermost layer of the Belle II vertex detector, PXD, which is crucial for precise tracking and vertex reconstruction [3]. It is the first full-scale detector to use DEPFET sensor technology in a high-energy physics experiment. Here, each DEPFET pixel combines sensing and amplification within a single structure. When a charged particle passes through the fully depleted silicon bulk, it generates electron–hole pairs. The electrons are collected in an internal gate located beneath the p-channel transistor, while the holes drift toward the backside contact. The accumulated charge in the internal gate modulates the drain current of the FET when the pixel is activated during readout, providing in-pixel signal amplification with high spatial resolution and low noise, ideal for the precision requirements of Belle II.

The PXD is based on self-supporting all-silicon modules, where the sensor area known as active area is thinned down to around 75 µm. This design minimizes multiple scattering and keeps the average material per layer at roughly 0.21% of a radiation length ($X_0$), preserving the precision of track reconstruction near the interaction point. At the end of each module, custom ASICs manage the readout and digitization processes for the DEPFET signals. These include Drain Current Digitizers (DCDs), that convert the analog pixel currents into digital form, Data Handling Processors (DHPs), responsible for zero suppression and data compression, and Switcher chips that control the rolling-shutter readout. Each module consumes about 8–9 W, mainly due to the power dissipation of the DCD and DHP ASICs [3]. Two modules are combined to form a ladder, and in total, the PXD contains 20 ladders distributed over two layers. The PXD is divided into two half-shells, each supporting ten ladders mounted on support cooling blocks (SCBs) which provide both mechanical support and cooling, interconnected by carbon-fiber tubes. The SCBs are cooled using a two-phase $CO_2$ system that removes the heat generated by the readout ASICs (DCDs and DHPs), while a continuous flow of $N_2$ gas is directed toward the sensor matrix and the Switcher ASICs to maintain stable thermal conditions near the sensor areas.

### 2.2 Operation Challenges in Run 1 and Run 2

During Run 1 (2019–2022), Belle II operated a reduced PXD setup (PXD1) consisting of a fully equipped inner-layer and only two outer-layer ladders. Despite this limitation, PXD1 delivered excellent performance, di-muon hit efficiency reached approximately 99% within the fiducial region [4]. Noise levels remained impressively low, below 1 ADU (analog-to-digital units), and the impact parameter resolution improved by a factor of 1.5 to 2 compared to the predecessor Belle experiment. However, the detector also faced significant challenges from sudden beam loss (SBLs) events. These caused intense radiation doses $O(10\,\mathrm{Gy})$ in 40 µs [5], causing damage to several switcher ASICs. To mitigate this, faster beam loss detection and emergency power-down procedures were implemented during LS1. These improvements reduced the time to detect beam loss and triggered automatic shutdowns, protecting the detector from damage. Additionally, new sensors were installed around the accelerator rings during LS1 to better understand the origin of SBLs.

During LS1 in 2023, the complete two-layer PXD (PXD2) was integrated into Belle II for Run 2. Pre-commissioning tests at DESY optimized module configurations and revealed that thermal stress at higher operating temperatures could weaken the adhesive joints, causing slight ladder distortion. Once the detector was installed at KEK, subsequent cosmic-ray alignment checks demonstrated overall structural stability. For most ladders, bending remained below 0.5 mm, except for 2 ladders bending around 1 mm, but still within safe limits. Modules with higher deformation were powered down during early Run 2, with continuous monitoring to ensure stability.

Full data-taking with PXD2 began in February 2024, operating 35 out of 40 modules. PXD achieved a pixel-hit efficiency above 98% in the fiducial volume, confirming excellent operational stability. In April 2024, two SBL events caused localized radiation damage, affecting the readout for $\approx 2\%$ of pixels and increasing noise in some Switcher ASICs, which led to a rise in temperature. To study the SBL events in more detail and to prevent similar damage in future operation, PXD was powered off during beam operation as a safety measure. As the investigation of the SBL events continues, PXD will remain off during the 2025 operation period. The plan is to restart PXD operation once the source of SBLs is identified and corrective actions have been implemented. Additionally, the PXD group is developing a fast-shutdown board that will reduce the power-off reaction time in future runs, limiting the risk of damage if other SBLs occur.

## 3. SVD: Silicon Vertex Detector

### 3.1 The Silicon Vertex Detector

This section focuses on the outer component of the Belle II Vertex Detector, SVD, consisting of four layers of double-sided silicon strip detectors (DSSDs) positioned at radial distances from about 39 mm to 135 mm [6]. Each DSSD is built on an n-type silicon bulk, with p-doped strips on one side (P-side) and n-doped strips on the other (N-side). The p-side and n-side strips are oriented orthogonally, measuring the $r\phi$ coordinate and the $z$ coordinate respectively. This geometry provides large angular coverage and enables accurate projection of charged-particle tracks toward the inner PXD. In addition, SVD performs stand-alone tracking for low-momentum particles, reconstructs decay vertices of long-lived neutral hadrons such as $K_S^0$ and $\Lambda$, and contributes in particle identification through measurements of specific energy loss.

Each layer of SVD is built from rectangular and trapezoidal DSSDs, designed to optimize coverage in both the barrel and forward regions. Every sensor employs AC-coupled readout strips on both sides, allowing accurate two-dimensional position determination. Altogether, the SVD comprises 172 sensors with approximately 224000 readout strips, providing an active detection area of around 1.2 $m^2$. With a material budget of roughly 0.7% $X_0$ per layer, the design minimizes multiple scattering while maintaining mechanical stability. Signal processing is handled by the radiation-tolerant APV25 ASIC, which contains 128 input channels and operates with a 50 ns shaping time. The APV25 is operated in multi-peak mode at 31.8 MHz (one-eighth of the SuperKEKB bunch frequency), enabling hit-time reconstruction with about 3 ns resolution. SVD combines a hit efficiency above 99% with excellent spatial and temporal resolution, ensuring high-quality tracking performance [7].

### 3.2 Operation Challenges in Run 1 and Run 2

During Run 1 (2019–2022), SVD operated stably, with fewer than 1% of strips masked due to sensor defects. The detector maintained a hit efficiency above 99%, and the signal cluster charge was consistent with expectations for minimum-ionizing particles ($\approx 24000\ e^-$) within a 15% calibration uncertainty. Cluster signal-to-noise ratios for all 172 DSSD sensors range from 13 to 30, depending on sensor side and position. The position resolution remained stable within 10–25 µm, while the hit-time resolutions were 2.9 ns for the P-side and 2.4 ns for the N-side during Run 1.

Despite the stable performance, beam-induced background was continuously monitored during operation, as it can increase hit occupancy and cause radiation damage that affects strip noise, leakage current, and depletion voltage. In Layer 3, hit occupancy stayed below 0.5%, maintaining tracking capability. The integrated radiation dose reached about 70 krad ($1.6 \times 10^{11}\ \mathrm{n_{eq}/cm^2}$), causing a moderate increase in noise, about 20% on the N-side and 30% on the P-side [7]. Sensor noise rose during Run 1 primarily due to radiation but partially recovered after LS1, thanks to lower operating temperature.

During Run 2 (2024 - ongoing), SVD was reinstalled without major issues. Performance metrics such as cluster charge, signal-to-noise ratio, and hit efficiency remained stable, with most sensors achieving efficiencies above 99%. The detector showed stable operation throughout the entire data-taking period. Background levels during this run were approximately 1%, indicating a well-controlled environment that preserved the detector's performance. The integrated dose in Layer 3 increased to about 100 krad ($\sim 2.5 \times 10^{11}\ \mathrm{n_{eq}/cm^2}$), with no evidence of any degrading impact on SVD performance. Across both runs, SVD operated with high reliability and no significant degradation was observed. To further enhance performance under higher background conditions, new algorithms are being developed that utilize the SVD's precise timing information to improve background suppression and reconstruction efficiency [7].

## 4. VTX: New Vertex Detector Upgrade

### 4.1 New Vertex Detector

In order to achieve the requirements of the luminosity target of $6 \times 10^{35}\ \mathrm{cm^{-2}s^{-1}}$, Belle II collaboration is preparing to significantly improve its vertex detection system. The current Vertex Detector, consisting of PXD and SVD, has so far provided excellent spatial resolution, but as luminosity increases, its occupancy and background sensitivity become limiting factors for tracking and vertex reconstruction. To ensure long-term performance and accommodate changes in the interaction region envelope required to reach higher luminosity, the collaboration plans to install a fully pixelated VTX during a second long shutdown planned around 2032. [8].

This new design (see Figure 2) is based entirely on depleted monolithic active pixel sensors (DMAPS) arranged in six layers, with an overall material budget around 3% $X_0$ to maintain efficiency for low-momentum particles. In the upgraded design, inner VTX (iVTX) consists of two ultra-thin layers located at radii of 14 mm and 22 mm, each integrating four OBELIX chips fabricated on the same wafer, while the outer VTX (oVTX) adds four outer layers that extend the detector radius to approximately 140 mm (see Figure 3). The iVTX modules feature an all-silicon structure with a material budget about 0.3% $X_0$ per layer, and are exploring cooling options such as thermal conduction via Thermal Pyrolytic Graphite layers, and liquid cooling with thin aluminum pipes along the ladder edges. In contrast, the omega-shaped oVTX modules use lightweight carbon-fiber supports with a cold plate and embedded liquid cooling pipes, maintaining a material budget of up to 0.8% $X_0$ per layer.

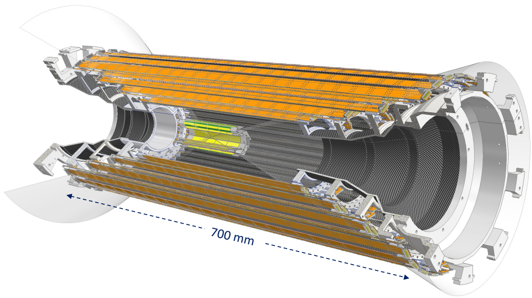


**Figure 2:** Schematic of the new Belle II Vertex Detector (VTX) upgrade based on DMAPS.

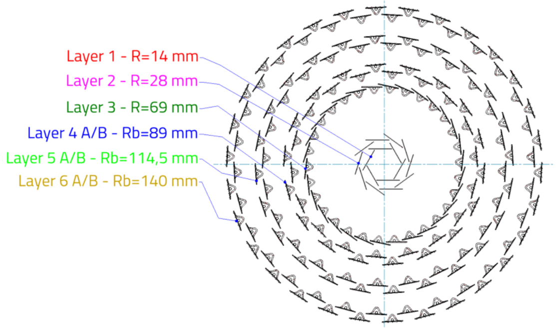


**Figure 3:** Layered structure of the new Belle II VTX.

The central component of the upgrade is the OBELIX chip (see Figure 4), a monolithic CMOS pixel sensor derived from the TJ-Monopix2 chip [9], with an extended area and a new digital periphery developed for the application in Belle II [10]. The design of the OBELIX chip is now in its final development phase. It will be manufactured using 180-nm CMOS technology, modified to improve radiation hardness, and will feature a 33 µm pixel pitch with a timestamp resolution of 50 ns. The chip's high readout speed enables it to efficiently handle hit rates up to 120 MHz/cm$^2$, matching the background conditions expected at peak SuperKEKB luminosity. The uniform adoption of DMAPS technology across all VTX layers not only improves spatial and timing resolution but also enables reduced integration times and lower power consumption. With these advancements, VTX is expected to significantly improve vertex resolution and tracking performance, particularly for low-momentum particles. These upgrades will allow Belle II to maintain and extend its sensitivity to flavor physics and rare-decay processes well into the next decade.

### 4.2 Validation, Beam Tests, and Integration Outlook

Here, we summarize performance studies of the predecessor TJ-Monopix2 sensor, that were crucial to validate key features for the OBELIX sensor design [11]. Beam tests with 3–5 GeV electrons at DESY demonstrated hit detection efficiency above 99% and spatial resolutions of about 9 µm could be achieved with non-irradiated TJ-Monopix2 devices.

In March 2025, the radiation tolerance of the sensor was examined through a new beam tests on proton and electron irradiation TJ-Monopix2 chips, with fluences up to $5 \times 10^{14}$ $n_{eq}/cm^2$, operated at high temperature. The results indicate that efficiency above 99% could be achieved increasing the bias voltage, that the DC-coupled front-end design maintain stable and efficient operation up to approximately 40 °C, while AC coupled implementation showed lower efficiency and stronger temperature dependence. These findings inform the iVTX cooling design, where efficient thermal management is critical due to the limited space and low material budget requirements. The final cooling solution, however, is still under evaluation.

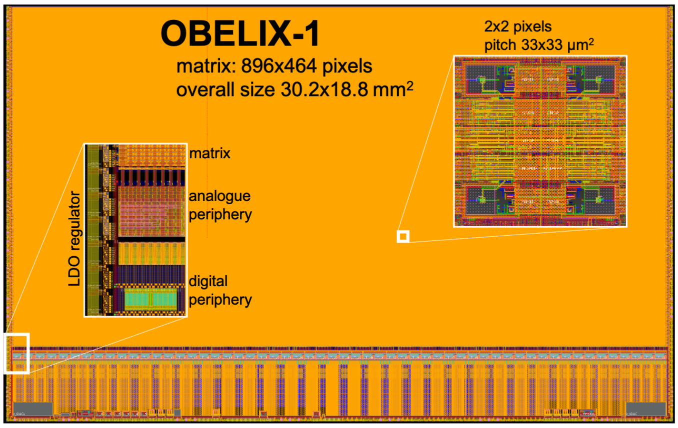


**Figure 4:** The layout of OBELIX-1 chip

As integration efforts continue, full prototyping and thermal validation are planned ahead of the OBELIX-1 submission in December 2025. These developments aim to ensure that the VTX meets the performance requirements of high-luminosity Belle II throughout its operation.

## 5. Summary and Outlook

The current Belle II Vertex Detector has delivered excellent hit efficiency, spatial resolution, and operational stability throughout Runs 1 and 2, even under increasing background conditions. Looking ahead to operation at significantly higher luminosity, the fully pixelated VTX upgrade has been proposed to enhance vertexing performance. Its DMAPS-based structure, focused on the OBELIX chip, has confirmed high efficiency, good spatial resolution, and radiation tolerance in recent beam and irradiation studies performed on its predecessor, TJ-Monopix2 sensor. The next phase of development focuses on full-system prototyping, thermal optimization, and integration toward the OBELIX-1 submission in 2025. With these advancements, the VTX will provide the precision and robustness required for Belle II to achieve its long-term physics goals in the coming decade.

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