Reliability evaluation of the CAEN DT5202 for high-rate data acquisition

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Abstract. Multichannel readout systems play an important role in contemporary physics experiments. Apart from custom-designed highly specialized electronics, several commercial solutions exist on the market. The CAEN DT5202 readout module, comprised of two Citiroc 1A ASICs for a total of 64 channels, was chosen as a typical example. Its performance was studied in specific use cases in a laboratory test environment. The preliminary results of the tests and the evaluation of the hardware module for its applicability in particle detector readout systems are presented. In addition, the control software shipped together with the module has also been studied and its current limitations are discussed.

1. Introduction

Nowadays, silicon photomultipliers (SiPMs) [1] are a common choice as photodetectors in various experimental systems, replacing conventional photomultipliers due to their lower operating voltage, lower price and the smaller size of the final experimental modules. Also, their low power dissipation makes them extremely suitable for space applications. However, the small size (1-36 mm^2) sometimes requires many individual optically isolated subdetecto particularly when it is necessary to cover large active volume detectors. In addition, particle detector systems with SiPMs often require positional sensitivity, usually achieved by dividing the detector system into many individual subdetectors. All these requirements make multichannel systems necessary when operating large arrays of SiPMs. Since SiPMs exhibit temperature sensitive gain [2] and require highly stable operating voltage [2] which may differ among individual sensors, the simultaneous operation of numerous photodetectors presents additional technological challenges.

Currently, several solutions exist for the control and readout of SiPM arrays. While some of them are highly aggregated solutions based on standard market components, relying on a single bias voltage supply and providing an output in the form of a sum of several channels [3], others are based on specially developed ASICs [4, 5], where each analog channel is processed separately and each SiPM has independent bias voltage. Usable systems for the different solutions already exist, in various stages of development, with some still at the prototype stage while others are already commercially available.

In this paper, we describe our initial experience and the first preliminary results from using such a multichannel SiPM bias voltage supply and signal processing system - the commercially available CAEN DT5202 module [6].

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2. DT5202 description

2.1. Hardware module

The FERS-5200 is a readout system designed to handle large detector arrays. It is modular and scalable, consisting of multiple synchronised but self-sufficient units, each having 64 or 128 channels. The first unit in development is the 64-channel A5202 readout board [6]. The DT5202 is nothing more than a boxed version of the A5202, so the two can be used interchangeably. The core of the A5202 module is the two 32-channel Citiroc 1A chips, which handle the SiPM readout. Each channel consists of: a Preamplifier, a configurable Slow Shaper (12.5 $\sim$ 87.5 ns shaping time [6]) followed by a peak detector for amplitude measurements and a Fast Shaper (15 ns shaping time [6]) followed by a discriminator. The peak values for each channel are processed by an ADC through a multiplexer. The discriminator outputs from the Fast Shaper's side can be further processed and used for bunch triggering and time-related measurements. The board also houses an FPGA, which reads out the ADCs and configures the ASICs. The FPGA, along with a low-resolution TDC (0.5 ns LSB), is also responsible for processing the discriminator outputs in timing measurements - a functionality absent in the Citiroc 1A ASICs themselves. Aside from those chips, the board also contains an A7585D power supply for SiPM biasing, an internal pulser that can be used for testing and triggering purposes and a local memory buffer. A block diagram is presented in Figure 1.

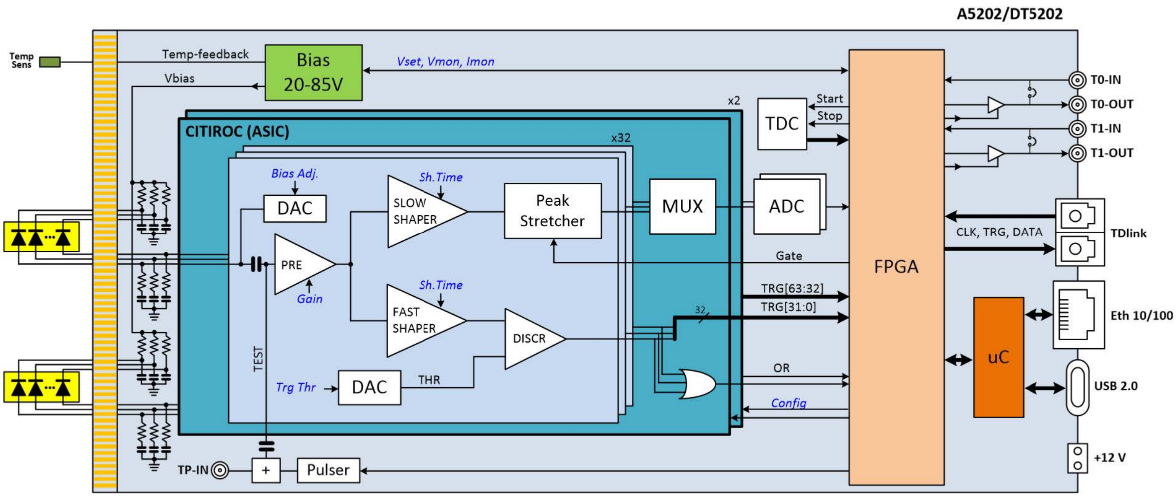

Figure 1. Block diagram of the main components of the DT5202 module. Retrieved from [6].

The front side of the DT5202 is where the DC input and the main communication ports are located. A USB 2.0 port and an Ethernet port are used to communicate with a computer, configure the board and read out the data from the board's buffer. A substantial part of the focus of this study is to determine whether there are performance differences when using either USB or Ethernet connection. Also important are the four LEMO I/O ports dubbed T0-IN, T1-IN, T0-OUT and T1-OUT. These programmable ports are multi-purpose, with examples of possible uses being: external triggering, input/output visualisation and synchronising multiple boards to work together. It should be noted that there is a difference in the signal standards between the ports. As input, the board accepts both LVTTL and NIM signals. However, the T0-OUT and T1-OUT ports can only output LVTTL. The last connector on the board's front is the TDLink port, which is supposed to be usable for communication and triggering/syncing purposes. However, since it is not yet implemented [6], it is not of interest to this study.

2.2. Data acquisition

The data output given by the board can be summarised as "count, charge and time". There are three main data acquisition modes available: Counting mode, which independently counts registered events on every channel; Spectroscopy mode, which outputs the measured charge in connected SiPMs for all channels simultaneously; Timing mode, which allows for ToA (time of arrival) and ToT (time over threshold) analysis. As per the specifications in the user manual, the Counting mode is able to achieve up to 20 Mcps (counts per second) per channel [6]. Spectroscopy mode is limited by a systematic conversion time of ∼10 µs, leading to a claimed maximum trigger rate of ∼100 kHz [6]. Timing mode is currently limited by the 0.5 ns LSB of the low-resolution TDC [6]. However, the board is also equipped with a not-yet-usable 50 ps TDC, which should allow for better timing resolutions in the future.

Configuration and communication with a computer are possible through the official Janus software, currently available both for Linux and Windows-based systems [7]. It allows for setting values such as the SiPM bias voltage, charge and timing thresholds; reprogramming the LEMO ports; run (series) configurations and choosing output file formats. When the GUI is utilised, one can also see real-time statistics for the run in progress as well as visualise spectra, channel activation plots and other similar data. The software is written in C, with a Python-based GUI available, but not required for its use.

3. Test setup description

The main aim of this study is to test the usability of the DT5202 module for experimental purposes. To that end, the focus was on a number of points. The first one is the actual trigger rate. Since in an experiment we would have an expected load of events from the detector, we need to know up to what load the board can perform satisfactorily. This also brings us to the second point - losses. Of course, the board can be put under a high load and still capture a certain percentage of the events, but chances are there is a maximum amount of losses that can be accepted during the experiment. Therefore, the actual performance evaluation needs to take into account the way the trigger rate and loss rate are connected. There is also the issue of connection. With both USB and Ethernet available, it is important to test whether using one or the other offers clear advantages, so the trigger rate and loss analyses were performed for both connection types.

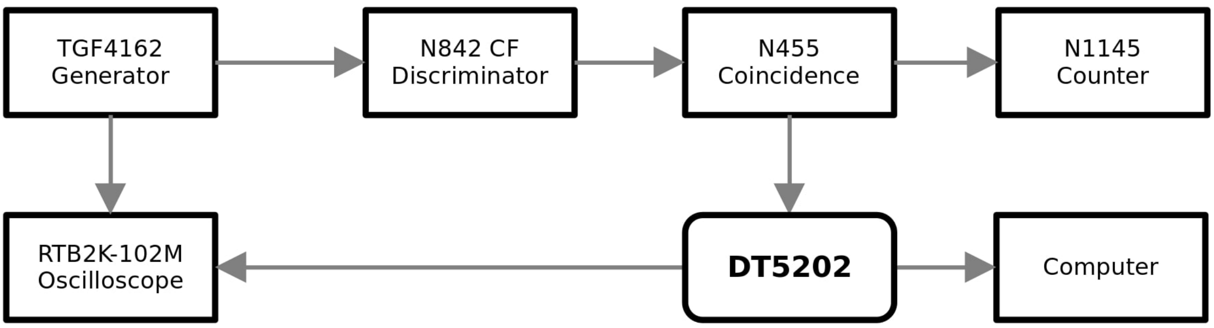

Figure 2. Schematic of the test setup.

The test setup, shown in Figure 2, consists of the board itself being triggered through an external generator connected to one of the LEMO IN ports. The input and output signals are visualised with an oscilloscope for control purposes. Trigger counting is performed via the Janus software (Windows edition, version 2.10). The results shown by the software are controlled using an external counter receiving the same input as the board. The chosen acquisition mode is

Counting, but with this specific setup and purpose there was no difference between the Counting and Spectroscopy modes. The loss rate is gauged by the software, seemingly by division of the number of triggers processed by the number of triggers sent to the board - it seems capable of registering the existence of a trigger even if it cannot actually process it. For losses, the control measure used is to reproduce the calculation made by the software but with total trigger data from outside of Janus. Therefore, we use the frequency of the generator, or rather the triggers detected by the external counter, since at high frequencies the actual number of signals sent by the generator is not perfectly consistent with the frequency given.

4. Preliminary results

The results of the trigger rate sweep are presented in Figure 3.

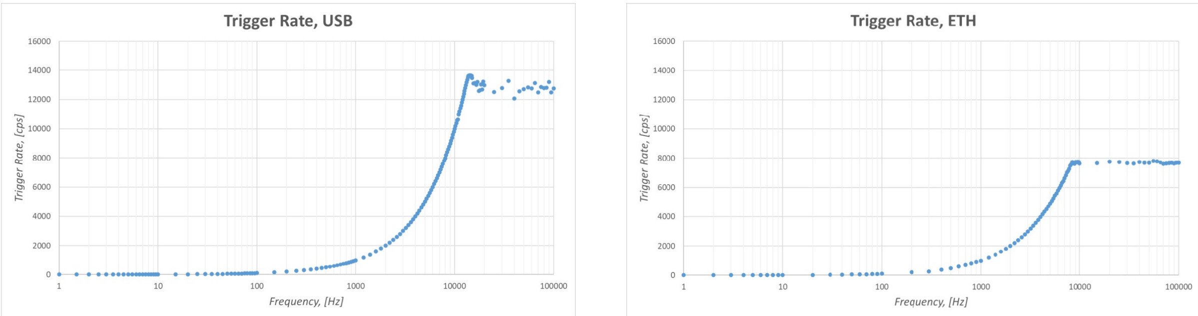

Figure 3. The achieved trigger rate as opposed to the signal generator frequency for both USB and Ethernet.

The graphs above show a good linear growth of the trigger rate with the frequency. However, figure 3 shows that the trigger rate hits a ceiling. The frequency for this occurrence is different for the two connection types. In this regard USB seems to perform better, hitting its limit at about 14 kHz, compared to less than 8 kHz for Ethernet. Above 14 kHz however the trigger rate for USB seems to become extremely unstable. The trigger rate not only starts taking values anywhere between 10 and 14 kHz, but also the average drops to about 13 kHz. Ethernet on the other hand, while having a lower trigger rate cap, shows much greater stability, with the values forming an almost perfect plateau.

The results of the loss rate sweep are presented in Figure 4.

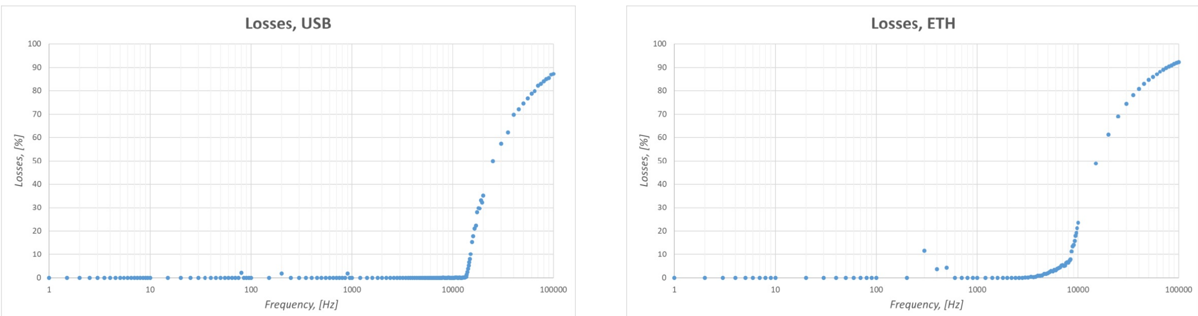

Figure 4. The observed loss rate as opposed to the generator's target frequency for both USB and Ethernet.

These data suggest that the trigger rate cap and the loss rate correlate well. For USB especially, one can see that the losses start rising stably when the frequency of the trigger cap is hit. However, it should also be noted that there are some minor losses in the lower frequencies as well, and this seems to be true for both connection types. In truth, it is not. USB exhibits random losses at any frequency. It would seem that here we again see a type of instability. At times the USB protocol seems to pause the connection between the board and the controlling PC for a second or so, resulting in losses that follow no pattern. And while the Ethernet graph also shows some losses in the 200 $\sim$ 500 Hz range, these losses, while baffling at first, turned out to be a mistake. They result from the board not being connected directly to the computer during the testing, but rather routed through a local network. And in moments when the network saw outside traffic, the measurements were affected. With a direct connection, the losses on Ethernet are zero up to about 2 kHz. But while USB perfectly matches the trigger rate cap and the losses' appearance, the same does not hold for Ethernet. Here the losses seem to start much sooner, possibly due to specifics of the Ethernet protocol's data transferring routines. Still, it can also be seen that there are two distinct profiles of the loss rise. One is from 2 kHz to $\sim$8 kHz, where we see a slow rise. The other one seems to appear at the trigger rate cap's frequency and with the same shape as when using USB.

Finally, a possible explanation for why these limits appear was discovered during testing. It turned out that the readout rate (or the data transfer rate between the board and the computer) has a maximum reminiscent of the trigger rate. This suggests that the trigger rate is limited by the communication type used. It also indicates that the difference in the cap's frequency between the two connections has to the with their maximum data transfer speed. And indeed, per specifications, the Ethernet port of the DT5202 reaches up to 100 Mbit/s [6]. Meanwhile, the USB 2.0 standard should achieve up to 480 Mbit/s. This could account for different maximum readout rates and, consequently, different trigger rate caps. There also seems to be an agreement between the USB frequency to ETH frequency ratio and the USB readout to ETH readout ratio. From the graphs, by eye, the former is $13600/7800 \approx 1.744$ (using the peak achieved value for USB), while the latter is $3900/2250 \approx 1.73(3)$. The readout rate data is presented in Figure 5.

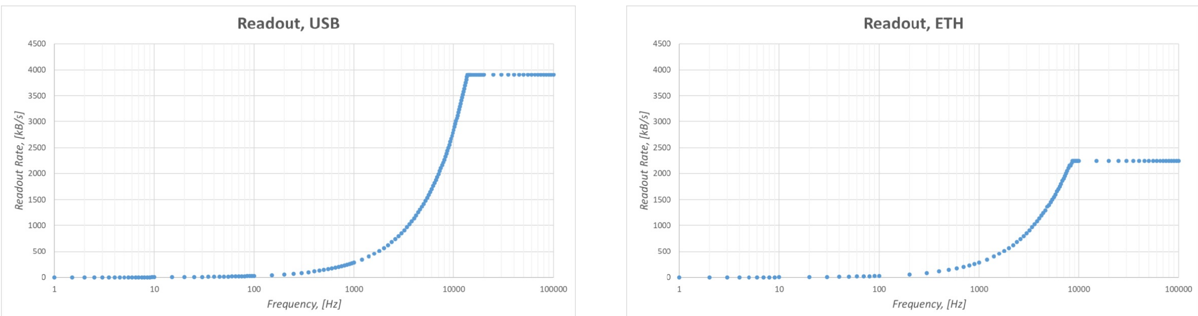

Figure 5. The observed readout rate as opposed to the generator's target frequency for both USB and Ethernet.

5. Discussion

The results observed suggest that the DT5202 module might have a future, but as of now has its fair share of problems. Currently it is severely limited in its achievable trigger rates - with a (quite unstable) maximum of about 14 kHz - far below the advertised 100 kHz. If for any reason, it is impossible to use USB, the rate drops even further. A good reason why one would not want to use it lies in the unpredictable losses that seem to be an inherent weakness of the USB protocol itself. Such random instabilities could ruin multiple types of measurements. A possible solution to this maximum trigger rate problem lies in the TDLink connection. However, until it is properly implemented, nothing can be said. As of now, the boards are usable for testing initial detector prototypes where the losses might not be so painful, or for low count rate experiments with small amounts of data per event. We should also note problems with the Janus control software. We have seen numerous cases of connection loss between the software and the board - some of them only fixable by a manual restart of the DT5202 module. Moreover, it is not rare for random freezes to happen in the GUI, requiring its restart and potentially compromising a measurement. We have also had cases of strange values appearing in the files - trigger IDs and time stamps much too large to be realistic and instances of broken records or incomplete data in some runs. These problems might have to do with manually ending runs - they do not seem to appear if an automatic ending based on some criteria (run duration or trigger counts) is used. However, they might cause issues in the later data analysis if one does not expect them. Here, it should be noted that Janus is still being actively developed, so these problems and bugs might get fixed in the future.

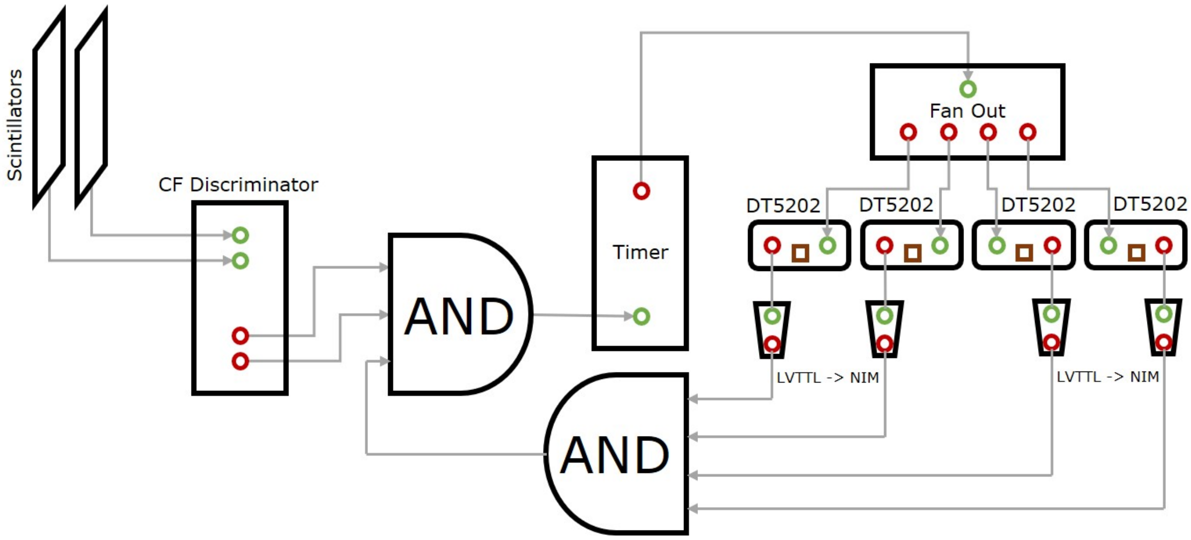

Figure 6. An example of a circuit that can be used to synchronise multiple boards using bunch triggers. Here green circles represent an "IN" port; red circles represent an "OUT" port, brown squares are the I/O communication ports (USB/ETH/TDLink).

A positive point about the module's use is scalability. It is quite easy to synchronise multiple modules using the LEMO I/O ports for synchronisation and bunch triggering. This would allow one to easily use the DT5202 modules in detectors with large numbers of channels. An example of a synchronisation circuit using four boards is presented in Figure 6. Here, rather than using the boards' own triggering capabilities, we use external triggering. Signals from two scintillators are sent to a discriminator the output of which is provided to a coincidence module to ensure that both scintillators have detected the same event. Another signal, also fed to the coincidence, checks if all DT5202 modules are ready for data acquisition. The coincidence's output is fed into a timer, which sets the time windows during which trigger signals are accepted and data acquisition occurs. In the circuit provided, the aim is to use four modules for a total of 256 channels. However, it could easily be extended to work with larger arrays. The Janus software is currently capable of handling up to 16 boards connected at once, so the current limit is 1024 channels, but as the FERS-5200 system's development continues, this number should rise.

6. Conclusions

The CAEN DT5202 readout module is made to handle the bias voltage supply of SiPMs, as well as the processing of the signals detected. Each board houses two Citiroc 1A chips, totalling 64 channels per module. We selected the DT5202 for its potential use in the testing stages of new SiPM detectors. To that purpose, some of its performance limits - more specifically maximum trigger rate, readout rate and losses, have been tested using "synthetic" triggering with a generator. The control software included with the module has also been studied along with its limitations. The preliminary results show disparities between the actual performance of the board and the specifications given in the user manual. The maximum trigger rate does not exceed approximately 14 kHz without significant losses. This seems to be tied to the connection type (and speed) between the board and the computer receiving the data is being sent to. Cases of communication loss between the software and the board have also been observed, as well as issues in the final data output, such as cases of missing or unrealistic values that could impede later data analysis. It can be said that the DT5202 currently has value mainly as a tool for testing purposes. In its current "in development" stage, that is its limit. There are however hardware sections that are not fully (or at all) utilised. The results, and especially the dependence on the readout rate discovered, suggest that the full introduction of TDLink might solve some of the problems found.

Acknowledgements

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