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Application of the new Check-Sort-Push mechanism in the iRPC subsystem for the CMS Phase-2 upgrade

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Abstract: Backend electronics (BEE) commonly employ a high speed link to provide both fast and slow control to frontend electronics (FEE). In addition, the backend is responsible for trigger preprocessing and data readout. Typically, this high-speed link is shared by many frontend channels. Under such conditions, the processing time in the BEE for channels with lower readout priority varies significantly, especially in scenarios with high hit rate. This variability results in unpredictable or even unacceptable processing latency for demultiplexing and trigger preprocessing, even when zero-suppression and multiplexing are applied in FEE before data transmission. This paper addresses these issues through emulation study and proposes the Check-Sort-Push (CSP) mechanism as a solution. The necessity and advantages of this proposal are demonstrated using simulation and emulation under high hit rate conditions. An implementation in firmware is presented. Finally, the application of the CSP mechanism in the improved Resistive Plate Chamber (iRPC) system for CMS Phase-2 upgrade will be discussed, along with analysis results based on test beam data.

Keywords: Data processing methods; Front-end electronics for detector readout; Simulation methods and programs; Data acquisition concepts

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1 Introduction

Modern high energy physics experiments utilize serial links to transmit zero-suppressed data from multiple channels to the backend electronics (BEE). Such a system is employed in the Resistive Plate Chamber (RPC) link system in the Compact Muon Solenoid (CMS) experiment [1]. In the backend, the Concentration-PreProcessing-and-Fanout (CPPF) board performs its functions under low hit rates [2, 3]. On the transmitter side, channel hit data are discriminated to provide a one bit, 0 or 1, digitization. The digitized data are read out in a polling manner using a 40 MHz system clock based on the Bunch Crossing (BX) interval of 25 ns. Zero-suppression is then applied at the partition level, grouping 8 adjacent strips into a two-digit hexadecimal number. Only nonzero data, partition number, and partition delay in BX are packed [4]. Data with delays beyond 8 BX are truncated and flagged with an End-of-Data (EOD) marker. As illustrated in figure 1, the left block shows the hits generated in each BX for different partitions, while the right block represents the serialized data frames transmitted per BX. Each frame contains the partition data, partition number, partition delay, and the EOD flag. Since only one frame can be transmitted per BX, if multiple hits occur in the same BX, the data from the higher partition number is sent first, and the others are sent in subsequent BXs with the corresponding partition delay. The partition delay thus encodes the difference between the BX when the hit was generated and the BX when it is transmitted (e.g., “03” has delay 0, while “C0” has delay 1). On the receiver side, deserialization and decompression are performed, where the partition delay is applied to restore the original BX timing of hits. This allows the complete hit map to be reconstructed within 8 BX cycles, providing the input for subsequent cluster finding.

New readout systems for high-energy physics experiments employ the unified high-speed link (HSL) for all subsystems. For example, Belle II [5] uses Belle2Link [6], while the CMS Phase-2 improved RPC (iRPC) upgrade adopts the Gigabit Transceiver (GBT) [7, 8]. Through these links, fast control (FC) signals are distributed by the Trigger and Clock Distribution System (TCDS), slow control

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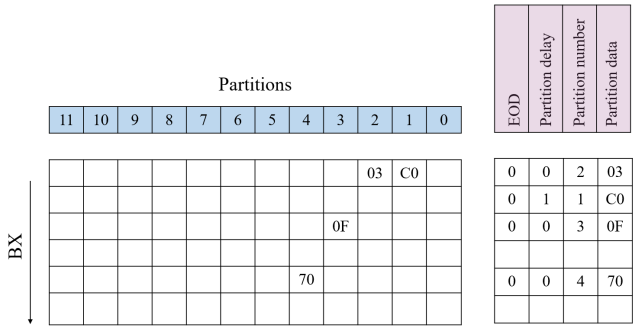

Figure 1. Data transmission scheme from the current CMS RPC Link Board to the CPPF board.

(SC) is provided from the console PC, and detector signals digitized by Analog-to-Digital Converters (ADCs) and Time-to-Digital Converters (TDCs) are transmitted to the backend electronics (BEE). Then BEE preprocesses the detector data and sends trigger primitives to the Global Trigger (GT) for the Level-1 Accept (L1A) decision. Once the L1A is issued by the GT and redistributed through the TCDS, the event data are read out from the BEE. The generalized system architecture is illustrated in figure 2.

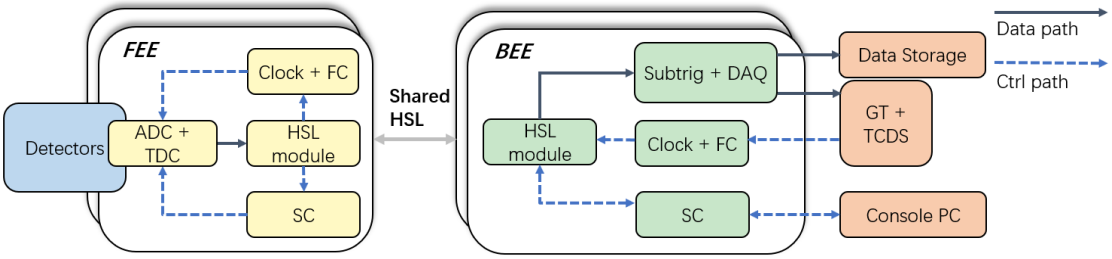

Figure 2. System architecture consisting of FEE, BEE, and the data flow chain

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In this paper, the CMS Phase-2 iRPC subsystem is used as a representative case to introduce the generalized architecture and to carry out the subsequent study. The iRPC system is at the heart of CMS detection capabilities, playing a crucial role in identifying and tracking muons, particularly in the challenging high $|\eta|$ (pseudorapidity) regions of the detector. Here, $\eta \equiv -\ln\tan(\theta/2)$ is a standard coordinate variable in collider physics, with high $|\eta|$ corresponding to particles emitted close to the beam axis. A Petiroc2C Application-Specific Integrated Circuit (ASIC) chip has been used for signal amplification and discrimination in FEE for the iRPC system [9]. The signal time from the Petiroc2C is measured by a TDC implemented in a Field-Programmable Gate Array (FPGA) with 2.5 ns steps for coarse time binning and 2.5/256 ns steps for fine time binning. Due to mechanical constraints, channels are grouped to include only one end of each strip, rather than combining both ends within the same group. The TDC data are read out in a polling manner and transmitted together with the channel number and the TDC FPGA ID to the BEE via the GBT link [10]. In the BEE, TDC data are deserialized and demultiplexed (Demux), restoring the relative timing correlation of hit information which is used to compute a precise hit position along the strip, enabling accurate localization of muon tracks. This enhancement is particularly critical for improving trigger efficiency, especially in scenarios with high particle densities.

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Despite these advancements, the current system faces several challenges as particle collision rates increase:

- Polling Readout: the existing polling readout method may not efficiently handle high rates of particle hits.
- Sending Delays: increasing hit rates can cause significant delays between data generation in FEE and its transmission to BEE.
- Demux and DAQ Time Window: the size of the Demux and DAQ time window plays a crucial role in determining the efficiency of Level-1 trigger decisions and ensuring complete data capture.

In this paper, an emulation-based R&D setup and real beam tests at the CERN Gamma Irradiation Facility (GIF++) are used to reproduce and analyze these issues. Based on the findings, a Check-Sort-Push (CSP) mechanism is proposed and its functionality and performance are evaluated using the same systems.

2 Emulation of iRPC electronics

To facilitate the development and testing of the CSP mechanism, a Micro Telecommunications Computing Architecture (MicroTCA)-based R&D system for iRPC electronics was established. The system was composed of several key components. Two user Micro/Advanced TCA Mezzanine Cards (AMCs) were employed, one serving as a FEE emulator to generate simulated data and SC signals, and the other functioning as the BEE board (BEB), responsible for data processing and SC tasks. In addition, an AMC13 card [11] was integrated to provide timing and trigger control. The setup also included a MicroTCA Carrier Hub (MCH) connected to a PC, which was responsible for SC and data storage. Together, these components provided a flexible and realistic platform for emulating the iRPC readout chain and validating the CSP mechanism.

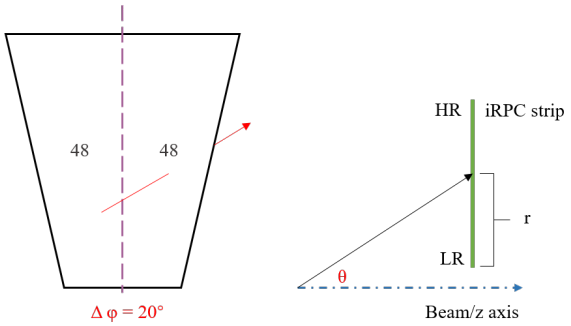

Figure 3. Hit generation in a half-chamber with 48 strips over 10°, where r ranges from LR to HR. Hit coordinates in r and ϕ are uniformly simulated for muons and background gammas.

Detector data in the emulation system were produced by simulation. A muon produced from a p-p collision is detected in iRPC strips, as shown in figure 3. In the current iRPC design, each half-chamber is serviced by a single Front-End Board (FEB), and the present emulation corresponds to the data domain of one such half-chamber. Within this region, every strip has an azimuthal coordinate ϕ and a

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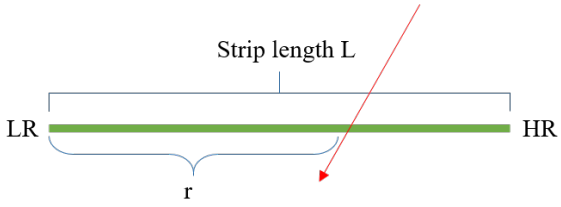
radial coordinate r ranging from the low radius (LR) to the high radius (HR). The hit coordinates are generated with a flat distribution in (r, ϕ). A cluster is formed by a set of consecutive strips, with cluster sizes ranging from 1 to 8 with a mean of 3, as described in [12]. Background hits were produced similarly, but with a cluster size of either 1 or 2 strips, with an average of 1.5. Different hit rate scenarios are emulated by combining muon hits with background gamma hits (γ) at various intensities.

For each hit, the radial position r along a strip of length L is determined from the TDC values t_1 and t_2 read out from the ends of the strip at the lowest radius (LR) and highest radius (HR), respectively, as illustrated in figure 4. Each hit (fired strip) results in two 32-bit words, one for LR and one for HR, that encode the TDC value and device address (FPGA ID). Three TDC words and valid flags are multiplexed to form a GBT data frame, which is then serialized for transmission to the backend.



$$r = \frac{1}{2}L - \frac{(t_2 - t_1) * v}{2}$$

Figure 4. Hit position r derived from arrival time difference at strip ends. The signal transmission speed along the strip is denoted v.

In the BEE, after deserialization and Demux, the hit map is recovered by taking the sending delay into account. A maximum Demux window of 23 BX is used as a temporary value, and a DAQ window of 63 BX is used.

3 Problem reproduced and new Check-Sort-Push mechanism

3.1 Problem reproduced in R&D system

Using the R&D system mentioned earlier, which adopts a polling readout scheme, the issues outlined in section 1 were reproduced and further analyzed with DAQ data, revealing that these problems become more severe as the hit rate increases. To aid in understanding the plots of the data analysis, a brief description of the connections between detector strips and TDC channels is given here. As shown in figure 3, each half-chamber has 48 strips. These strips generate 96 signals, 48 from the LR end and 48 from the HR end, that are read out by three 32-channel TDC FPGAs. Each FPGA reads out 16 LR ends and 16 HR ends. The sending delays produced in the emulation system, based on simulated data, are shown in figure 5 for two background rate scenarios: low and high. In the plots, the channels associated with the three FPGAs are labeled sequentially as 0–31, 32–63, and 64–95, respectively. Channels 0–15, 32–47, and 64–79 correspond to the LR ends, while the remaining channels correspond to the HR ends. Note that in either scenario, there are larger time delays for the HR ends compared to the LR ends in the same FPGA. Since the channels of the three FPGAs are read out in sequence, the later in the sequence, the higher are the delays. The maximum sending delays are significantly larger for the high background rate scenario. The problems of uneven sending delays among the channels and increasing delay with background rate are clearly evident.

The conclusion of these studies is clear: polling-based readout is problematic, as it produces inter-channel imbalance in sending delays and leads to increased latency at high hit rates. Therefore, the data transmission must be based on the actual time when the hit is generated.

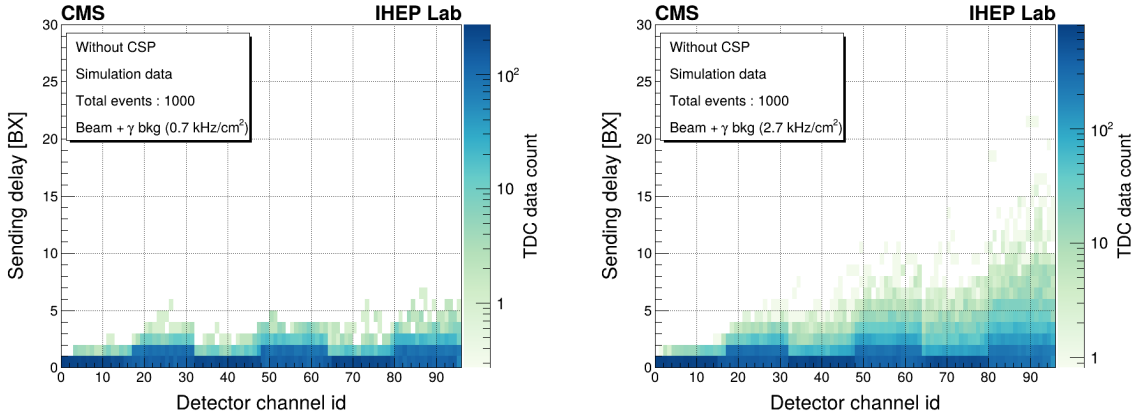


Figure 5. Sending delay distribution. Left: low hit rate scenario (0.7 kHz/cm^2). Right: high hit rate scenario (2.7 kHz/cm^2).

3.2 CSP: a new mechanism and its implementation in FEE

To reduce the data sending delay and simplify the Demux design of the BEE, a new timing-based mechanism called CSP has been proposed and implemented in the iRPC FEE, as illustrated in figure 6. The CSP mechanism operates in three steps:

- Check (performed with the 40 MHz clock): channels with above-threshold signals are checked in parallel, and for each active channel a data word is formed that includes the generation time, channel ID, device ID, and the measured TDC value, which is then stored in the corresponding channel First-In-First-Out (FIFO).
- Sort (priority encoding at 40 MHz $\times$ N clock): the data words are first sorted by generation time (BX) before being moved into the TDC FIFOs, and are then re-sorted by generation time prior to transfer to the concentrator FIFO.
- Push (performed with the 40 MHz clock): up to three earliest available data words are assembled into long GBT frames and transmitted to the backend.

As shown in figure 7, this diagram illustrates the operation of the first sorting process, which routes data words from 32 channel FIFOs into their corresponding TDC FIFOs. A divide-and-conquer strategy is applied to decompose the large comparison problem into multiple small steps within a pipelined structure, enabling efficient extraction of the earliest and second-earliest timestamps. Leveraging the iRPC both-ends readout feature, the timestamp comparison for 32 channels can be reduced to 16 inputs, since the both ends of the same strip produce timestamps only a few nanoseconds apart. For example, the earliest and second-earliest channels are selected from the 16 HR timestamps, and their corresponding LR channels are obtained through the mapping, which significantly simplifies the comparison logic.

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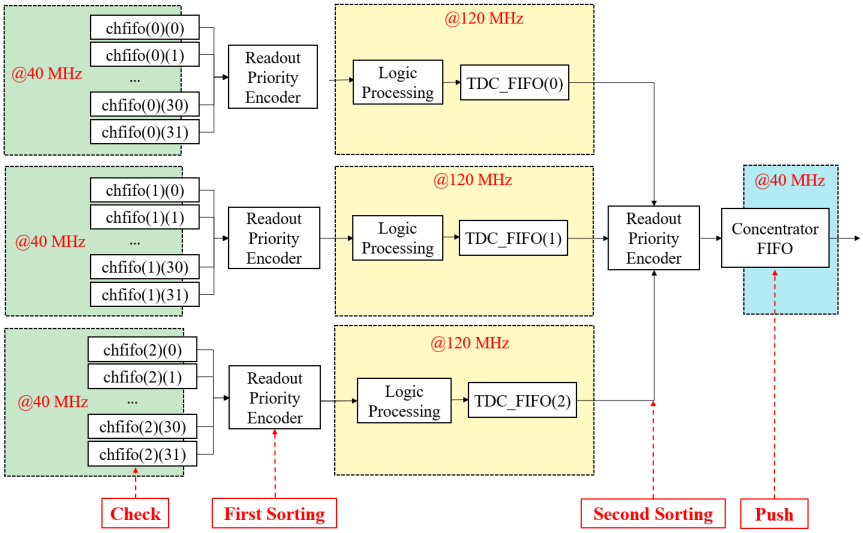

Figure 6. Block diagram of the Check-Sort-Push (CSP) mechanism.

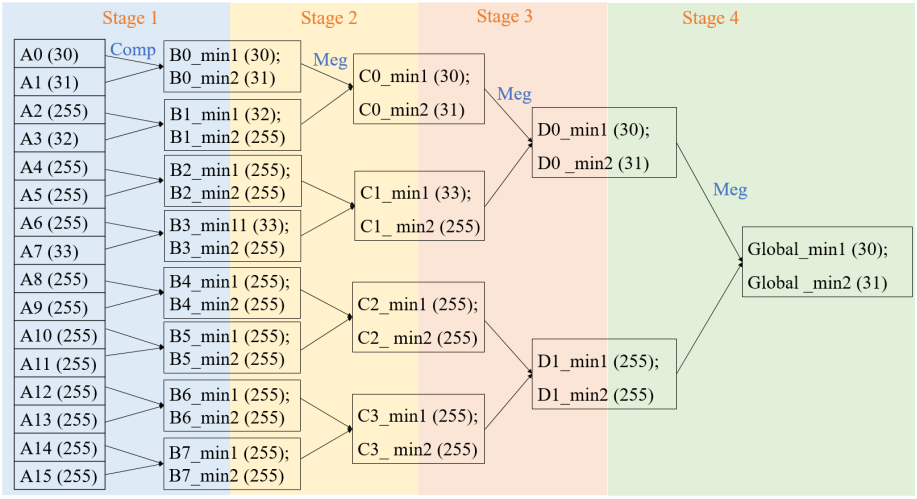

Figure 7. Expanded diagram explaining the operation of the first sorting process.

The first sorting pipeline operates at 160 MHz and consists of four stages. In stage 1, sixteen 8-bit timestamp inputs (e.g., from the HR side) are compared in pairs. The timestamps are provided by channel FIFOs operating in First-Word Fall-Through (FWFT) mode, allowing access to the next data word without asserting the read enable. Any empty FIFO is assigned the maximum value (255), and the pairwise comparison produces eight intermediate results. For stages 2–4, a reusable "meg" module merges two comparison groups. The module first determines min1 (the earliest timestamp) by comparing the two group minima, and then selects min2 (the second-earliest timestamp) from the two candidates eliminated during the min1 selection, as illustrated in figure 8. For example, comparing B0_min1 (30) and B1_min1 (32) yields B0_min1 (30) as the earliest timestamp. The second-earliest timestamp lies between B1_min1 (32) and B0_min2 (31), from which B0_min2 (31) is selected as

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min2. By cascading this module through stages 2–4, the earliest and second-earliest timestamps among all 16 inputs are obtained. The data words of the corresponding two HR channels and their mapped LR channels are then read out when the corresponding channel FIFOs are non-empty, and written into another FIFO for temporary storage and clock-domain crossing. To handle rare cases of single-end TDC data words, for example where signal attenuation on the HR side results in a valid hit appearing only on the LR side, a potential FIFO blocking issue may occur if the 16-input selection always favors HR-side timestamps. To prevent isolated LR-side data words from being stalled in the FIFO, the HR and LR timestamps are alternately used as the 16 comparison inputs, ensuring that both ends are periodically considered in stage 1 of the first sorting pipeline.

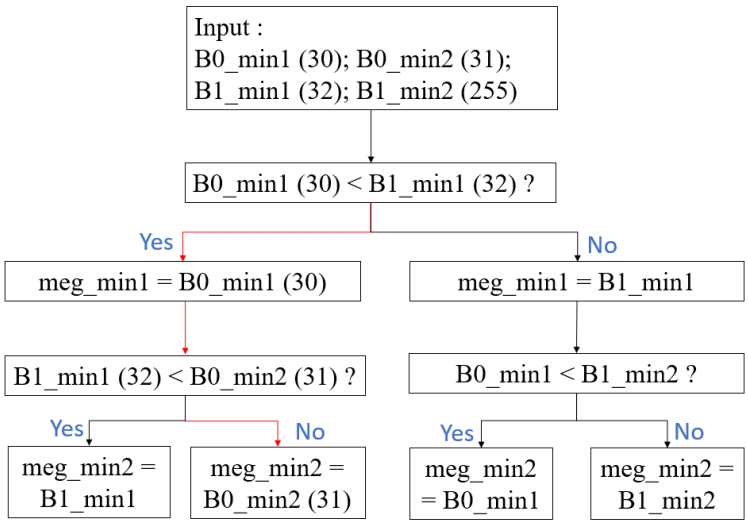

Figure 8. Two-level selection logic for the earliest and second-earliest timestamps of the meg module.

During the second sorting process, up to three timestamps from the TDC FIFOs are compared at 120 MHz. The FIFOs operate in FWFT mode, and any empty FIFO is excluded from the comparison.

4 CSP improvements confirmation

This section presents comprehensive tests with the emulation system and a beam test at the CERN GIF++. Test results are presented in the following.

4.1 CSP improvement verification with emulation

The emulated distribution of transmission delays using the CSP mechanism is shown in figure 9 for the high hit rate scenario of 2.7 kHz/cm^2. Compared to the distribution in figure 5 (right) using the polling mechanism, the maximum transmission delay is reduced from 15 BX to 7 BX. Furthermore, the distribution of transmission delays no longer depends on the detector channel, having eliminated the dependence on serial readout sequence and LR versus HR strip end.

4.2 Further verification with CERN beam test

A beam test was conducted at the GIF++ facility using a full-scale iRPC setup to further validate the emulation findings. The iRPC chamber was located inside a bunker containing the gamma source

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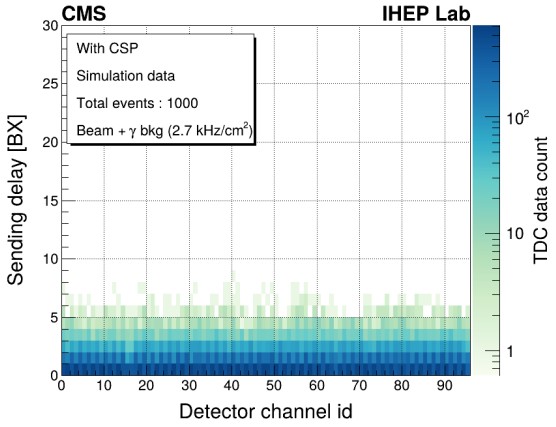

Figure 9. Emulated sending delay distribution with CSP.

and mounted in the muon beam line, with the FEB positioned just below it. Outside the bunker, the beam trigger electronics and a micro-TCA crate containing the BEE were placed. The BEE supported high-speed data transfer over a GBT link, while DAQ and slow-control functionalities were implemented via IPbus/SiTCP protocol. The results with the CSP mechanism are discussed below for γ background of 2.0–2.7 kHz/cm^2, which corresponds to the expected maximum background rates for the iRPC detectors under HL-LHC conditions.

1) *Sending delay.* The distribution of sending delay is shown in figure 10. Using the CSP mechanism, the maximum delay is decreased to less than 30 BX compared to 60 BX with polling readout. Moreover, with the CSP mechanism, the delay distribution is independent of detector channel ID, while the distribution is strongly channel-dependent with polling readout.

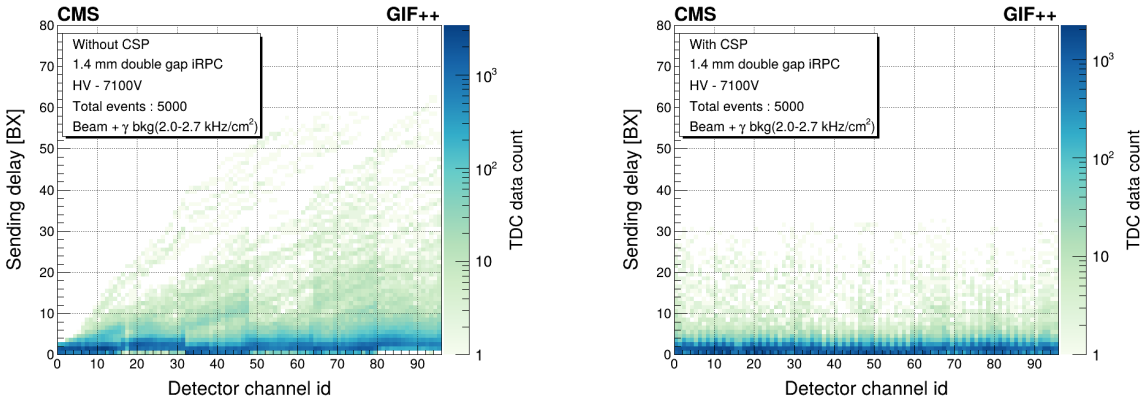

Figure 10. Sending delay distribution without (left) and with (right) CSP under high hit rate conditions.

2) *Transmission efficiency.* The efficiency for transmitting good hits from the passage of a charged particle can be affected by high chamber flux and can depend on the time width of the Demux window. For the beam data analysis, a good hit is defined by paired TDC data with position within the beam impact region and time fixed by the trigger signal. The Phase-1 RPC used a DEMUX window of 8 BX, which was assumed to be the maximum delay. In the beam

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test, we studied delays of 8, 12, 16, and 23 BX, the latter being the current default setting for HL-LHC. The transmission efficiencies were measured using both polling and CSP mechanisms, as shown in the left panel of figure 11. With the CSP mechanism, efficiencies are close to 100% even for the smallest window of 8 BX. In comparison, with polling readout, the transmission efficiency drops quickly as the window size decreases, falling below 92% at 8 BX. With the CSP mechanism, the data transmission is reliable under high-rate conditions.

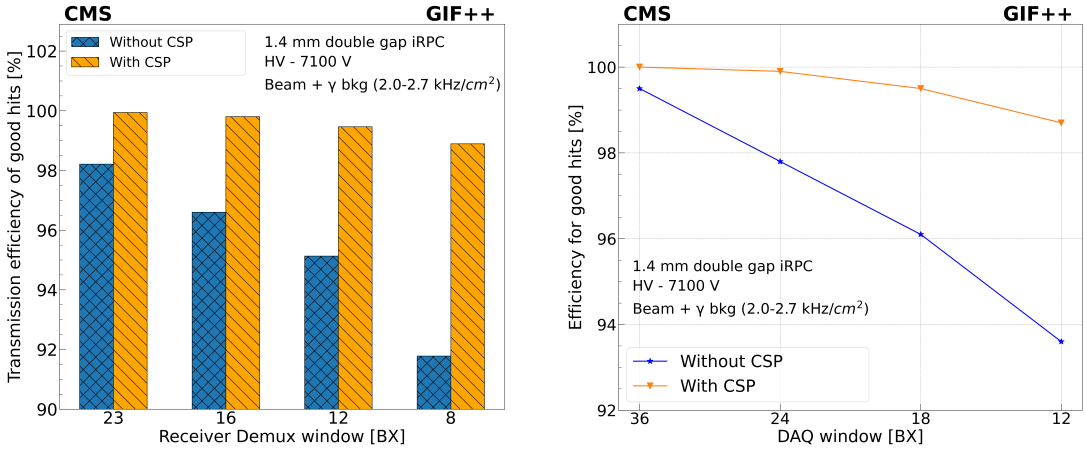

Figure 11. Impact of CSP on good hit efficiency for different Demux (left) and DAQ (right) windows.

3) *DAQ efficiency.* The efficiency for receiving good hits by the DAQ system can be affected by the time window utilized. For high background conditions similar to those expected at HL-LHC, measurements performed at the beam test show that approximately 90% of events contain no more than two muon clusters within a single BX. Given a maximum muon cluster size of eight, this corresponds to 32 TDC data points, or approximately 11 BX frames with three TDC data per frame. Adding a small safety margin, the minimum DAQ window is set to 12 BX. The efficiencies for good hits with DAQ windows of 36, 24, 18, and 12 BX are shown in the right panel of figure 11, comparing the polling and CSP mechanisms. With the CSP mechanism, the efficiency remains greater than 98% even for the smallest window of 8 BX. In contrast, with the polling mechanisms, the efficiency drops below 98% for the 24 BX window and falls to 93% for the smallest one. These results indicate that the CSP mechanisms provides an additional safety margin in maintaining data quality under reduced window widths.

5 Conclusion

The development of the Check-Sort-Push (CSP) mechanism represents a significant advancement in the data handling capabilities of the improved Resistive Plate Chamber (iRPC) electronics. This mechanism addresses key challenges associated with polling readout, which have been shown to introduce substantial delays, resulting in partial data loss and increased system latency. The successful implementation and testing of CSP indicate that it is a viable and effective option for the Phase-2 upgrade of the CMS iRPC subsystem, meeting the demands for efficient operation at the high-luminosity LHC.

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